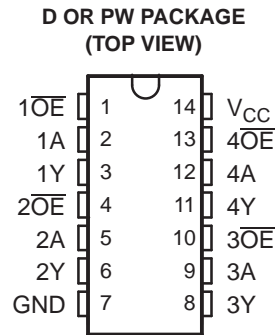


QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

FEATURES

- Qualified for Automotive Applications
- Operates From 1.65 V to 3.6 V
- Specified From -40°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC125AQDRQ1	LC125AQ
	TSSOP – PW	Reel of 2000	SN74LVC125AQPWRQ1	LC125AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

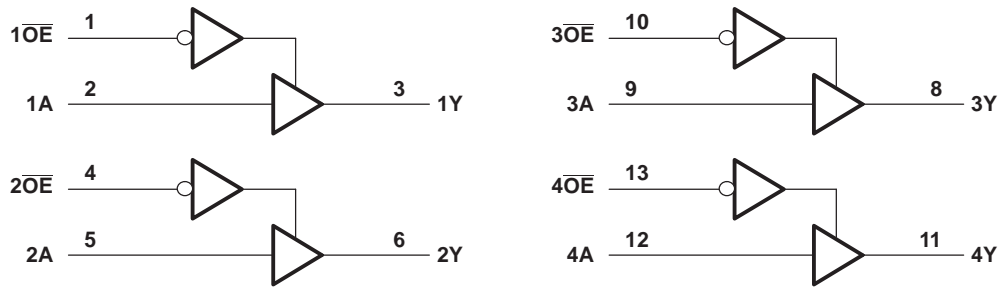
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)**Absolute Maximum Ratings⁽¹⁾**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range	-0.5	6.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current		-50	mA
		$V_I < 0$		
I_{OK}	Output clamp current		-50	mA
		$V_O < 0$		
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	D package	86	°C/W
		PW package	113	
T_{stg}	Storage temperature range	-65	150	°C
P_{tot}	Power dissipation ⁽⁵⁾⁽⁶⁾		500	mW
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (6) For the PW package: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT	
		MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.7		1.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	0.7		0.7		
		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$	0.8		0.8		
V_I	Input voltage	0	5.5	0	5.5	V	
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V	
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$	-4		-4		mA
		$V_{CC} = 2.3\text{ V}$	-8		-8		
		$V_{CC} = 2.7\text{ V}$	-12		-12		
		$V_{CC} = 3\text{ V}$	-24		-24		
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4		4		mA
		$V_{CC} = 2.3\text{ V}$	8		8		
		$V_{CC} = 2.7\text{ V}$	12		12		mA
		$V_{CC} = 3\text{ V}$	24		24		
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -100\ \mu\text{A}$	1.65 V to 3.6 V	$V_{CC} - 0.2$			$V_{CC} - 0.2$		V
	$I_{OH} = -4\text{ mA}$	1.65 V	1.29			1.1		
	$I_{OH} = -8\text{ mA}$	2.3 V	1.9			1.75		
	$I_{OH} = -12\text{ mA}$	2.7 V	2.2			2.1		
	$I_{OH} = -24\text{ mA}$	3 V	2.4			2.35		
	$I_{OH} = -24\text{ mA}$	3 V	2.3			2.1		
V_{OL}	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 3.6 V	0.1			0.2		V
	$I_{OL} = 4\text{ mA}$	1.65 V	0.24			0.45		
	$I_{OL} = 8\text{ mA}$	2.3 V	0.3			0.7		
	$I_{OL} = 12\text{ mA}$	2.7 V	0.4			0.5		
	$I_{OL} = 24\text{ mA}$	3 V	0.55			0.7		
I_I	$V_I = 5.5\text{ V or GND}$	3.6 V	± 1			± 10		μA
I_{OZ}	$V_O = V_{CC}\text{ or GND}$	3.6 V	± 1			± 10		μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	3.6 V	1			20		μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$	2.7 V to 3.6 V	500			500		μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V	5					pF

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

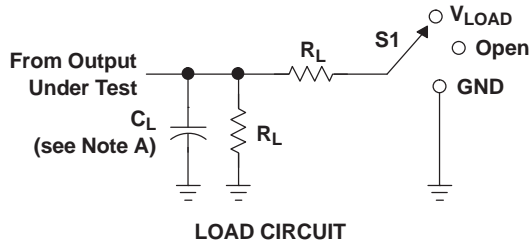
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A	Y	2.7 V	1	3	5.3	1	7	ns
			3.3 V ± 0.3 V	1	2.5	4.6	1	6	
t _{en}	\overline{OE}	Y	2.7 V	1	3.3	6.4	1	8.5	ns
			3.3 V ± 0.3 V	1	2.4	5.2	1	7	
t _{dis}	\overline{OE}	Y	2.7 V	1	2.5	4.8	1	6.5	ns
			3.3 V ± 0.3 V	1	2.4	4.4	1	6	
t _{sk(o)}			3.3 V ± 0.3 V					1.5	ns

Operating Characteristics

T_A = 25°C

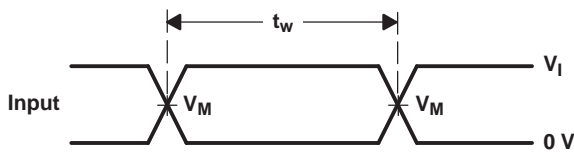
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	3.3 V	15	pF

PARAMETER MEASUREMENT INFORMATION

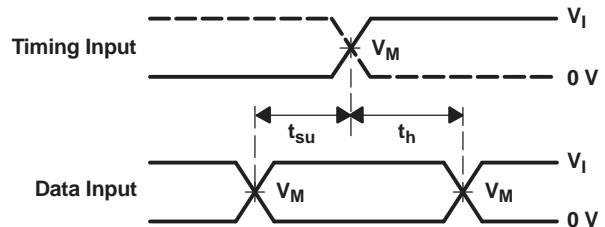


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

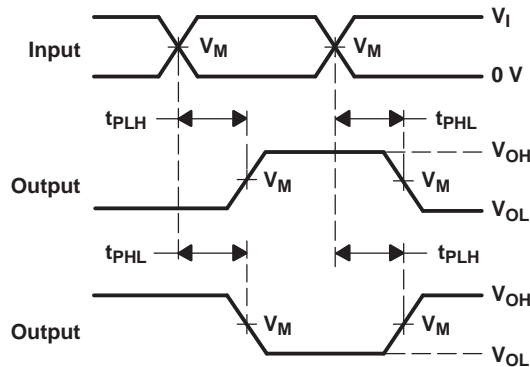
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVC125AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	Samples
SN74LVC125AQDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	Samples
SN74LVC125AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC125A-Q1 :

- Catalog: [SN74LVC125A](#)
- Enhanced Product: [SN74LVC125A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC125AQPWRG4Q1	TSSOP	PW	14	2000	853.0	449.0	35.0
SN74LVC125AQPWRQ1	TSSOP	PW	14	2000	853.0	449.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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