FAN604P

Product Preview

Offline Quasi-Resonant PWM Controller

Description

The FAN604P incorporates Quasi−Resonant (QR) control with proprietary Valley Switching with a limited frequency variation. QR switching provides high efficiency by reducing switching losses while Valley Switching with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

FAN604P burst mode operation with extremely low operating current (300 μA) and significantly reduces standby power consumption to meet the most stringent efficiency regulations such as Energy Star's 5−Star Level and CoC Tier II specifications.

FAN604P includes several user configurable features aimed at optimizing efficiency, EMI and protections. FAN604P has a wide blanking frequency range that improves light load efficiency. It incorporates user−configurable power limit reference (PLR), which allows controlling the maximum output power from primary−side, thereby optimizing transformer design to improve the overall efficiency. It also includes several rich programmable protection features such as over−voltage protection (OVP), under−voltage protection (UVP) and externally triggered shutdown protection (SD).

Features

- Valley Switch Operation for Highest Average Efficiency
- Wide Input and Output Conditions Achieve High Power Density Power Supply
  - User Configurable Power Limit Reference (PLR) to Limit the Maximum Output Power
  - Precise Constant Output Current Regulation with Programmable Line Compensation
- Ultra−Low Standby Power Consumption (<20 mW)
- Forced and Inherent Frequency Modulation of Valley Switching for Low EMI Emissions and Common Mode Noise
- Built−In High−Voltage Startup to Reduce External Components
- Programmable Brown−In and Brown−Out Protection
- Output Over−Voltage Protection (OVP)
- Output Under−Voltage Protection (UVP)
- Programmable Over−Temperature−Protection through External NTC Resistor
- This is a Pb−Free Device

Typical Applications

- Battery Charges for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices or Battery Chargers that Require CV and Power Limit Control

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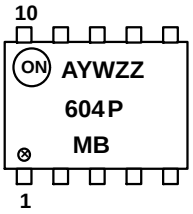
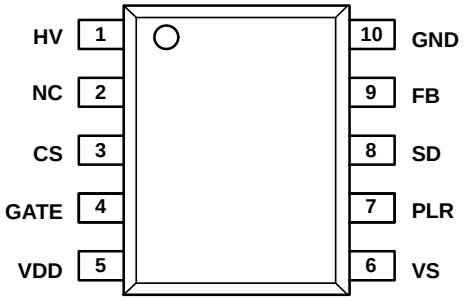
SOIC10
CASE 751EE

MARKING DIAGRAM



A	= Assembly Plant Code
Y	= Year Code
W	= Week Code
ZZ	= Die Run Code
M	= Package Type (M = SOIC)
B	= Manufacture Flow Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method†
FAN604PMX	−40°C to 125°C	SOIC10 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

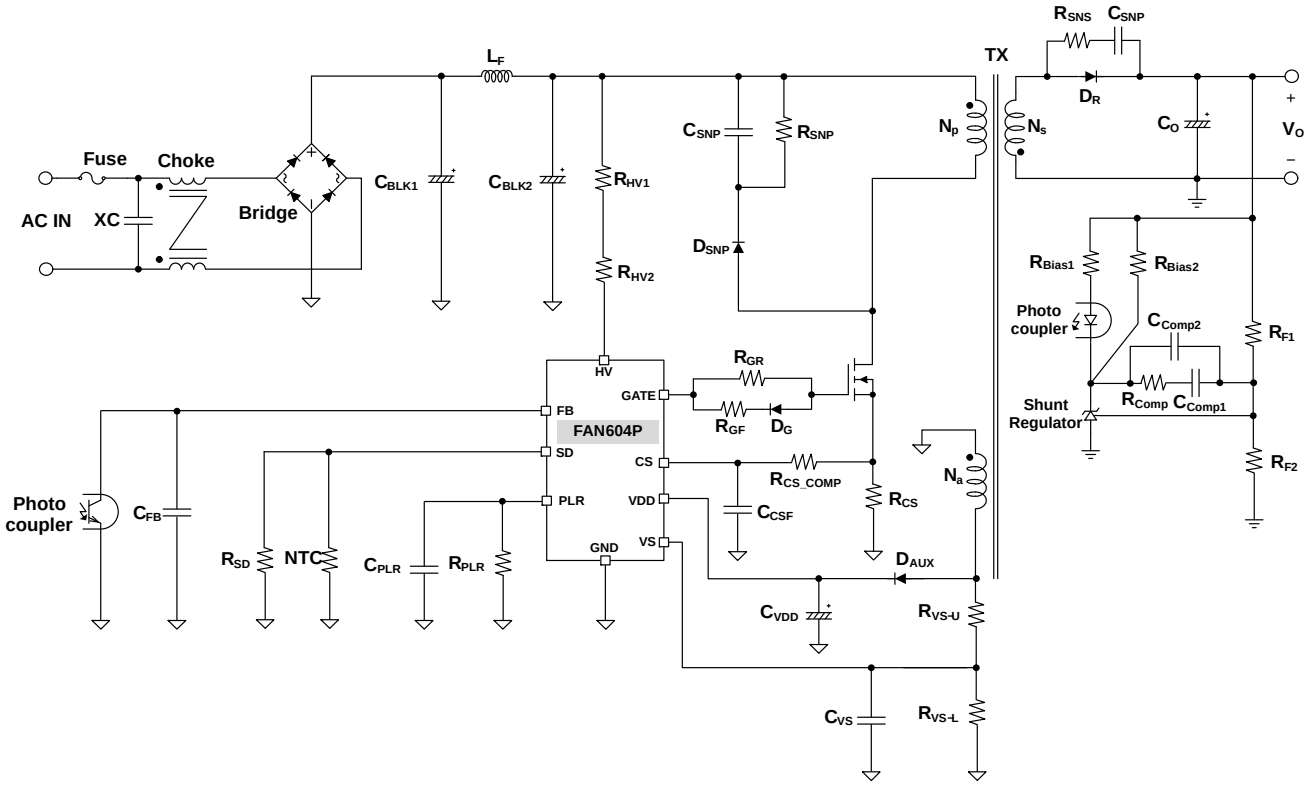


Figure 1. FAN604P Typical Application Schematic

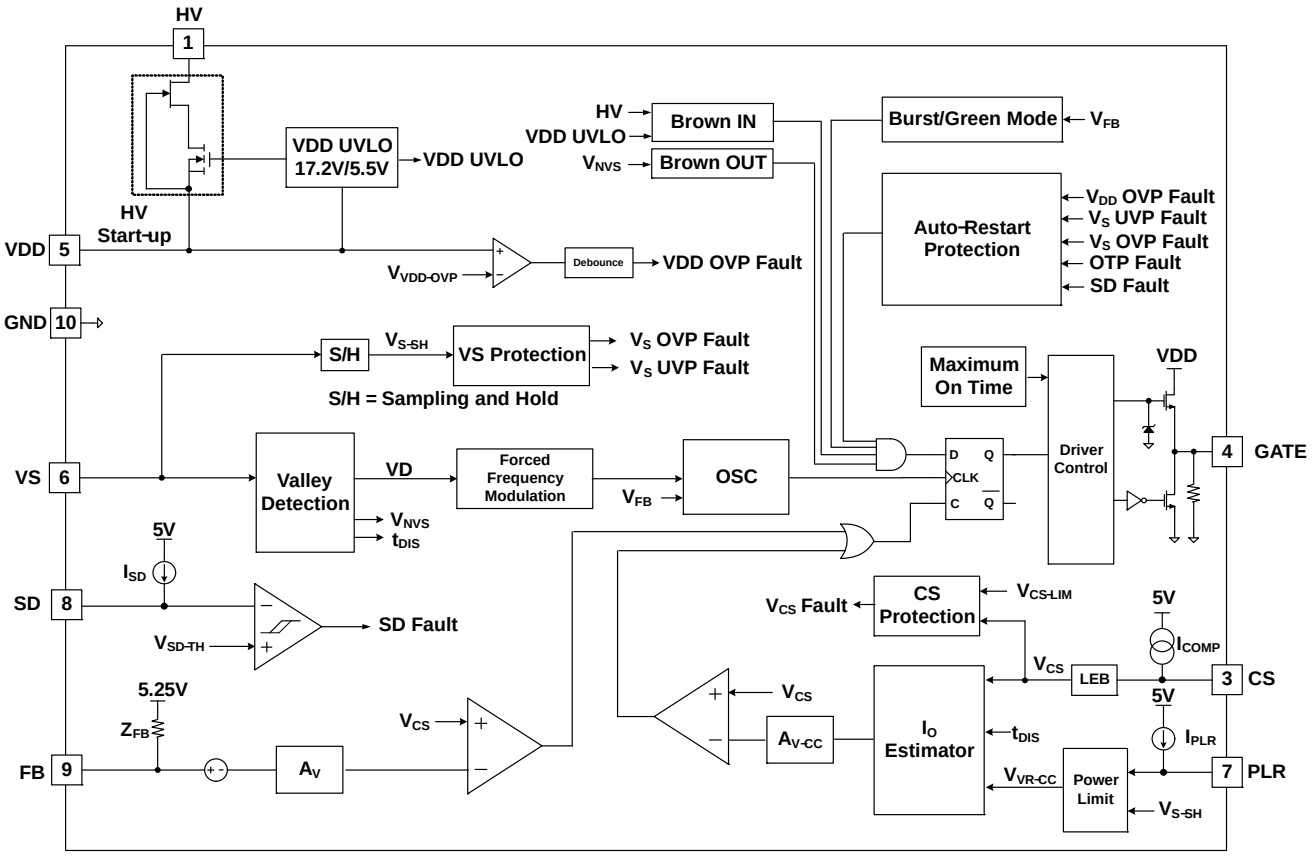


Figure 2. FAN604P Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	HV	**High Voltage**. This pin connects to DC bus for high−voltage startup.
2	NC	**No Connect**.
3	CS	**Current Sense**. This pin connects to a current−sense resistor to sense the MOSFET current for Peak−Current−Mode control for output regulation. The current sense information is also used to estimate the output current for CC regulation.
4	GATE	**PWM Signal Output**. This pin has an internal totem−pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 14.5 V.
5	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external VDD capacitor.
6	VS	**Voltage Sense**. The VS voltage is used to detect resonant valleys for quasi−resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brown−out protection.
7	PLR	**Power Limit Reference**. This pin connects to external resistor to program the reference voltage of output power limit level.
8	SD	**Shut Down**. This pin is implemented for external over−temperature−protect by connecting NTC thermistor.
9	FB	**Feedback**. Typically Opto−Coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
10	GND	**Ground**.

Table 2. MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Maximum Voltage on HV Pin		V_{HV}	500	V
DC Supply Voltage		V_{VDD}	30	V
Maximum Voltage on GATE Pin		V_{GETE}	−0.3 to 30	V
Maximum Voltage on Low Power Pins (Except Pin 3, Pin 4, Pin 6)		V_{max}	−0.3 to 6	V
Power Dissipation (T_A = 25°C)		P_D	850	mW
Thermal Resistance (Junction−to−Ambient)		θ_{JA}	140	°C/W
Thermal Resistance (Junction−to−Top)		θ_{JT}	13	°C/W
Operating Junction Temperature		T_J	−40 to +150	°C
Storage Temperature Range		T_{STG}	−40 to +150	°C
Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114	ESD	2.0	kV
	Charged Device Model, JEDEC:JESD22_C101		0.5	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101
4. ESD ratings including HV pin: HBM = 1.0 kV, CDM = 0.5 kV

Table 3. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
HV Pin Supply Voltage	V_{HV}	50	400	V
VDD Pin Supply Voltage	V_{VDD}	6	25	V
VS Pin Supply Voltage	V_{VS}	1	3.65	V
CS Pin Supply Voltage	V_{CS}	0	0.9	V
FB Pin Supply Voltage	V_{FB}	0	5.25	V
PLR Pin Supply Voltage	V_{PLR}	1	3.5	V
SD Pin Supply Voltage	V_{SD}	0	5	V
Operating Temperature	T_A	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. ON Semiconductor does not recommend exceeding them or designing to Maximum Ratings.

Table 4. ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C, V_{DD} = 15 V; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
HV Section						
Supply Current Drawn from HV Pin	V_{HV}=120 V, V_{DD}=0 V	I_{HV}	1.2	2.0	10	mA
Leakage Current Drawn from HV Pin	V_{HV}=500 V, V_{DD}=V_{DD-OFF}+1 V	I_{HV-LC}	0	0.8	10	μA
Brown−In Threshold Voltage	R_{HV}=150kΩ, V_{IN} =80V_{AC}	$V_{Brown-IN}$	100	110	120	V
VDD Section						
Turn−On Threshold Voltage	V_{DD} Rising	V_{DD-ON}	15.3	17.2	18.7	V
Turn−Off Threshold Voltage	V_{DD} Falling	V_{DD-OFF}	5.0	5.5	5.7	V
Threshold Voltage for HV Startup	T_J = 25°C	$V_{DD-HV-ON}$	4.1	4.7	5.4	V
Startup Current	V_{DD}=V_{DD-ON}−0.16 V	I_{DD-ST}	-	300	450	μA
Operating Supply Current		I_{DD-OP}	-	2	3	mA
Burst−Mode Operating Supply Current		$I_{DD-Burst}$	-	300	600	μA
V_{DD} Over−Voltage−Protection Level	T_J = 25°C	$V_{VDD-OVP}$	27.5	29.0	29.5	V
V_{DD} Over−Voltage−Protection Debounce Time		$t_{D-VDDOVP}$	-	70	140	μs
Oscillator Section						
Maximum Blanking Frequency	V_{FB} > $V_{FB-BNK-H}$	$f_{BNK-MAX}$	125	130	135	kHz
Minimum Blanking Frequency	V_{FB} < $V_{FB-BNK-L}$	$f_{BNK-MIN}$	22	25	28	kHz
Minimum Frequency	V_{VS} = 1V	$f_{OSC-MIN}$	15	17	19	kHz
Forced Frequency Modulation Range	$V_{FB>}$ $V_{FB-Burst--H}$	$\Delta t_{FM-Range}$	210	265	310	ns
Forced Frequency Modulation Period		$\Delta t_{FM-Period}$	2.1	2.5	2.9	ms
Current−Sense Section						
Current Limit Threshold Voltage	T_J = −5°C to 85°C	V_{CS-LIM}	0.865	0.890	0.915	V
Threshold Voltage of Current Sense		$V_{CS-IMIN}$	0.19	0.24	0.29	V
GATE Output Turn−Off Delay (Note 6)		t_{PD}	-	50	100	ns
Leading−Edge Blanking Time		t_{LEB}	-	300	350	ns
Power Limit Section						
PLR Pin Source Current	T_J = 25°C	I_{PLR}	19.8	20	20.2	μA
Peak Value Amplifying Gain (Note 6)		A_{PK}	−	2.7	−	V/V
Internal Voltage Attenuator of FB CC (Note 6)		A_{V-CC}	-	0.444	-	V/V
Constant Current Control Reference Voltage (Note 7)	V_{VS-SH} = 3.0V, T_J = 25°C	$V_{VR-CC-CL-1}$	0.513	-	0.545	V
	V_{VS-SH} = 2.5V, T_J = 25°C	$V_{VR-CC-CL-2}$	0.603	-	0.667	V
	V_{VS-SH} = 2.0V, T_J = 25°C	$V_{VR-CC-CL-3}$	0.747	-	0.827	V
	V_{VS-SH} = 1.5V, T_J = 25°C	$V_{VR-CC-CL-4}$	0.987	-	1.096	V
	V_{VS-SH} = 1.0V, T_J = 25°C	$V_{VR-CC-CL-5}$	1.454	-	1.614	V
Constant Current Correction Section						
High Line Compensation Current	V_{IN} = 264 V_{rms}	I_{COMP-H}	90	100	110	μA
Low Line Compensation Current	V_{IN} = 90 V_{rms}	I_{COMP-L}	32	36	40	μA
Over−Temperature Protection Section						
Threshold Temperature for Over−Temperature−Protection (Note 6)	Threshold Temperature for Over−Temperature−Protection (Note 6)	T_{OTP}	-	140	-	°C
Voltage−Sense Section						
Maximum VS Source Current Capability		I_{VS-MAX}	-	-	3	mA
VS Sampling Blanking Time L	V_{FB} < 2.0V	$t_{VS-BNK-L}$	0.84	1.0	1.23	μs
VS Sampling Blanking Time H	V_{FB} > 2.2V	$t_{VS-BNK-H}$	1.45	1.8	2.15	μs

Table 4. ELECTRICAL CHARACTERISTICS (continued)
For typical values T_J = 25°C, for min/max values T_J = −40°C to 125°C, V_{DD} = 15 V; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VS Source Current Threshold to Enable Brown−OUT		$I_{VS-Brown-OUT}$	360	450	530	μA
Brown−OUT Debounce Time		$t_{D-Brown-OUT}$	12.5	16.5	21	ms
Output Over−Voltage-Protection with Vs Sampling Voltage		V_{VS-OVP}	3.395	−	3.655	V
Output Over−Voltage-Protection Debounce Pulse Counts		N_{VS-OVP}	−	2	−	Pulse
Output Under−Voltage-Protection with Vs Sampling Voltage	T_J = 25°C	V_{VS-UVP}	1.25	1.35	1.45	V
Output Under−Voltage Protection Blanking Time at start−up		$t_{VS-UVP-BLANK}$	120	150	180	ms
Auto−Restart Cycle Counts when Extend Auto−Restart Mode is triggered	$V_{VS} < V_{VS-UVP}$	$N_{VDD-Hiccup}$	-	2	-	Cycle
Feedback Input Section						
FB Pin Input Impedance		Z_{FB}	39	42	45	kΩ
Internal Voltage Attenuator of FB Pin (Note 6)		A_V	1/3	1/3.5	1/4	V/V
FB Pin Pull−Up Voltage	FB Pin Open	$V_{FB-Open}$	4.55	5.25	5.90	V
Frequency Foldback Starting/Stopping VFB		$V_{FB-BNK-H}$	1.5	1.85	2.2	V
		$V_{FB-BNK-L}$	0.75	1.0	1.2	V
FB Threshold to Enable/Disable Gate Drive in Burst Mode	V_{FB} Rising	$V_{FB-Burst-H}$	0.65	0.75	0.85	V
	V_{FB} Falling	$V_{FB-Burst-L}$	0.60	0.70	0.80	V
Shut−Down Function Section						
SD Pin Source Current		I_{SD}	90	103	110	μA
Threshold Voltage for Shut−Down Function Enable		V_{SD-TH}	0.95	1.00	1.05	V
Debounce Time for Shut−Down Function		t_{D-SD}	200	400	600	μs
Ratio between threshold voltage and source current		Z_{SD-TH}	8.5	10	11	kΩ
Hysteresis of Threshold Voltage for Shut−Down Function Enable		$V_{SD-TH-ST}$	1.10	1.15	1.20	V
Duration of $V_{SD-TH-ST}$ at startup		t_{SD-ST}	0.4	1.0	1.6	ms
GATE Section						
Gate Output Voltage Low		V_{GATE-L}	0	-	1.5	V
Internal Gate PMOS Driver ON		$V_{DD-PMOS-ON}$	7.0	7.5	8.0	V
Internal Gate PMOS Driver OFF		$V_{DD-PMOS-OFF}$	9.0	9.5	10.0	V
Rising Time		t_r	70	110	150	ns
Falling Time		t_f	30	50	70	ns
Gate Output Clamping Voltage	T_J = 25°C	$V_{GATE-CLAMP}$	13.6	14.5	15	V
Maximum On Time		t_{ON-MAX}	20	22	25	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Design guaranteed.
7. $V_{VR-CC-CL-x} = (0.75*V_{PLR}/V_{VS-SH})*(1/A_{V-CC})*(1/A_{PK})$; V_{PLR} = 2.54V.

TYPICAL CHARACTERISTICS

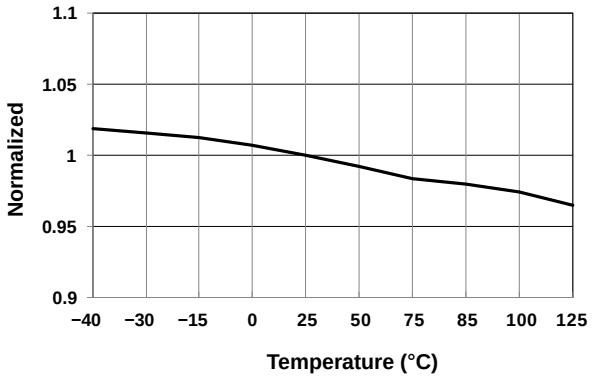


Figure 3. Turn−On Threshold Voltage ($V_{DD−ON}$) vs. Temperature

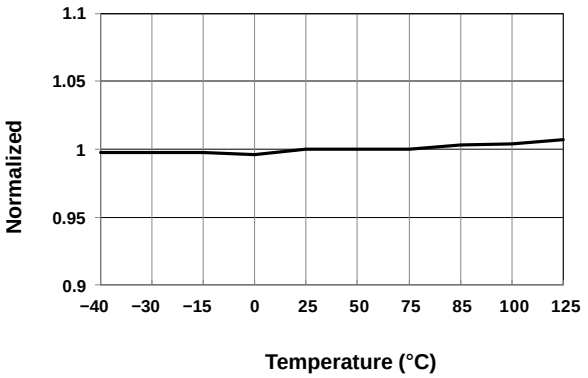


Figure 4. Turn−Off Threshold Voltage ($V_{DD−OFF}$) vs. Temperature

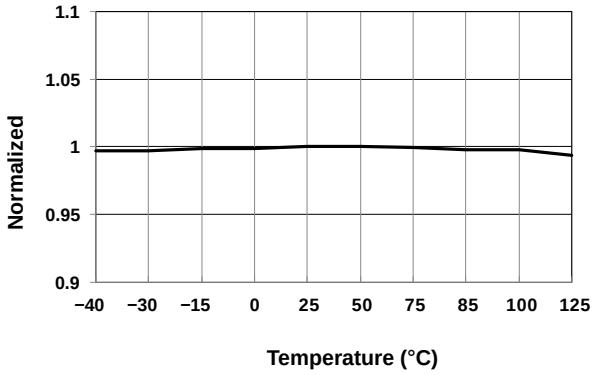


Figure 5. V_{DD} Over Voltage Protection Level ($V_{VDD−OVP}$) vs. Temperature

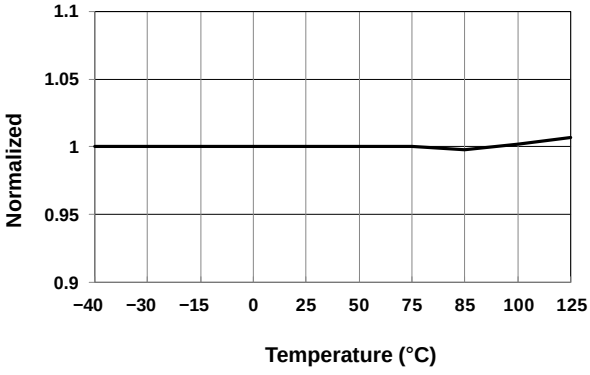


Figure 6. VS Brown−In Threshold Voltage ($V_{Brown−IN}$) vs. Temperature

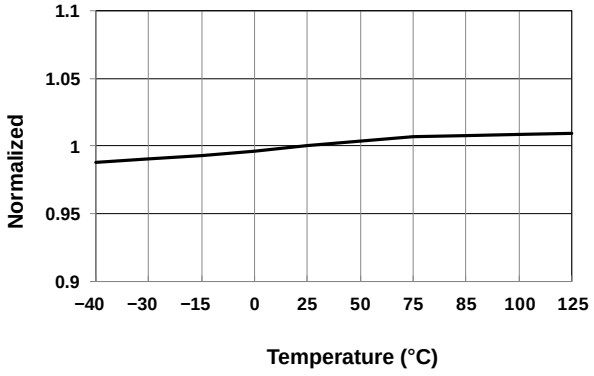


Figure 7. Maximum Blanking Frequency ($f_{BNK−MAX}$) vs. Temperature

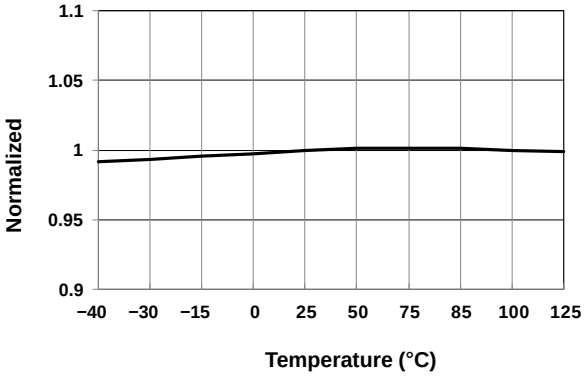


Figure 8. Minimum Blanking Frequency ($f_{BNK−MIN}$) vs. Temperature

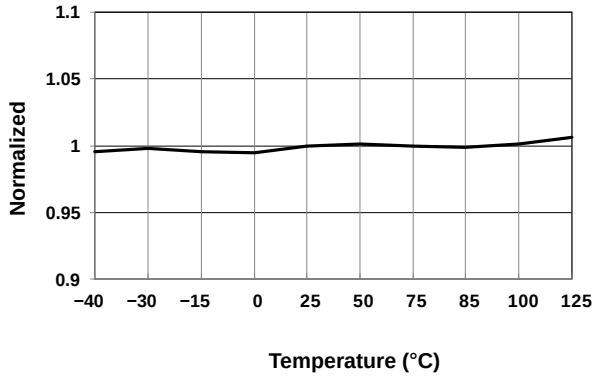


Figure 9. Frequency Foldback Starting VFB ($V_{FB-BNK-H}$) vs. Temperature

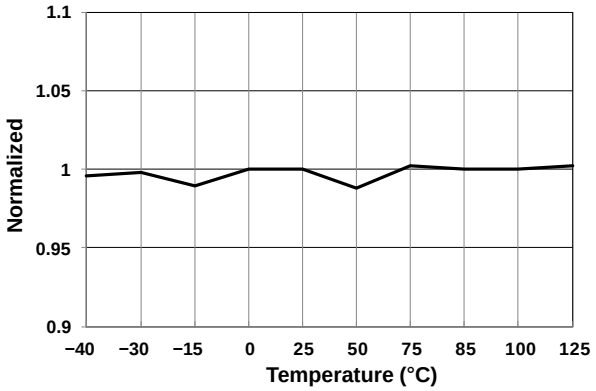


Figure 10. Frequency Foldback Stopping VFB ($V_{FB-BNK-L}$) vs. Temperature

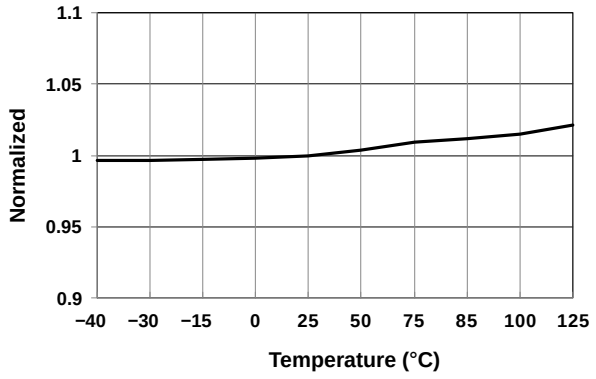


Figure 11. VS Sampling Blanking Time L ($t_{VS-BNK-L}$) vs. Temperature

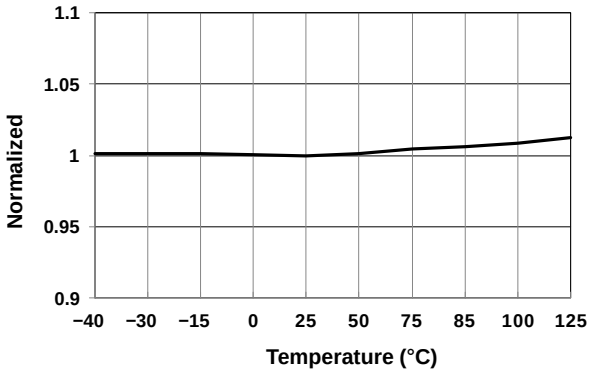


Figure 12. VS Sampling Blanking Time H ($t_{VS-BNK-H}$) vs. Temperature

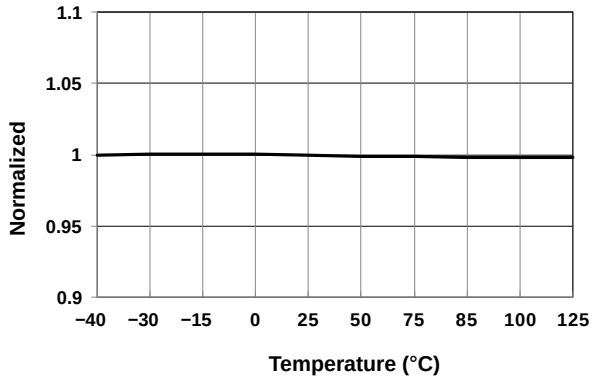


Figure 13. Output Over−Voltage Protection (V_{VS-OVP}) vs. Temperature

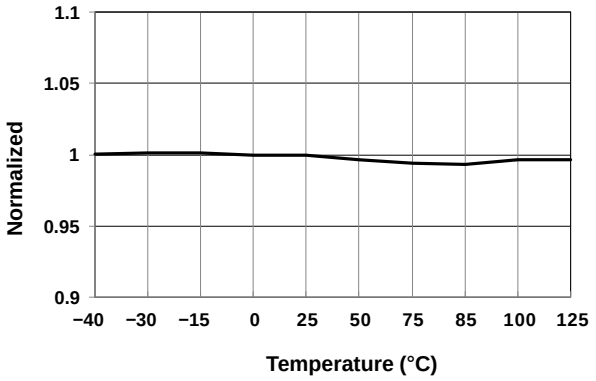


Figure 14. Output Under−Voltage Protection (V_{VS-UVP}) vs. Temperature

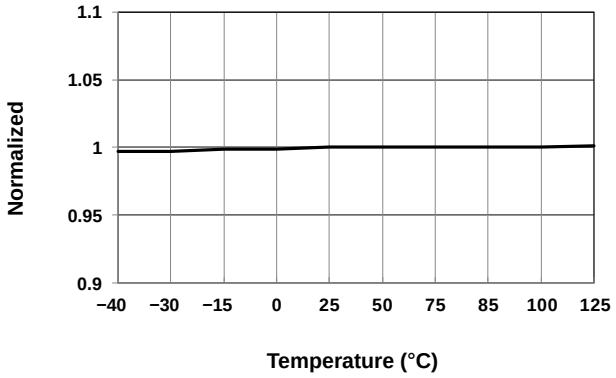


Figure 15. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

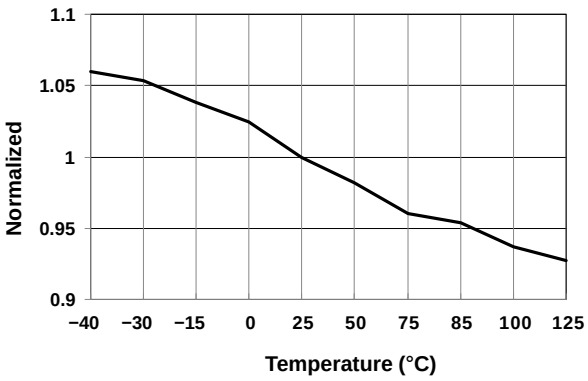


Figure 16. Threshold Voltage of Current Sense ($V_{CS-IMIN}$) vs. Temperature

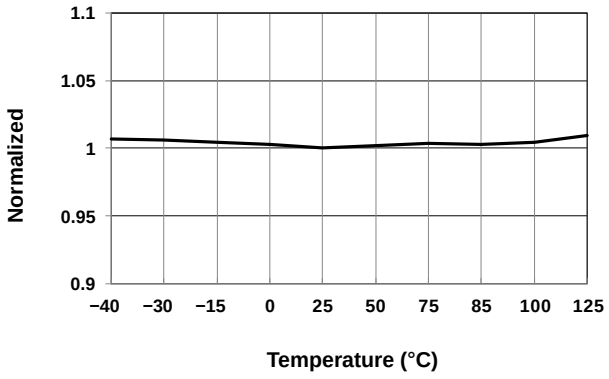


Figure 17. Ratio between Threshold Voltage and Source Current (Z_{SD-TH}) vs. Temperature

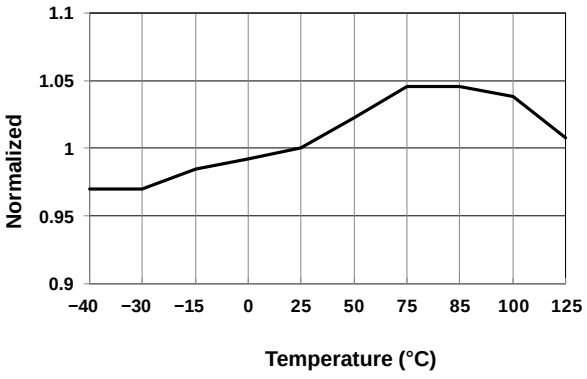


Figure 18. During of $V_{SD-TH-ST}$ at Startup (t_{SD-ST}) vs. Temperature

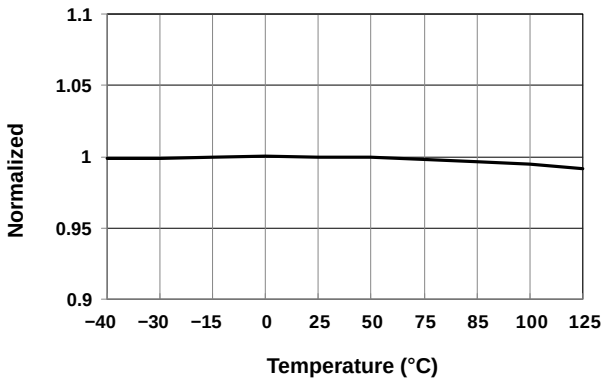


Figure 19. RLR Pin Source Current (I_{PLR}) vs. Temperature

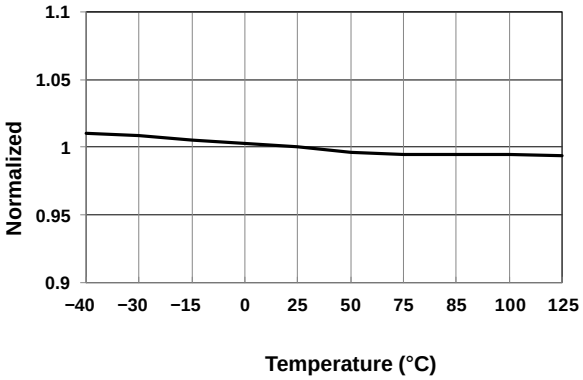


Figure 20. Maximum On Time (t_{ON-MAX}) vs. Temperature

APPLICATIONS INFORMATION

FAN604P is an offline PWM controller which operates in a quasi−resonant (QR) mode and significantly enhances system efficiency and power density. Its control method is based on the load condition (valley switching with fixed blanking time at heavy load and valley switching with variable blanking time at medium load) to maximize the efficiency. It offers constant output voltage (CV) regulation through opto−coupler feedback circuitry.

Line voltage compensation gain can be programmed by using an external resistor to minimize the effect of line voltage variation on output current regulation due to turn−off delay of the gate drive circuit.

FAN604P incorporates HV startup and accurate brown−in through HV pin. The brown−in voltage is programmed by using an external HV pin resistor. The power limit reference (PLR), which sets the maximum output power level, is programmable via an external resistor connected to the PLR pin.

Protections such as V_{DD} Over−Voltage Protection (V_{DD} OVP), V_S Over−Voltage Protection (V_S OVP), V_S Under−Voltage Protection (V_S UVP), internal Over−Temperature Protection (OTP), Brownout protection and externally triggered shut−down (SD) function improve reliability.

Basic Operation Principle

Quasi−resonant switching is a method to reduce primary MOSFET switching losses low line is more effective. In order to perform QR turn−on of the primary MOSFET, the valley of the resonance occurring between transformer magnetizing inductance (L_m) and MOSFET effective output capacitance ($C_{oss-eff}$) must be detected.

$$C_{OSS-eff} = C_{OSS-MOSFET} + C_{Trans} + C_{Parasitic} \quad \text{(eq. 1)}$$

$$t_{Resonance} = 2\pi\sqrt{L_m \cdot C_{OSS-eff}} \quad \text{(eq. 2)}$$

For heavy load condition (50%~100% of full load), the blanking time for the valley detection is fixed such that the switching time is between $1/f_{BNK-MAX}$ and $1/f_{BNK-MAX} + t_{Resonance}$ and primary side peak current will be modulated by voltage level of feedback. For the medium load condition (25%~50% of full load), the blanking time is modulated as a function of load current such that the upper limit of the blanking frequency varies from $f_{BNK-MAX}$ as load decreases where the blanking frequency reduction stop point is $f_{BNK-MIN}$. For the light load condition (5%~25%)), the blanking time for the valley detection is fixed such that the switching time is between $f_{BNK-MIN}$ and $f_{BNK-MIN} + t_{resonance}$ and primary side peak current will be modulated by the function of $V_{CS-IMIN}$ modulation, as shown in Figure 22.

Burst Mode Operation

Figure 21 shows when V_{FB} drops below $V_{FB-Burst-L}$, the PWM output shuts off and the output voltage drops at a rate which is depended on the load current level. This causes the feedback voltage to rise. Once V_{FB} exceeds $V_{FB-Burst-H}$, FAN604P resumes switching. When the FB voltage drops below the corresponding $V_{CS-IMIN}$, the peak currents in switching cycles are limited by $V_{CS-IMIN}$ regardless of FB voltage. Thus, more power is delivered to the load than required and once FB voltage is pulled low below $V_{FB-Burst-L}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the MOSFET to reduce the switching losses.

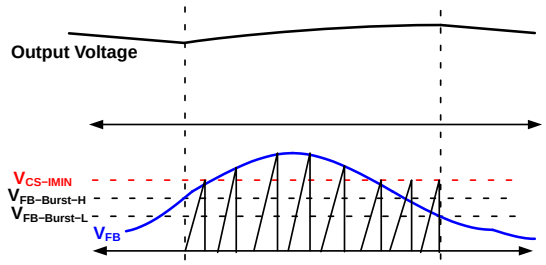


Figure 21. Burst−Mode Operation

Deep Burst Mode

FAN604P enters deep burst mode if FB voltage stays lower than $V_{FB-Burst-L}$ for more than $t_{Deep-Burst-Entry}$ (640 μs). Once FAN604P enters deep burst mode, the operating current is reduced to $I_{DD-Burst}$ (300 μA) to minimize power consumption. Once feedback voltage is more than $V_{FB-Burst-H}$, power−on−reset occurs within a time period of $t_{Deep-Burst-Exit}$ (25 μs) and IC resumes switching with normal operating current, I_{DD-OP}.

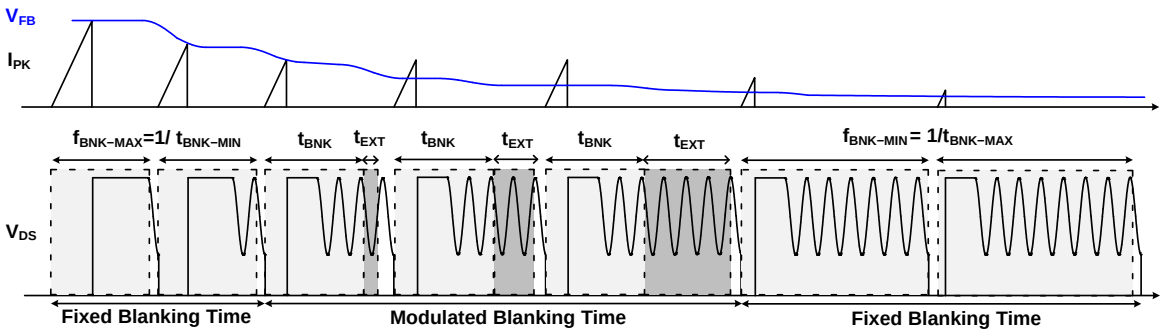


Figure 22. Frequency Fold−Back Function

Valley Detection

There will be a logic propagation delay from VS Zero−Crossing Detection (V_{S-ZCD}) to IC GATE turn on and a MOSFET gate drives propagation delay from GATE pin to MOSFET turn on. We can assume the sum of these propagation delays to be $t_{ZCD-to-PWM}$ (175 ns), as shown in Figure 23. However, if 1/2 t_F is longer than $t_{ZCD-to-PWM}$, the switching occurs away from the valley causing higher losses. The time period of resonant ringing is dependent on L_m and $C_{oss-eff.}$ Typically, the time period of resonance ringing is around 1~1.5 μs depending on the system parameters. Hence, the switching may occur at a point different from the valley depending on the system. When PCB layout is poor, it may cause noise on the VS pin. The VS pin needs to be in parallel with the capacitor (C_{VS}) less than 10 pF to filter the noise.

Inherent and Forced Frequency Modulation

Typically, the bulk capacitor of flyback converter has a longer charging time in low line than in high line. Thus, the voltage ripple (ΔV_{DC}) in low line is higher as shown in Figure 24. This large ripple results in 4~6% variation of the switching frequency in low line for a valley switched converter, the switching frequency could vary accordingly. This frequency variation scatters EMI noise nearby frequency band, this is helpful to meet EMI requirement easily. Hence, the EMI performance in low line is satisfied. However, in high line, the ripple is very small and consequently the EMI performance for high line may suffer. In order to maintain good EMI performance for high line, forced frequency modulation is provided. FAN604P varies the valley switching point from 0 to $\Delta t_{FM-Range}$ (265 ns) in every $\Delta t_{FM-Period}$ (2.5 ms) as shown in Figure 25. Since the drain voltage at which the switching occurs does not change much with this variation, there is minimum impact on the efficiency.

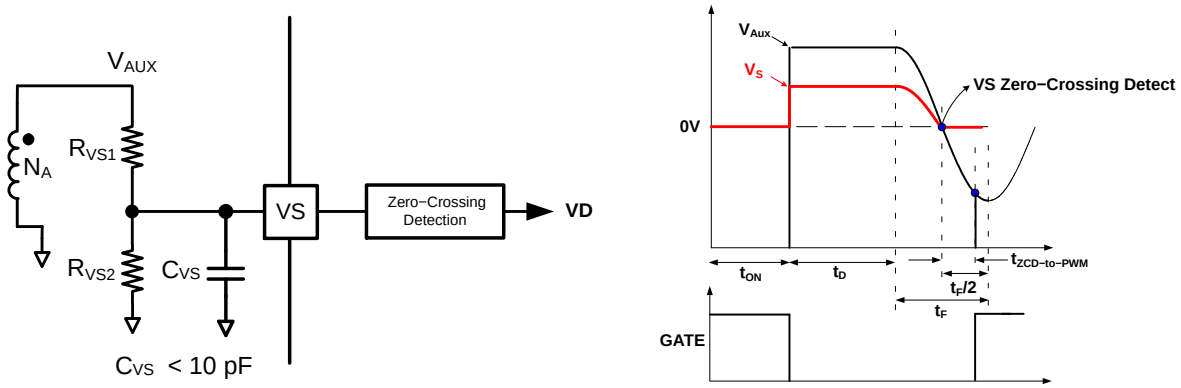


Figure 23. The Valley Detection Circuit and Behavior

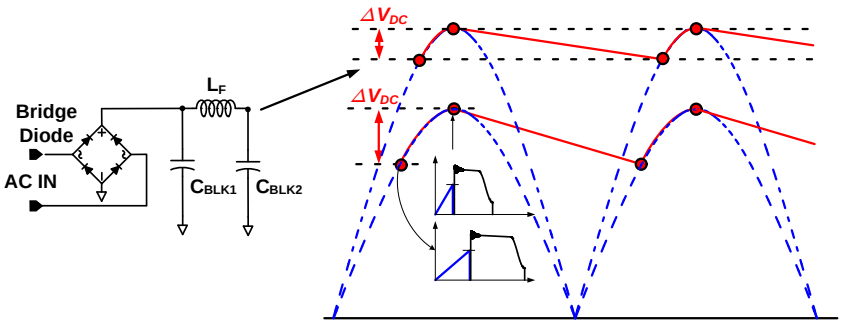


Figure 24. Inherent Frequency Modulation

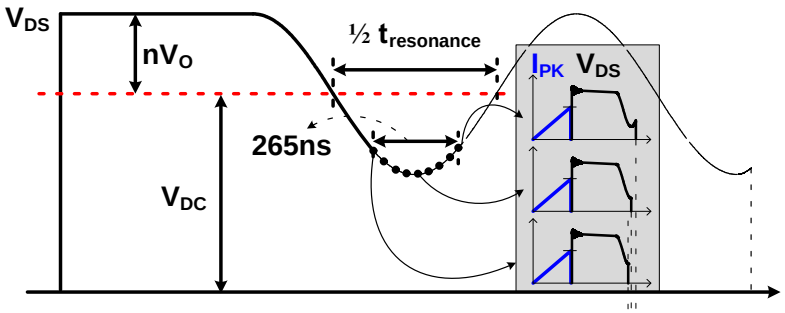


Figure 25. Forced Frequency Modulation

Output Voltage Detection

Figure 26 shows the VS voltage is sampled (V_{S-SH}) after t_{VS-BNK} of GATE turn−off so that the ringing does not introduce any error in the sampling. FAN604P dynamically varies t_{VS-BNK} with load. At heavy load, $t_{VS-BNK}=t_{VS-BNK1}$ (1.8 μs) when V_{FB} > 2.2 V. At light−load, $t_{VS-BNK}=t_{VS-BNK2}$ (1.0 μs) when V_{FB} < 2.0 V. This dynamic variation ensures that VS sampling occurs after ringing due to leakage inductance has stopped and before secondary current goes to zero.

$$V_{S-SH} = V_O \times \frac{N_A}{N_S} \times \frac{R_{VS2}}{R_{VS1} + R_{VS2}} \quad \text{(eq. 3)}$$

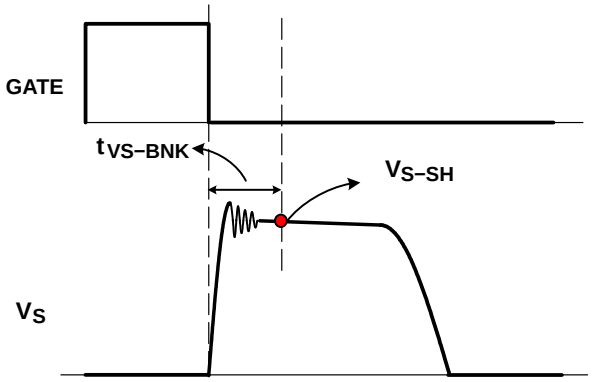


Figure 26. Output Voltage Detection

Line Voltage Detection

The FAN604P indirectly senses the line voltage through the VS pin while the MOSFET is turned on, as illustrated in Figure . MOSFET turn−on period, the auxiliary winding voltage, V_{AUX}, is proportional to the input bulk capacitor voltage, V_{BLK}, due to the transformer coupling between the primary and auxiliary windings. During the MOSFET conduction time, the line voltage detector clamps the VS pin voltage to $V_{S-Clamp}$ (0 V), and then the current I_{VS} flowing out of VS pin is expressed as:

$$I_{VS} = \frac{N_A}{N_P} \times \frac{V_{BLK}}{R_{VS1}} \quad \text{(eq. 4)}$$

The I_{VS} current, reflecting the line voltage information, is used for brownout protection and CC control correction weighting.

CV / CC PWM Operation Principle

Figure 27 shows a simplified CV / CC PWM control circuit of the FAN604P. The Constant Voltage (CV) regulation is implemented in the same manner as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal reference of the shunt regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an opto−coupler and scaled down by attenuator A_V to generate a COMV signal. This COMV signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary−side control. The output current estimator calculates the output current using the transformer primary−side current and diode current discharge time. By comparing the estimated output current with internal reference signal, a COMI signal is generated to determine the duty cycle.

These two control signals, COMV and COMI, are compared with an internal sawtooth waveform (V_{SAW}) by two PWM comparators to determine the duty cycle. Figure 27 illustrates the outputs of two comparators, combined with an OR gate, to determine the MOSFET turn−off instant. Either of COMV or COMI, the lower signal determines the duty cycle. During CV regulation, COMV determines the duty cycle while COMI is saturated to HIGH level. During CC regulation, COMI determines the duty cycle while COMV is saturated to HIGH level.

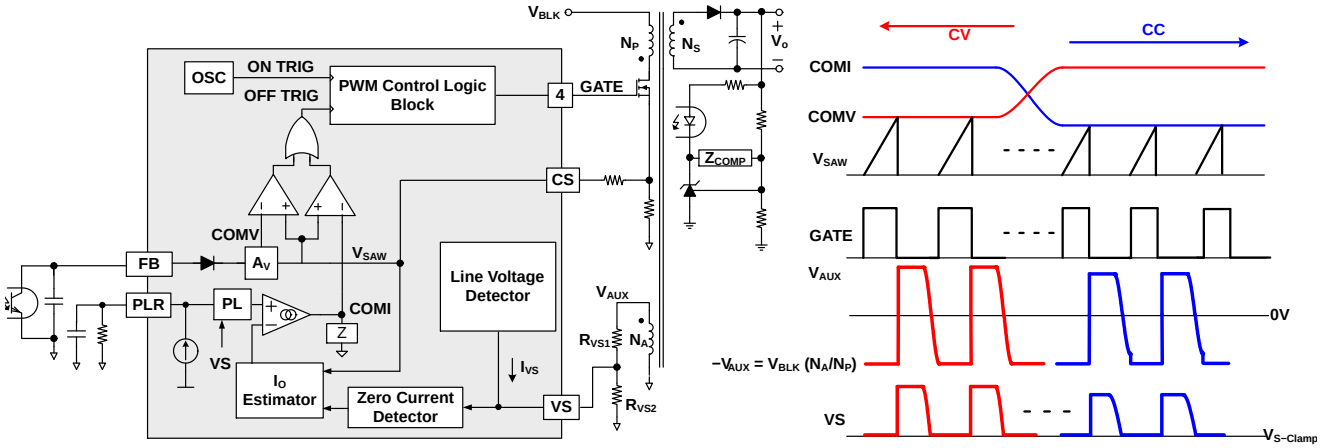


Figure 27. Simplified PWM Control Circuit and PWM Operation for CV/CC Regulation

Power Limit and Output Current Regulation

Figure 28 shows the key waveforms of a flyback converter operation in DCM. The output current is estimated by calculating the average of output diode current in one switching cycle:

$$I_O = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{CS-PK}\,T_{dts}}{T_S}\frac{N_P}{N_S}E_{ff} = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{VR-CC}}{A_{PK}}\frac{N_P}{N_S}E_{ff} \quad \text{(eq. 5)}$$

When the diode current reaches zero, the transformer winding voltage begins to drop sharply and VS pin voltage drops as well. When VS pin voltage drops below the V_{S-SH} by more than 500 mV, zero current detection of diode current is obtained. The V_{VR-CC} is a reference of output current and it can be programmed by setting the resistor as of PLR:

$$V_{VR-CC} = \frac{V_{PLR}}{V_{S-SH}} \times 0.75 = \frac{I_{PLR} \times R_{PLR}}{V_{S-SH}} \times 0.75 \quad \text{(eq. 6)}$$

Where V_{PLR} is a reference voltage for power limit which allows controlling the maximum output power from primary−side.

$$R_{PLR} = \frac{1.33}{I_{PLR}}\left(V_{S-SH} \times 2 \times I_O \times R_{CS} \times A_{PK} \times \frac{N_S}{N_P} \times \frac{1}{E_{ff}}\right) \quad \text{(eq. 7)}$$

When PCB layout is poor, it may cause noise on the PLR pin. The PLR pin needs to be in parallel with the capacitor (C_{PLR}) less than 4.7 nF stabilizing the voltage against noise.

Line Voltage Compensation

The output current estimation is also affected by the turn−off delay of the MOSFET as illustrated in Figure 29. The actual MOSFET's turn−off time is delayed due to the MOSFET gate charge and gate driver's capability, resulting in peak current detection error as

$$\Delta I_{DS}^{PK} = \frac{V_{BLK}}{L_m} \times t_{OFF.FLY} \quad \text{(eq. 8)}$$

Where L_m is the transformer's primary side magnetizing inductance. Since the output current error is proportional to the line voltage, the FAN604P incorporates line voltage compensation to improve output current estimation accuracy. Line information is obtained through the line voltage detector as shown in Figure 27. I_{COMP} is an internal current source, which is proportional to line voltage. The line compensation gain is programmed by using CS pin series resistor, R_{CS_COMP}, depending on the MOSFET turn−off delay, $t_{OFF.DLY}$. I_{COMP} creates a voltage drop, V_{OFFSET}, across R_{CS_COMP}. This line compensation offset is proportional to the DC link capacitor voltage, V_{BLK}, and turn−off delay, $t_{OFF.DLY}$. Figure 29 demonstrates the effect of the line compensation.

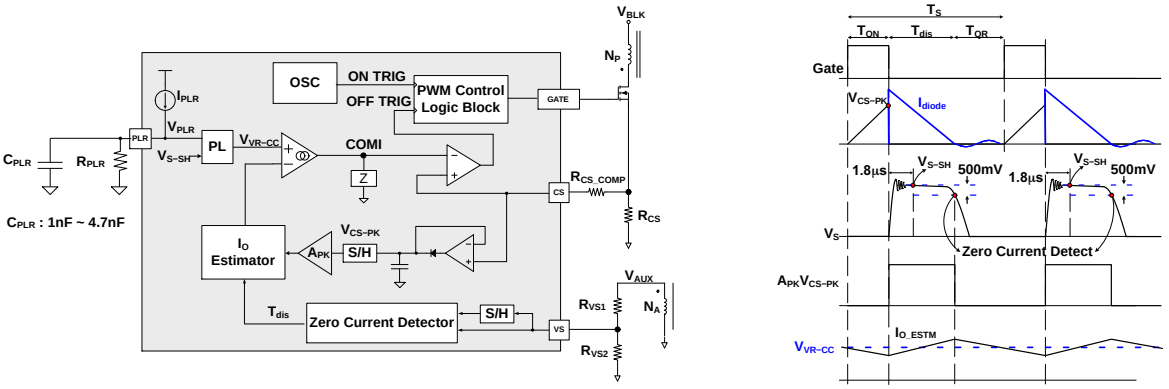


Figure 28. Waveforms for Estimate Output Current

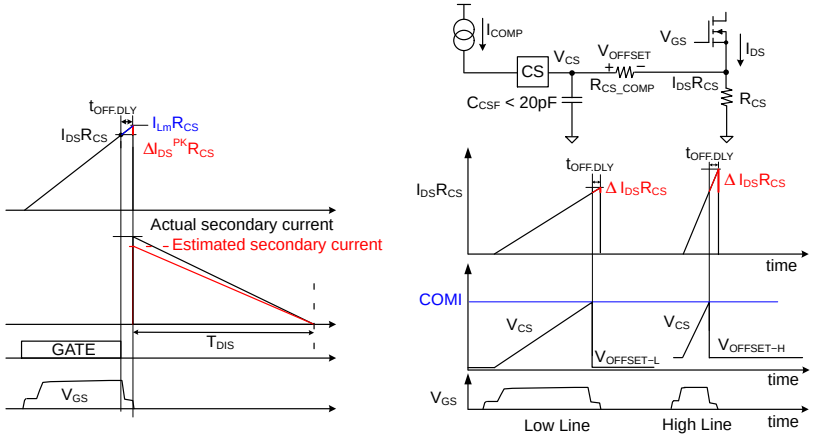


Figure 29. Effect of MOSFET Turn−off Delay and Line Voltage Compensation

CCM Prevention

The constant current calculation logic is based on flyback converter operation in DCM. The output current is estimated by calculating the average of output diode current in one switching cycle. If flyback converter goes into CCM operation, the discharge time of magnetizing current will be fixed. Once this discharge time is fixed, it will increase the average of output diode current.

During the CC region, when output voltage becomes lower, the time that the magnetizing current decreases down to zero is longer, as shown in Figure 30. FAN604P provides the lower operation frequency that can be down to 17 kHz ($f_{OSC-MIN}$) to prevent the system goes into CCM operation.

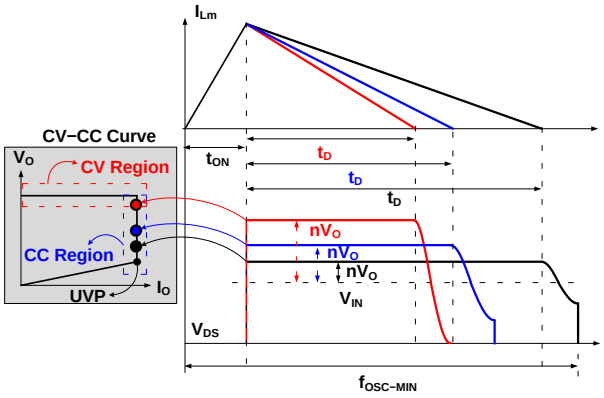


Figure 30. The Minimum Operation Frequency

HV Startup and Brown−In

Figure 31 shows the high−voltage (HV) startup circuit. An Internal JFET provides a high voltage current source, whose characteristics are shown in Figure 32. To improve reliability and surge immunity, it is typical to use a R_{HV} resistor between the HV pin and the bulk capacitor voltage. The actual current flowing into the HV pin at a given bulk capacitor voltage and startup resistor value is determined by the intersection point of characteristics I−V line and the load line as shown in Figure 32.

During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current, I_{HV}, to charge the hold−up capacitor, C_{VDD}, through R_{HV}. When the V_{DD} voltage reaches V_{DD-ON}, the sampling circuit shown in Figure 31 is turned on for t_{HV-det} (100 μs) to sample the bulk capacitor voltage. Voltage across R_{LS} is compared with reference which generates a signal to start switching. If brown−in condition is not detected within this time, switching does not start. Equation (9) can be used to program the brown−in of the system. If line voltage is lower than the programmed brown−in voltage, FAN604P goes in auto−restart mode.

$$V_{IN} = \frac{R_{LS} + R_{JEFT} + R_{HV}}{R_{LS}} \times V_{REF} \qquad \text{(eq. 9)}$$

Once switching starts, the internal HV startup circuit is disabled. During normal switching, the line voltage information is obtained from the I_{VS} signal. Once the HV startup circuit is disabled, the energy stored in C_{VDD} supplies the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{VDD} should be properly designed to prevent V_{DD} from dropping below V_{DD-OFF} threshold (typically 5.5 V) before the auxiliary winding builds up enough voltage to supply V_{DD}. During startup, the IC current is limited to I_{DD-ST} (300 μA).

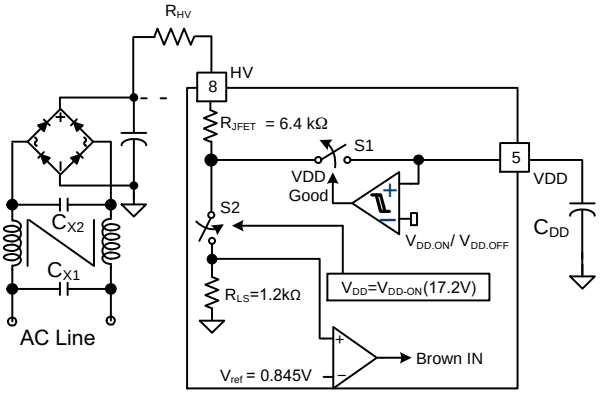


Figure 31. HV Startup Circuit

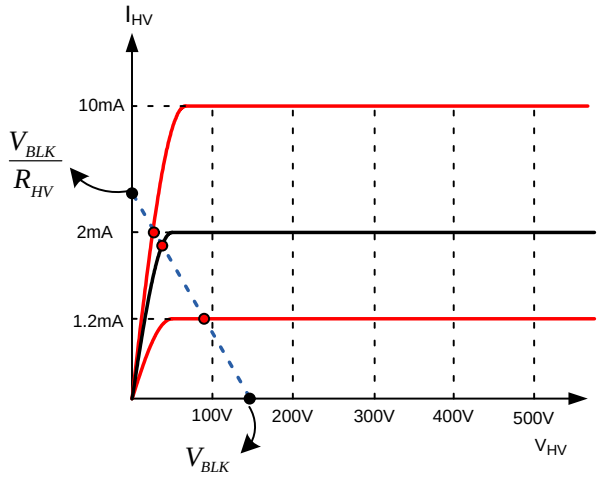


Figure 32. Characteristics of HV Pin

Protections

The FAN604P protection functions include VDD Over−Voltage Protection (VDD−OVP), brownout protection, VS Over−Voltage Protection (VS−OVP), VS Under−Voltage Protection (VS−UVP), and IC internal Over−Temperature Protection (OTP). The VDD−OVP, brownout protection, VS−OVP and OTP are implemented with Auto−Restart mode. The VS−UVP is implemented with Extend Auto−Restart mode.

When the Auto−Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing VDD to drop because of IC operating current I_{DD-OP} (2 mA). When VDD drops to the VDD turn−off voltage of V_{DD-OFF} (5.5 V), operation current reduces to $I_{DD-Burst}$ (300 μA). When the VDD voltage drops further to $V_{DD-HV-ON}$, the protection is reset and the supply current drawn from HV pin begins to charge the VDD hold−up capacitor. When VDD reaches the turn−on voltage of V_{DD-ON} (17.2 V), the FAN604P resumes normal operation. In this manner, the Auto−Restart mode alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated as shown in Figure 33. When the Extend Auto−Restart Mode protection is triggered via VS under−voltage protection (VS−UVP), switching is terminated and the MOSFET remains off, causing VDD to drop. While V_{DD} drops to $V_{DD-HV-ON}$ for HV startup circuit enable, then IC enters Extend Auto−Restart period with two cycles as shown Figure 34. During Extend Auto−Restart period, VDD voltage swings between V_{DD-ON} and $V_{DD-HVON}$ without gate switching, and IC operation current is reduced to $I_{DD-Burst}$ of 300 μA for slowing down the VDD capacitor discharging slope. As Extend Auto−Restart period ends, normal operation resumes.

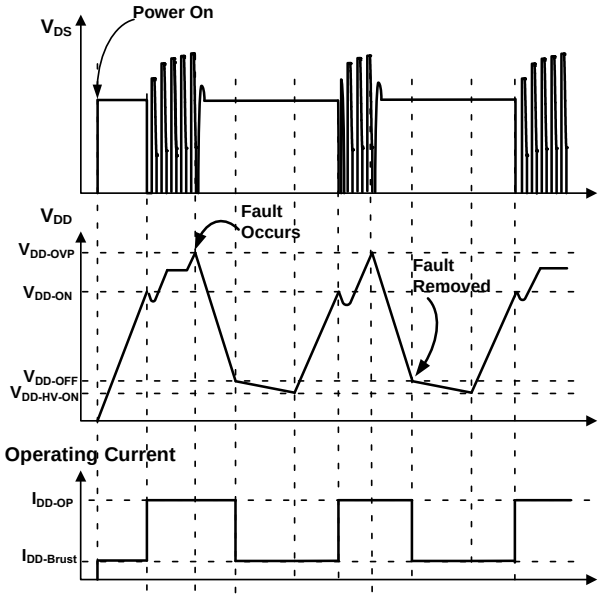


Figure 33. Auto−Restart Mode Operation

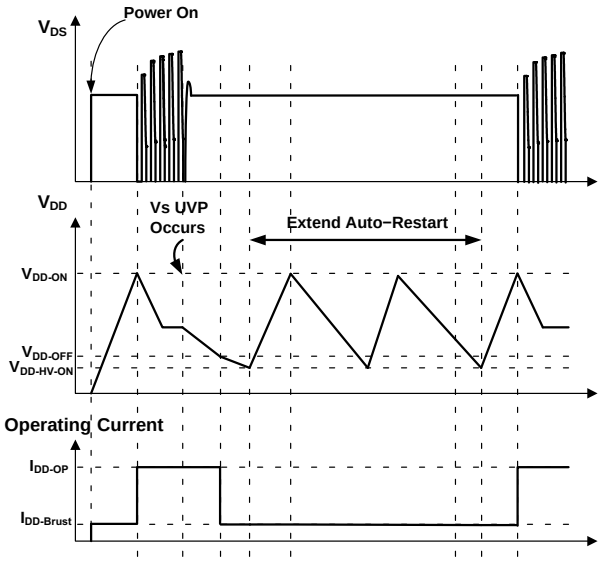


Figure 34. Extend Auto−Restart Mode Operation

VDD Over−Voltage−Protection (VDD−OVP)

VDD over−voltage protection prevents IC damage from over−voltage stress. It is operated in Auto−Restart mode. When the VDD voltage exceeds V_{DD-OVP} (29.0 V) for the de−bounce time, $t_{D-VDDOVP}$ (70 μs), due to abnormal condition, the protection is triggered. This protection is typically caused by an open circuit of secondary side feedback network.

Brownout Protection

Line voltage information is used for brownout protection. When the I_{VS} current out of the VS pin during the MOSFET conduction time is less than 450 μA for longer than 16.5ms, the brownout protection is triggered. The input bulk capacitor voltage to trigger brownout protection is given as

$$V_{BO} = \frac{V_{BLK.MIN}}{1.2} = I_{VS-Brown-OUT} \times \frac{R_{VS1}}{\frac{N_a}{N_P}} \quad \text{(eq. 10)}$$

IC Internal Over−Temperature−Protection (OTP)

The internal temperature−sensing circuit disables the PWM output if the junction temperature exceeds 140°C (T_{OTP}) and the FAN604P enters Auto−Restart Mode protection.

Pulse−by−Pulse Current Limit

During startup or overload condition, the feedback loop is saturated to high and is unable to control the primary peak current. To limit the current during such conditions, FAN604P has pulse−by−pulse current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, V_{CS-LIM} (0.89 V).

VS Over−Voltage−Protection (VS−OVP)

VS over−voltage protection prevents damage caused by output over−voltage condition. It is operated in Auto−Restart mode. Figure 35 shows the internal circuit of VS−OVP protection. When abnormal system conditions occur, which cause VS sampling voltage to exceed V_{VS-OVP} (3.55 V) for more than 2 consecutive switching cycles (N_{VS-OVP}), PWM pulses are disabled and FAN604P enters Auto−Restart protection. VS over−voltage conditions are usually caused by open circuit of the secondary side feedback network or a fault condition in the VS pin voltage divider resistors. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10), and R_{VS2} is determined by the desired VS−OVP protection function as

$$R_{VS2} = R_{VS1} \times \frac{1}{\frac{V_{O-OVP}}{V_{VS-OVP}} \frac{N_A}{N_S} - 1} \quad \text{(eq. 11)}$$

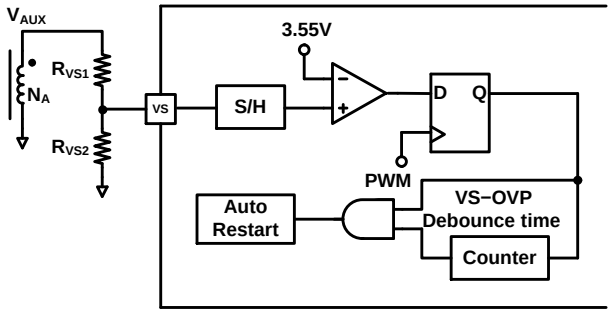


Figure 35. VS−OVP Protection Circuit

VS Under−Voltage−Protection (VS−UVP)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN604P incorporates under−voltage protection through VS pin. Figure 36 shows the internal circuit for VS−UVP. By sampling the auxiliary winding voltage on the VS pin at the end of diode conduction time, the output voltage is indirectly sensed. When V_S sampling voltage is less than V_{VS-UVP} (1.35 V) and longer than de−bounce time, $t_{VS-UVP-BLANK}$ (150 ms), VS−UVP is triggered and the FAN604P enters Extend Auto−Restart Mode.

To avoid VS−UVP triggering during the startup sequence, a startup blanking time, $t_{VS-UVP-BLANK}$ (150 ms), is included for system power on. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10) and R_{VS2} is determined by Equation (11). V_{O-UVP} can be determined by Equation (12).

$$V_{O-UVP} = \frac{N_S}{N_A} \times \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \times V_{VS-UVP} \quad \text{(eq. 12)}$$

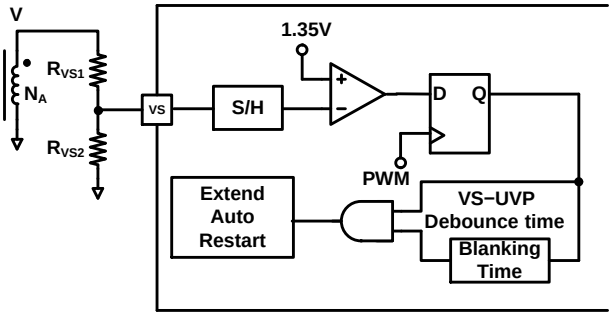


Figure 36. VS−UVP Protection Circuit

Externally Triggered Shutdown (SD)

When V_{DD} is V_{DD-ON}, Shut−Down comparing level is $V_{SD-TH-ST}$ (1.15 V), after the startup time t_{SD-ST} (1 ms), the comparing level is changed to V_{SD-TH} (1.0 V). By pulling down SD pin voltage below the V_{SD-TH} (1.0 V) shutdown can be externally triggered and the FAN604P will enter Auto−Restart mode protection. It can be also used for external Over−Temperature−Protection by connecting a NTC thermistor between the shutdown (SD) programming pin and ground. An internal constant current source I_{SD} (103 μA) creates a voltage drop across the thermistor. The resistance of the NTC thermistor becomes smaller as the ambient temperature increases, which reduces the voltage drop across the thermistor.

SD pin voltage is sampled every gate cycle when $V_{FB} > V_{FB-Burst-H}$ and sampled continuously when $V_{FB} < V_{FB-Burst-L}$. When the voltage at SD pin is sampled to be below the threshold voltage, V_{SD-TH} (1.0 V), for a

de−bounce time of t_{D-SD} (400 μs), Auto−Restart protection is triggered. A capacitor may also be placed in parallel with the NTC thermistor to further improve the noise immunity. The capacitor should be designed such that SD pin voltage is more than $V_{SD-TH-ST}$ within the time of t_{SD-ST}.

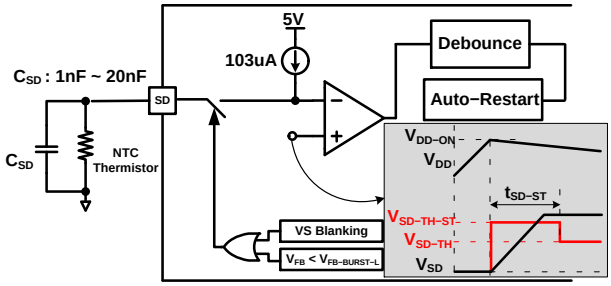


Figure 37. External OTP using SD Pin

Secondary−Side Diode Shot Protection

When the secondary−side diode is damaged, the slope of the primary−side peak current will be sharp within leading−edge blanking time. To limit the current during such conditions, FAN604P has secondary−side diode short protection which forces the GATE to turn off when the CS pin voltage reaches 1.6 V. After one switching cycle, it will operate in Auto−Restart mode.

PCB Layout Guideline

Print circuit board (PCB) layout and design are very import for switching power supplies where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes excessive EMI and prevent the power supply from being disrupted during surge/ESD tests. The following guidelines are recommended for layout designs.

- To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitors C_{BLK1} and C_{BLK2} first, then to the transformer and MOSFET.
- The primary−side high−voltage current loop is **C_{BLK2} − Transformer − MOSFET − R_{CS} − C_{BLK2}**. The area enclosed by this current loop should be as small as possible. The trace for the control signal (FB, CS, VS and GATE) should not go across this primary high−voltage current loop to avoid interference.
- Place R_{HV} for protection against the inrush spike on the HV pin (150 kΩ is recommended).
- R_{CS} should be connected to the ground of C_{BLK2} directly. Keep the trace short and wide (Trace **4** to **1**) and place it close to the CS pin to reduce switching noise. High−voltage traces related to the drain of MOSFET and RCD snubber should be away from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground.
- As indicated by **2**, the area enclosed by the transformer auxiliary winding, D_{AUX} and C_{VDD}, should also be small.
- Place C_{VDD}, C_{VS}, R_{VS2}, C_{FB}, R_{CCR}, C_{CCR}, R_{CS_COMP} and C_{CSF} close to the controller for good decoupling and low switching noise.
- As indicated by **3**, the ground of the control circuits should be connected as a single point first, then to other circuitry.
- Connect ground by **3** to **2** to **4** to **1** sequence. This helps to avoid common impedance interference for the sense signal.
- Regarding the ESD discharge path, use the shortcut pad between AC line and DC output (most recommended). Another method is to discharge the ESD energy to the AC line through the primary−side main ground 1. Because ESD energy is delivered from the secondary side to the primary side through the transformer stray capacitor or the Y capacitor, the controller circuit should not be placed on the discharge path. 5 show where the point−discharge route can be placed to effectively bypass the static electricity energy.

For the surge path, select fusible resistor of wire wound type to reduce inrush current and surge energy and use π input filter (two bulk capacitors and one inductance) to share the surge energy.

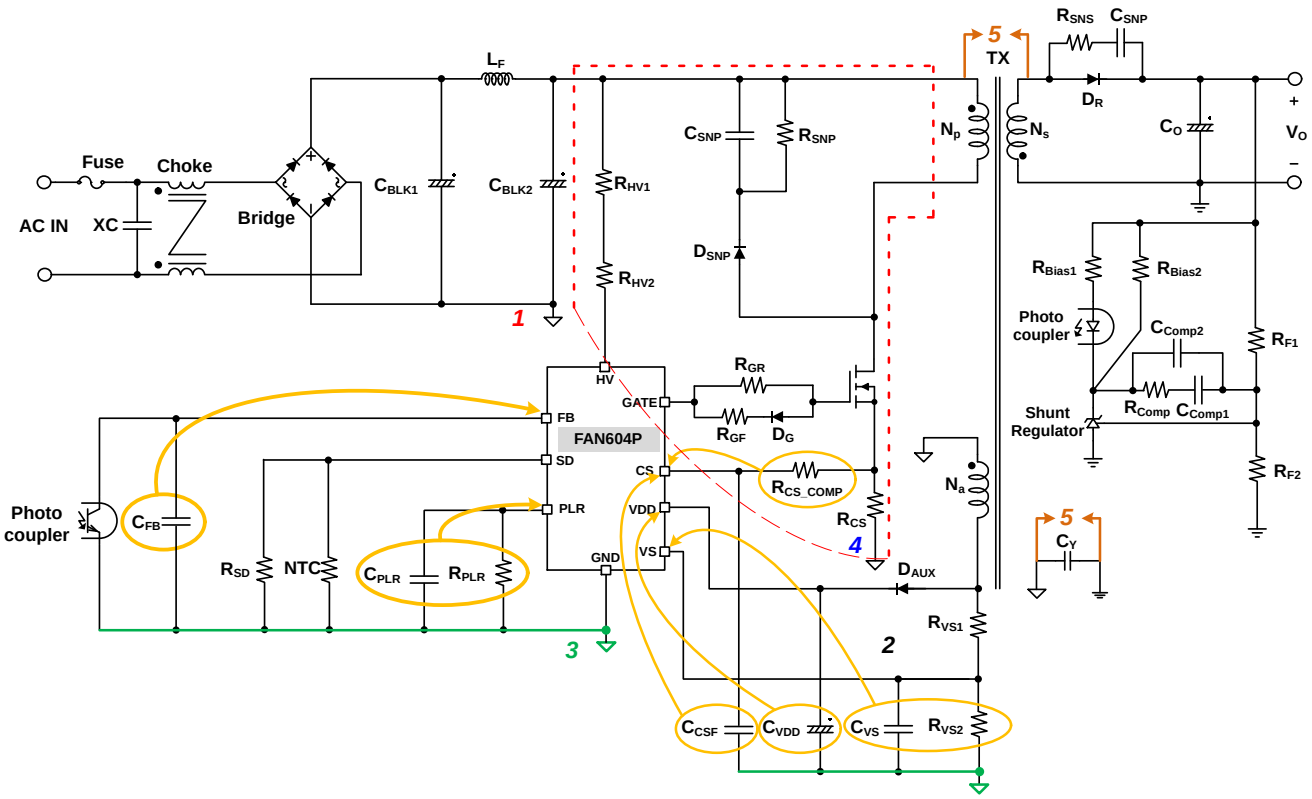
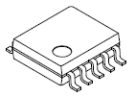


Figure 38. Recommended Layout for FAN604P

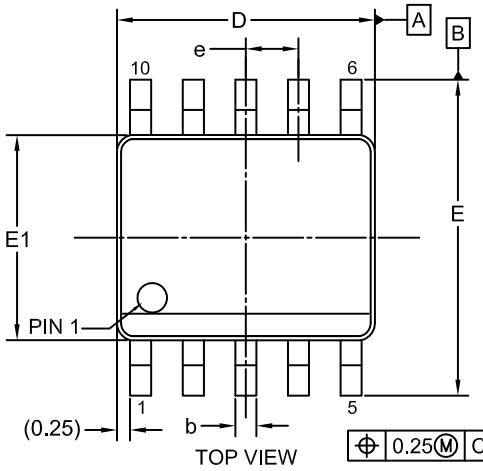
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

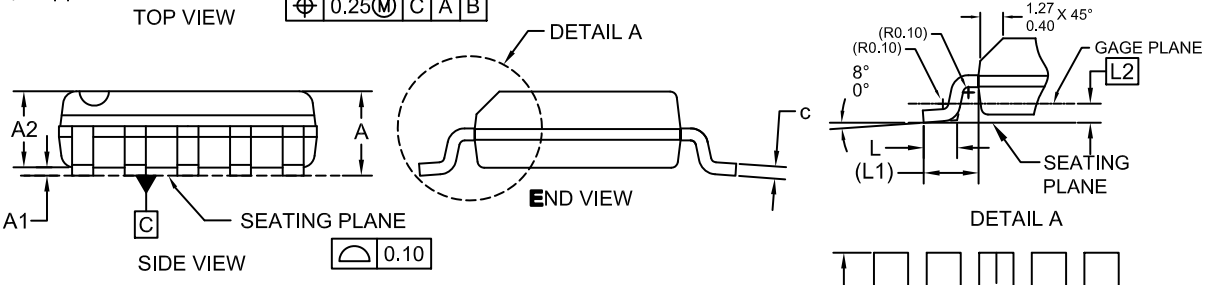


SOIC10, 4.9x6.0, 1.0P
CASE 751EE
ISSUE A

DATE 28 MAY 2019



DIM	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
b	0.30	0.40	0.45
c	0.10	0.20	0.25
D	4.80	4.90	5.00
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.00 BSC		
L	0.40	0.65	1.27
L1	1.04 Reference only		
L2	0.36 BSC		

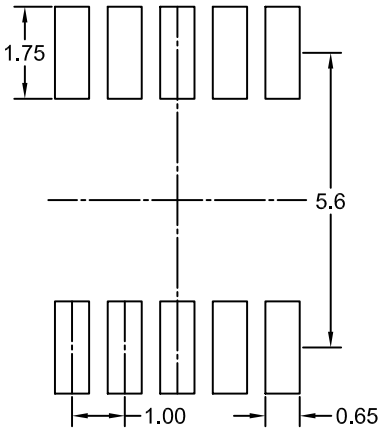


NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
E. LAND PATTERN STANDARD : SOIC127P600X175.10M

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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