AN2020-05 EVAL-1ED3491Mx12M (1ED-X3 Analog)

Evaluation board description

Single-channel isolated gate driver IC with adjustable DESAT and soft-off

About this document

Scope and purpose

The gate driver evaluation board ***EVAL-1ED3491Mx12M*** with the 1ED3491MU12M or 1ED3491MC12M gate driver IC demonstrates the functionality, adjustment possibilities, and key features of the Infineon EiceDRIVER™ 1ED-X3 Analog gate driver ICs.

The boards contain a short circuit protection which is described in more detail in the key feature section of this document.

Details about the EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M or 1ED3491MC12M can be found at our product pages at ***https://www.infineon.com/gdisolated*** or the product search.

The design of the EVAL-1ED3491Mx12M was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full range of operating conditions. The boards provided by Infineon are not subject to full production test.

Evaluation boards are not subject to the same procedures as regular products regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD). Evaluation boards are intended to be used under laboratory conditions and by trained specialists only.

Intended audience

- Engineers who want to learn how to use the Infineon EiceDRIVER™
- Experienced design engineers designing circuits with Infineon EiceDRIVER™, IGBT and CoolSiC™ SiC MOSFET
- Design engineers designing power electronic devices, like inverters

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Gate driver IC information

Features

- 600 V, 650 V, 900 V, and 1200 V IGBTs, SiC and Si MOSFETs
- 40 V absolute maximum output supply voltage
- ±3 A, ±6 A, and ±9 A typical sinking and sourcing peak output current
- Separate source and sink outputs for hard switching and with active Miller clamp/clamp driver
- Adjustment pins for parameter configuration from input side
- Precise V_{CEsat} detection (DESAT) with fault output and adjustable filter time and leading edge blanking time with resistor at *ADJB* pin
- Adjustable IGBT soft turn-off after desaturation detection with resistor at *ADJA* pin
- Operation at high ambient temperature up to 125 °C with over-temperature shut down at 160 °C (±10 °C)
- Tight IC-to-IC propagation delay matching ($t_{PDD,max}$ = 30 ns)
- Undervoltage lockout protection with hysteresis for input and output side with active shut-down
- High common-mode transient immunity CMTI = 200 kV/µs
- Small space-saving DSO-16 fine-pitch package with large creepage distance (>8 mm)
- Safety certification
  - UL 1577 recognized (planned) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - IEC 60747-17/VDE 0884-11 approval (planned) with V_{IORM} = 1.4 kV (peak, reinforced)
- Evaluation board available ***EVAL-1ED3491MX12M***

Potential applications

- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters
- UPS systems
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

PG-DSO-16

Device information

Product type	Output current	CLAMP type[1)]	Isolation class	Marking	OPN
1ED3431MC12M	3 A (typ)	CLAMP	reinforced	3431MC12	coming soon
1ED3461MC12M	6 A (typ)	CLAMPDRV	reinforced	3461MC12	coming soon
1ED3491MC12M	9 A (typ)	CLAMPDRV	reinforced	3491MC12	coming soon
1ED3431MU12M	3 A (typ)	CLAMP	UL 1577	3431MU12	***1ED3431MU12MXUMA1***
1ED3461MU12M	6 A (typ)	CLAMPDRV	UL 1577	3461MU12	***1ED3461MU12MXUMA1***
1ED3491MU12M	9 A (typ)	CLAMPDRV	UL 1577	3491MU12	***1ED3491MU12MXUMA1***

1 Electrical description

The evaluation board EVAL-1ED3491Mx12M is intended for the product feature evaluation of the Infineon EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M or 1ED3491MC12M in an application circuit.

The key elements of the board and the product are listed below:

- Evaluation board in half-bridge configuration with two gate driver ICs to drive power switches such as IGBTs, Si MOSFETs, and CoolSiC™ SiC MOSFETs. The switch type can be freely chosen as seen in ***Figure 1***
- Galvanically isolated power supply for both secondary sides
- Resistors marking for the adjustable functions of each gate driver IC

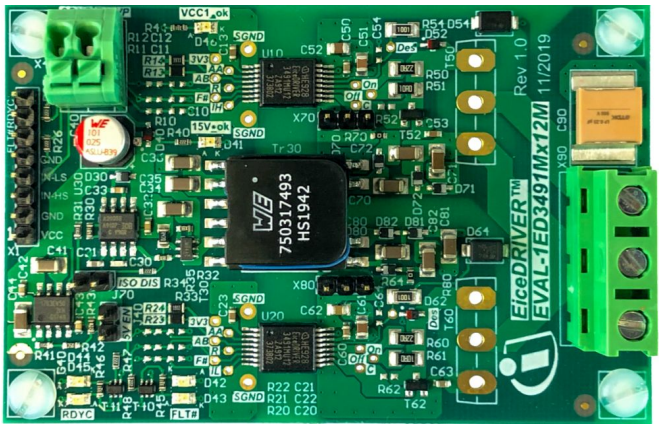

Figure 1 EVAL-1ED3491Mx12M top view

The board has a size of 85 x 55 x 15 mm^3 without any power switch assembled.

This board is best suited for so-called double-pulse testing and evaluation. For continuous operation, the thermal and load power should be taken into consideration. It is also recommended to add an additional high-voltage DC blocking capacitor at the high-voltage supply.

The low-voltage interface can be controlled by a pulse generator, a microcontroller or any other digital circuits.

The adjustable DESAT filters can be adjusted by replacing the resistor attached to the *ADJB* pin of each gate driver IC. Similarly, the soft-off current after DESAT detection can be adjusted by replacing the resistor attached to the *ADJA* pin of each gate driver IC.

The evaluation board has a power supply for the primary and secondary sides implemented. This allows the user to evaluate the gate driver by only supplying a 15 V input voltage. Jumper J40 can be used to adjust the primary side operation voltage, between 5 V and 3.3 V. In case the user wants to use its own power supply,

1 Please refer to ***CLAMP output types*** for circuit connection to avoid damage to the gate driver IC

jumper J70 can be used to disable the power supply for the primary and secondary sides. This will be discussed in more details in the following chapters.

Different LEDs across the board are used to visually feedback the state of the board, showing the presence of the supply voltages and the state of the fault pins. This will be discussed in more details in the following chapters.

1.1 Absolute maximum ratings, operating conditions, and supply voltages

The selected components on this evaluation board as well as the gate driver ICs have maximum ratings and operating conditions to avoid damaging the individual parts and the evaluation board overall.

Table 1 Absolute maximum ratings

Pin/parameter name	Abs. max. rating	Unit	Note
P15VP	-0.3 … 20	V	Input supply voltage of the power supply stage (referenced to *SGND*)
VCC	-0.3 … 6.5	V	Primary side supply voltage (referenced to *SGND*).[2]
RDYC	-0.3 … 6.5	V	Input/output digital signal
FLT#	-0.3 … 6.5	V	Input/output digital signal
IN_HS	-0.3 … 6.5	V	Input digital signal
IN_LS	-0.3 … 6.5	V	Input digital signal
VCC2H,*VCC2L*	-0.3 … 40	V	Isolated secondary positive supply with reference to *GND2H*/*GND2L*[2]
VCC2H,*VCC2L*	-0.3 … 40	V	Overall secondary supply voltage with reference to *VEE2H*/*VEE2L*[2]
VEE2H,*GEE2L*	-40 … 0.3	V	Isolated secondary negative supply with reference to *GND2H*/*GND2L*[2]
P1000VP	-0.2 … 900	V	Input, high-voltage supply reference to GND power terminal, for voltages above 42 V, special safety measures should be taken
Phase peak current	30	A	Phase peak output current for double pulse tests. Maximum current is only limited by the thermal capabilities of the PCB
t_{pulse}	100	µs	maximum ON pulse length for double-pulse tests
f_{sw}	100	kHz	maximum switching frequency for continuous operation, power dissipation should be considered

This evaluation board is optimized for both 5 V and 3.3 V *VCC* supply voltage. Depending on the used input signals, by using jumper J40 (5V EN) the end user can select 5 V or 3.3 V operation. This will affect the input threshold values, which are referenced to *VCC*.

It is recommended to use the board with the built-in power supply circuit. This provides a +15 V/-7 V supply voltage on the secondary sides for both upper and lower side gate drivers.

In case a separate, external power supply is to be used, the built in power supply can be disabled by using the jumper J70 (ISO DIS).

2 Not to be used when power supply circuit is enabled

Table 2 Recommended operating conditions and supply voltages for 5 V operation

Pin name	Min.	Typ.	Max.	Unit	Note
P15VP	15.0	15.5	16.0	V	Power supply input voltage
VCC	4.9	5.0	5.1	V	Gate driver IC primary side input voltage[2)]
FLT#	-0.1	*VCC*	*VCC1*+ 0.1	V	Input/output digital signal
RDYC	-0.1	*VCC*	*VCC1*+ 0.1	V	Input/output digital signal
IN_HS	-0.1	*VCC*	*VCC1*+ 0.1	V	Input digital signal
IN_LS	-0.1	*VCC*	*VCC1*+ 0.1	V	Input digital signal
VCC2H,*VCC2L*	12	22	30	V	Overall isolated secondary power supply as referenced to *VEE2H*/*VEE2L*[2)]
GND2H,*GND2L*	0	7	15	V	Gate reference supply pin as referenced to *VEE2H*/ *VEE2L*[2)]
P1000VP	25		800	V	Input, high voltage supply, for voltages above 42 V, special safety measures should be taken

1.2 Initial settings

The evaluation board comes preconfigured from assembly.

The present DESAT leading edge blanking time is 1150 ns and the DESAT filter time is 2375 ns corresponding to the resistors R13 and R23 with a value of: 13.7 kΩ.

The preset soft-off current for DESAT events is set to a typical value of 131 mA corresponding to the resistors R14 and R24 with a value of: 1.91 kΩ.

1.3 Start-up

In this chapter the prerequisites and power up sequence are described. This will allow the evaluation of the Infineon EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M in a half-bridge configuration.

Prerequisites

- Assemble suitable power switches in the sockets T50 and T60 at the location Q1 and Q2. E.g. IKW40N120H3 IGBTs or IMW120R030M1H CoolSiC™ SiC MOSFETs
- Assemble an external high-voltage decoupling capacitor (> 100 µF) across the high voltage power terminal, X90-1 (*P1000VP*) and X90-3 (*GND*)
- Have a low-voltage power supply for supplying the power supply circuit, capable of supplying 15 V, 100 mA (*P15VP*, *SGND*)
- Have a high-voltage power supply for supplying the power stage between X90-1 (*P1000VP*) and X90-3 (*GND*)
- Have an inductive load for double-pulse testing
- Have a signal generator for half-bridge operation or double-pulse testing
- E96 resistor kit with 0805 1% values to adjust the DESAT and soft-off settings on the EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M

In order to adapt the board to other applications or evaluation scenarios, resistor and capacitor values might require to be changed in order to optimize the evaluation boards for the desired scenarios.

2 Not to be used when power supply circuit is enabled

Starting sequence

1. Select the input voltage operation, between 5 V or 3.3 V. Either close J40 (5V EN) for 5 V operation, or leave it open for 3.3 V operation.
2. Make sure J70 (ISO DIS) is open in order to have the built-in isolated power supply enabled.
3. Connect the PWM signals to the digital interface at connector X1, for the upper switch (*IN-HS*,*GND*) and lower switch (*IN-LS*,*GND*)
4. Connect one end of the inductive load to X90-2 (*PHASE*) and the other end according to the double-pulse requirements to either X90-1 (*P1000VP*) or X90-3 (*GND*) for low side or high side testing
5. Supply *P15VP* at the connector X40-2 with +15.5 V and connect the supply return, *SGND*, to connector X40-2.
6. The green LED D41 (15V_ok) will turn on signaling the input supply is present
7. The green LED D46 (VCC1_ok) will turn on signaling the primary side of the gate drivers is present.
8. The green LEDs D42 (*FLT#*) and D44 (*RDYC*) will turn on signaling the secondary sides of both chips have been properly supplied, no fault condition is detected by the gate driver ICs and the driver ICs are ready for operation
9. Connect the high voltage supply to connector X90-3 (*GND*) and X90-1 (*P1000VP*)
10. The board is now ready for double-pulse evaluation

1.4 Fault detection

The gate driver IC comes with adjustable DESAT filter times and soft-off current. The functionality and complete explanation of the settings are detailed in the product datasheet.

This application note only covers the minimum information needed for evaluation and it is highly recommended to review the datasheet before designing with the gate driver IC.

1.4.1 DESAT protection with filter time and leading edge blanking time adjustment

The gate driver IC comes with desaturation protection aimed at protecting the external switch from destruction during short-circuit events. The simplified sequence for the desaturation protection is as following:

1. The voltage at the *DESAT* pin reaches the DESAT threshold level
2. The gate driver IC switches the external switch off, using the soft-off method
3. The gate driver IC pulls *FLT#* low to indicate the fault and latches the signal
4. The red LED D43 (*FLT#*) turns on and the green LED D44 (*FLT#*) turns off
5. The short-circuit event is cleared.

Because the *FLT#* signal is shared between the *FLT_N* open drain output/input pins of both gate drivers. A DESAT or fault even on one of the gate drivers will automatically disable both gate drivers operation.

In order to clear the fault, the *RDYC* signal has to be pulled down for at least t_{CLRMIN} as described in the datasheet. As *RDYC* is attached to both gate driver ICs *RDYC* pin, both gate driver ICs will be cleared.

Filter and leading edge blanking time adjustment

The EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M comes with an adjustable DESAT leading edge blanking time, $t_{DESATleb}$, and DESAT filter time, $t_{DESATfilter}$ by means of a resistor connected between pin *ADJB* and the primary side ground pin, *GND1*. By choosing one of the 16 values for the resistor, as shown in the table below, allows the user to select a suitable DESAT filter time setting for their application without the use of external RC filters.

Table 3 DESAT filter timing ADJB adjustment

DESAT filter time set up	stopped	0	1	2	3	4	5	6	7
Resistance at *ADJB* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. $t_{DESATleb}$	inhibit gate driver operation	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns
typ. $t_{DESATfilter}$		1575 ns	1775 ns	1975 ns	2375 ns	2775 ns	3175 ns	3575 ns	3975 ns

Table 3 DESAT filter timing ADJB adjustment

DESAT filter time set up	8	9	10	11	12	13	14	15	default
Resistance at *ADJB* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. $t_{DESATleb}$	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	400 ns
typ. $t_{DESATfilter}$	3975 ns	3575 ns	3175 ns	2775 ns	2375 ns	1975 ns	1775 ns	1575 ns	*225* ns

For the lower side gate driver IC, the resistor connected to *ADJB* is R24. For the higher side gate driver IC, the resistor connected to *ADJB* is R14.

1.4.2 Soft turn-off current adjustment

During normal operation the gate driver IC always uses hard switch-off.

In case a fault, or a forced turn-off by pulling *RDYC* low, the gate driver IC will turn-off the connected power switch using the soft-off function.

The gate of the connected power device is discharged via the *OFF* pin by an internal current sinking circuit. This discharge current can be adjusted to a value, lower than the hard-off current used during normal operation.

During an overcurrent event, such as short-circuit, the current in the circuit is mainly limited by the switch channel as the switch goes into saturation. Turning off such high currents with a hard-off event results, most of the times, due to the parasitic inductances in the power loop, into over-voltage conditions across the switch. This over-voltage could degrade or even damage the switch. By employing soft turn-off current functionality, the high overcurrent event is slowly turned off, reducing the overshoot voltage.

Since the soft turn-off events are a one off occurrence after failures, the gate driver IC is designed to internally handle the extra power dissipation.

The soft-off current source can be selected by changing the value of the resistance between pin *ADJA* and *GND1* of the gate driver IC. Connecting the *ADJA* pin to *VCC1* will inhibit the start-up sequence and disable the gate driver operation.

By choosing one of the 16 values for the resistor, as shown in the table below, allows the user to select a suitable soft-off current setting for their application without the use of other external components.

Table 4 Soft-off adjustment with *ADJA*

Soft-off set up	default	0	1	2	3	4	5	6	7
Resistance from *ADJA* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. I_{CSOFF} 1ED3431M	146 mA	15 mA	29 mA	44 mA	58 mA	73 mA	87 mA	102 mA	116 mA
typ. I_{CSOFF} 1ED3461M	291 mA	29 mA	58 mA	87 mA	116 mA	146 mA	175 mA	204 mA	233 mA
typ. I_{CSOFF} 1ED3491M	437 mA	44 mA	87 mA	131 mA	175 mA	218 mA	262 mA	306 mA	349 mA

Table 4 Soft-off adjustment with *ADJA*

Soft-off set up	8	9	10	11	12	13	14	15	stopped
Resistance from *ADJA* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. I_{CSOFF} 1ED3431M	131 mA	146 mA	160 mA	175 mA	189 mA	204 mA	218 mA	233 mA	inhibit gate driver operation
typ. I_{CSOFF} 1ED3461M	262 mA	291 mA	320 mA	349 mA	379 mA	408 mA	437 mA	466 mA	
typ. I_{CSOFF} 1ED3491M	393 mA	437 mA	480 mA	524 mA	568 mA	612 mA	655 mA	699 mA	

For the lower side gate driver IC, the resistor connected to *ADJA* is R23. For the higher side gate driver IC, the resistor connected to *ADJA* is R13

1.5 Adjusting the DESAT and soft-off settings

The datasheet contains a detailed description of the DESAT and soft-off turn-off functions, including typical values and it is recommended to consult it before proceeding further with the adjustments and investigation of the gate driver.

As mentioned earlier the EiceDRIVER™ 1ED-X3 Analog 1ED3491MU12M comes with adjustable DESAT leading edge blanking time and filter time and adjustable soft-off fault currents.

During the start-up procedure, the gate driver IC reads the external resistor values from the *ADJA* and *ADJB* pins. These values and their linked parameters are stored within the gate driver IC until the next supply voltage drop-out. This ensures that during operation, any source of noise, will not influence these settings. Depending on the application, topology, control method and switches used, the DESAT protection might need to be adjusted to offer reliable protection of the power switches.

1.5.1 DESAT leading edge blanking time and filter time options

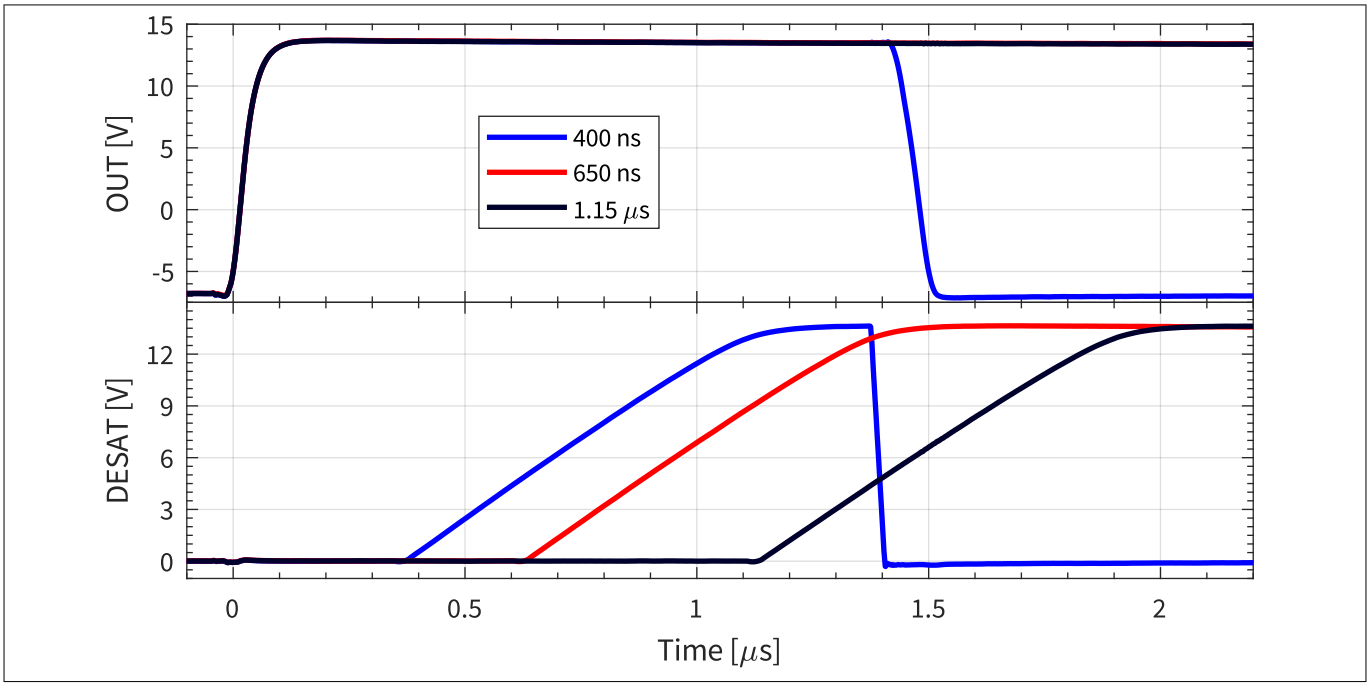

Figure 2 Leading edge blanking time filters

Figure 2 shows the three selectable leading edge blanking settings in relationship to the output signal of the gate driver. The power switched used in this example was in saturation for all three measurements. The $t_{DESATleb,d}$ = 400 ns option is only selectable with a $t_{DESATfilter,def}$ = *225* ns.

For the leading edge blanking filter $t_{DESATleb,s}$ = 650 ns and $t_{DESATleb,l}$ = 1150 ns, eight different DESAT filter times can be selected, from 1575 ns to 3975 ns.

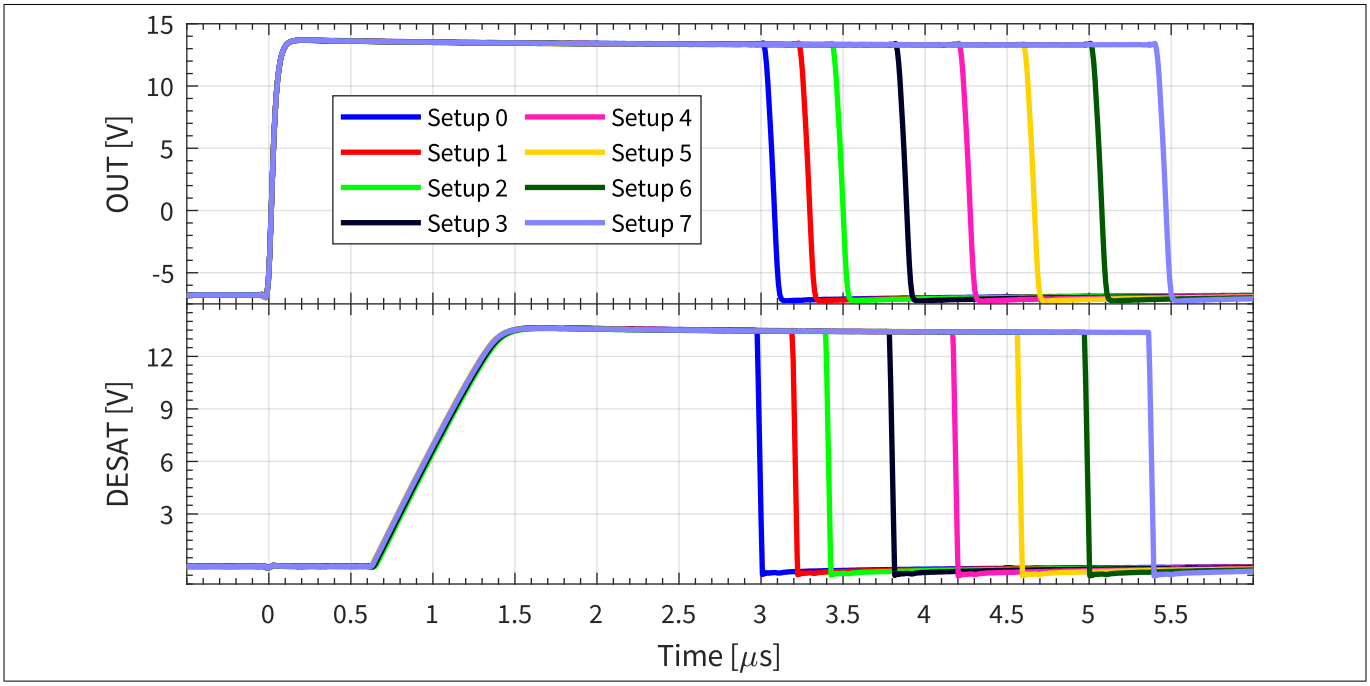

Figure 3 DESAT filter times

Figure 3 shows the eight different DESAT filter settings in relation to the gate driver IC *OUT* signal. The gate driver IC in the example was configured with a $t_{DESATleb,s}$ = 650 ns but similar behavior would be observed for the $t_{DESATleb,l}$ = 1150 ns setting.

This evaluation board was designed with an unpopulated footprint for a DESAT capacitor. In case the vast settings built into the gate driver IC are not covering intended application, a capacitor can be added to adjust the DESAT parameters even further.

1.5.2 Soft-off current setting

As mentioned earlier, in the event a fault is detected the gate driver IC will initiate a soft-off current turn-off of the power switch in order to avoid over voltage of the power transistor due to the overcurrent.

These fault, generally are either detected by the gate driver IC, via the DESAT protection, or externally by the microcontroller and signaled by pulling *RDYC* pin low. As shown earlier the gate driver IC can be adjusted to 16 discrete values of the off current.

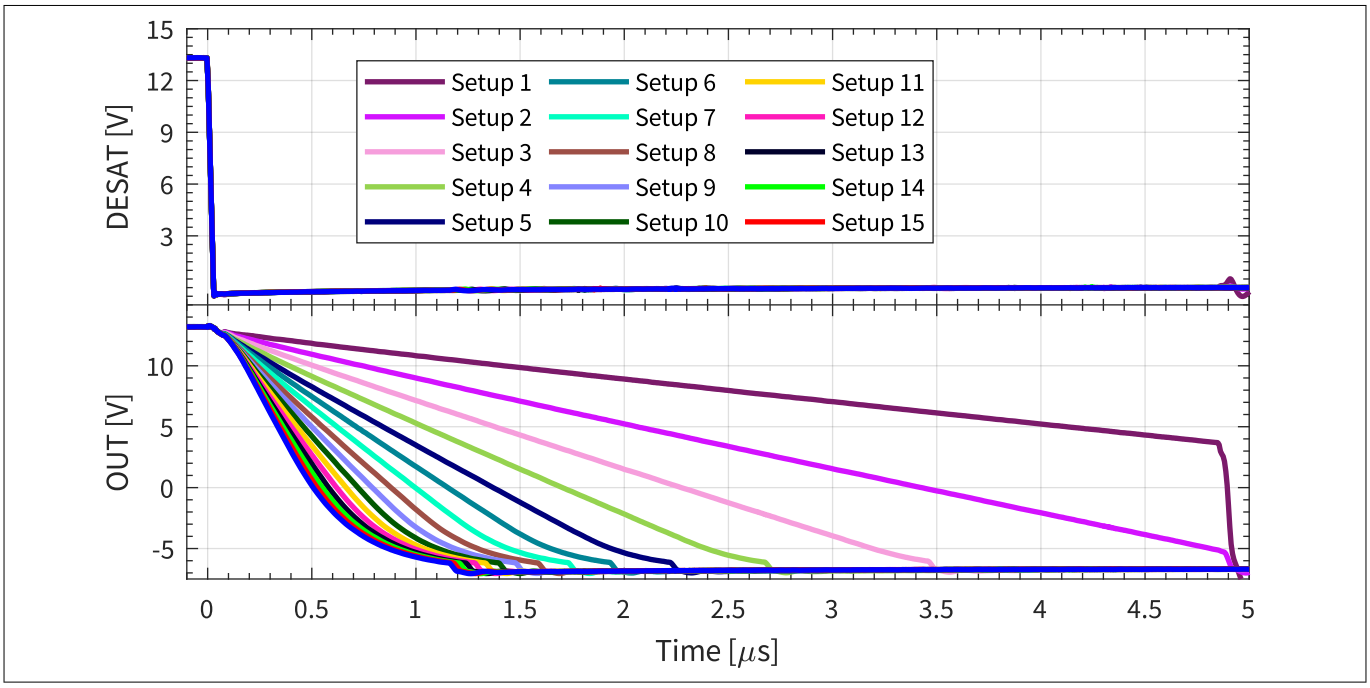

Figure 4 Soft-off current with a load of R_{GOFF} = 10 Ω and C_{load} = 22 nF

Figure 4 shows the measurement of the I_{CSOFF} for 15 different setups. The output of the gate driver was connected to a capacitive load C_{load} = 22 nF via a resistor R_{GOFF} = 10 Ω.

These different soft-off turn-off currents can allow for a controlled discharge of the power transistor gate, thus limiting the overcurrent induced voltage overshoot. The gate driver IC has a built in timeout function for the soft-off current. If the *OUT* voltage does not reach V_{VEE2} + 2 V in a present amount of time, the gate driver uses all available means to switch-off the output. This includes changing soft-off into hard switch-off and activating the *CLAMPDRV* output. This timing is defined in the product datasheet and can be clearly observed in the measurement marked with Setup 1.

1 Electrical description

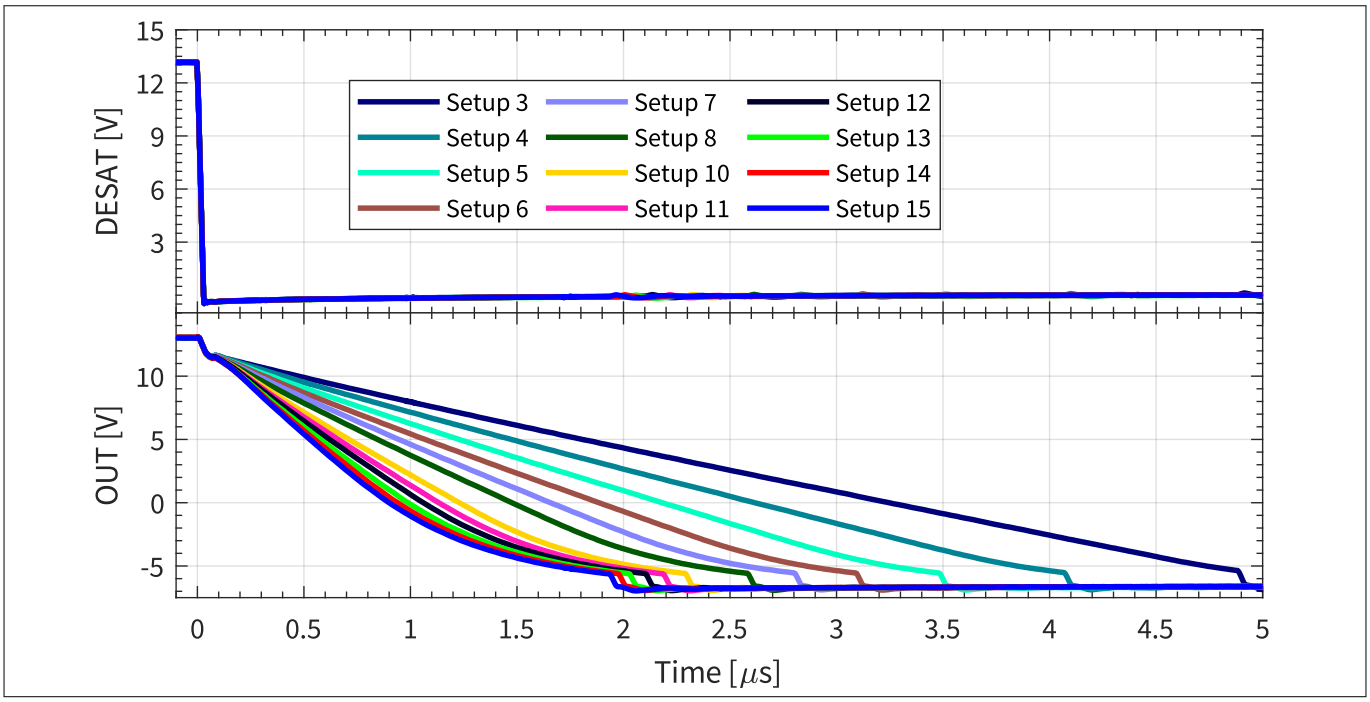

Figure 5 Soft-off current with a load of R_{GOFF} = 10 Ω and C_{load} = 47 nF

Figure 5 shows similar measurements of *OUT* and *DESAT* pins with a load R_{GOFF} = 10 Ω and C_{load} = 47 nF. Setups 0 to 2 are not shows as the switch-off timeout was already reached in setup 3, limiting the turn-off time to the timeout value.

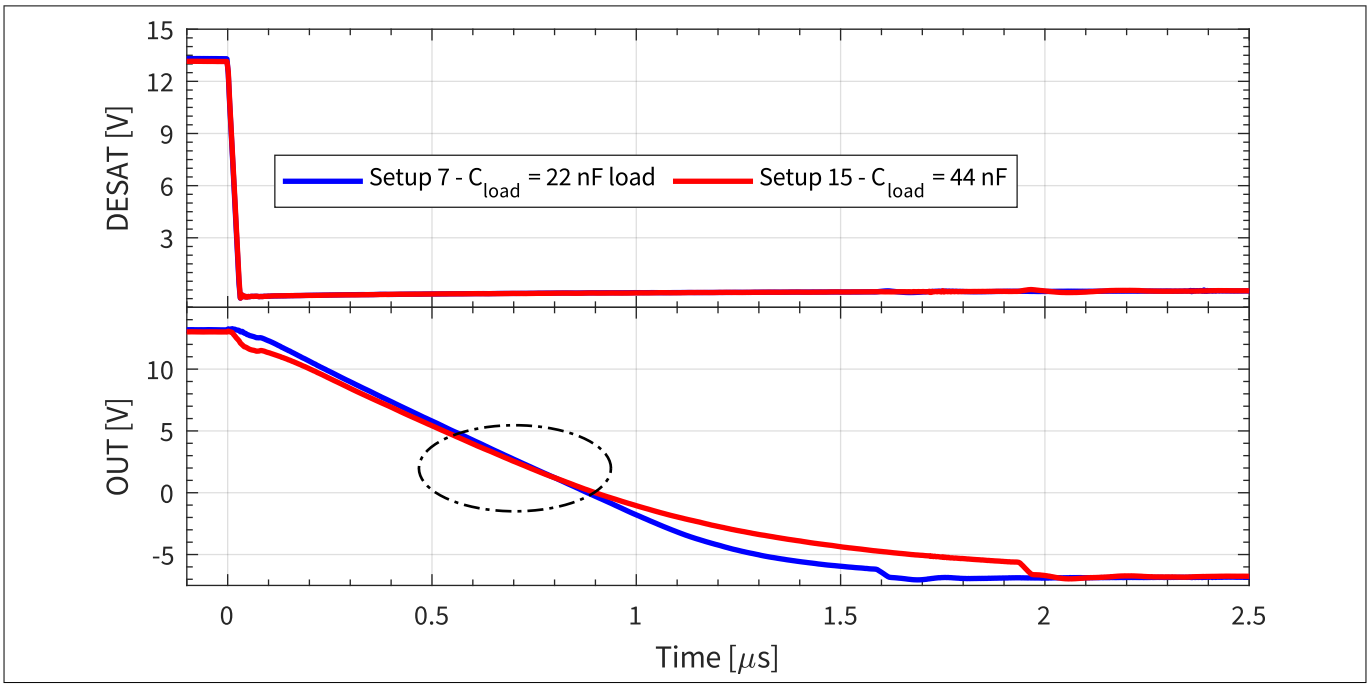

Figure 6 Maintaining the same turn-off time for two switches with different input capacitances

Figure 6 compares the soft turn-off of two different capacitive loads, C_{load1} = 22 nF and C_{load2} = 47 nF, associated with two different power transistors gate capacitances. The soft turn-off is performed using the same gate resistor. By selecting different resistors at *ADJA* for the soft-off function, the threshold voltage of both switches can be reached in the same time. This allows to maintain similar behavior of the circuit, despite deploying different power switches.

1.6 Connectors and pin assignment

The following table describes connectors and their pin assignments on the PCB.

Table 5 Connectors and pin assignment

Connector	Pin	Marking/function	Note
X1	1	*VCC*	VCC1 power supply for both gate driver ICs primary side
X1	2, 5, 8	*SGND*	Signal ground for primary side, connected to *GND1* of both driver ICs
X1	3	*IN-HS*	Logic PWM input high side gate driver, referenced to *SGND*
X1	4	*IN-LS*	Logic PWM input low side gate driver, referenced to *SGND*
X1	6	*FLT#*	Fault output, low active and soft- off input, low active, reference to *SGND*
X1	7	*RDYC*	Combined ready output, high active and fault clear input and soft-off input, low active, reference to *SGND*
X40	1	*SGND*	Signal ground for primary side, connected to *GND1* of both driver ICs
X40	2	*P15VP*	+15 V input supply voltage built in power supply for primary and isolated power supply for secondary side
X70	1	*VCC2H*	High side positive gate driver supply
X70	2	*PHASE/GNDH*	High side gate driver supply reference
X70	3	*VEE2H*	High side negative gate driver supply
X80	1	*VCC2L*	Low side positive gate driver supply
X80	2	*GNDL*	Low side gate driver supply reference
X80	3	*VEE2L*	Low side negative gate driver supply
X90	1	*P1000VP*	Half-bridge high voltage positive input
X90	2	*PHASE*	Half-bridge mid-point, output connected to *GNDH*
X90	3	*GND*	Half-bridge high voltage negative input, connected to *GNDL*
J40	1, 2	*5V EN*	Jumper to enable 5 V primary operation
J70	1, 2	*ISO DIS*	Jumper to disable isolated power supply

1.7 Adjusting the negative gate voltage value for CoolSiC™ SiC MOSFETs

By default, the board's bipolar power supply is designed to output +15 V/-7.5 V. These voltages are suitable for driving IGBTs but might not be suitable for driving CoolSiC™ SiC MOSFETs.

In order to support evaluation of the gate drivers with CoolSiC™ SiC MOSFETs, the evaluation board was designed with a transistor-zener diode regulator circuit which was left unpopulated. The schematic for the high side negative supply is shown in ***Figure 7***. During the evaluation, the various negative gate voltage requirements of CoolSiC™ SiC MOSFETs have to be considered when selecting the components to populate this circuit.

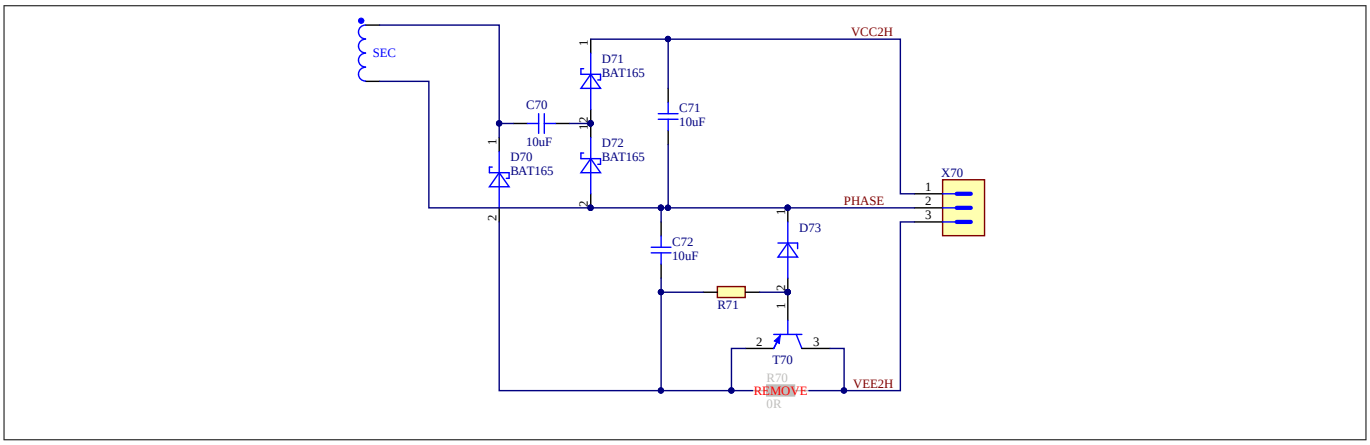

Figure 7 High side supply for CoolSiC™ SiC MOSFET adaption

Resistors R70, R80 must be removed and diodes D73, D83, resistors R71, R81, and transistors T70, T80 should be populated in order to adjust the voltage on the *VEE2L* or *VEE2H* to the desired voltage.

The value of the negative voltage *VEE2L*/*VEE2H* rail is given by the breakdown voltage of the Zener diode D73/D83 plus the V_{BE} voltage drop of the transistor, T70/T80. The current biasing resistors R71/R81 should be selected as such to ensure enough current is drawn from the transistor's base, while at the same time ensuring that the Zener diodes are not overloaded.

The table below shows a bill of materials required to enable -3 V *VEE2* operation required for CoolSiC™ SiC MOSFETs switching.

Table 6 Component change to enable -3 V *VEE2* for CoolSiC™ SiC MOSFETs

Designator	Manufacturer	Manufacturer part number	Value
D73, D83	Vishay	BZX384B3V6-E3-08	3.6 V
R71, R81	Vishay	CRCW0603560RFK	560 Ω
T70, T80	Diodes inc.	BC857A	-
R70, R80	Remove	Remove	Remove

2 Schematics

The schematics of the evaluation board are separated into the following parts:

- Gate driver ICs with surrounding circuit
- Power supply for primary and secondary sides
- Status interface LEDs
- Interfaces with connectors

2 Schematics

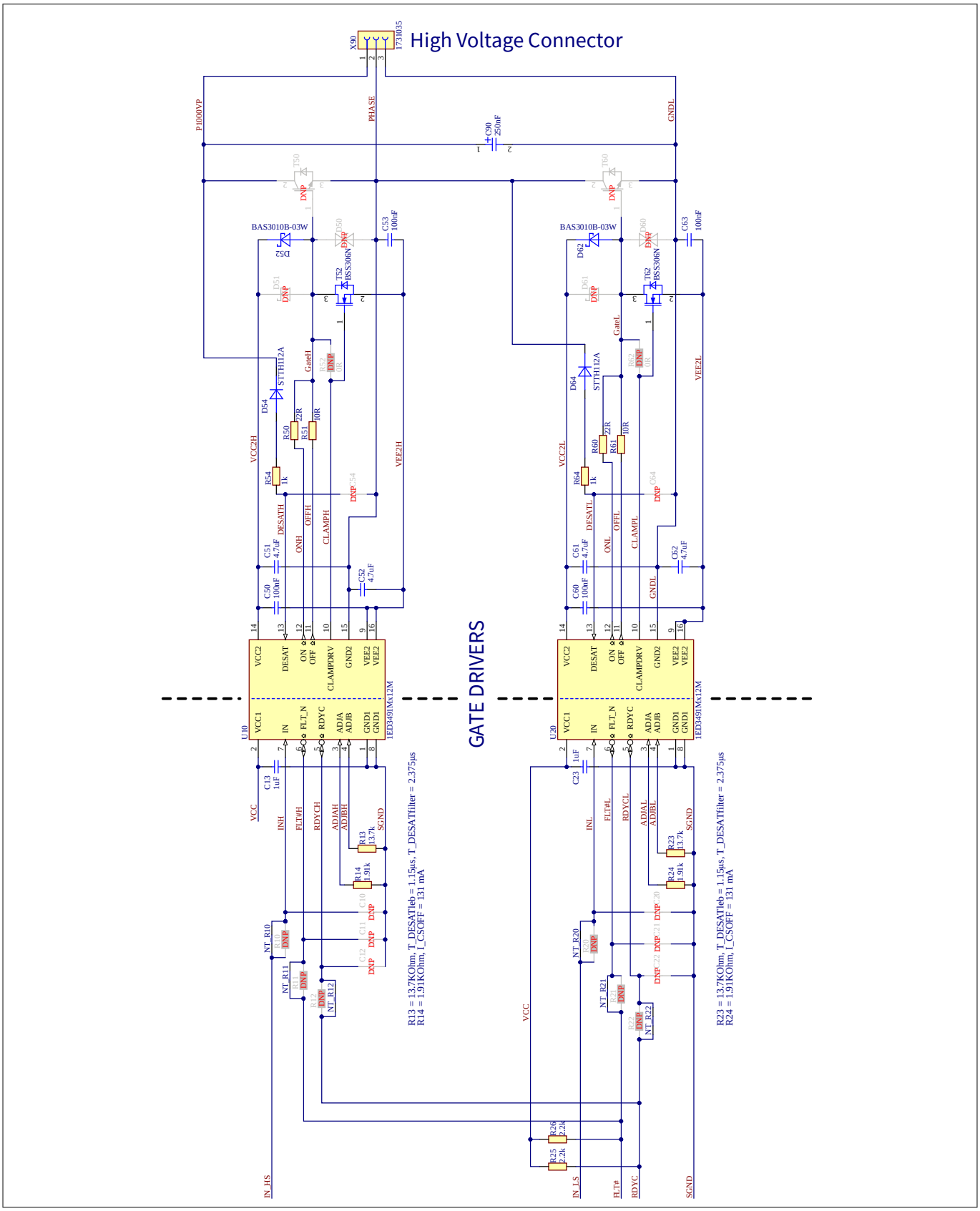

Figure 8 **Schematic of gate driver ICs and surrounding circuit**

2 Schematics

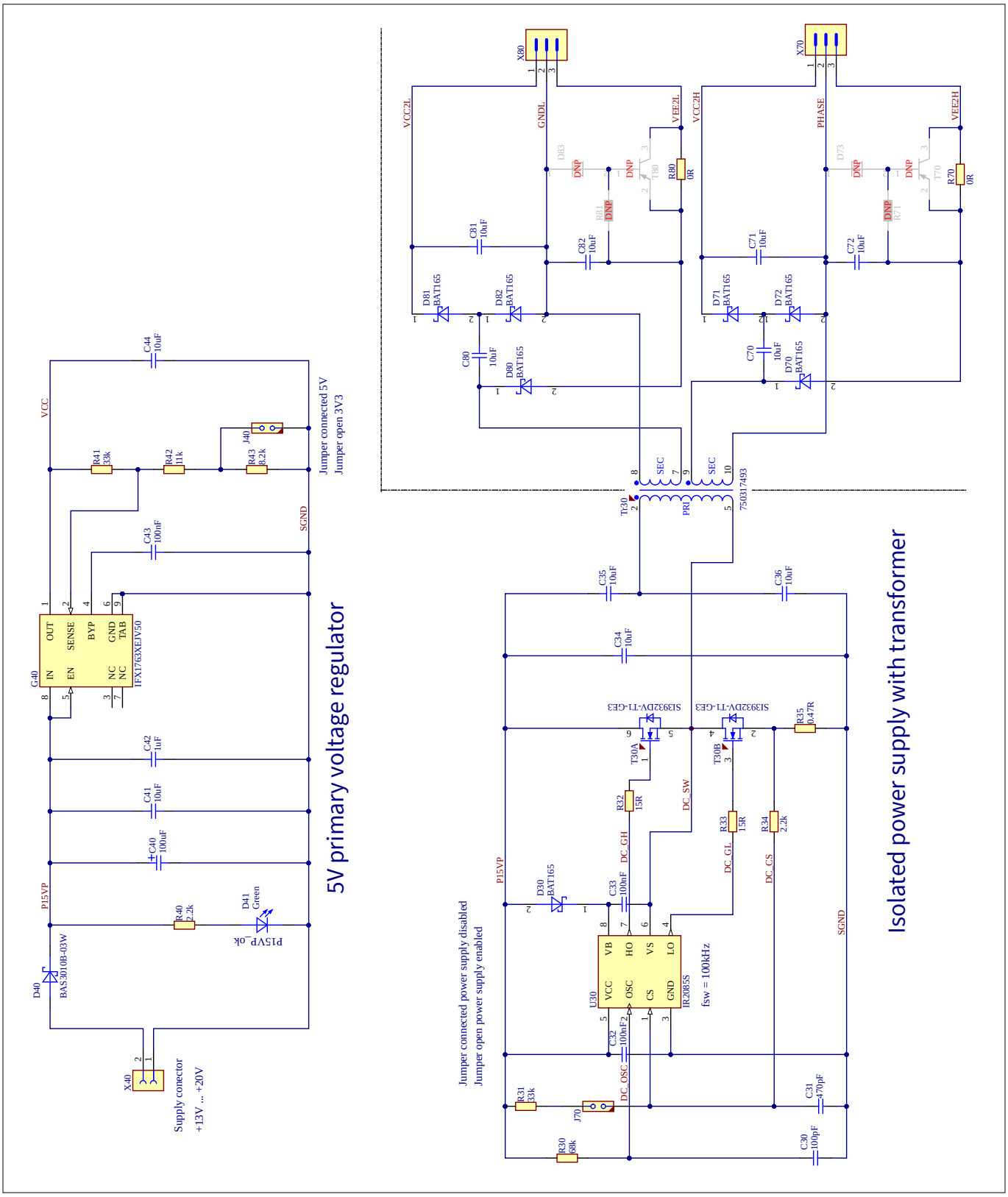

Figure 9 Schematic of power supply and voltage regulators

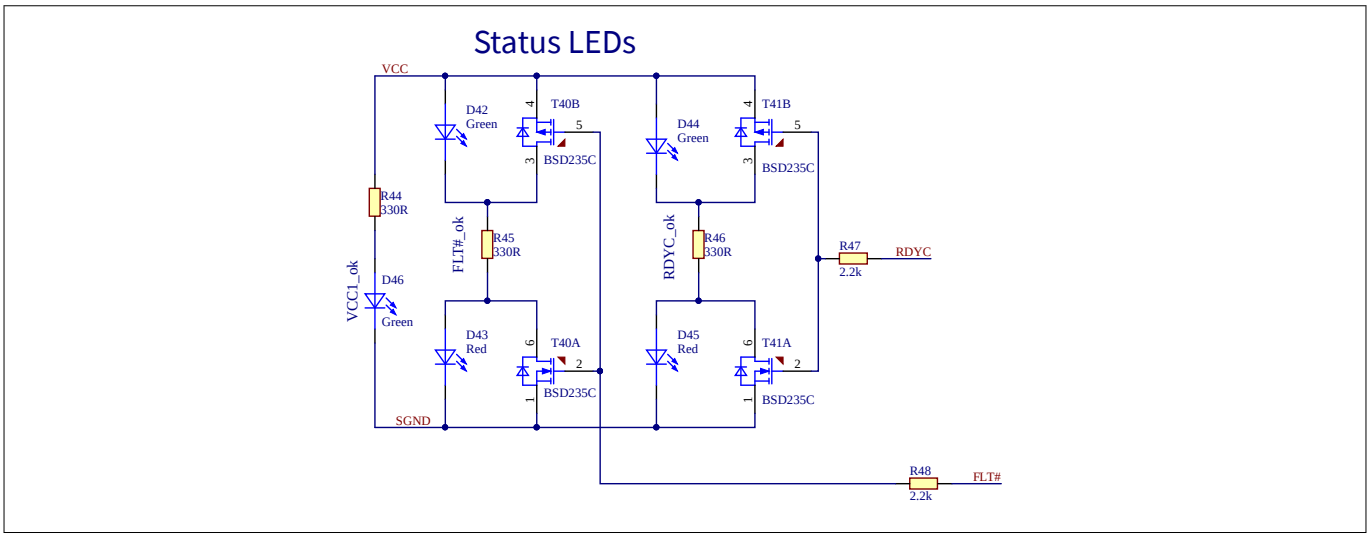

Figure 10 Schematic of status LEDs

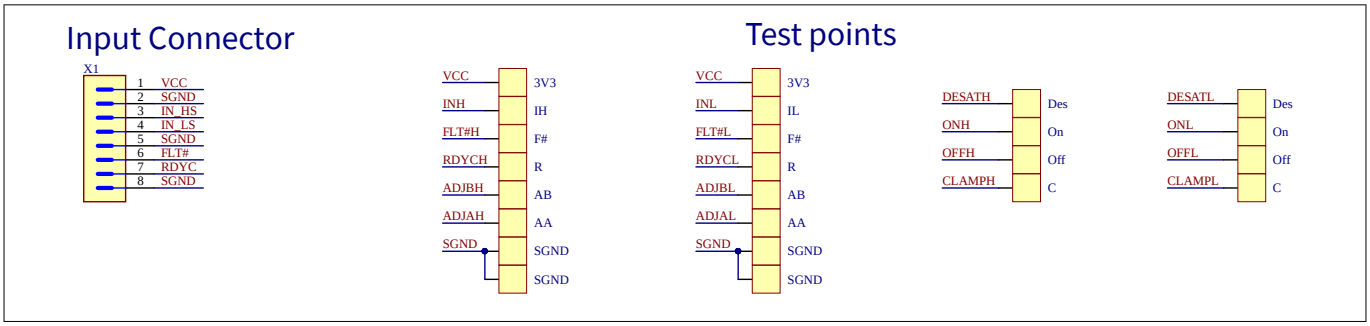

Figure 11 Schematic of input connectors and test points

3 PCB layout

The layout from this basic schematic is intended as a starting point for developing more complex application circuits. The evaluation board has a four-layer PCB. For orientation, only the assembly diagram and the top and bottom layer are shown.

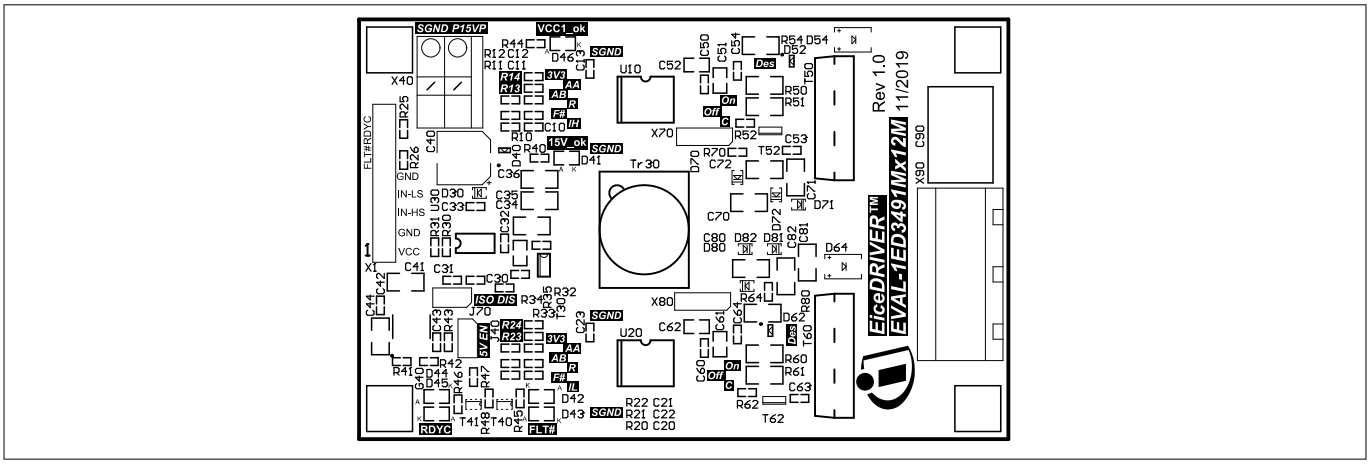

Figure 12 Assembly drawing top side

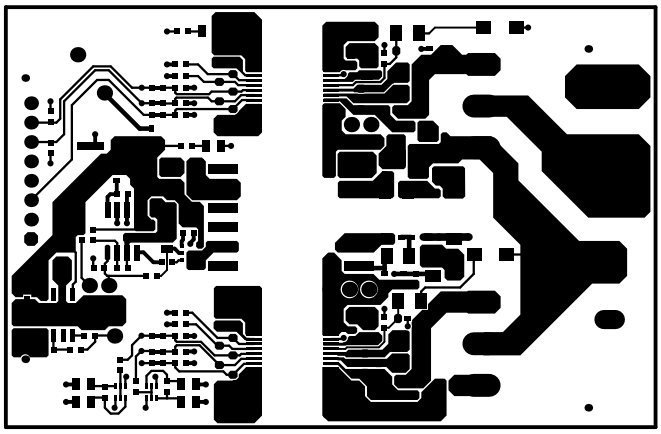

Figure 13 PCB top layer

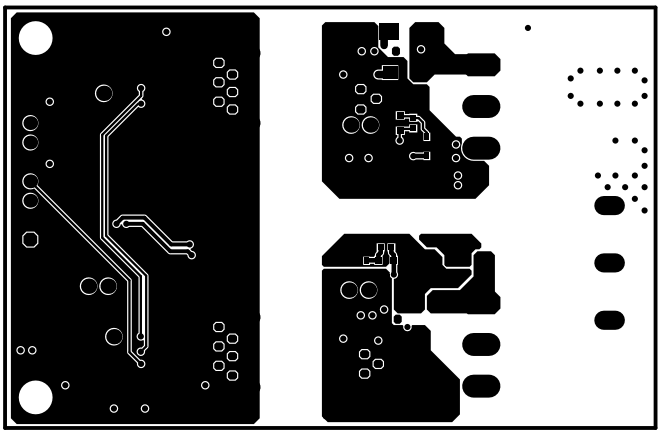

Figure 14 PCB bottom layer

4 Bill of material

The BOM lists all components used for the PCB.

Designator	Quantity	Description	Manufacturer	PartNumber
C13, C23	2	CAP, CERM, 1 µF, 10%, 25 V	Taiyo Yuden	GMK107AB7105KAHT
C30	1	CAP, CERM, 100 pF	Kemet	C0603C101F5GAC
C31	1	CAP, CERM, 470 pF	Wurth Elektronik	885012006061
C32, C33, C43, C50, C60, C63	6	CAP, CERM, 100 nF, 20%, 100 V, 0603	Wurth Elektronik	885012206120
C34, C35, C36, C41, C44, C70, C71, C72, C80, C81, C82	11	CAP, CERM, 10 µF, 10%, 25 V	Wurth Elektronik	885012208069
C40	1	CAP, ELECTROLYTE, 100 µF	Wurth Elektronik	865090445008
C42	1	CAP, CERM, 1 µF	Wurth Elektronik	885012106022
C51, C52, C61	3	CAP, CERM, 4.7 µF	MuRata	GRM21BR61H475KE51
C53	1	CAP, CERM, 100 nF	Wurth Elektronik	885012206095

4 Bill of material

Designator	Quantity	Description	Manufacturer	PartNumber
C62	1	CAP, CERM, 4.7 µF	Wurth Elektronik	885012107018
C90	1	CAP, CERM, 250 nF, 900 V, 20% CeraLink	TDK Corporation	B58031I9254M062
D30, D70, D71, D72, D80, D81, D82	7	Diode, Schottky, 40 V, 0.75 A, SOD-323	Infineon	BAT165
D40, D52, D62	3	Diode, Schottky, 30 V, 1 A, SOD-323	Infineon	BAS3010B-03W
D41, D42, D44, D46	4	LED, Green, SMD	Wurth Elektronik	150080VS75000
D43, D45	2	LED, Red, SMD	Wurth Elektronik	150080RS75000
D54, D64	2	Diode, 1200 V, 1 A, ultrafast	ST	STTH112A
G40	1	Voltage regulator, 500 mA, 5 V, LDO	Infineon	IFX1763XEJV50
J40, J70	2	SQ Post Header, 2.54mm pitch, 1x2 pin, vertical, TH	Wurth Elektronik	61300211121
R13, R23	2	RES, 13.7k, 1%, 0.1 W, 0805	Vishay	CRCW080513K7FK
R14, R24	2	RES, 1.91k, 1%, 0.1 W, 0805	Vishay	CRCW08051K91FK
R25, R26, R34, R40, R47, R48	6	RES, 2.2k, 1%, 0.1 W, 0603	Vishay	TNPW06032K20BE
R30	1	RES, 68k, 1%, 0.1 W, 0603	Vishay	CRCW060368K0FK
R31, R41	2	RES, 33k, 1%, 0.1 W, 0603	Vishay	CRCW060333K0FK
R32, R33	2	RES, 15R, 1%, 0.1 W, 0603	Vishay	CRCW060315R0FK
R35	1	RES, 1R, 1%, 0.1 W, 0805	Yageo	RL0805JR-070R47L
R42	1	RES, 11k, 1%, 0.1 W, 0603	Vishay	CRCW060311K0FK
R43	1	RES, 8.2k, 1%, 0.1 W, 0603	Vishay	CRCW06038K20FK
R44, R45, R46	3	RES, 330R, 1%, 0.1 W, 0603	Vishay	CRCW0603330RFK
R50, R60	2	RES, 22R, 1%, 0.25 W, 1206	Vishay	CRCW120622R0FK
R51, R61	2	RES, 10R, 1%, 0.25 W, 1206	Yageo	RC1206FR-0710RL
R54, R64	2	RES, 1k, 1%, 0.25 W, 1206	Vishay	CRCW12061K00FK
R70, R80	2	RES, 0R, 0.1 W, 0603	Vishay	CRCW06030000Z0
T30	1	MOSFET, Dual N-Channel, 30 V	Vishay	SI3932DV-T1-GE3
T40, T41	2	MOSFET, Complemenary P/N-Channel, OptiMOS™	Infineon	BSD235C
T52, T62	2	MOSFET, N-Channel, 30 V, OptiMOS™	Infineon	BSS306N
Tr30	1	Transformer, 1.07:1, 2%	Wurth Elektronik	750317493
U10, U20	2	Gate driver IC, Single-channel, DSO-16 300 mil fine-pitch	Infineon	1ED3491MC12M
U30	1	Gate driver IC, Half-Bridge, Self-oscillating, 100 V	Infineon	IR2085S

4 Bill of material

Designator	Quantity	Description	Manufacturer	PartNumber
X1	1	SQ Post Header, 2.54mm pitch, 1x8 pin, vertical, TH	Wurth Elektronik	61300811121
X40	1	TERM BLOCK, 2POS, TH	Phoenix Contact	1985195
X70, X80	2	SQ Post Header, 2.54mm pitch, 1x3 pin, vertical, TH	Wurth Elektronik	61300311121
X90	1	TERM BLOCK, 3POS 5 mm, TH	Wurth Elektronik	691216910003

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