Finisar

Product Specification

100m 40G Ethernet CFP Optical Transceiver Module

FTLQ8181EBLM

PRODUCT FEATURES

- Hot-pluggable CFP form factor
- Supports 41.2 Gb/s aggregate bit rate
- Power dissipation < 6W
- RoHS-6 compliant
- Commercial temperature range 0°C to 70°C
- Single 3.3V power supply
- Maximum link length of 100m on OM3 Multimode Fiber (MMF)
- Uncooled 4x10Gb/s 850nm transmitter
- XLAUI electrical interface
- Single MPO receptacle
- Built-in digital diagnostic functions

APPLICATIONS

- 40GBASE-SR4 40G Ethernet

Finisar's FTLQ8181EBLM 40G CFP transceiver modules are designed for use in 40 Gigabit Ethernet links over multimode fiber. They are compliant with the CFP MSA[1] and IEEE 802.3ba 40GBASE-SR4[2]. Digital diagnostics functions are available via an MDIO interface, as specified by the CFP MSA and Finisar Application Note AN-2078[5]. The transceiver is RoHS-6 compliant per Directive 2011/65/EU[3] and Finisar Application Note AN-2038[4].

PRODUCT SELECTION

FTLQ8181EBLM

E:	40G Ethernet maximum bit rate
B:	4x10G 850nm parallel optical architecture
L:	Integrated heat sink
M:	MPO receptacle

I. Pin Descriptions

Per CFP MSA[1], Table 5-6 and 5-7.

	Top Row		Bottom Row
148	GND	1	3.3V_GND
147	*REFCLKn*	2	3.3V_GND
146	*REFCLKp*	3	3.3V_GND
145	GND	4	3.3V_GND
144	*N.C.*	5	3.3V_GND
143	*N.C.*	6	3.3V
142	GND	7	3.3V
141	*N.C.*	8	3.3V
140	*N.C.*	9	3.3V
139	GND	10	3.3V
138	*N.C.*	11	3.3V
137	*N.C.*	12	3.3V
136	GND	13	3.3V
135	*N.C.*	14	3.3V
134	*N.C.*	15	3.3V
133	GND	16	3.3V_GND
132	*N.C.*	17	3.3V_GND
131	*N.C.*	18	3.3V_GND
130	GND	19	3.3V_GND
129	*N.C.*	20	3.3V_GND
128	*N.C.*	21	VND_IO_A
127	GND	22	VND_IO_B
126	*N.C.*	23	GND
125	*N.C.*	24	*TX_MCLKn*
124	GND	25	*TX_MCLKp*
123	TX3n	26	GND
122	TX3p	27	VND_IO_C
121	GND	28	VND_IO_D
120	TX2n	29	VND_IO_E
119	TX2p	30	PRG_CNTL1
118	GND	31	PRG_CNTL2
117	TX1n	32	PRG_CNTL3
116	TX1p	33	PRG_ALRM1
115	GND	34	PRG_ALRM2
114	TX0n	35	PRG_ALRM3
113	TX0p	36	TX_DIS
112	GND	37	MOD_LOPWR

	Top Row		Bottom Row
111	GND	38	MOD_ABS
110	*N.C.*	39	MOD_RSTn
109	*N.C.*	40	RX_LOS
108	GND	41	GLB_ALRMn
107	*N.C.*	42	PRTADR4
106	*N.C.*	43	PRTADR3
105	GND	44	PRTADR2
104	*N.C.*	45	PRTADR1
103	*N.C.*	46	PRTADR0
102	GND	47	MDIO
101	*N.C.*	48	MDC
100	*N.C.*	49	GND
99	GND	50	VND_IO_F
98	*N.C.*	51	VND_IO_G
97	*N.C.*	52	GND
96	GND	53	VND_IO_H
95	*N.C.*	54	VND_IO_J
94	*N.C.*	55	3.3V_GND
93	GND	56	3.3V_GND
92	*N.C.*	57	3.3V_GND
91	*N.C.*	58	3.3V_GND
90	GND	59	3.3V_GND
89	RX3n	60	3.3V
88	RX3p	61	3.3V
87	GND	62	3.3V
86	RX2n	63	3.3V
85	RX2p	64	3.3V
84	GND	65	3.3V
83	RX1n	66	3.3V
82	RX1p	67	3.3V
81	GND	68	3.3V
80	RX0n	69	3.3V
79	RX0p	70	3.3V_GND
78	GND	71	3.3V_GND
77	*RX_MCLKn*	72	3.3V_GND
76	*RX_MCLKp*	73	3.3V_GND
75	GND	74	3.3V_GND

Bottom Row Pin Descriptions

PIN #	Name	I/O	Logic	Description
1	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			
8	3.3V			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V			
14	3.3V			
15	3.3V			
16	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
22	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
23	GND			
24	TX_MCLKn	O		**Not Supported**
25	TX_MCLKp	O		**Not Supported**
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
28	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
29	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
30	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO, Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset; "1" or NC: enabled (i.e., not used).
31	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO, Default: Hardware Interlock LSB, "00": ≤8W; "01": ≤16W; "10": ≤24W; "11" or NC: ≤32W (i.e., not used).
32	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO, Default: Hardware Interlock MSB, "00": ≤8W; "01": ≤16W; "10": ≤24W; "11" or NC: ≤32W (i.e., not used).
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, Default: HIPWR_ON, "1": module power up completed; "0": module not high powered up.
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, Default: MOD_READY, "1": Ready; "0": not Ready.
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, Default: MOD_FAULT, fault detected, "1": Fault; "0": No Fault.
36	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O F. Do Not Connect!
51	VND_IO_G	I/O		Module Vendor I/O G. Do Not Connect!
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do Not Connect!
54	VND_IO_J	I/O		Module Vendor I/O J. Do Not Connect!
55	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
56	3.3V_GND			

PIN #	Name	I/O	Logic	Description
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			
62	3.3V			
63	3.3V			
64	3.3V			
65	3.3V			
66	3.3V			
67	3.3V			
68	3.3V			
69	3.3V			
70	3.3V_GND			**3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground**
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

Notes:
1. REFCLK is not required.
2. Host side loopback is supported; network side loopback is not supported.
3. Tx_MCLK and Rx_MCLK functionality is not supported

II. Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VI). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_{OP}	0		70	°C	
Relative Humidity	RH	0		85	%	1
Receiver Damage Threshold, per Lane	P_{Rdmg}	3.4			dBm	

Notes:
1. Non-condensing.

III. Electrical Characteristics (T_{OP} = 0 to 70 °C, V_{CC} = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.13		3.47	V	
Supply Current	Icc			1.74	A	
Module total power	P			6	W	1
Transmitter						
Signaling rate per lane				10.3125	Gb/s	2
Input differential impedance	R_{in}		100		Ω	3
Differential data input swing per lane	Vin,pp			760	mV	4
Data input rise time tolerance	t_r	24			ps	5
Data input rise time tolerance	t_f	24			ps	5
Electrical input eye mask definition	{X1, X2} {Y1, Y2}		{0.31, 0.5} {42.5, 425}		UI mV	
Receiver						
Signaling rate per lane				10.3125	Gb/s	2
Differential data output swing per lane	Vout,pp			760	mV	
Data output rise time	t_r	24			ps	5
Data output fall time	t_f	24			ps	5
Electrical output eye mask definition	{X1, X2} {Y1, Y2}		{0.2, 0.5} {136, 380}		UI mV	
Power Supply Noise Tolerance	Vrip		See Note 5 below			6

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. +/- 100ppm
3. After internal AC coupling.
4. Host is expected to be compliant with IEEE 802.3ba, clause 83A.
5. 20% to 80%
6. Per Table 4-1 in the CFP MSA Specification[1].

FTLQ8181EBLM Clocking Signals

Clock Name	Status	I/O	Value
REFCLK	Not Required	I	N/A
TX_MCLK	Not Supported	O	N/A
RX_MCLK	Not Supported	O	N/A

IV. Optical Characteristics (T_{OP} = 0 to 70 °C, V_{CC} = 3.13 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling Speed per Lane			10.3125		GBd	1
Center wavelength		840		860	nm	
RMS Spectral Width	SW			0.65	nm	
Total Average Launch Power	P_{OUT}	-3.9		7.0	dBm	2
Average Launch Power per Lane	TXP_x	-7.6		2.4	dBm	
Transmit OMA per Lane	TxOMA	-5.6		3.0	dBm	
Difference in Launch Power between Lanes				4.0	dB	
Peak Power per Lane	PP_x			4.0	dBm	
Optical Extinction Ratio	ER	3.0			dB	
Optical Return Loss Tolerance	ORL			12	dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	3
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				
Receiver						
Signaling Speed per Lane			10.3125		GBd	4
Center wavelength		840		860	nm	
Average Receive Power per Lane	RXP_x	-9.5		2.4	dBm	
Receive Power (OMA) per Lane	RxOMA			3.0	dBm	
Receiver Sensitivity (OMA) per Lane	Rxsens			-8.7	dBm	
Stressed Receiver Sensitivity (OMA) per Lane	SRS			-5.4	dBm	
Peak Power, per lane	PP_x			4	dBm	
Receiver Reflectance	Rfl			-12	dB	
Vertical eye closure penalty, per lane				2	dB	
LOS De-Assert	LOS_D			-12	dBm	
LOS Assert	LOS_A	-28			dBm	
LOS Hysteresis			1		dB	

Notes:
1. Transmitter consists of 4 lasers operating at 10.3Gb/s each.
2. Values are informative.
3. RIN is scaled by 10*log(10/4) to maintain SNR outside of transmitter.
4. Receiver consists of 4 photodetectors operating at 10.3Gb/s each.

V. General Specifications

Parameter		Symbol	Min	Typ	Max	Units	Ref.
Bit Rate (all wavelengths combined)		BR			41.2	Gb/s	1
Bit Error Ratio		BER			10^{-12}		2
Maximum Supported Distances							
Fiber Type							
OM3 MMF		Lmax1			100	m	
OM4 MMF		Lmax2			150	m	

Notes:
1. Supports 40GBASE-SR4 per IEEE 802.3ba. Contact Finisar for higher data-rate support.
2. Tested with a $2^{31} – 1$ PRBS

VI. Environmental Specifications

Finisar FTLQ8181 CFP transceivers have a commercial operating temperature range from -5°C to +75°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar FTLQ8181EBLM CFP transceivers are Class 1 laser eye safety compliant per IEC 60825-1.
They are certified per the following standards:

Feature	Agency	Standard	Certificate Number
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	9210176
Laser Eye Safety	TÜV	EN 60825-1: 1994+A11:1996+A2:2001 IEC 60825-1: 1993+A1:1997+A2:2001 IEC 60825-2: 2000, Edition 2	R72102454
Electrical Safety	TÜV	EN 60950	R72102454
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87	2375840

Copies of the referenced certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostic Functions

FTLQ8181 CFP transceivers support the MDIO-based diagnostics interface specified in the CFP MSA[1]. See Finisar Application Note AN-2078[5].

IX. Memory Contents

Per the CFP MSA[1]. See Finisar Application Note AN-2078[5].

X. Host PCB Layout and Bezel Recommendations

Per CFP MSA Hardware Specification, Rev 1.4[1].

XI. Mechanical Specifications

Finisar FTLQ8181 CFP transceivers are compatible with the CFP MSA specification for 40G/100G pluggable form factor modules.

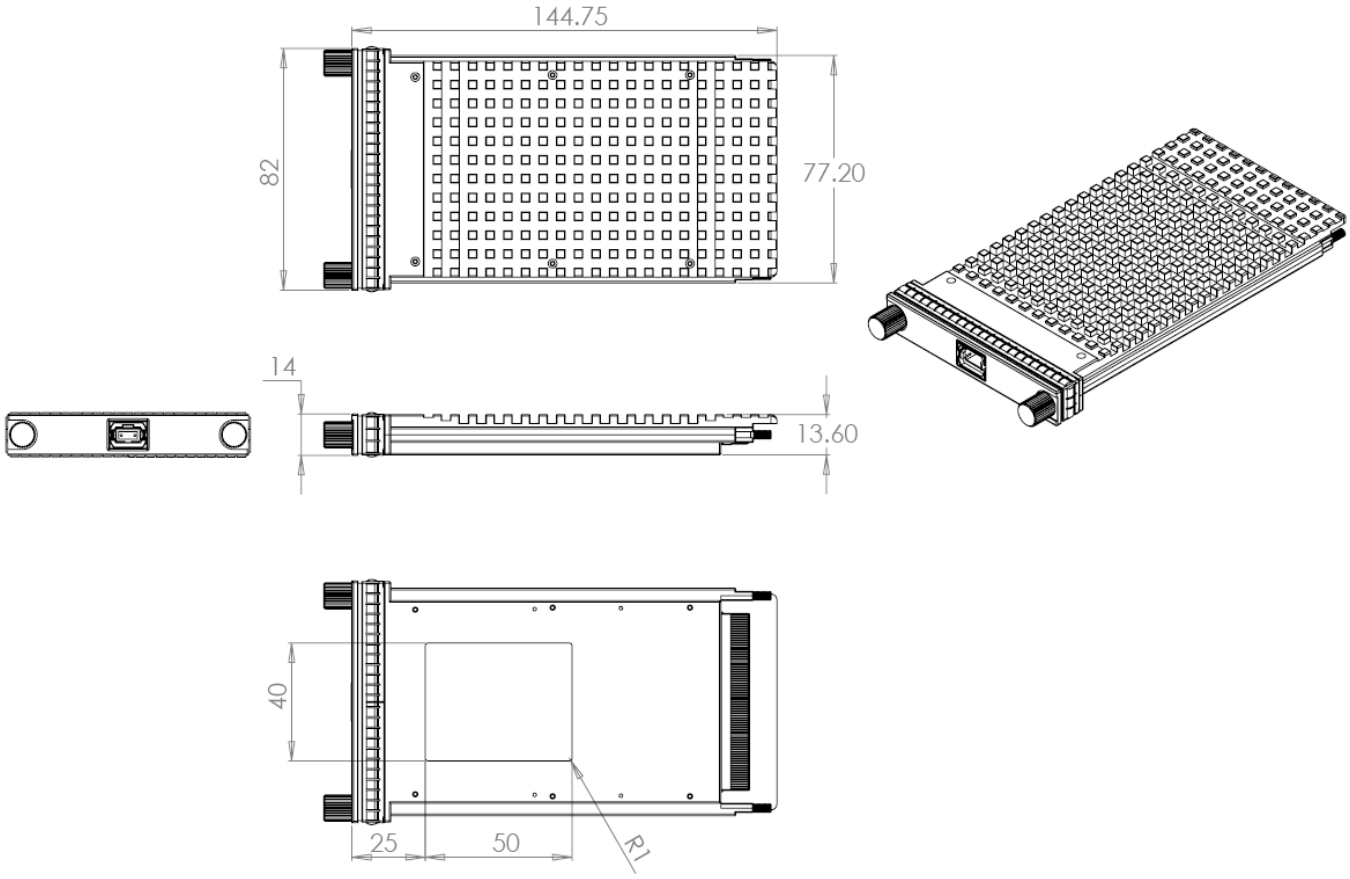

Figure 1. FTLQ8181EBLM Mechanical Dimensions.

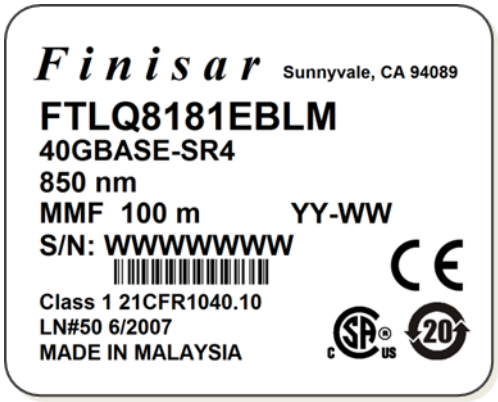

Figure 2. Product Label

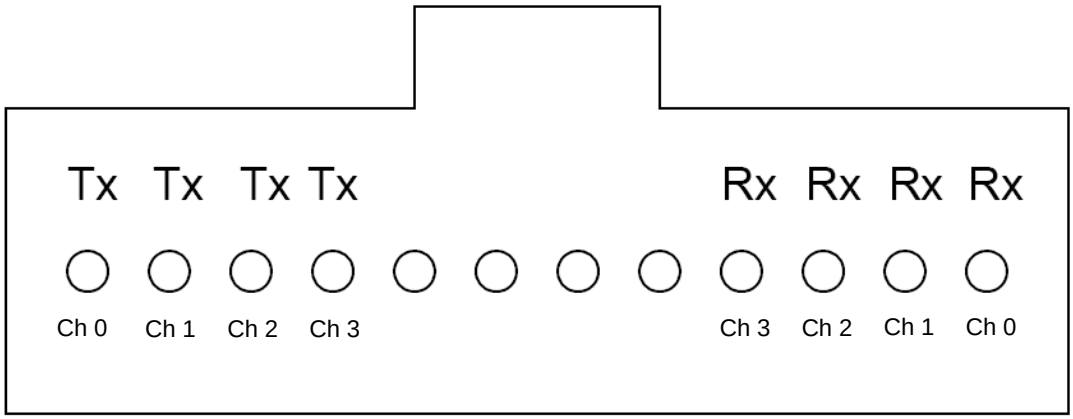

Figure 3. Optical Lane Assignment (front view of MPO receptacle).

XII. References

1. CFP MSA Hardware Specification, Rev 1.4 and Management Interface Specifications, Rev 1.4., www.cfp-msa.org

2. IEEE 802.3ba, PMD Type 40GBASE-SR4.

3. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," June 8, 2011, which supersedes the previous RoHS Directive 2002/95/EC.

4. "Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.

5. "Application Note AN-2078: NVR1 and MDIO Compatibility List, 40GE Base SR4 CFP (FTLQ8181) and 40GE Base LR4 CFP (FTLQ7181)", Finisar Corporation, December 23, 2009.

For More Information

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