

# TC7LX1102FK

## 1. Functional Description

- Low-Voltage, Low-Power 2-Bit Dual-Supply Bus Transceiver with Auto Direction Sensing

## 2. General

The TC7LX1102FK is an advanced high-speed dual-supply 2-bit bus transceiver fabricated with silicon-gate CMOS technology.

The TC7LX1102FK is designed for use as an interface between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage systems.

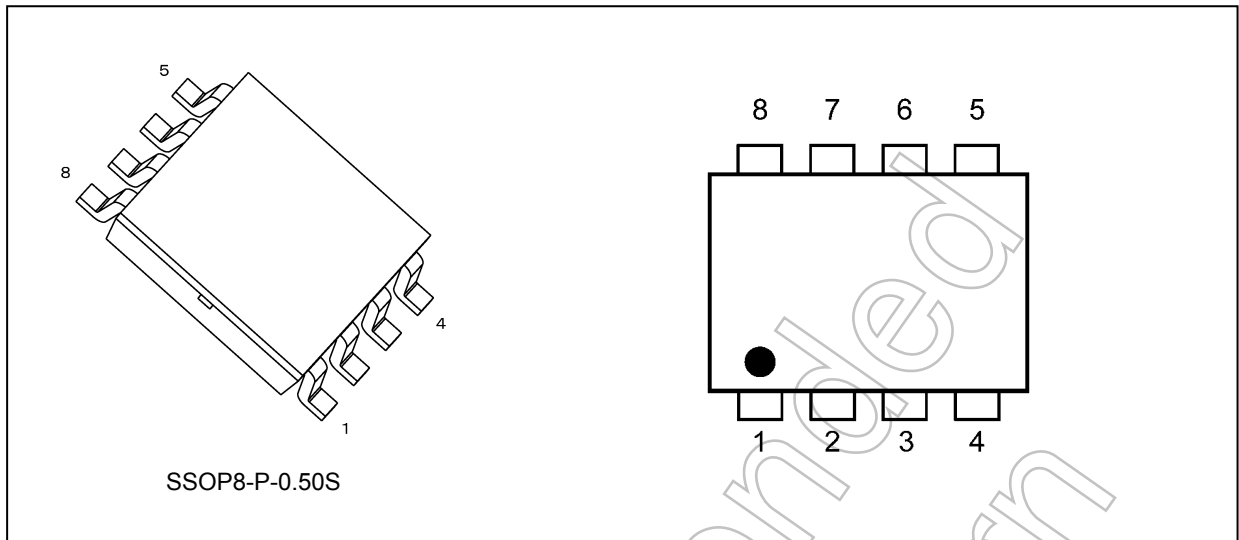
The voltage translator automatically senses the direction of data transmission, eliminating the need for a direction control input. When the Output Enable (OE) input is low, the device is disabled, effectively isolating the buses. All inputs and outputs of the TC7LX1102FK can tolerate overvoltage conditions up to 3.6 V.

## 3. Features

- (1) Voltage translation between arbitrary voltage levels from 1.2 V to 3.6 V.
- (2) High-speed operation:  $t_{pd} = 5.0 \text{ ns (max)}$  ( $V_{CCA} = 1.8 \pm 0.15 \text{ V}$ ,  $V_{CCB} = 3.3 \pm 0.3 \text{ V}$ )
- (3) Latch-up performance:  $\pm 300 \text{ mA}$
- (4) ESD performance:  
Machine model  $\geq \pm 200 \text{ V}$ , Human body model  $\geq \pm 2000 \text{ V}$
- (5) Ultra-small package: US8
- (6) The A-bus and B-bus are allowed to float. (when OE = Low)
- (7) 3.6-V tolerant function and power-down protection provided on all inputs and outputs.
- (8) All output ports are disabled when either  $V_{CC}$  is switched off ( $V_{CCA/B} = 0\text{V}$ )

Not Recommended for New Design

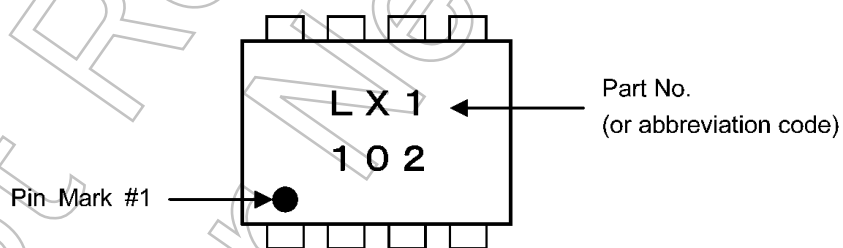
**4. Packaging and Pin Assignment (Top View)**



**4.1. Pin Assignment**

Pin No.	Pin Name
1	V <sub>CCA</sub>
2	A1
3	A2
4	GND
5	OE
6	B2
7	B1
8	V <sub>CCB</sub>

**5. Marking**



**Fig. 5.1 Marking**

6. Block Diagram

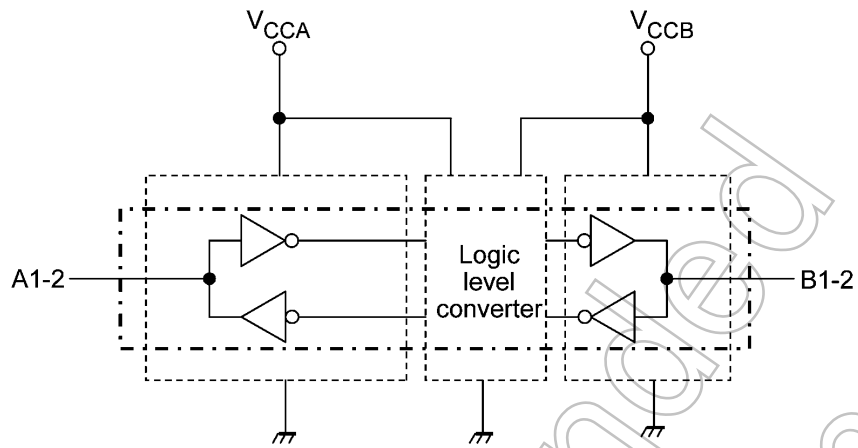


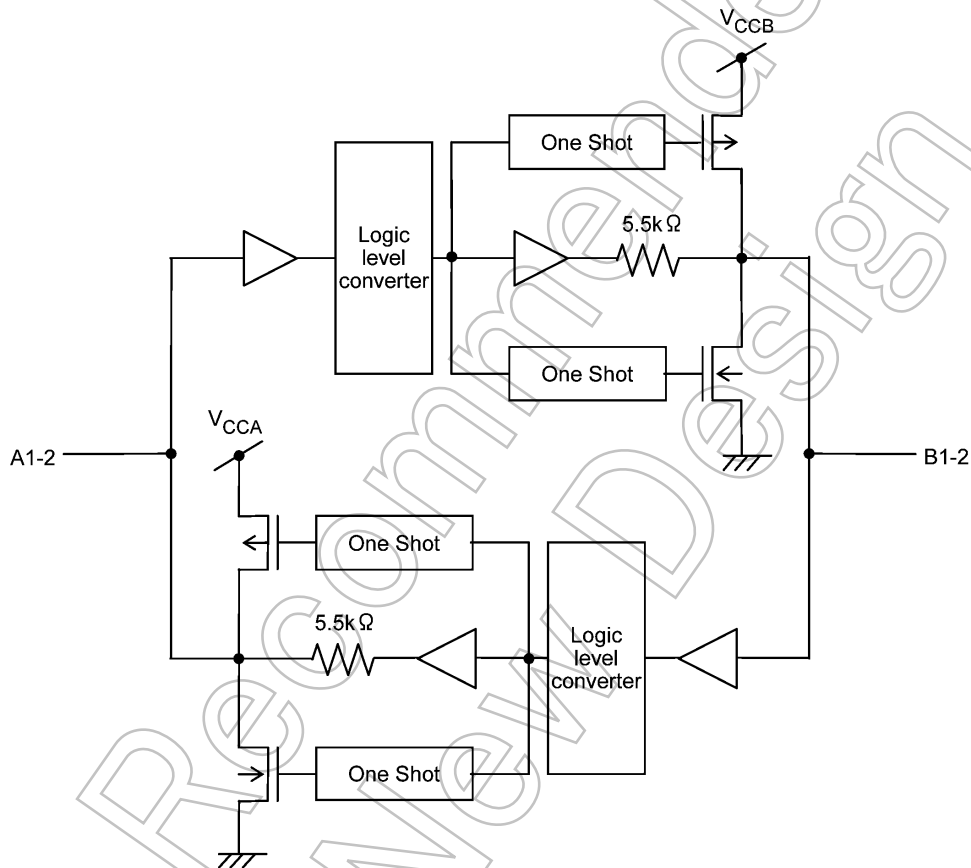
Fig. 6.1 Block Diagram

Not Recommended for New Design

**7. Internal Equivalent Circuit**

The TC7LX1102FK does not have a control signal that controls the direction of data flow between A and B. In a DC state, the output circuit holds either High or Low level, but since it is designed to have a weak drive strength (with a typical output resistance of 5.5 kΩ), an overdrive signal from the external driver can change the direction of data flow.

The output one-shot circuits detect either a rising or falling edge on the A or B port. During the rise time, the output one-shot circuit associated with the PMOS transistors turns it on for a certain period to speed up a transition from Low to High. Likewise, during the fall time, the output one-shot circuit associated with the NMOS transistors turns it on to speed up a transition from High to Low.



**Fig. 7.1 Internal Equivalent Circuit**

**8. Principle of Operation**

**8.1. Truth Table**

Input OE	Function
H	A port = B port
L	Disconnect

**9. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CCA}$		-0.5 to 4.6	V
	$V_{CCB}$		-0.5 to 4.6	
Input voltage (OE)	$V_{IN}$		-0.5 to 4.6	
Bus I/O voltage	$V_{I/OA}$	(Note 1)	-0.5 to 4.6	
		(Note 2)	-0.5 to $V_{CCA} + 0.5$	
	$V_{I/OB}$	(Note 1)	-0.5 to 4.6	
		(Note 2)	-0.5 to $V_{CCB} + 0.5$	
Input diode current	$I_{IK}$		-50	mA
I/O diode current	$I_{I/OK}$	(Note 3)	$\pm 50$	
Output current	$I_{OUTA}$		$\pm 25$	
	$I_{OUTB}$		$\pm 25$	
$V_{CC}$ /ground current per supply pin	$I_{CCA}$		$\pm 50$	
	$I_{CCB}$		$\pm 50$	
Power dissipation	$P_D$		150	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 3:  $V_{OUT} < \text{GND}$ ,  $V_{OUT} > V_{CC}$

**10. Operating Ranges (Note)**

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	$V_{CCA}$			1.2 to 3.6	V
	$V_{CCB}$			1.2 to 3.6	
Input voltage (OE)	$V_{IN}$			0 to 3.6	
Bus I/O voltage	$V_{I/OA}$	(Note 1)		0 to 3.6	
		(Note 2)		0 to $V_{CCA}$	
	$V_{I/OB}$	(Note 1)		0 to 3.6	
		(Note 2)		0 to $V_{CCB}$	
Input rise time	dt/dv		$V_{IN} = 0.8 \text{ to } 2.0 \text{ V}$ , $V_{CCA} = 2.5 \text{ V}$ , $V_{CCB} = 3.0 \text{ V}$	0 to 10	ns/V
Input fall time				0 to 10	
Operating temperature	$T_{opr}$			-40 to 85	$^{\circ}\text{C}$

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND. Please connect both bus inputs and the bus outputs with  $V_{CC}$  or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 1: Output in OFF state.

Note 2: High or low state

**11. Electrical Characteristics**

**11.1. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IHA}$	OE, An	1.2	1.2 to 3.6	1.10	—	V
			1.4		1.20	—	
			1.65		1.35	—	
			2.3		1.70	—	
			3.0		2.00	—	
			3.6		2.20	—	
	$V_{IHB}$	Bn	1.2 to 3.6	1.2	1.10	—	
			1.4	1.20	—		
			1.65	1.35	—		
			2.3	1.70	—		
			3.0	2.00	—		
			3.6	2.20	—		
Low-level input voltage	$V_{ILA}$	OE, An	1.2	1.2 to 3.6	—	0.10	V
			1.4		—	0.20	
			1.65		—	0.30	
			2.3		—	0.50	
			3.0		—	0.70	
			3.6		—	0.80	
	$V_{ILB}$	Bn	1.2 to 3.6	1.2	—	0.10	
			1.4	—	0.20		
			1.65	—	0.30		
			2.3	—	0.50		
			3.0	—	0.70		
			3.6	—	0.80		
High-level output voltage	$V_{OHA}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OHA} = -20 \mu\text{A}$	1.2 to 3.6	1.2 to 3.6	$V_{CCA} - 0.4$	—	V
	$V_{OHB}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OHB} = -20 \mu\text{A}$	1.2 to 3.6	1.2 to 3.6	$V_{CCB} - 0.4$	—	
Low-level output voltage	$V_{OLA}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OLA} = 20 \mu\text{A}$	1.2 to 3.6	1.2 to 3.6	—	0.4	V
	$V_{OLB}$	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OLB} = 20 \mu\text{A}$	1.2 to 3.6	1.2 to 3.6	—	0.4	
3-state output OFF-state leakage current	$I_{OZA}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = 0$ to $3.6$ V	1.2 to 3.6	1.2 to 3.6	—	$\pm 2.0$	$\mu\text{A}$
	$I_{OZB}$		1.2 to 3.6	1.2 to 3.6	—	$\pm 2.0$	
Output resistance	$R_{OUT}$	—	1.2 to 3.6	1.2 to 3.6	3.85	7.15	$\text{k}\Omega$
Input leakage current	$I_{IN}$	$V_{IN}$ (OE) = 0 to 3.6 V	1.2 to 3.6	1.2 to 3.6	—	$\pm 1.0$	$\mu\text{A}$
Power-OFF leakage current	$I_{OFF}$	$V_{IN}$ , $V_{OUT} = 0$ to 3.6 V	0	0	—	2.0	$\mu\text{A}$
Quiescent supply current	$I_{CCA}$	$V_{INA} = V_{CCA}$ or GND	1.2 to 3.6	1.2 to 3.6	—	2.0	$\mu\text{A}$
	$I_{CCB}$	$V_{INB} = V_{CCB}$ or GND	1.2 to 3.6	1.2 to 3.6	—	2.0	
	$I_{CCA}$	$V_{CCA} \leq (V_{IN}, V_{OUT}) \leq 3.6$ V	1.2 to 3.6	1.2 to 3.6	—	$\pm 2.0$	
	$I_{CCB}$	$V_{CCB} \leq (V_{IN}, V_{OUT}) \leq 3.6$ V	1.2 to 3.6	1.2 to 3.6	—	$\pm 2.0$	

**11.2. AC Characteristics**

**11.2.1.  $V_{CCA} = 3.3 \pm 0.3$  V**

(Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ , Input:  $t_r = t_f = 2.0$  ns)

Characteristics	Symbol	Test Condition	$V_{CCB}$ (V)	Min	Max	Unit
Propagation delay time ( $B_n \rightarrow A_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	14.9	ns
			$1.5 \pm 0.1$	1.0	6.9	
			$1.8 \pm 0.15$	1.0	5.0	
			$2.5 \pm 0.2$	1.0	3.6	
			$3.3 \pm 0.3$	1.0	3.1	
3-state output enable time ( $OE \rightarrow A_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	108.8	
			$1.5 \pm 0.1$	1.0	104.7	
			$1.8 \pm 0.15$	1.0	102.5	
			$2.5 \pm 0.2$	1.0	98.7	
			$3.3 \pm 0.3$	1.0	96.2	
3-state output disable time ( $OE \rightarrow A_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	127.1	
			$1.5 \pm 0.1$	1.0	133.1	
			$1.8 \pm 0.15$	1.0	127.6	
			$2.5 \pm 0.2$	1.0	131.6	
			$3.3 \pm 0.3$	1.0	134.9	
Propagation delay time ( $A_n \rightarrow B_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	7.7	
			$1.5 \pm 0.1$	1.0	5.3	
			$1.8 \pm 0.15$	1.0	3.8	
			$2.5 \pm 0.2$	1.0	3.3	
			$3.3 \pm 0.3$	1.0	3.1	
3-state output enable time ( $OE \rightarrow B_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	98.0	
			$1.5 \pm 0.1$	1.0	94.6	
			$1.8 \pm 0.15$	1.0	92.8	
			$2.5 \pm 0.2$	1.0	93.2	
			$3.3 \pm 0.3$	1.0	94.1	
3-state output disable time ( $OE \rightarrow B_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	145.1	
			$1.5 \pm 0.1$	1.0	121.9	
			$1.8 \pm 0.15$	1.0	131.5	
			$2.5 \pm 0.2$	1.0	89.3	
			$3.3 \pm 0.3$	1.0	119.4	
Output skew (Note 1)	$t_{osLH}/t_{osHL}$	—	1.2	—	0.5	
			$1.5 \pm 0.1$	—	0.5	
			$1.8 \pm 0.15$	—	0.5	
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: Parameter guaranteed by design.

$$(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$$

**11.2.2.  $V_{CCA} = 2.5 \pm 0.2$  V**  
**(Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ , Input:  $t_r = t_f = 2.0$  ns)**

Characteristics	Symbol	Test Condition	$V_{CCB}$ (V)	Min	Max	Unit
Propagation delay time ( $B_n \rightarrow A_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	14.7	ns
			$1.5 \pm 0.1$	1.0	7.0	
			$1.8 \pm 0.15$	1.0	5.1	
			$2.5 \pm 0.2$	1.0	3.8	
			$3.3 \pm 0.3$	1.0	3.3	
3-state output enable time ( $OE \rightarrow A_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	108.3	
			$1.5 \pm 0.1$	1.0	105.7	
			$1.8 \pm 0.15$	1.0	102.0	
			$2.5 \pm 0.2$	1.0	98.5	
			$3.3 \pm 0.3$	1.0	96.9	
3-state output disable time ( $OE \rightarrow A_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	70.4	
			$1.5 \pm 0.1$	1.0	69.5	
			$1.8 \pm 0.15$	1.0	71.3	
			$2.5 \pm 0.2$	1.0	73.9	
			$3.3 \pm 0.3$	1.0	76.3	
Propagation delay time ( $A_n \rightarrow B_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	7.8	
			$1.5 \pm 0.1$	1.0	5.4	
			$1.8 \pm 0.15$	1.0	4.3	
			$2.5 \pm 0.2$	1.0	3.8	
			$3.3 \pm 0.3$	1.0	3.6	
3-state output enable time ( $OE \rightarrow B_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	101.9	
			$1.5 \pm 0.1$	1.0	98.4	
			$1.8 \pm 0.15$	1.0	96.1	
			$2.5 \pm 0.2$	1.0	96.1	
			$3.3 \pm 0.3$	1.0	98.1	
3-state output disable time ( $OE \rightarrow B_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	134.7	
			$1.5 \pm 0.1$	1.0	113.5	
			$1.8 \pm 0.15$	1.0	119.5	
			$2.5 \pm 0.2$	1.0	81.1	
			$3.3 \pm 0.3$	1.0	124.8	
Output skew (Note 1)	$t_{osLH}/t_{osHL}$	—	1.2	—	0.5	
			$1.5 \pm 0.1$	—	0.5	
			$1.8 \pm 0.15$	—	0.5	
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: Parameter guaranteed by design.  
 $(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$



**11.2.3.  $V_{CCA} = 1.8 \pm 0.15$  V**  
**(Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ , Input:  $t_r = t_f = 2.0$  ns)**

Characteristics	Symbol	Test Condition	$V_{CCB}$ (V)	Min	Max	Unit
Propagation delay time ( $B_n \rightarrow A_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	15.0	ns
			$1.5 \pm 0.1$	1.0	7.4	
			$1.8 \pm 0.15$	1.0	5.6	
			$2.5 \pm 0.2$	1.0	4.4	
			$3.3 \pm 0.3$	1.0	3.9	
3-state output enable time ( $OE \rightarrow A_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	111.3	
			$1.5 \pm 0.1$	1.0	106.4	
			$1.8 \pm 0.15$	1.0	104.4	
			$2.5 \pm 0.2$	1.0	101.6	
			$3.3 \pm 0.3$	1.0	99.5	
3-state output disable time ( $OE \rightarrow A_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	122.2	
			$1.5 \pm 0.1$	1.0	121.4	
			$1.8 \pm 0.15$	1.0	123.8	
			$2.5 \pm 0.2$	1.0	123.6	
			$3.3 \pm 0.3$	1.0	118.5	
Propagation delay time ( $A_n \rightarrow B_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	8.7	
			$1.5 \pm 0.1$	1.0	6.3	
			$1.8 \pm 0.15$	1.0	5.6	
			$2.5 \pm 0.2$	1.0	5.1	
			$3.3 \pm 0.3$	1.0	5.0	
3-state output enable time ( $OE \rightarrow B_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	108.5	
			$1.5 \pm 0.1$	1.0	103.1	
			$1.8 \pm 0.15$	1.0	101.7	
			$2.5 \pm 0.2$	1.0	101.1	
			$3.3 \pm 0.3$	1.0	101.5	
3-state output disable time ( $OE \rightarrow B_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	120.7	
			$1.5 \pm 0.1$	1.0	98.3	
			$1.8 \pm 0.15$	1.0	109.5	
			$2.5 \pm 0.2$	1.0	74.8	
			$3.3 \pm 0.3$	1.0	124.5	
Output skew (Note 1)	$t_{osLH}/t_{osHL}$	—	1.2	—	0.5	
			$1.5 \pm 0.1$	—	0.5	
			$1.8 \pm 0.15$	—	0.5	
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: Parameter guaranteed by design.  
 $(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$

**11.2.4.  $V_{CCA} = 1.5 \pm 0.1$  V**  
**(Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ , Input:  $t_r = t_f = 2.0$  ns)**

Characteristics	Symbol	Test Condition	$V_{CCB}$ (V)	Min	Max	Unit
Propagation delay time ( $B_n \rightarrow A_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	15.6	ns
			$1.5 \pm 0.1$	1.0	8.1	
			$1.8 \pm 0.15$	1.0	6.3	
			$2.5 \pm 0.2$	1.0	5.4	
			$3.3 \pm 0.3$	1.0	5.2	
3-state output enable time ( $OE \rightarrow A_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	115.3	
			$1.5 \pm 0.1$	1.0	108.5	
			$1.8 \pm 0.15$	1.0	107.3	
			$2.5 \pm 0.2$	1.0	103.5	
			$3.3 \pm 0.3$	1.0	101.7	
3-state output disable time ( $OE \rightarrow A_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	89.9	
			$1.5 \pm 0.1$	1.0	93.6	
			$1.8 \pm 0.15$	1.0	90.2	
			$2.5 \pm 0.2$	1.0	95.1	
			$3.3 \pm 0.3$	1.0	98.7	
Propagation delay time ( $A_n \rightarrow B_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	10.1	
			$1.5 \pm 0.1$	1.0	7.9	
			$1.8 \pm 0.15$	1.0	7.2	
			$2.5 \pm 0.2$	1.0	6.8	
			$3.3 \pm 0.3$	1.0	6.8	
3-state output enable time ( $OE \rightarrow B_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	112.3	
			$1.5 \pm 0.1$	1.0	107.3	
			$1.8 \pm 0.15$	1.0	106.0	
			$2.5 \pm 0.2$	1.0	105.0	
			$3.3 \pm 0.3$	1.0	104.5	
3-state output disable time ( $OE \rightarrow B_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	123.8	
			$1.5 \pm 0.1$	1.0	99.1	
			$1.8 \pm 0.15$	1.0	113.8	
			$2.5 \pm 0.2$	1.0	71.8	
			$3.3 \pm 0.3$	1.0	127.0	
Output skew (Note 1)	$t_{osLH}/t_{osHL}$	—	1.2	—	0.5	
			$1.5 \pm 0.1$	—	0.5	
			$1.8 \pm 0.15$	—	0.5	
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: Parameter guaranteed by design.  
 $(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$

**11.2.5.  $V_{CCA} = 1.2\text{ V}$**   
**(Unless otherwise specified,  $T_a = -40\text{ to }85^\circ\text{C}$ , Input:  $t_r = t_f = 2.0\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$ (V)	Min	Max	Unit
Propagation delay time ( $B_n \rightarrow A_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	17.1	ns
			$1.5 \pm 0.1$	1.0	10.6	
			$1.8 \pm 0.15$	1.0	8.8	
			$2.5 \pm 0.2$	1.0	8.0	
			$3.3 \pm 0.3$	1.0	7.8	
3-state output enable time ( $OE \rightarrow A_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	127.4	
			$1.5 \pm 0.1$	1.0	115.8	
			$1.8 \pm 0.15$	1.0	112.2	
			$2.5 \pm 0.2$	1.0	109.5	
			$3.3 \pm 0.3$	1.0	107.3	
3-state output disable time ( $OE \rightarrow A_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	123.0	
			$1.5 \pm 0.1$	1.0	118.9	
			$1.8 \pm 0.15$	1.0	121.2	
			$2.5 \pm 0.2$	1.0	116.0	
			$3.3 \pm 0.3$	1.0	124.4	
Propagation delay time ( $A_n \rightarrow B_n$ )	$t_{PLH}/t_{PHL}$	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	14.1	
			$1.5 \pm 0.1$	1.0	12.7	
			$1.8 \pm 0.15$	1.0	12.2	
			$2.5 \pm 0.2$	1.0	11.8	
			$3.3 \pm 0.3$	1.0	12.0	
3-state output enable time ( $OE \rightarrow B_n$ )	$t_{PZL}/t_{PZH}$	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	125.6	
			$1.5 \pm 0.1$	1.0	114.8	
			$1.8 \pm 0.15$	1.0	112.2	
			$2.5 \pm 0.2$	1.0	112.0	
			$3.3 \pm 0.3$	1.0	112.2	
3-state output disable time ( $OE \rightarrow B_n$ )	$t_{PLZ}/t_{PHZ}$		1.2	1.0	113.5	
			$1.5 \pm 0.1$	1.0	94.8	
			$1.8 \pm 0.15$	1.0	112.8	
			$2.5 \pm 0.2$	1.0	71.5	
			$3.3 \pm 0.3$	1.0	124.0	
Output skew (Note 1)	$t_{osLH}/t_{osHL}$	—	1.2	—	0.5	
			$1.5 \pm 0.1$	—	0.5	
			$1.8 \pm 0.15$	—	0.5	
			$2.5 \pm 0.2$	—	0.5	
			$3.3 \pm 0.3$	—	0.5	

Note 1: Parameter guaranteed by design.  
 $(t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)$

**11.3. Timing Requirements**

**11.3.1.  $V_{CCA} = 3.3 \pm 0.3$  V (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$	Min	Max	Unit
Pulse duration (data input)	$t_w$	Fig. 11.2.1	1.2	40	—	ns
			$1.5 \pm 0.1$	16	—	
			$1.8 \pm 0.15$	11	—	
			$2.5 \pm 0.2$	6	—	
			$3.3 \pm 0.3$	5	—	
Data rate	$f_D$	—	1.2	—	25	Mbps
			$1.5 \pm 0.1$	—	60	
			$1.8 \pm 0.15$	—	90	
			$2.5 \pm 0.2$	—	170	
			$3.3 \pm 0.3$	—	200	

**11.3.2.  $V_{CCA} = 2.5 \pm 0.2$  V (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$	Min	Max	Unit
Pulse duration (data input)	$t_w$	Fig. 11.2.1	1.2	40	—	ns
			$1.5 \pm 0.1$	20	—	
			$1.8 \pm 0.15$	11	—	
			$2.5 \pm 0.2$	6	—	
			$3.3 \pm 0.3$	6	—	
Data rate	$f_D$	—	1.2	—	25	Mbps
			$1.5 \pm 0.1$	—	50	
			$1.8 \pm 0.15$	—	90	
			$2.5 \pm 0.2$	—	170	
			$3.3 \pm 0.3$	—	170	

**11.3.3.  $V_{CCA} = 1.8 \pm 0.15$  V (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$	Min	Max	Unit
Pulse duration (data input)	$t_w$	Fig. 11.2.1	1.2	40	—	ns
			$1.5 \pm 0.1$	20	—	
			$1.8 \pm 0.15$	11	—	
			$2.5 \pm 0.2$	11	—	
			$3.3 \pm 0.3$	11	—	
Data rate	$f_D$	—	1.2	—	25	Mbps
			$1.5 \pm 0.1$	—	50	
			$1.8 \pm 0.15$	—	90	
			$2.5 \pm 0.2$	—	90	
			$3.3 \pm 0.3$	—	90	

**11.3.4.  $V_{CCA} = 1.5 \pm 0.1$  V (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$	Min	Max	Unit
Pulse duration (data input)	$t_w$	Fig. 11.2.1	1.2	40	—	ns
			$1.5 \pm 0.1$	20	—	
			$1.8 \pm 0.15$	20	—	
			$2.5 \pm 0.2$	20	—	
			$3.3 \pm 0.3$	20	—	
Data rate	$f_D$	—	1.2	—	25	Mbps
			$1.5 \pm 0.1$	—	50	
			$1.8 \pm 0.15$	—	50	
			$2.5 \pm 0.2$	—	50	
			$3.3 \pm 0.3$	—	50	

**11.3.5.  $V_{CCA} = 1.2$  V (Unless otherwise specified,  $T_a = -40$  to  $85^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCB}$	Min	Max	Unit
Pulse duration (data input)	$t_w$	Fig. 11.2.1	1.2	40	—	ns
			$1.5 \pm 0.1$	40	—	
			$1.8 \pm 0.15$	40	—	
			$2.5 \pm 0.2$	40	—	
			$3.3 \pm 0.3$	40	—	
Data rate	$f_D$	—	1.2	—	25	Mbps
			$1.5 \pm 0.1$	—	25	
			$1.8 \pm 0.15$	—	25	
			$2.5 \pm 0.2$	—	25	
			$3.3 \pm 0.3$	—	25	

**11.4. Capacitive Characteristics (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Typ.	Unit
Input capacitance	$C_{IN}$	OE	2.5	3.3	8	pF
Bus I/O capacitance	$C_{I/O}$	An, Bn			8	
Power dissipation capacitance (Note 1)	$C_{PDA}$	OE = Low (A → B)			0.01	
		OE = Low (B → A)			0.01	
		OE = High (A → B)			19	
		OE = High (B → A)			27	
	$C_{PDB}$	OE = Low (A → B)			0.01	
		OE = Low (B → A)			0.01	
		OE = High (A → B)			29	
		OE = High (B → A)			20	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2 \text{ (per bit)}$$

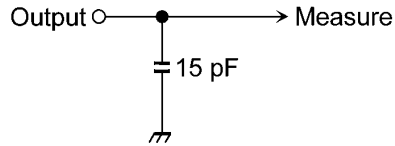


Fig. 11.2.1 AC Test Circuit

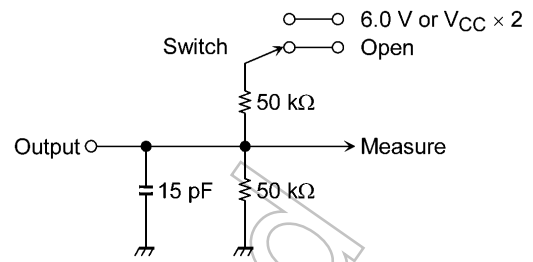


Fig. 11.2.2 AC Test Circuit

Table 11.2.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
$t_{PLZ}, t_{PZL}$	6.0 V	$V_{CC} = 3.3 \pm 0.3 \text{ V}$
	$V_{CC} \times 2$	$V_{CC} = 2.5 \pm 0.2 \text{ V}$
		$V_{CC} = 1.8 \pm 0.15 \text{ V}$
		$V_{CC} = 1.5 \pm 0.1 \text{ V}$
		$V_{CC} = 1.2 \text{ V}$
$t_{PHZ}, t_{PZH}$	OPEN	—

Not Recommended for New Design

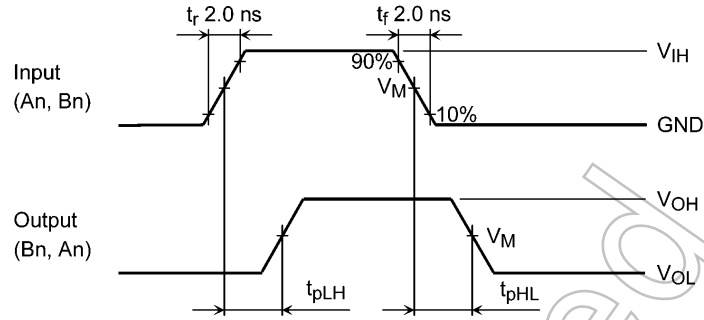


Fig. 11.2.3 AC Waveform of  $t_{pLH}$ ,  $t_{pHL}$

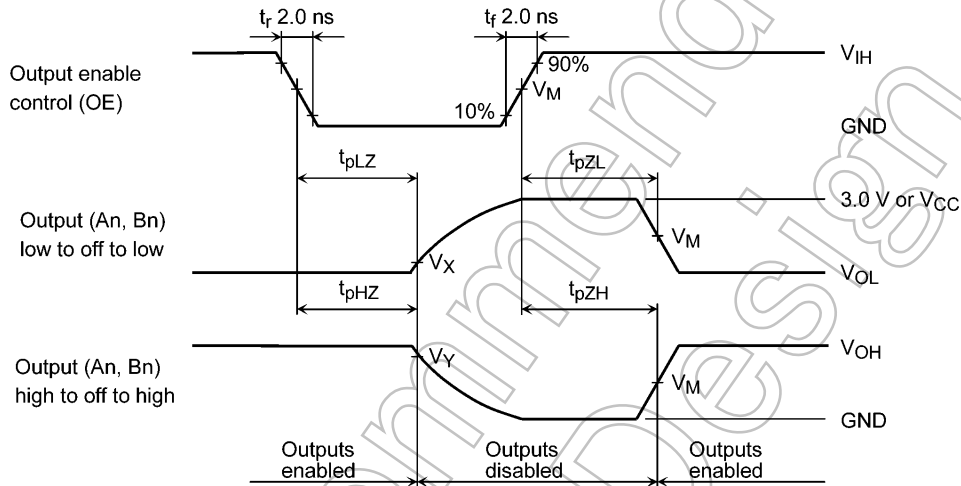


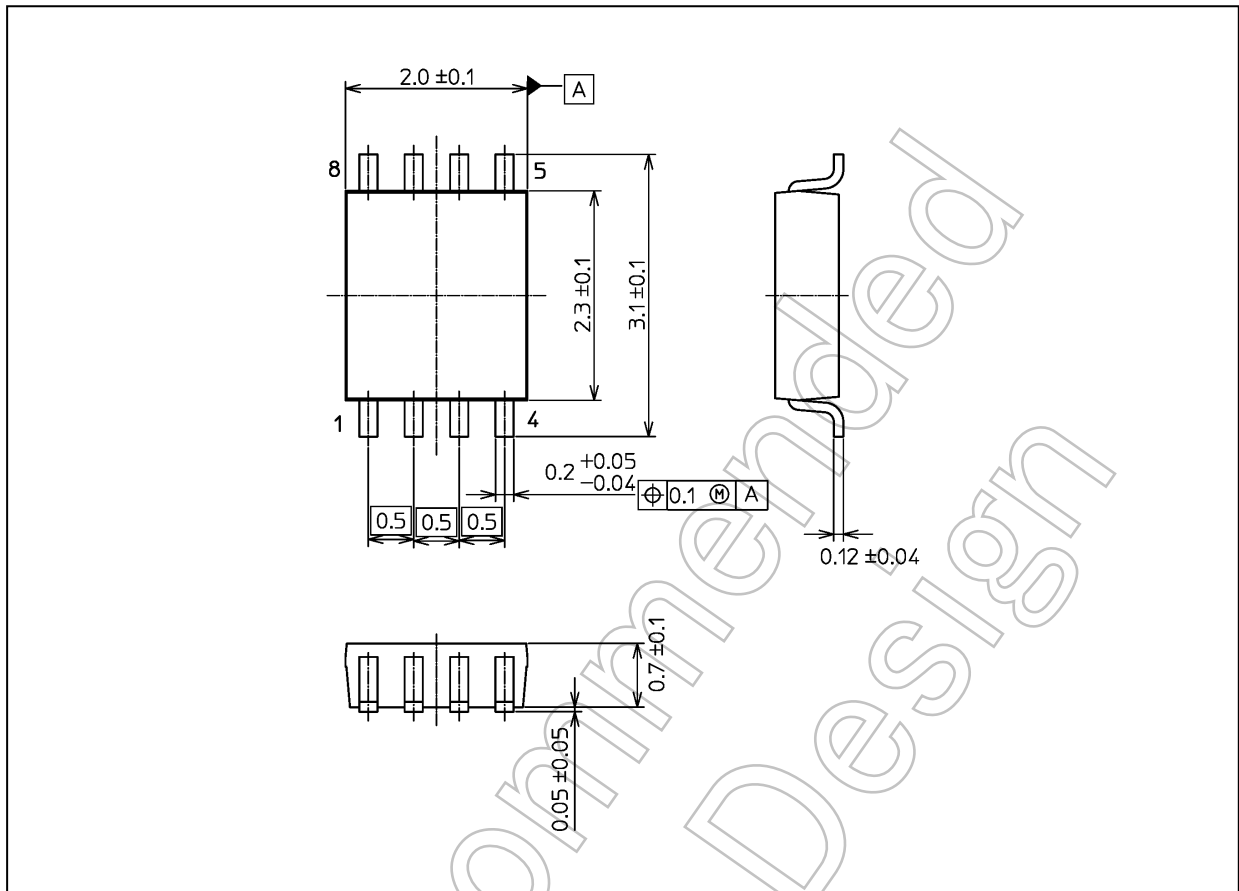
Fig. 11.2.4 AC Waveform of  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$

Table 11.2.2 AC Waveform Symbols

$V_{CC}$	Symbol	Value
$3.3 \pm 0.3 \text{ V}$	$V_{IH}$	2.7 V
	$V_M$	1.5 V
	$V_X$	$V_{OL} + 0.3 \text{ V}$
	$V_Y$	$V_{OH} - 0.3 \text{ V}$
$2.5 \pm 0.2 \text{ V}$ $1.8 \pm 0.15 \text{ V}$	$V_{IH}$	$V_{CC}$
	$V_M$	$V_{CC}/2$
	$V_X$	$V_{OL} + 0.15 \text{ V}$
	$V_Y$	$V_{OH} - 0.15 \text{ V}$
$1.5 \pm 0.1 \text{ V}$ $1.2 \text{ V}$	$V_{IH}$	$V_{CC}$
	$V_M$	$V_{CC}/2$
	$V_X$	$V_{OL} + 0.1 \text{ V}$
	$V_Y$	$V_{OH} - 0.1 \text{ V}$

**Package Dimensions**

Unit: mm



Weight: 10 mg (typ.)

Package Name(s)
TOSHIBA: SSOP8-P-0.50S
Nickname: US8

Not Recommended for New Design



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