

# NVD5C478N

## MOSFET – Power, Single N-Channel

### 40 V, 8.4 mΩ, 42 A

#### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	40	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	$T_C = 25^\circ\text{C}$	43	A
		$T_C = 100^\circ\text{C}$	30	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	30	W
		$T_C = 100^\circ\text{C}$	15	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	$T_A = 25^\circ\text{C}$	14	A
		$T_A = 100^\circ\text{C}$	10	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	3.0	W
		$T_A = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	210	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	25	A	
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, I_{L(pk)} = 3.4 \text{ A}$ )	$E_{AS}$	97	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	5.0	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	49.6	

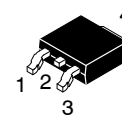
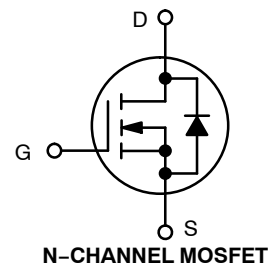
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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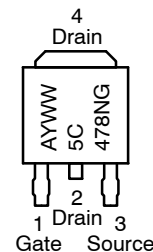
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
40 V	8.4 mΩ @ 10 V	42 A



DPAK  
CASE 369C  
STYLE 2

#### MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location  
Y = Year  
WW = Work Week  
5C478N = Device Code  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NVD5C478N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			22		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 30\ \mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		7.1	8.4	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 3\text{ V}, I_D = 15\text{ A}$		36		S

## CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		840		pF
Output Capacitance	$C_{oss}$			430		
Reverse Transfer Capacitance	$C_{rss}$			24		
Total Gate Charge	$Q_G(TOT)$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 15\text{ A}$		14		nC
Threshold Gate Charge	$Q_G(TH)$			2.8		
Gate-to-Source Charge	$Q_{GS}$			4.5		
Gate-to-Drain Charge	$Q_{GD}$			2.8		
Plateau Voltage	$V_{GP}$			4.8		

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 15\text{ A}, R_G = 2.5\ \Omega$		9.0		ns
Rise Time	$t_r$			16		
Turn-Off Delay Time	$t_{d(off)}$			15		
Fall Time	$t_f$			3.0		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	$T_J = 25^\circ\text{C}$	0.85	1.2	V
			$T_J = 125^\circ\text{C}$	0.73		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 15\text{ A}$		43		ns
Charge Time	$t_a$			21		
Discharge Time	$t_b$			22		
Reverse Recovery Charge	$Q_{RR}$			30		

4. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
5. Switching characteristics are independent of operating junction temperatures.

# NVD5C478N

## TYPICAL CHARACTERISTICS

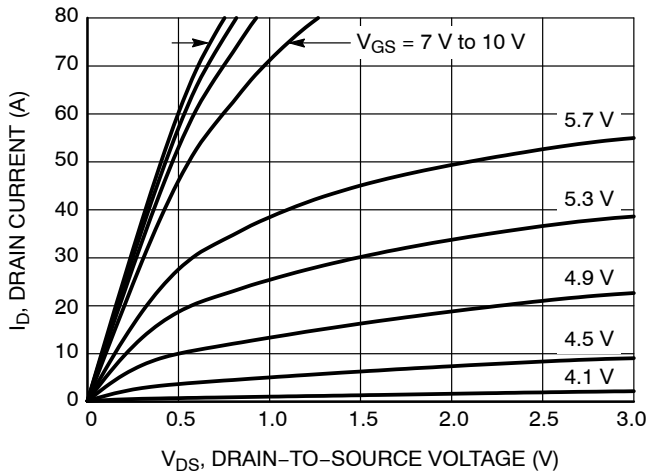


Figure 1. On-Region Characteristics

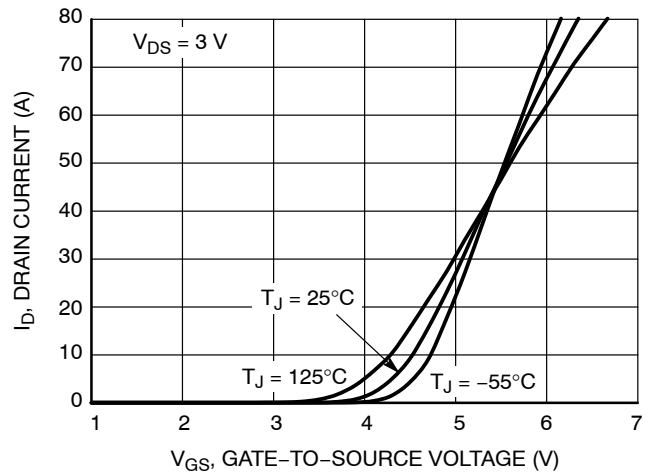


Figure 2. Transfer Characteristics

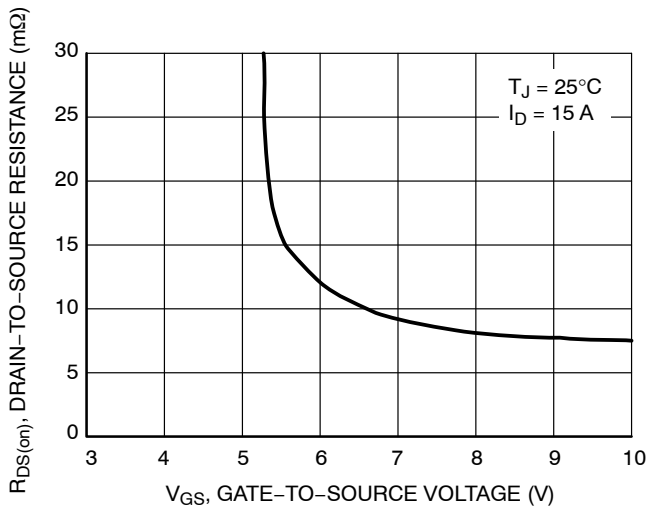


Figure 3. On-Resistance vs. Gate-to-Source Voltage

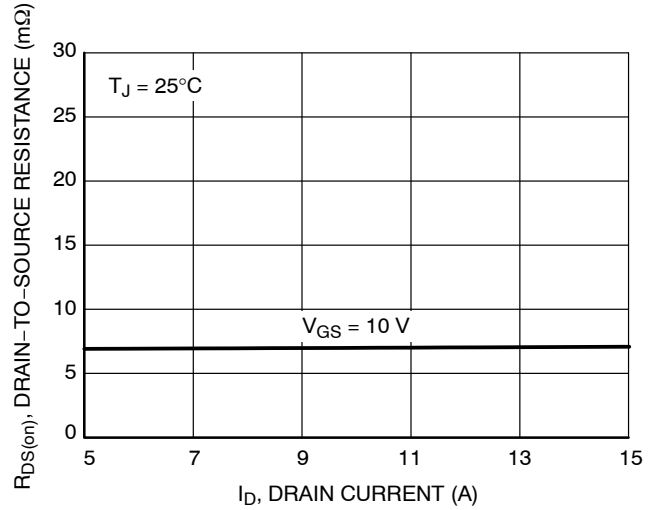


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

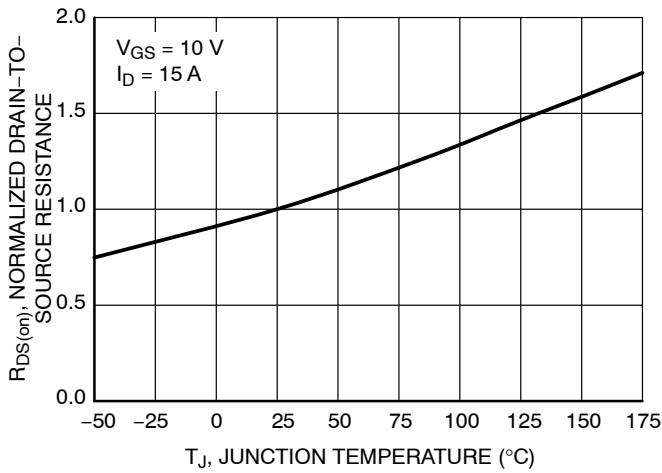


Figure 5. On-Resistance Variation with Temperature

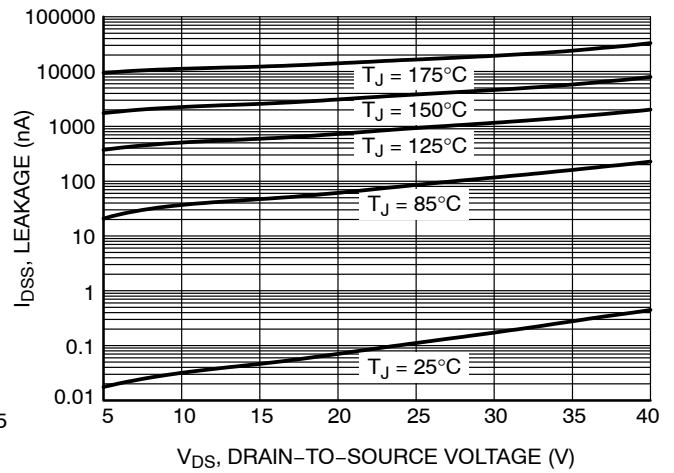


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVD5C478N

## TYPICAL CHARACTERISTICS

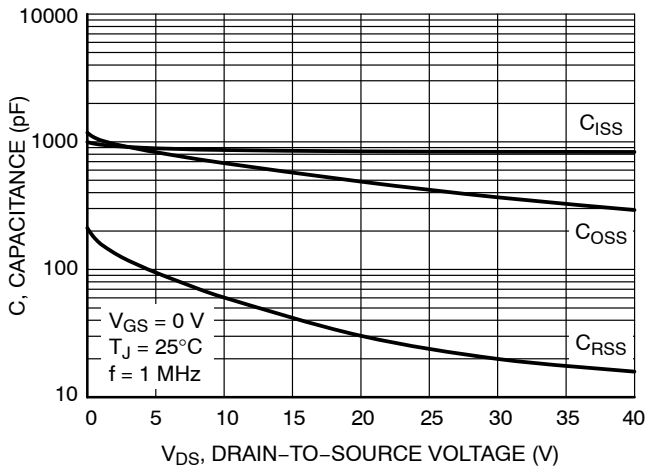


Figure 7. Capacitance Variation

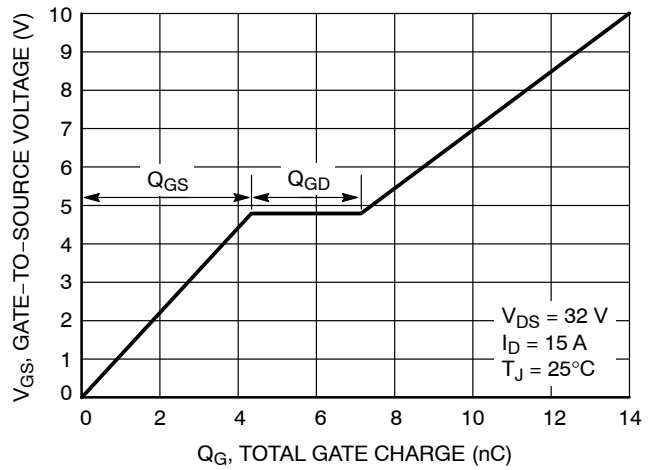


Figure 8. Gate-to-Source vs. Total Charge

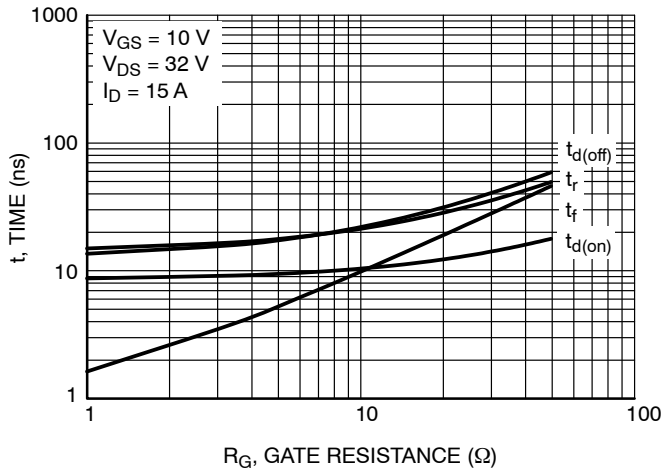


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

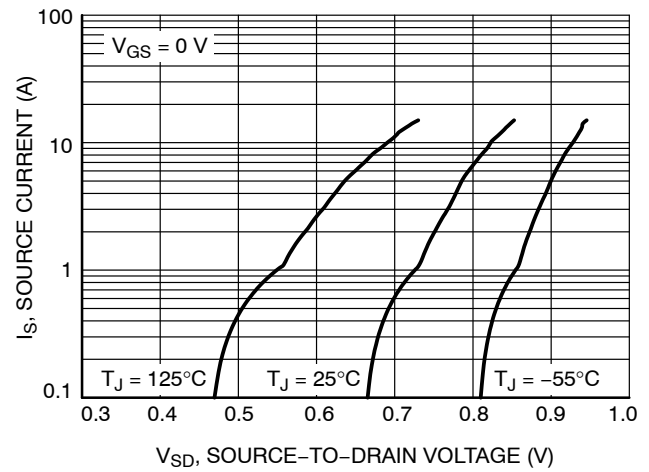


Figure 10. Diode Forward Voltage vs. Current

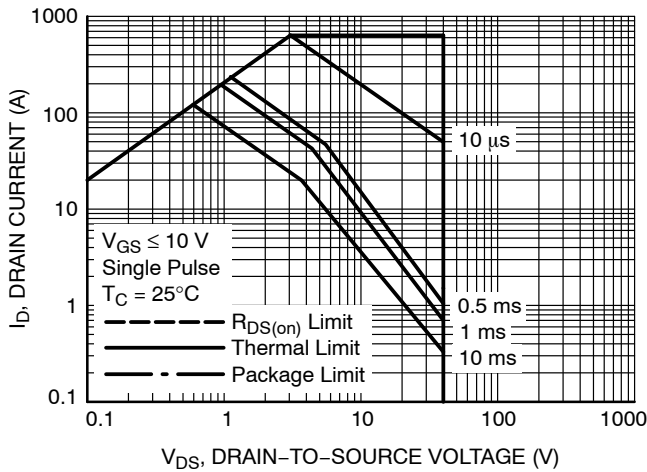


Figure 11. Maximum Rated Forward Biased Safe Operating Area

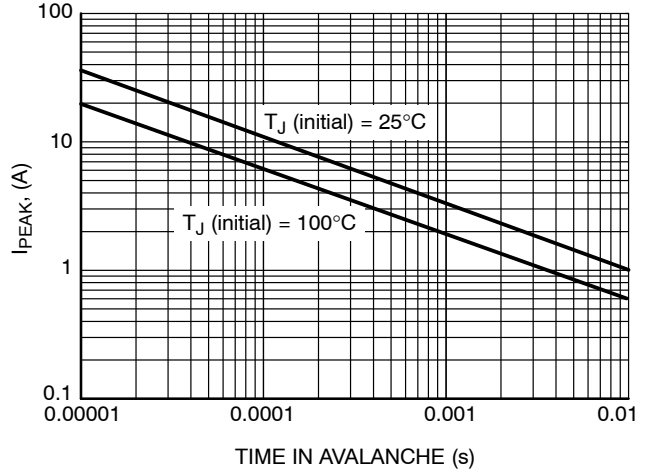
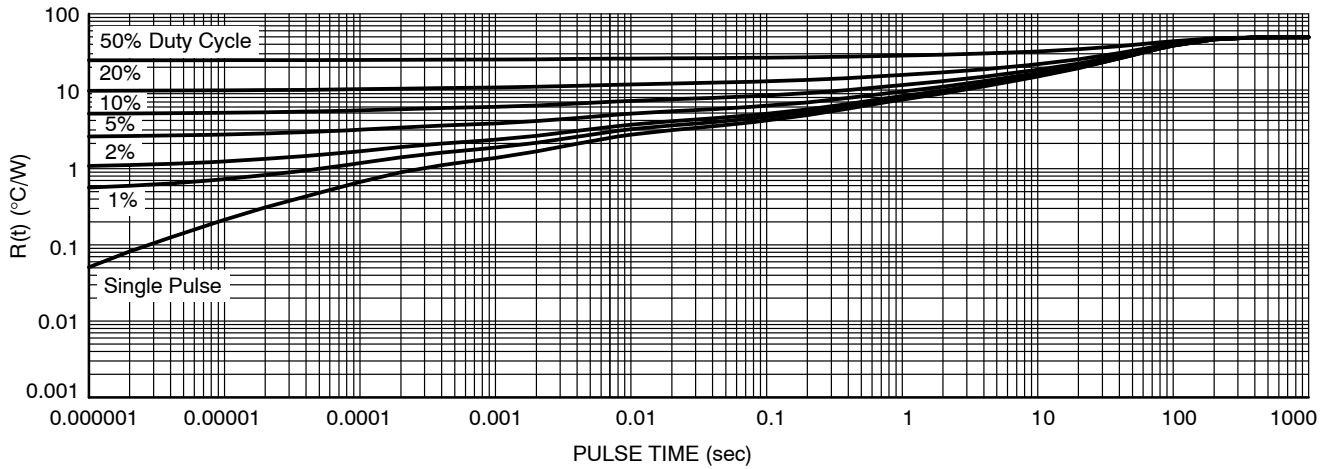


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVD5C478N

## TYPICAL CHARACTERISTICS



**Figure 13. Thermal Characteristics**

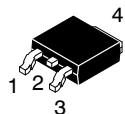
### ORDERING INFORMATION

Order Number	Package	Shipping <sup>†</sup>
NVD5C478NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

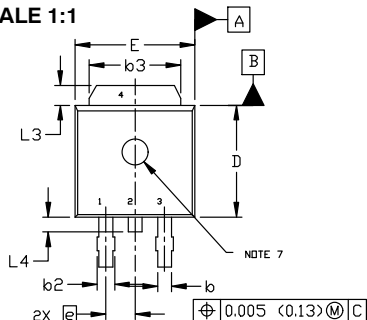
## PACKAGE DIMENSIONS



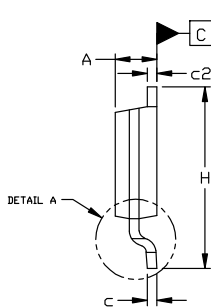
### DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW

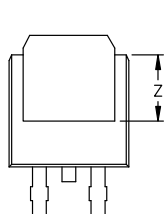


SIDE VIEW

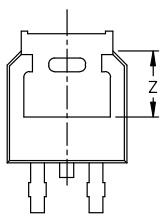
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

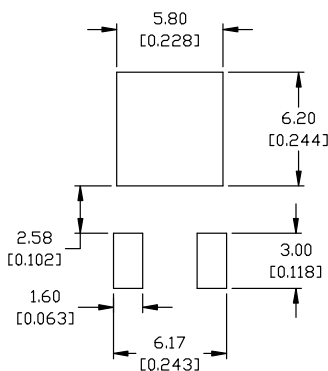


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



#### RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

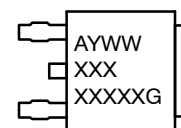
- |                                                                       |                                                              |                                                                  |                                                               |                                                               |
|-----------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|
| STYLE 1:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 2:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE | STYLE 5:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |
|-----------------------------------------------------------------------|--------------------------------------------------------------|------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|

- |                                                       |                                                                       |                                                                |                                                                            |                                                                   |
|-------------------------------------------------------|-----------------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|
| STYLE 6:<br>PIN 1. MT1<br>2. MT2<br>3. GATE<br>4. MT2 | STYLE 7:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | STYLE 8:<br>PIN 1. N/C<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | STYLE 9:<br>PIN 1. ANODE<br>2. CATHODE<br>3. RESISTOR ADJUST<br>4. CATHODE | STYLE 10:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE |
|-------------------------------------------------------|-----------------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|

#### GENERIC MARKING DIAGRAM\*



IC



Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>DPAK (SINGLE GAUGE)</b>	<b>PAGE 1 OF 1</b>

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