InnoSwitch3-PD Family

Off-Line QR Flyback Switcher IC with Integrated USB Type-C and USB PD Controller, High-Voltage Switch, Synchronous Rectification and FluxLink Feedback

Product Highlights

USB Type C and PD Controller

- USB Power Delivery 3.0 + PPS provider and QC4 support
- Compliant with USB Type-C Rev. 1.3
- Integrated VCONN FETs with soft start and over-current protection
- Supports electronically marked cables
- Configurable pull-up resistor Rp
- On chip temperature sensor
- Telemetry for power supply status and fault monitoring
- PowiGaN™ technology – up to 100 W without heat sinks
- Dedicated NTC pin for temperature sense

Highly Integrated, Compact Footprint

- Multi-mode Quasi-Resonant (QR) / DCM / CCM flyback controller, high-voltage switch, secondary-side sensing and synchronous rectifier driver
- Optimized efficiency across line and load range
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Instantaneous transient response
- Drives low-cost N-channel FET series load switch

EcoSmart™ – Energy Efficient

- No-load consumption as low as 14 mW
- Enables power supply designs that easily comply with all global energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Input voltage monitoring with accurate brown-in/brown-out and overvoltage protection
- Output OV/UV fault detection with independently configured responses
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Programmable watchdog timer for system faults
- Integrated high voltage FETs for VBUS short protection on CC1, CC2

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 isolation voltage 4000 VAC (max) and TUV (EN62368) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- High efficiency USB PD 3.0 + PPS adapters for smart phones, tablets, notebooks, digital cameras, and Bluetooth accessories
- Quick Charge protocol based power adapters
- Direct-charge mobile device chargers

Description

The InnoSwitch™3-PD dramatically simplifies the development and manufacturing of USB PD power supplies by incorporating primary switch and controller, isolated feedback, secondary control and USB PD controller into a single package.

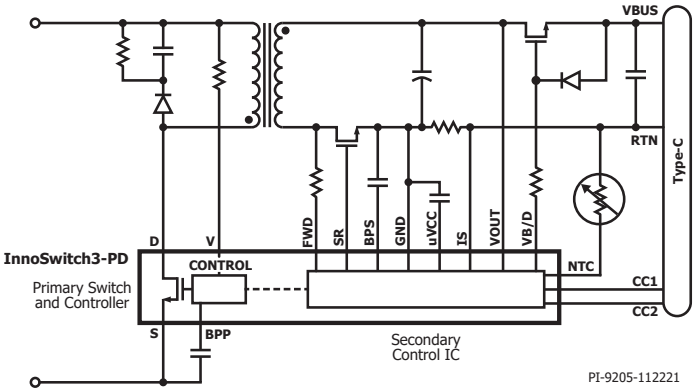


Figure 1. Typical Application Schematic.

Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table[1]

Product[4,5]	230 VAC ± 15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
INN3865C/75C	25 W	30 W	22 W	25 W
INN3866C/76C	35 W	40 W	27 W	36 W
INN3877C	40 W	45 W	36 W	40 W
INN3867C	45 W	50 W	40 W	45 W
INN3868C	55 W	65 W	50 W	55 W
INN3878C	70 W	75 W	55 W	65 W
INN3879C	80 W	85 W	65 W	75 W
INN3870C	90 W	100 W	75 W	85 W
INN3896C	25 W	35 W	20 W	30 W

Table 1. Output Power Table.

Notes:

1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. C Package: InSOP-24D.
5. INN386xC – 650 V MOSFET, INN387xC – 725 V MOSFET, INN389xC – 900 V MOSFET, INN3878C, INN3879C and INN3870C – 750 V PowiGaN switch.

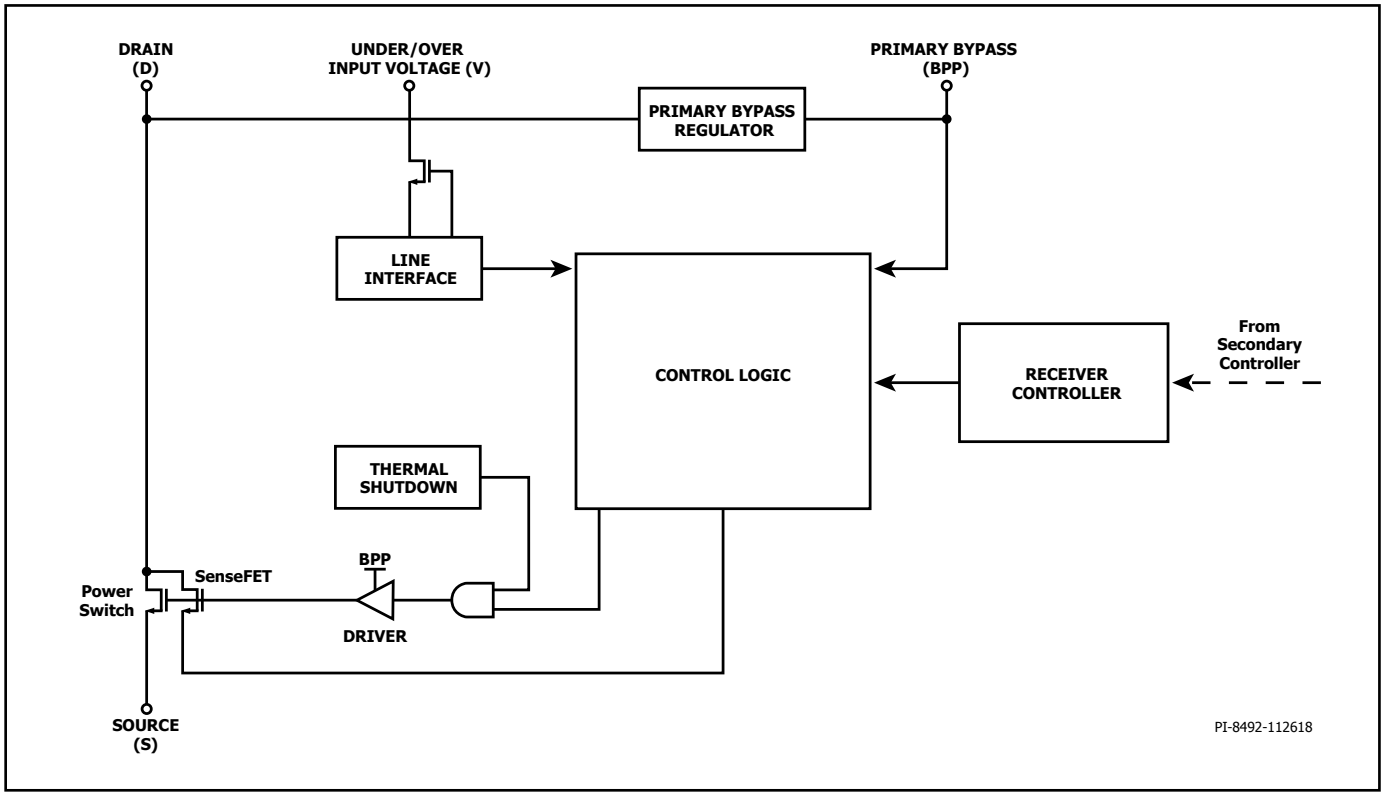


Figure 3. Primary Controller Block Diagram.

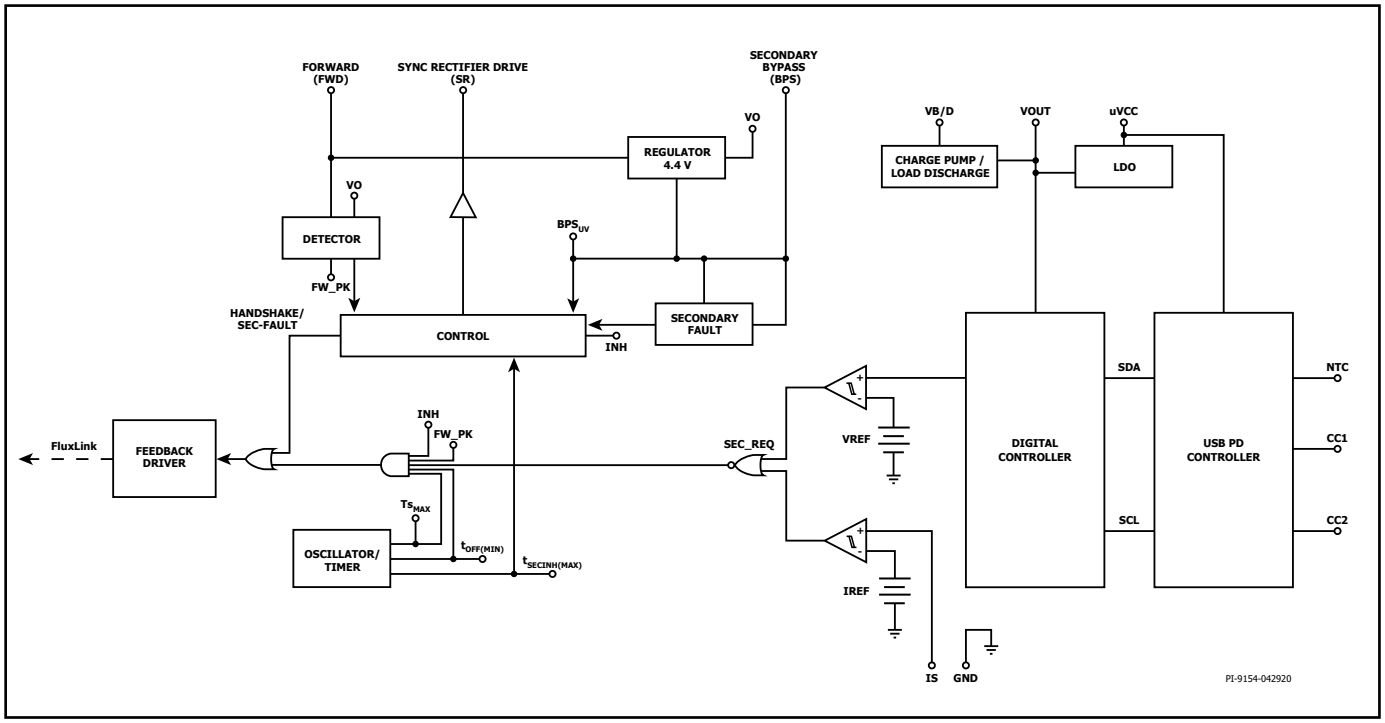


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) (Pin 2)
Ground reference for the secondary IC. Note this is not the power supply output ground due to the presence of the sense resistor between this and the ISENSE pin.

CC2 Pin (Pin 3)
USB Type-C configuration channel.

CC1 Pin (Pin 4)
USB Type-C configuration channel.

SECONDARY BYPASS (BPS) Pin (Pin 5)
It is the connection point for an external bypass capacitor for the secondary IC supply.

TEMPERATURE SENSE (NTC) Pin (Pin 6):
This pin has an internal current source. With NTC resistor connected on this pin, it can be used to monitor external temperature.

VCC SUPPLY (uVCC) Pin (Pin 7)
This is a supply pin for the internal controller. An external 2.2 μF capacitor is required between this pin and the GND pin.

VBUS Series Switch Drive and Load Discharge (VB/D) Pin (Pin 8)
VBUS enable and driver for NMOS gate for VOUT to VBUS series pass FET(s). This pin is used to discharge output load voltage(VBUS).

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver output and connection to external SR FET gate terminal.

OUTPUT VOLTAGE (VOUT) Pin (Pin 10)
Connected directly to the output voltage providing current for the secondary IC and sense for output voltage regulation. This pin also has an active/programmable pull-down current source.

FORWARD (FWD) Pin (Pin 11)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing plus providing power for the secondary IC when VOUT is below a threshold value.

NC Pin (Pin 12)
Leave open. Should not be connected to any other pins.

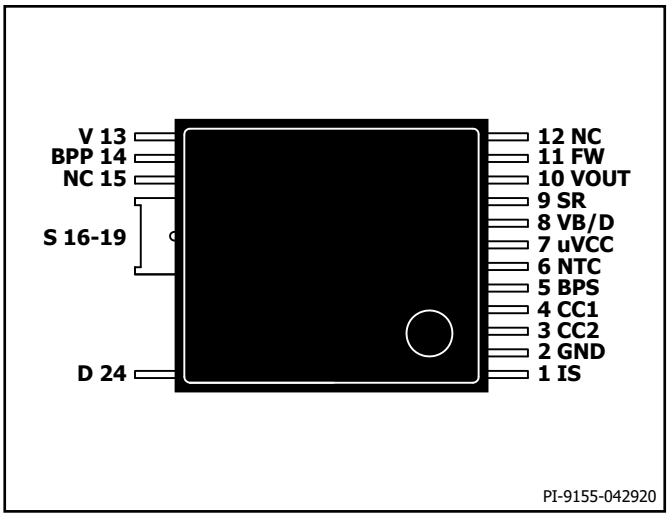


Figure 5. Pin Configuration.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting under and overvoltage conditions at the power supply input. When connected to the AC side of the bridge, a high-voltage switch is opened when not sensing to reduce power consumption. This pin should be tied to GND to disable UV/OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
It is the connection point for an external bypass capacitor for the primary IC supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open or connect to SOURCE pin or BPP pin.

SOURCE (S) Pin (Pin 16-19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
This pin is the power switch drain connection.

InnoSwitch3-PD Functional Description

The InnoSwitch3-PD combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device. The architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to communicate accurate direct sensing of the output voltage and output current on the secondary IC to the primary IC.

The primary controller on InnoSwitch3-PD is a quasi-resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection and leading edge blanking.

The InnoSwitch3-PD secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, an I^2C interface to control power supply parameters and telemetry functions, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, QR mode circuit, oscillator and timing functions, and a host of integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

InnoSwitch3-PD has variable frequency QR controller plus CCM/CrM/DCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to VBPP by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-PD to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW.

Primary Bypass ILIM Programming
InnoSwitch3-PD ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value.

There are 2 selectable capacitor sizes - 0.47 μF and 4.7 μF for setting standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP}-$V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{BP} to re-enable turn-on of the power switch.

Primary Bypass Output Overvoltage Function
The PRIMARY BYPASS pin has a OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds ISD, the device will latch-off or auto-restart depending on the H-code.

VOUT OV protection is also included as an integrated feature on the secondary controller.

Over-Temperature Protection
The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response depending on the H-code.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

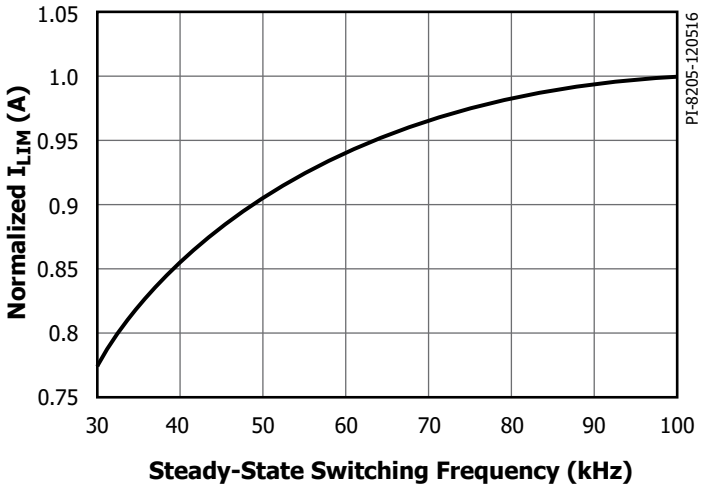


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100% I_{LIM}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter
The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart
In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-PD enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:
1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection
In the event that there are two consecutive cycles where the drain current is reached 110% of I_{LIM} within ~500 ns (the blanking time + current limit delay time) (including leading edge current spike), the controller will skip 2.5 cycles or ~25 ms (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring
The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage switch on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. The controller samples the input line at light load conditions when the time between switching cycles is 50 µsec or more. At <50 µsec between switching cycles, the high-voltage switch will remain on making sensing continuous.

Primary-Secondary Handshake
At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

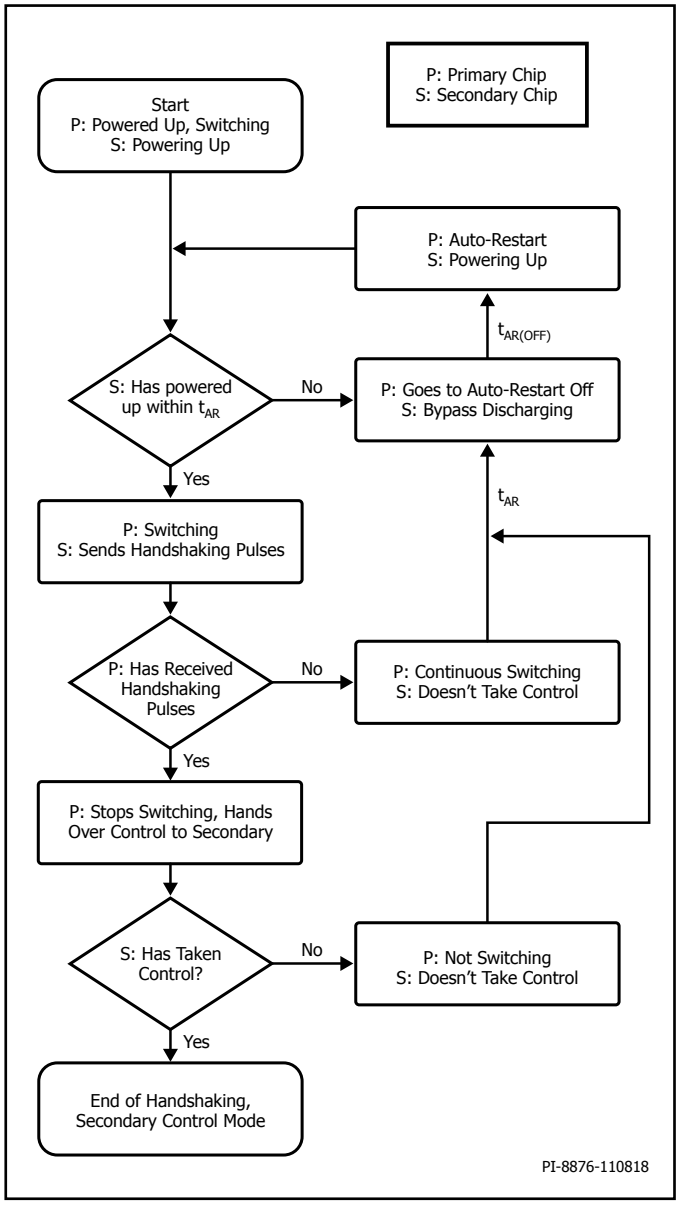


Figure 7. Primary-Secondary Handshake Flow Chart.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, tAR (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine

The InnoSwitch3-PD features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the transformer is most likely to resonate – increasing noise amplitude) between 5 kHz and 12 kHz – 200 µs and 83 µs period respectively. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power switch is inhibited. This feature is disabled in INN3878C, INN3879C and INN3870C.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered through regulator 4.4 V block by either VOUT or FW connections to the SECONDARY BYPASS pin. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block. The USB Type-C and PD controller is powered through uVCC internally generated from VOUT as shown in the block diagram in Figure 4.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin is used to sense when to turn off the SR FET in discontinuous mode operation when the voltage across the FET on resistance drops below the $V_{SR(TH)}$ threshold.

In continuous conduction mode (CCM) operation of the SR FET is turned off when the feedback pulse is sent to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off while operating in continuous mode.

The output voltage is regulated on the VOUT pin and defaults to 5 V at start-up.

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins regulates the output current in constant current regulator mode.

The controller implements the hardware and firmware required for key feature implementations like USB Type-C, USB PD controller and proprietary Quick Charge 4 protocol.

USB Type-C

Controller implements the USB-C Source CC FSM that interacts with firmware. Firmware enables the USB-C CC FSM by configuring the Rp current advertisements and controls VBUS (enable/disable), VCONN (enable, restart, latch-off), USB PD control (enable/disable) and QC control (enable/disable).

USB Power Delivery
USB PD stack includes Policy Engine (PE), Protocol layer (PRL) and Physical layer (PHY). USB PD block interacts with firmware. Firmware responsibilities include cable discovery, PDO management (source capabilities), message handling (control message, data message or vendor defined message), hard reset and VBUS management for voltage and current transitions.

Programmable Voltage and Current
The output voltage is programmable from 3.3 V to 21 V depending on the source capabilities and request from sink. The fast response feedback loop of the IC features 10 mV (ΔV_{OUT}) voltage change resolution, easily meeting the 20 mV programming step size required to meet PPS requirements. The programmable current set point features 20% to 100% operating range, with a programming step size of 0.8% of full-scale current, thereby meeting the iPpsCLMin and iPpsCLStep requirements of PPS. Below 5 V and for load current less than 50 mA, voltage command step size of 10 mV may result in non-montonicity since operating frequency is very low.

The full-scale constant-current threshold is set with the sense resistor between the IS and GND pins. The typical value for the full-scale current voltage drop is 32 mV (ISV(TH)). The resolution step size is (0.78% /step):
32 mV / 128 = 0.25 mV / step / R_S

For a 5 A CC threshold, the current sense resistor is 6.4 mΩ. The current limit step size for this example is 39.1 mA / step.

Bus Switch Driver and Discharge
InnoSwitch3-PD has an internal driver that guarantees turn-on of an n-channel FET series bus switch with source voltage as high as 24 V. The VB/D pin, which enables the bus switch is also configurable as the discharge path for the load. The functionality of VB/D pin is controlled in the firmware.

Protections
Protection features include output undervoltage (UV), overvoltage (OV) protection and over-temperature protection.

The output UV/OV thresholds are programmable through firmware. The response to these faults are configurable in firmware to auto-restart, latch-off and no-response. Default is set to auto-restart. The secondary controller also features generation of an interrupt signal to USB PD controller if one or more of the faults is detected.

Telemetry Feature
The status of the power supply is accessible using the Vendor Defined Messages (VDM) if enabled in the firmware. The telemetry can include CV, CC and constant power set points, OV/UV thresholds, all protection settings and complete fault status.

Minimum Off-Time
The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 70% of the maximum programmed current limit (at f_{SREQ} operation).

After handshake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above ~3.6 V before the expiration of the soft start timer ($t_{SS(RAMP)}$) after handshake has occurred.

If the output voltage reaches regulation within the $t_{SS(RAMP)}$ period, the frequency ramp is immediately aborted and the secondary controller is permitted to go to full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 ms.

Output Voltage Weak Bleeder
In the event that the sensed voltage on the OUTPUT VOLTAGE pin is slightly higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

SECONDARY BYPASS Pin Overvoltage Protection
The InnoSwitch3-PD secondary controller features a SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ the secondary will initiate a fault response dictated by sec-fault response.

SR Disable Protection
In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. At start-up the controller will apply a current to the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF the resulting voltage is above the reference voltage, and the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF (the resulting voltage is below the reference voltage), the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-PD features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous- conduction mode (CCM). See Figure 8.

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-resonant (QR) mode is enabled for 20 μsec after DCM is detected. QR switching is disabled after 20 μsec, at which point switching may occur at any time a secondary request is initiated. The secondary controller includes blanking of ~1 μs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

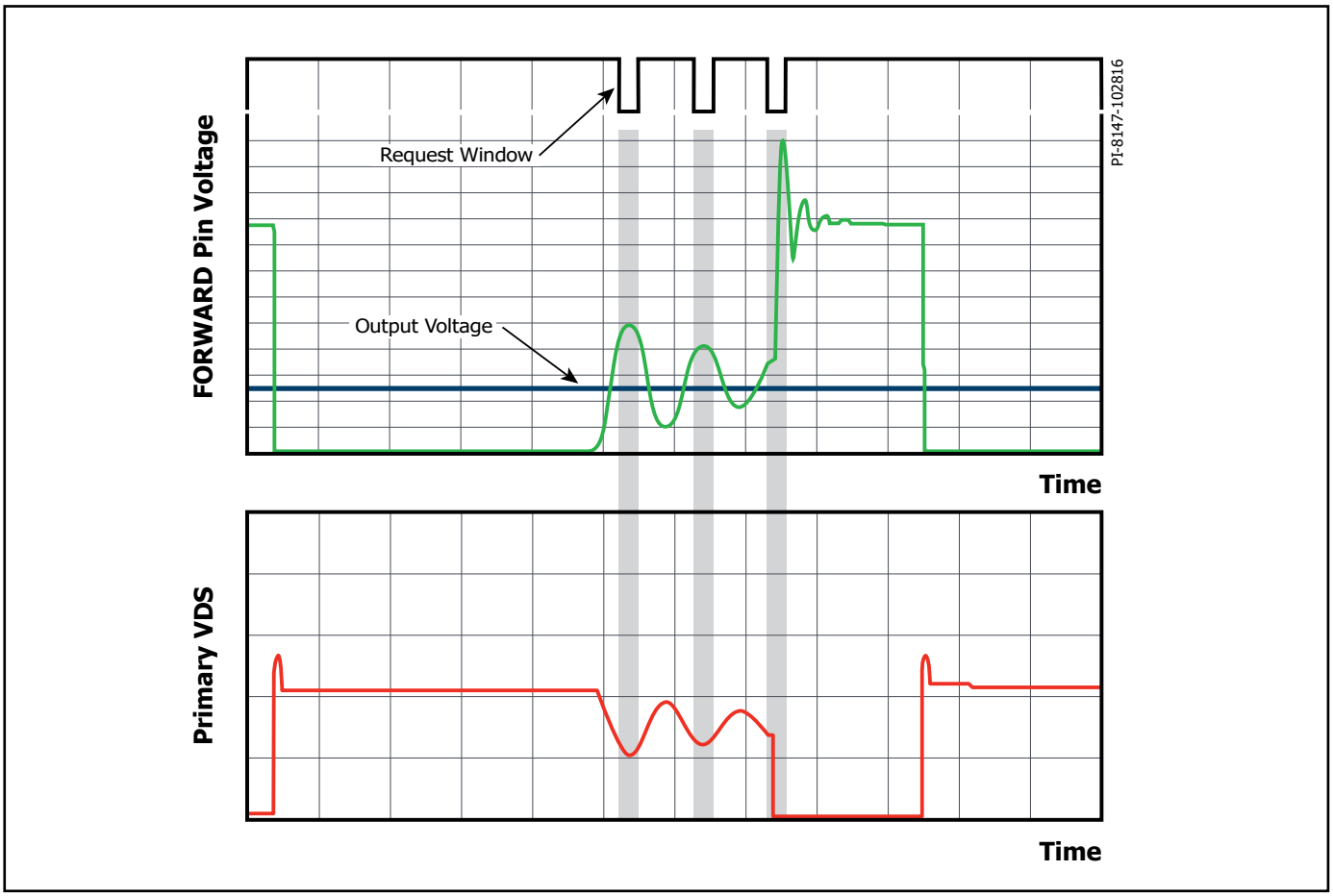


Figure 8. Intelligent Quasi-Resonant Mode Switching.

Constant Output Power Voltage Threshold VKP

A constant output power characteristic is programmable in firmware using the "knee power voltage" in conjunction with the 100% constant current regulation threshold (full-scale current setting). If the full-scale CC is 2.5 A and the knee power voltage is set to 8 V, the constant power is 20 W. If the VKP were set to 12 V, the resultant constant power characteristic above the VKP threshold would be 30 W. This feature can be enabled through firmware.

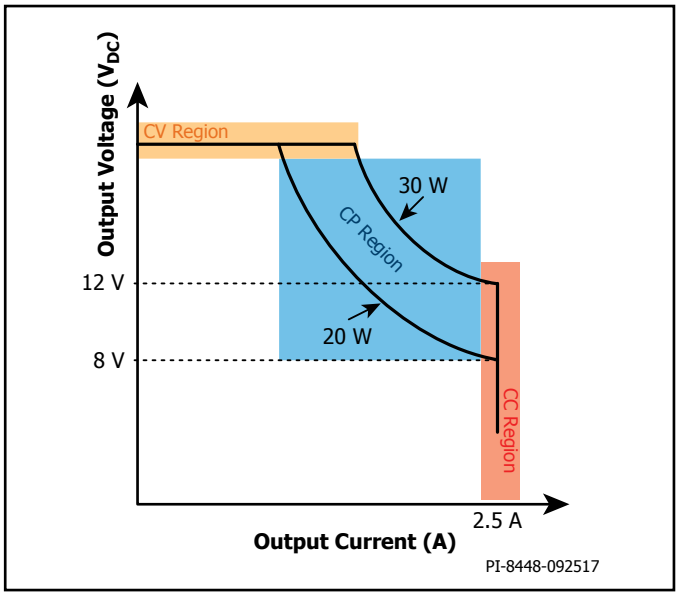


Figure 9. Constant Output Power Profile.

From no-load to heavy loading conditions, InnoSwitch3-PD will operate in CV then transition into CP then into CC region below the VKP threshold. Setting VKP to value greater than maximum output voltage results in no Constant Output Power regulation region.

Reducing the constant current regulation threshold does not modify the maximum-programmed output power with a given VKP setting.

From the example, setting CC regulation to 2 A (full-scale CC is still 2.5 A), with VKP = 8 V, would result in output profile shown in Figure 10 with CP characteristic intercept of 10 V for the same 20 W constant power characteristic.

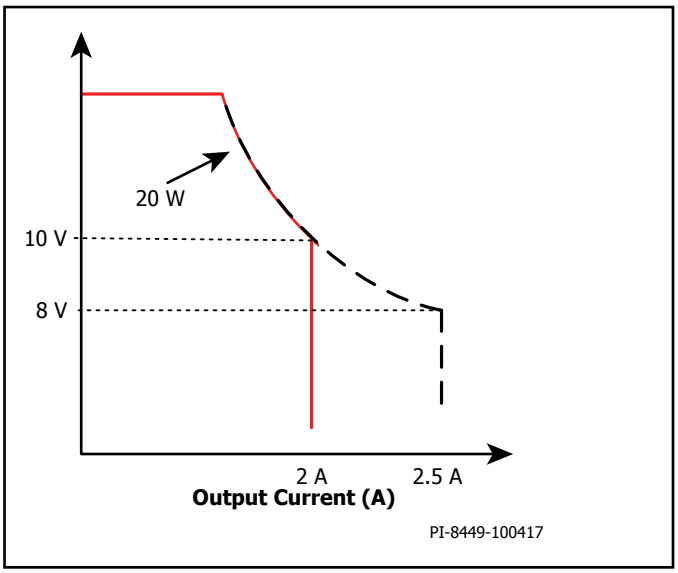


Figure 10. Constant Output Power Profile with Reduced CC Regulation Threshold.

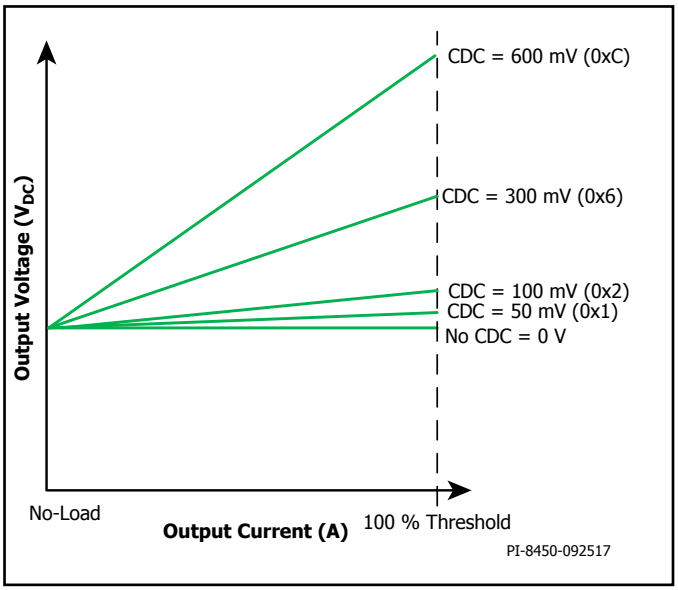


Figure 11. CDC as Function of Load Current.

Cable Drop Compensation (CDC)
The amount of cable drop compensation has a controllable range of 0 V to 600 mV in 50 mV/steps. CDC is applied as a function of the current through the sense resistor (resistor between IS and GND pins) used to program the constant current regulation threshold. At no-load there is no CDC and the compensation is increased linearly as load increases and reaches the maximum-programmed value at the onset of the 100% constant-current regulation threshold (full- scale voltage across the current sense resistor).

If the current sense resistor between IS pin to GND pin is shorted, there will be neither any cable drop compensation nor any constant current regulation.

Constant Voltage Only Mode
The InnoSwitch3-PD can be programmed to operate with constant voltage only for fixed PDOs and have no constant current regulation mode. The set output current sets the over-load threshold instead of regulating the constant current when the CVO mode is enabled. Once the load current exceeds the programmed current a peak load timer (t_{PLT}) is started. The options for the peak load timer are 8, 16, 32 and 64 ms. If the peak load exceeds the programmable timer, the InnoSwitch3-PD can be programmed to respond to this fault as auto-restart, latch-off or no-response through the firmware. The default response for CVOL (CVO response) is no-response with 8 ms timer.

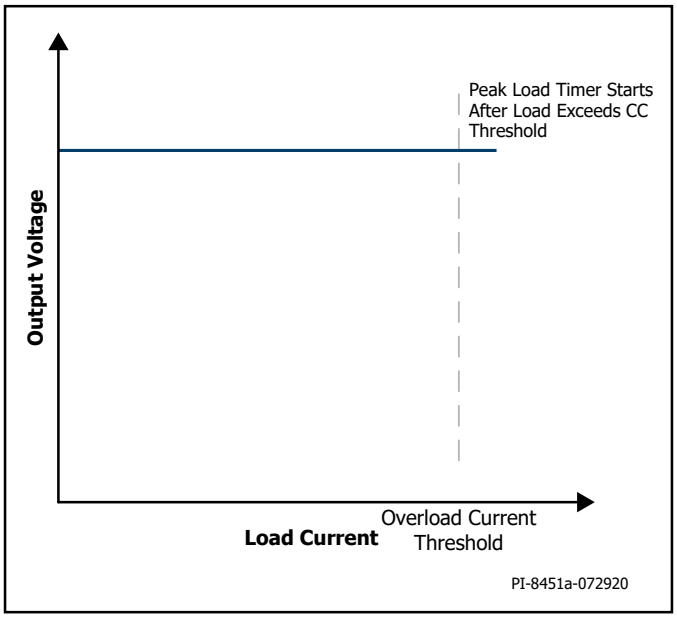


Figure 12. Constant Voltage Only (CVO) Mode.

The output undervoltage protection mode discussed in Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior section is still active in the CVO mode of operation.

Type-C Connection Detection
Type-C block detects the cable connection and disconnection events by comparing the voltage levels on CC line with reference voltage. Depending on the USB Type-C current advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V), the reference voltage is set. Comparator will compare CC line voltage with the set reference voltage and enable the sink detection signal.

For e-marker detection, depending on the USB Type-C current advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V), the reference voltage is set. Comparator will compare CC line voltage with the set reference voltage and enable the e-marker detection.

VCONN Supply
On detection of the e-marker cable, integrated VCONN switch closes and provides the VCONN supply to appropriate CC pin. The gate voltage applied to VCONN switch uses soft start to control the inrush current. In the case of over current and short circuit faults, the VCONN switch will turn off.

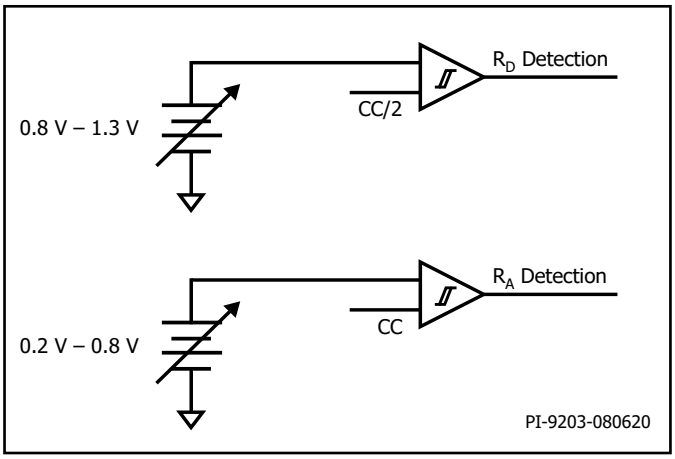


Figure 13. Type-C Detection.

Internal Die Temperature Sense
InnoSwitch3-PD has the feature of sensing the die temperature on the secondary side. This feature can be used to sense IC temperature.

External Connector Temperature Sense Using NTC Resistor
InnoSwitch3-PD includes an internal current source on the NTC pin. Connecting a Negative Temperature Coefficient temperature sense resistor on this pin enables the external temperature sense feature. The resistor value used will determine the threshold for Type-C Connector Fault Protection feature implemented in the firmware. ADC is used to sense the voltage on the NTC pin.

Protection Mechanisms

Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior
Besides the ability of programing the OV/UV thresholds on the fly as a function of the set CV, the behavior of the power supply once a fault occurs can be (a. No-Response (NR), b. Auto-restart (AR) or c. Latch-off (LO)). The timing for the UV fault detection is programmable with following options – 8 ms, 16 ms, 32 ms and 64 ms. The output overvoltage delay is fixed at ~80 µs.

IS Pin and Output Short-Circuit Fault Protection
The InnoSwitch3-PD can be configured to monitor whether a short-circuit fault occurs across the output current sense resistor or a short-circuit fault across the IS to GND pins. A fault is annunciated in the event the IS pin voltage does not exceed approximately 50% of the full constant-current threshold ($I_{SV(TH)}$) with a switching frequency exceeding a programmed threshold. Switching frequency programming options include – 30 kHz, 40 kHz, 50 kHz and 60 kHz which is set in the firmware.

An IS pin short (ISSC) can be programmed to have a response to be a. No-Response (NR), b. Auto-restart (AR) or c. Latch-off (LO).

The InnoSwitch3-PD sets the CCSC fault once the voltage across the IS pin resistor exceeds more than ~3 times the $I_{S(VTH)}$. The CCSC fault can be programmed to have response of a (a.) No Fault or (b.) Auto-Restart. In applications where the output capacitance after the series bus-switch exceeds 100 µF, the response for CCSC should be set to No-Response for proper start-up and may be programmed back to Auto-restart during normal operation after the series bus-switch is closed. See firmware configuration table for the device fault response setting.

Note: Setting CCSC fault to No-response and creating a short-circuit condition at output will result in auto-restart.

Opening and Closing the Series VBUS Switch

Closing the VBUS Series switch speeds up the ADC sampling frequency in order to achieve high control accuracy. When the VBUS switch is open, the system is reset to the default output voltage of 5 V. Disabling the series VBUS switch also resets all the programmed faults and thresholds to default values. Enabling the VBUS Series switch automatically disables the Active VOUT Pin Bleeder. In the event of an auto-restart or latch-off, firmware controls the bus switch enable/disable state.

Active VOUT Pin Bleeder and Output Load Discharge Functions

There may be circumstances where the VOUT pin strong bleeder function must be activated to discharge the output voltage from a high to low regulation set point. The BLEEDER function is controlled in firmware to bleed the output voltage from high to low set point.

The InnoSwitch3-PD automatically activates a weak current bleeder (<5 mA) on the VOUT pin until the output voltage settles within the set regulation threshold.

The InnoSwitch3-PD can also discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. Load discharge function is controlled in firmware to discharge VBUS output after opening the VBUS switch.

Secondary Over-Temperature Protection

As the secondary controller die temperature increases beyond ~125 °C, the active VOUT pin bleeder function described above will be turned off. The bleeder will not be permitted to be re-enabled until the controller temperature falls below the programmable hysteresis value.

Transient Response

If faster transient response is required in the application the InnoSwitch3-PD includes command registers which can be configured in the firmware to reduce the time for low to high output voltage transitions.

Constant Voltage Load
The constant current regulation mode in the InnoSwitch3-PD can be optimized for constant voltage (CV) type load if this is required by the end application. Enabling this command register through firmware reduces the output current ripple for CV load only.

VCONN Switch Over-Current Protection
At the end of soft start for VCONN supply, a current sense branch is enabled which mirrors the VCONN supply current. This is compared to the over-current threshold 35 mA, 40 mA or 45 mA programmed in the firmware. Once the load current is more than programmed threshold, sense circuit will generate a fault signal and turn off VCONN switch.

VCONN Switch Short-Circuit Protection
Before enabling the soft start for VCONN supply, device will detect for any short-circuit fault on the CC line. Any load resistance below ~18 Ohm is treated as short-circuit on the CC line and the detection circuit will generate a fault signal and turn off VCONN switch if the load resistance is less than the value specified above. Firmware controls enable/disable of this feature.

Type-C Connector Over-Temperature Fault Protection
InnoSwitch3-PD has an internal current source on the NTC pin. With NTC resistor connected on this pin and mounted close to type-C connector, it can be used to implement the over temperature protection feature. ADC is used to detect the voltage on NTC pin and send PSU OFF command if temperature exceeds the set threshold in firmware. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold. Firmware controls the logic implementation of this feature.

Output Voltage Measurement
The voltage on the VOUT pin has accuracy of ±3% over the entire regulation range. The report back resolution step size depending on output voltage is tabulated below:

Output Voltage Range (V)		Resolution Step Size
3	7.2	20 mV
7.2	10	50 mV
10	24	100 mV

Table 2. Output Voltage Measurement Resolution.

When the output voltage is below 5 V at loads below ~50 mA, the voltage may fluctuate due to very low switching frequency of the converter but within the specified tolerance. This is normal and expected behavior.

Output Current Measurement
The load current is available on a relative basis with respect to the full-scale constant current regulation threshold programmed by the sense resistor tied between the IS and GND pin of the InnoSwitch3-PD. The ADC full range is 128, which denotes 100% threshold across the current sense resistor.

The accuracy of the output current read-back is tightest at full scale and decreases as the voltage threshold across the current sense resistor decreases as shown in Figure 14.

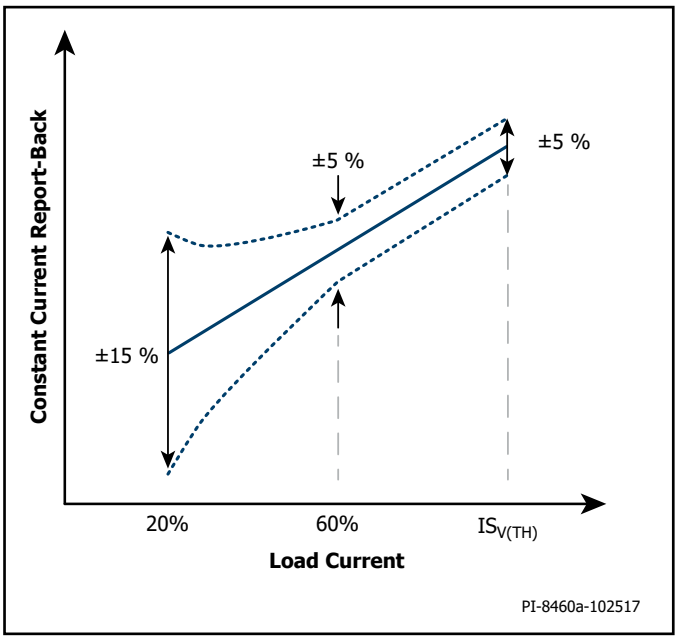


Figure 14. Constant-Current Report Back Tolerance.

The device uses 16 sample-rolling averages of the measured output current and output voltage for regulation. The output voltage and current measurements are updated every 100 ms.

uVCC Power Supply
The uVCC pin provides an accurately regulated 3.6 V supply to the internal PD controller. The uVCC pin should be decoupled to the GND pin with at least a 2.2 µF ceramic capacitor. No external load should be connected on this pin. When the VOUT pin voltage is less than 3.9 V, the internal LDO will droop and follow VOUT pin voltage. Under these conditions, the uVCC pin voltage is dependent on internal load current and internal series impedance. At VOUT pin = 3 V and 6 mA load current on uVCC, the expected output on uVCC will be ~2.85 V (3 V – 24 Ohm x 6 mA). If uVCC pin voltage falls below the minimum operating voltage then PD controller will shut down.

Applications Example

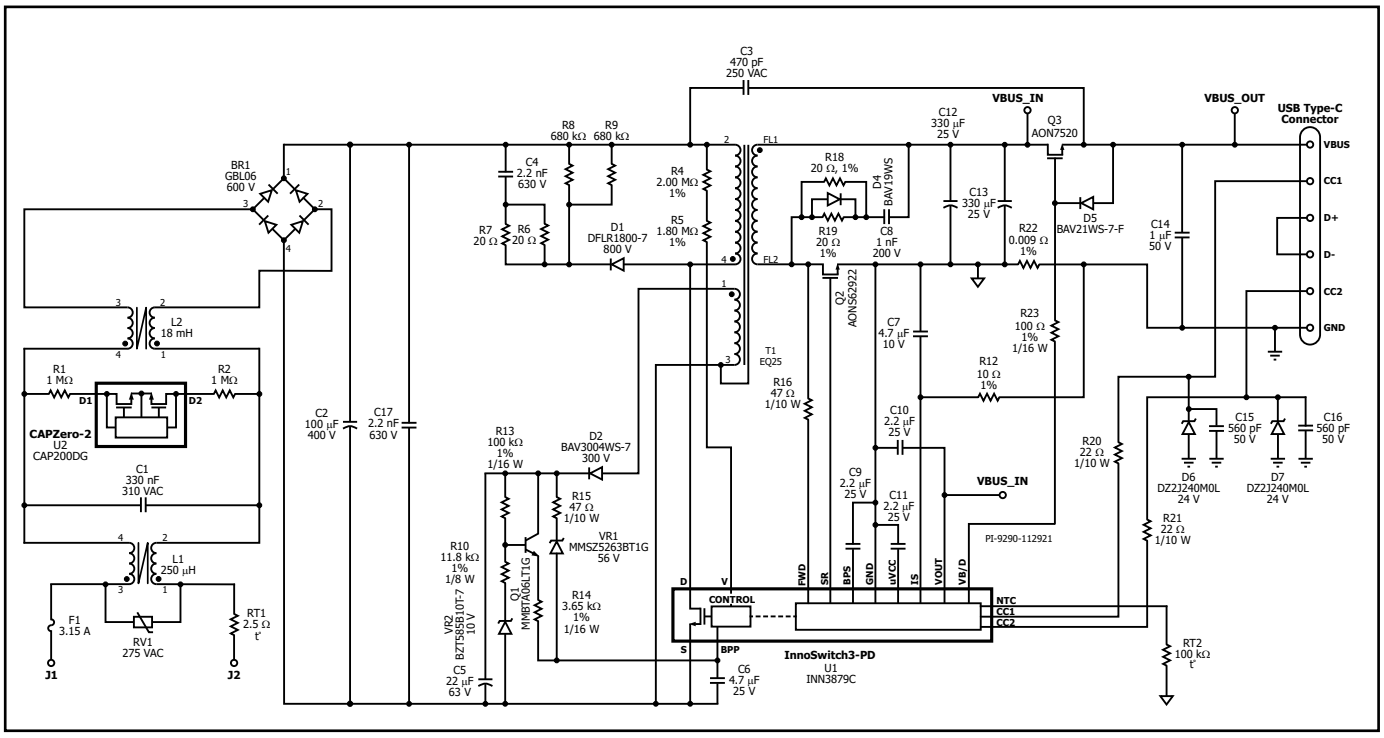


Figure 15. 60 W 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A; 3.3 V – 21 V PPS USB PD 3.0 Compliant Adapter.

The circuit shown in Figure 15 is a 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 3 A; 3.3 V – 21 V PPS USB PD 3.0 compliant adapter using Power Integration's InnoSwitch3-PD integrated power supply controller IC. The power stage is controlled by a USB PD controller. This design features DOE Level 6 and EC CoC 5 compliance.

Common mode choke L1 and L2 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Fuse F1 isolates the circuit and provides protection from component failure.

One end of the transformer primary is connected to the rectified DC bus; the other end is connected to the drain terminal of the integrated FET in the InnoSwitch3-PD IC (U1).

A low-cost RCD clamp formed by diode D1, resistors R6, R7, R8 and R9 and capacitor C4 limits the peak Drain voltage of U1 at the instant of turn-off of the FET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch3-PD IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS BPP pin capacitor (C6) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistors R10, R13 and R14 along with Q1 and VR2 form a linear regulator circuit to limit the current being supplied to the PRIMARY BYPASS pin of the InnoSwitch3-PD IC (U1) irrespective of the output voltage. The Zener VR1 along with resistor R15 provides latching OVP in the event of an output overvoltage condition.

In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In the event of an overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1. This causes a current to flow into the PRIMARY BYPASS pin of InnoSwitch3-PD IC (U1). If the current flowing into the PRIMARY BYPASS pin increases above the ISD threshold, the InnoSwitch3-PD IC controller will latch-off and prevent any further increase in output voltage.

The secondary-side of the InnoSwitch3-PD IC provides output voltage and output current sensing along with drive to a MOSFET providing synchronous rectification. The secondary output of the transformer is rectified by MOSFET Q2 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI, is reduced via a RC snubber, R18, R19 and C8. The gate of Q2 is turned on by secondary-side controller inside U1, based on the winding voltage sensed via resistor R16 and fed into the FORWARD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side requesting the start of a new switching cycle from the primary. In discontinuous or continuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C9, connected to the SECONDARY BYPASS BPS pin of InnoSwitch3-PD IC U1 provides decoupling for the internal circuitry. Capacitor C10 is needed between the VOUT pin and the SECONDARY GROUND pin for enhanced ESD protection.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS decoupling capacitor C9 via resistor R16 and an internal regulator. This allows output current regulation to be maintained down to the minimum auto-restart threshold set by the I²C interface. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistor R11 between the IS and SECONDARY GROUND pins. A threshold of approximately 32 mV reduces losses. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current. Below the CC threshold, the device operates in constant voltage mode.

In this design, USB PD controller is integrated inside InnoSwitch3-PD IC U1. The sink requests output voltage and current using the PD communication protocol. The µVCC pin needs a decoupling capacitor C11.

USB PD communication occurs over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected. The communication sets the CV, CC, V_{KP}, OVA and UVA parameters, which correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-PD IC, respectively.

N-MOSFETS Q3 forms the bus switch and makes the USB Type-C receptacle cold socket when no device is attached to the charger as per the USB Type-C specification. Resistor R23 and diode D5 are needed for providing a voltage discharge path when the bus switch is opened. Capacitor C17 is needed at the output for ESD protection and ripple reduction. Capacitors C15, C16, resistors R20, R21, and Zener diodes D6, and D7 provide protection from ESD to pins CC1 and CC2.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage-doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device assumes efficiency >84% and increases to efficiency >89% for the largest device.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (V_{OR}) is set to maintain K_P = 0.8 at minimum input voltage conditions for universal line and K_P = 1 for high input line conditions.
5. Maximum conduction losses for adapter ratings is limited to 0.6 W and 0.8 W for open frame.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink is used to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*Below a value of 1, KP is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient KP limit of ≥0.25 is recommended. This prevents the initial current limit (IINT) from being exceeded at switch turn-on.

Primary-Side Overvoltage Protection

The primary-side output overvoltage protection provided by the InnoSwitch3-PD IC triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode and a resistor from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5x or 2x the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. The value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during any output overvoltage.

Reducing No-Load Consumption
The InnoSwitch3-PD IC can start in self-powered mode from the PRIMARY BYPASS pin capacitor charged through the internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-PD IC has become operational. Auxiliary or bias winding provided on the transformer is required for this purpose. The addition of a bias winding that provides bias supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption down to <30 mW for most designs. Resistor R14 shown in Figure 15 should be adjusted to achieve current into BPP that is just slightly over I_{S1} which is also the condition when no-load power is the lowest.

Secondary-Side Overvoltage Protection (Auto-Restart Mode)
The secondary-side output overvoltage protection provided by the InnoSwitch3-PD IC uses an internal auto-restart circuit that is triggered by a threshold current of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The direct output sensed OVP function, if desired, could be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between the 1.25 times output voltage and 4.4 V SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into SECONDARY BYPASS pin. The secondary-side OVP function is disabled during soft-start.

Under some conditions, the secondary OVP may take several switching cycles to initiate.

Component Selection

Components for InnoSwitch3 PD IC Primary-Side Circuit

BPP Capacitor
Capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-PD IC provides decoupling for the primary-side controller and also selects current limit. A 0.47 μF or 4.7 μF capacitor may be used as indicated in InnoSwitch3-PD IC data sheet. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for design of compact switching power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit
The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch3-PD IC primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin.
Turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest (or no-load) load condition. If the voltage is lower than this, the no-load input power will increase. Generally, in USB PD or rapid charge applications, the output voltage range is very wide. For example, a 45 W adapter would need to support 5 V, 9 V and 15 V whereas a 100 W adapter would have output voltages selectable from 5 V to 20 V. Such a wide output voltage variation results in a large change in bias winding output voltage as well. As shown in Figure 15, a linear regulator circuit is generally required to limit the current injected into the PRIMARY BYPASS pin of the InnoSwitch3-PD IC.

The bias current from the external circuit should be set to $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at 230 VAC input voltage, (V_{BPP} > 5 V).

A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to prevent the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 μF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and rated load with the lowest input AC supply voltage. It is recommended to ground the bias winding capacitor to the negative of the input bulk capacitor than the SOURCE pin.

Line UV and OV Protection
Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage to provide line under-voltage and overvoltage protection. For a typical universal input application, a resistor value of approximately 3.8 MΩ is recommended. Figure 16 shows circuit configurations that enable selectively either the line UV or the line OV feature, disabling the other.

The InnoSwitch3-PD IC features a primary sensed OV protection feature that can be used to latch-off/AR the power supply. Once the power supply is in latch-off/AR, it can be reset if the UNDER/OVER INPUT VOLTAGE pin current is reduced to zero. Once the power supply is latched off, even after input supply is turned off, it can take considerable amount of time to reset InnoSwitch3-PD IC controller as the energy stored in the DC bus will continue to provide bias supply to the controller. In case of latch-off, a fast AC reset can be achieved using the modified circuit configuration shown in Figure 17. The voltage across capacitor CS reduces rapidly after input supply is disconnected reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch3-PD IC and resetting the InnoSwitch3-PD IC controller.

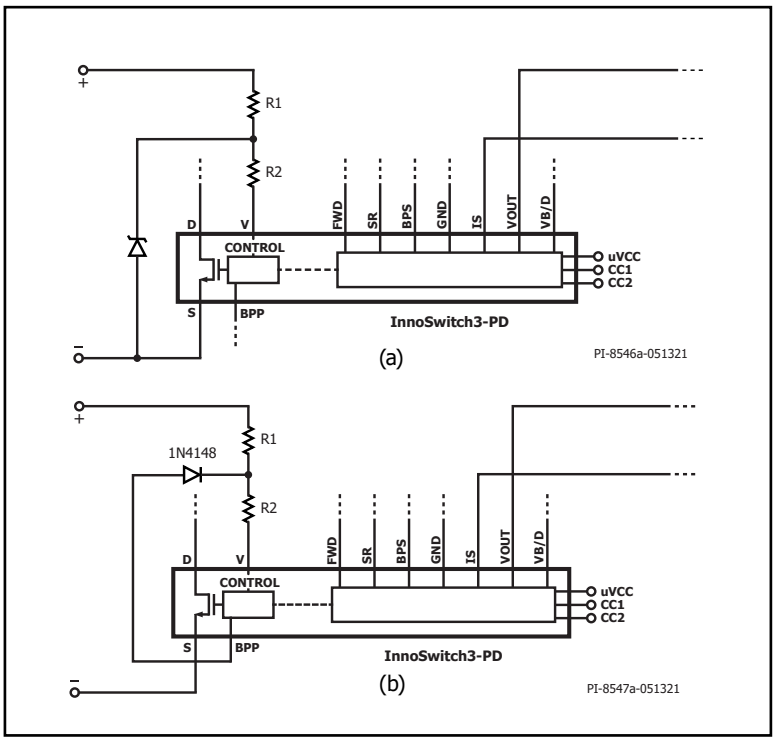


Figure 16. Figure 2. (a) Line UV Only; (b) Line OV Only.

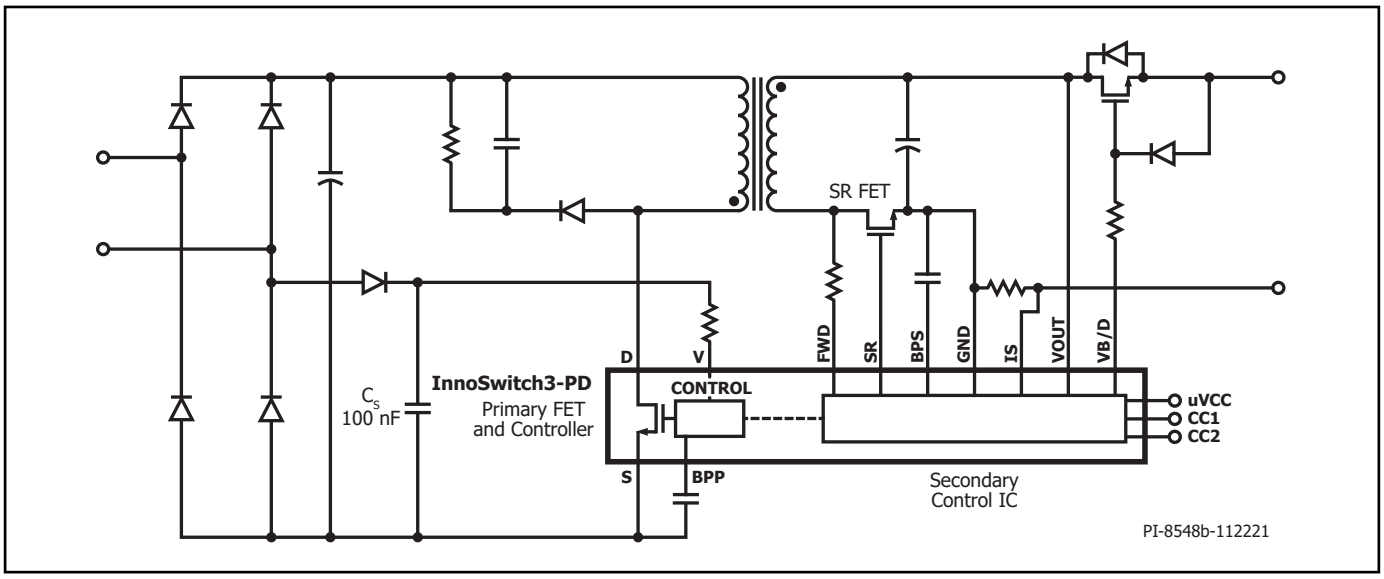


Figure 17. Fast AC Reset Configuration.

Primary Sensed OVP (Overvoltage Protection)
The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonable approximation of the state of the output voltage can be determined by the primary-side controller using the bias winding voltage. A Zener diode connected between the bias winding output and the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to latch-off/AR. It is recommended that the highest voltage at the output of the bias winding be measured for normal (steady-state) conditions at full rated load and lowest rated input voltage and also under transient load conditions. A Zener diode rated, for 1.25 times this measured voltage will ensure that OVP protection will not trigger under any normal operating conditions but will operate in case of a fault condition.

Primary-Side Snubber Clamp
A snubber circuit should be used on the primary-side as shown in the example circuit in Figure 15. This prevents excess voltage spikes at the Drain of the switch at the instant of turn-off of the switch during each switching cycle. Though conventional RCD clamps can be used, RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 15 uses RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

Components for InnoSwitch3-PD

Secondary-Side Circuit

SECONDARY BYPASS Pin – Decoupling Capacitor
A 2.2 µF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-PD IC. Since the SECONDARY BYPASS pin voltage needs to be 4.4 V before the output voltage reaches to the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. The values lower than 1.5 µF may not offer enough capacitance, which can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

When the output voltage of the power supply is 5 V or higher, the supply current for the secondary-side controller is supplied by the OUTPUT VOLTAGE (VOUT) pin of the IC as the voltage at this pin is higher than the SECONDARY BYPASS pin voltage. During start-up and operating conditions where the output voltage of the power supply is below 5 V, the secondary-side controller is supplied current from an internal current source connected to the FORWARD pin. If the output voltage of the power supply is below 5 V and the load at the output of the power supply is very light, the operating frequency can drop considerably and the current supplied to the secondary-side controller from the FORWARD pin may not be sufficient to maintain the SECONDARY BYPASS pin voltage at 4.4 V. For such applications, InnoSwitch3-PD IC has an internal charge pump to regulate the voltage of the SECONDARY BYPASS pin at 4.4 V.

FORWARD Pin Resistor
A 47 Ω 5% resistor is recommended to ensure sufficient IC supply current. A lower resistor value should not be used as it can affect device operation such as the synchronous rectifier drive timing. In some cases a higher value should be used if pulse grouping is observed. However this number should not exceed 150 Ω.

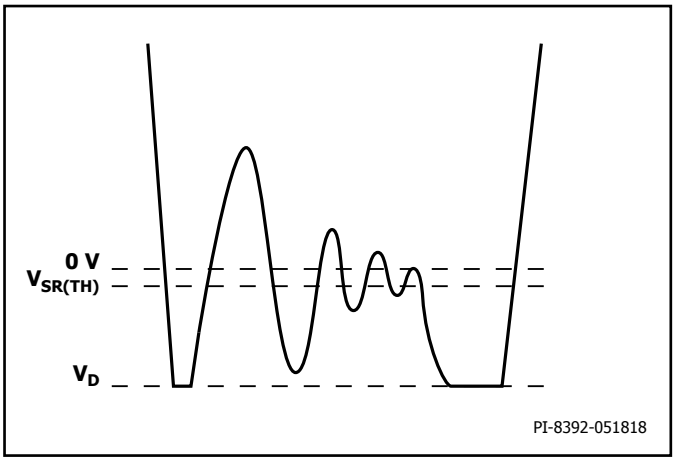


Figure 18. Unacceptable FORWARD Pin Waveform After Handshake With SR FET Conduction During Flyback Cycle.

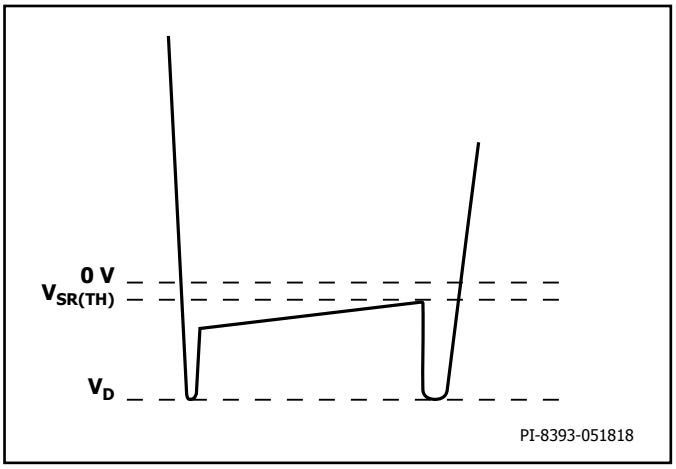


Figure 19. Acceptable FORWARD Pin Waveform After Handshake With SR FET Conduction During Flyback Cycle.

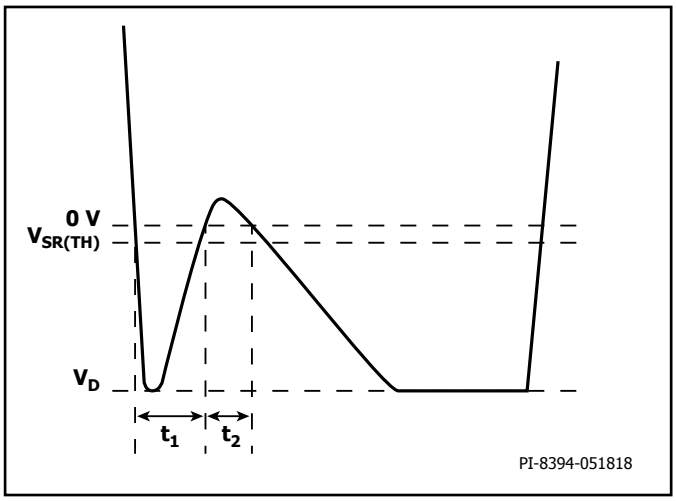


Figure 20. Unacceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

Note:
If $t_1 + t_2 = 1.5\ \mu s \pm 50$ ns, the controller may fail to handshake correctly and trigger a primary bias winding OVP latch-off/AR.

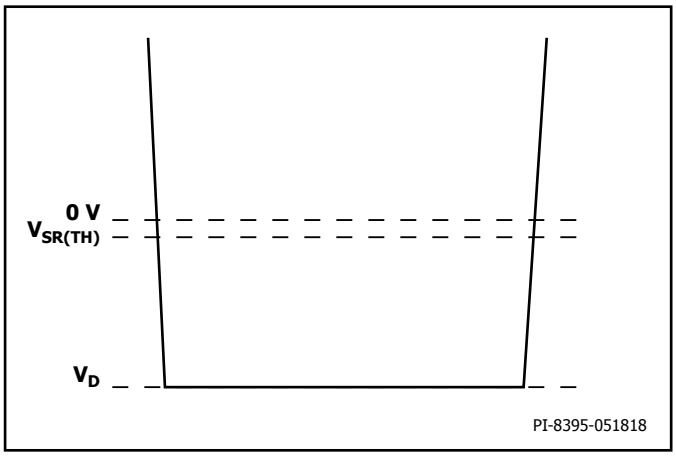


Figure 21. Acceptable FORWARD Pin Waveform Before Handshake With Body Diode Conduction During Flyback Cycle.

SR FET Operation and Selection

Although a simple diode rectifier and filter works for the output, use of a SR FET enables significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-PD IC (with no additional resistors connected to the gate circuit of the SR FET if a single SR FET is used). The SR FET is turned off once the Drain voltage of the SR FET drops below 0 V.

A FET with 18 mΩ $R_{DS(ON)}$ is good for 5 V, 2 A output, and a FET with 8 mΩ $R_{DS(ON)}$ is suitable for designs rated for 12 V, 3 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with too high a threshold voltage is therefore not suitable, and FETs with a low threshold voltage of 1.5 V to 2.5 V are ideal although FETs with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets clearly specify $R_{DS(ON)}$ over-temperature range for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-PD IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ drops below $V_{SR(TH)}$, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. A Schottky diode parallel to the SR FET may be added to provide higher efficiency. However, the gains are modest; for a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.3 to 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a V_{OR} <60 V, and 100 V rated FETs and diodes are suitable for most of the USB PD designs with output voltage >9 V.

The interaction between the leakage reactance of the secondary and the SR FET capacitance (COSS) leads to ringing on SR FET drain voltage waveform at the instance of voltage reversal at the winding due to the primary switch turn-on. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor in the range of 10 Ω to 47 Ω may be used (a higher resistance value leads to noticeable drop in efficiency). A capacitance of 1 nF to 2.2 nF is adequate for most designs. In designs where the SR FET drain waveform is not as shown in Figure 19 during voltage transitions, and looks similar to Figure 18 it is recommended that voltage transitions be made in small increments of 200 mV.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable design of ultra-compact chargers and adapters. Typically, 200 μF to 300 μF of aluminum-polymer capacitance per ampere of output current is generally adequate. The other factor that influences choice of the capacitance is the output ripple. Care should be taken to ensure that capacitors have a voltage rating higher than the highest output voltage with sufficient margin (>20%).

Output Overload Protection

The maximum power which can be delivered by the power supply is obtained by the product of the programmed V_{KP} and the full scale current limit. For output voltage below the programmed V_{KP} threshold, the InnoSwitch3-PD IC will limit the output current once the programmed current limit is reached (if it is less than the full scale current limit) or voltage across the IS and GND pins exceeds the $I_{SV(TH)}$ threshold and provides current limited or constant current operation. The full scale current limit is set by the resistor between the IS and GND pins. A lower value of current limit can be programmed over I²C. For any output voltage above the programmed V_{KP} threshold, InnoSwitch3-PD IC will provide a constant power characteristic. An increase in load current within the programmed current limit will result in a drop in output voltage such that the product of output voltage and current equals the maximum power set by the product of V_{KP} and set current limit.

Decoupling Capacitor at μVCC Pin

It is recommended that at least a 2.2 μF ceramic capacitor rated for 10 V or higher be placed between the uVCC and GND pins.

Decoupling Capacitor at V_O Pin

It is recommended that a 1-2.2 μF ceramic capacitor be placed close to the V_O pin. This capacitor should have a voltage rating higher than the highest output voltage with suitable margin (>20%).

Decoupling Capacitor at NTC Pin
It is recommended that at least a 560 pF ceramic capacitor be placed between the NTC and GND pins. A 10 V or higher rating capacitor should be used. The NTC pin should be connected to GND pin if a cost conscious customer does not intend to use the NTC.

CC1 and CC2 Pin Resistors, Capacitors, and Zener Diodes
These pins are connected to the USB Type-C connector for communication. There are resistors (R20 and R21, 22 Ω recommended) between these pins and the USB Type-C connector, and capacitors (C15, C16, 560pF X5R or X7R with 10 V or higher rating recommended) from these pins to output GND, which together form low pass RC filters that improve ESD susceptibility. There are also Zener diodes (D6 and D7, 24 V recommended) from CC1 and CC2 pins to output GND for improved ESD susceptibility.

IS to GND Pin Capacitor
It is recommended that 2.2 μF to 4.7 μF ceramic capacitor rated for 10 V or higher to be used between the IS and GND pins of the InnoSwitch3-PD IC for accurate constant current regulation. A 10 Ω resistor R12 is also recommended as shown in Figure 15 to provide a RC filter for current sense.

IS to GND Pin Current Sense Resistor
This sense resistor is chosen such that the required full scale current produces a 32 mV drop across IS and GND pins. A 1% or lower tolerance resistor is recommended. This resistor needs to be placed as close to the InnoSwitch3-PD IC pins as possible for accurate current measurement and CC regulation. This resistor is typically < 10 mohm for 3 A or higher output currents. As such the copper trace resistance can contribute to additional effective resistance. Careful attention should be paid to connections from InnoSwitch3-PD IC to this resistor to minimize effects of copper trace resistance.

Output Decoupling Capacitor
A ceramic output decoupling capacitor up to 10 μF is required to pass 18 kV ESD air discharge. This capacitor should have a voltage rating higher than the highest output voltage with sufficient margin (>20%).

Bus Switch
A low $R_{DS(ON)}$ N-channel FET bus switch is recommended to reduce impact of efficiency at high load currents. The FET need not be a logic level FET. It should be sufficiently enhanced at a gate threshold of 4 V.

Bus Discharge
The resistor value for bus discharge is chosen as per the discharge time requirements for high-voltage to low-voltage transitions. The resistor value should be sized not to exceed the current rating of VB/D pin specified in the electrical parameters table. A general purpose diode is recommended for unidirectional current flow.

Two different bus discharge circuits have been used in some of the reference designs and other documents. In one circuit, the bus discharge resistor is connected between the gate of the BUS switch and the VB/D pin. In another implementation, this resistor is connected in series with the diode across the BUS switch gate and source. For all new designs, the circuit configuration shown in this data sheet and also the design example in Figure 15 is recommended.

Recommendations for Circuit Board Layout

See Figure 22 for a recommended circuit board layout for a switching power supply using InnoSwitch3-PD IC.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize loop-distance from the clamp components to the transformer and IC.

Thermal Considerations
The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area should be maximized for good heat sinking. Similarly for output SR FET, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR FET.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage under highest rated operating temperature. Further de-rating can be applied depending on any additional specific requirements.

Y Capacitor
The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. Such a placement will route high amplitude common mode surge currents away from the IC. Note – if an input π (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR FET
For best performance, the area of the loop connecting the secondary winding, the output SR FET and the output filter capacitor, should be minimized. The Source pin connection of the SR FET should be connected to the output capacitor negative terminal and the GND pin of the InnoSwitch3-PD IC in a short connection to reduce the trace impedance drop as this is critical for FWD pin sensing wrt IC GND pin in order to turn OFF the SR FET during Discontinuous mode of operation. The connection between the Drain of the SR FET and the FWD pin resistor should also be made short and preferably use a separate trace to directly connect to SR FET Drain pin. In addition, sufficient copper area should be provided at the terminals of the SR FET for heat sinking.

IS-GND Pin, Sense Resistor Traces
It is recommended to have the traces from the current sense resistor to the IS-GND pins to be in a star connection at the respective two nodes of the current sense resistor in order to have an accurate CC set-point. The IS-GND sense traces should be at the innermost of the solder pads of the current sense resistor to avoid measuring any drop across the solder pads of the resistor or the load traces coming in and out of the sense resistor.

uVCC, CC1 and CC2 Pins
The traces to uVCC, CC1 and CC2 pins should be kept away from any noisy node or trace. If possible a shield trace should be made in parallel to the uVCC, CC1 and CC2 traces.

V_O Pin, Output Voltage Sense Traces
It is recommended to have the output voltage sense traces directly from the V_O pin to the output capacitor positive terminal, to avoid the influence of the voltage drop on power trace.

ESD
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / hi-pot requirements.

The spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration a 6.4 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the InnoSwitch3-PD IC primary to secondary spacing. To further improve ESD perfo mance, spark gaps can be added under common mode chokes.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected to the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and associated circuit trace lengths should be minimized.

The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example

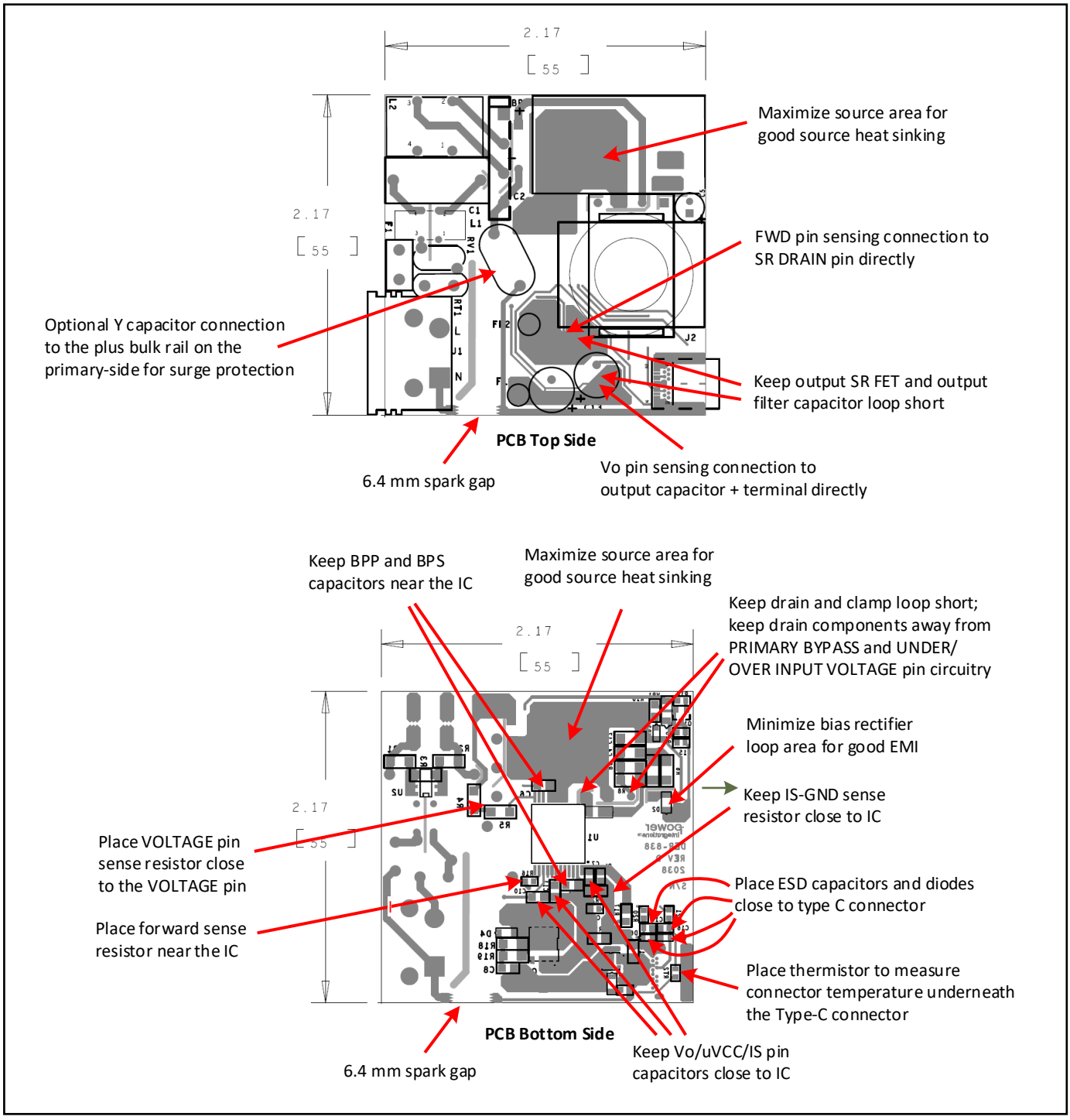


Figure 22. PCB Layout Recommendation.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area and keeping the switching nodes/traces away from the quiet nodes/traces.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduced radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. The same can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to achieve improved conducted and radiated EMI margins.
5. The RC snubber connected across the output SR FET can help reduce high frequency radiated and conducted EMI.
6. A π filter comprising of differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 μF or higher ceramic capacitor when connected at the output of the power supply helps to reduce radiated EMI.

Recommendations for Transformer Design

Transformer design must ensure that the power supply is able to deliver the rated power at the lowest input voltage. The lowest voltage on the rectified DC bus of the power supply depends on the capacitance of the filter capacitor used. At least 2 μF / W is recommended to keep the DC bus voltage always above 70 V, though 3 μF / W provides sufficient margin. The ripple on the DC bus should be measured and care should be taken to verify this voltage to confirm the design calculations for transformer primary-winding inductance selection.

Switching Frequency (F_{SW})

It is a unique feature in InnoSwitch3-PD ICs that a designer can set the switching frequency at full load between 25 kHz to 95 kHz depending on the design specification. To have lower device temperature, the switching frequency can be set to around 60 kHz. To have smaller size transformer, the switching frequency needs to be set to a value closer to a maximum of 95 kHz. When setting the full load switching frequency, it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection. The following table provides a guide for frequency selection based on the device size. This represents the best compromise between the overall device losses (conduction and switching losses) based on size of the internal high-voltage switch and transformer size.

INN3865C / INN3875C	80 kHz
INN3866C / INN3876C	75 kHz
INN3877C	70 kHz
INN3896C	70 kHz
INN3867C / INN3868C	65 kHz
PowiGaN device INN3878C	70 kHz
PowiGaN device INN3879C	65 kHz
PowiGaN device INN3870C	60 kHz

Reflected Output Voltage, V_{OR} (V)

This parameter describes the effect on the primary switch Drain voltage of the secondary-winding voltage during the diode / SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of QR capability and ensure flattest efficiency over line / load, it is better to set reflected output voltage (V_{OR}) to maintain K_P = 0.8 at minimum input voltage conditions for universal line input and K_P = 1 for high-line input only conditions.

The following should be kept in mind for design optimization:

1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-PD device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.
3. Higher V_{OR} increases leakage inductance that reduces efficiency of the power supply.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents where the V_{OR} should be reduced to get highest efficiency, and higher output voltages above 15 V, V_{OR} should be higher to maintain a reasonable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, K_P

A K_P below 1, indicates continuous conduction mode, K_P is the ratio of ripple-current to peak-primary-current (Figure 23).

$$K_P \equiv K_{RP} = I_R / I_P$$

A value of K_P higher than 1, indicates discontinuous conduction mode. In this case, K_P is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T / t = V_{OR} \times (1 - D_{MAX}) / (V_{MIN} - V_{DS}) \times D_{MAX}$$

It is recommended that a K_P close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-PD designs.

A K_P value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-PD IC temperature. The benefits of quasi-resonant switching start to diminish for a further reduction in K_P.

For typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. PIXls spreadsheet from Power Integrations can be used to effectively optimize selection of K_P, inductance of the primary winding, turns ratio of the transformer and the operating frequency while ensuring appropriate design margins.

Core Type

Choice of suitable core is dependent on the physical design constraints of the power supply enclosure. It is recommended that only cores with low loss be used as power supply designs are often thermally challenged due to the small enclosure requirement.

Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary but are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For universal input designs, a total margin of 6.2 mm is typically required, and a value of 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical.

However if a total margin of 6.2 mm is required then the physical margin can be placed only on one side of the bobbin. For designs using triple insulated wire it may still be necessary to use a small margin in order to meet the required safety creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required. As the margin reduces the available area for the windings, margin construction may not be suitable for small core sizes. It is recommended that for compact power supply designs using an InnoSwitch3-PD IC, triple insulated wire should be used for secondary which then eliminates need for large margins.

Primary Layers, L

Primary layers should be in the range of 1 < L < 3 and in general it should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs though higher values may be required based on thermal design constraints. Designs with more than 3 layers are possible but the increased leakage inductance and physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

Maximum Operating Flux Density, B_M (Gauss)

A maximum value of 3800 gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density under start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-PD IC provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

Transformer Primary Inductance, (LP)

Once the lowest operating input voltage, switching frequency at full load, and the required V_{OR} are determined, transformer primary inductance can be calculated. The PIXls design spreadsheet which is part of the free PI Expert™ suite can be used to assist in designing the transformer.

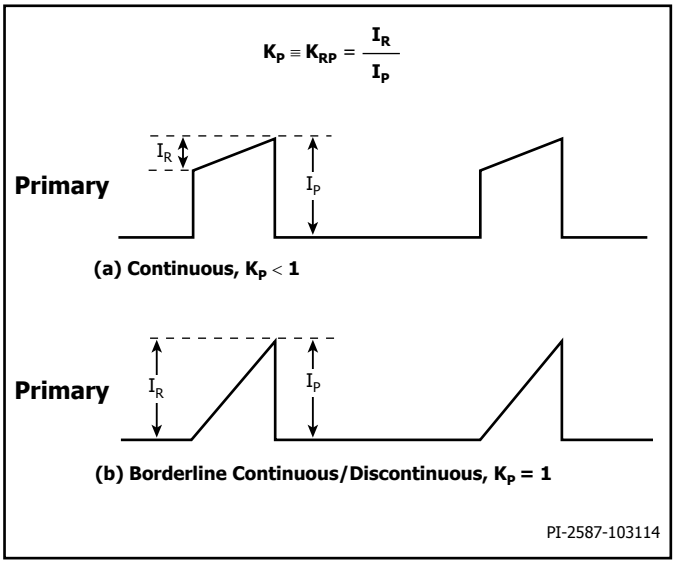


Figure 23. Continuous Mode Current Waveform, KP ≤ 1.

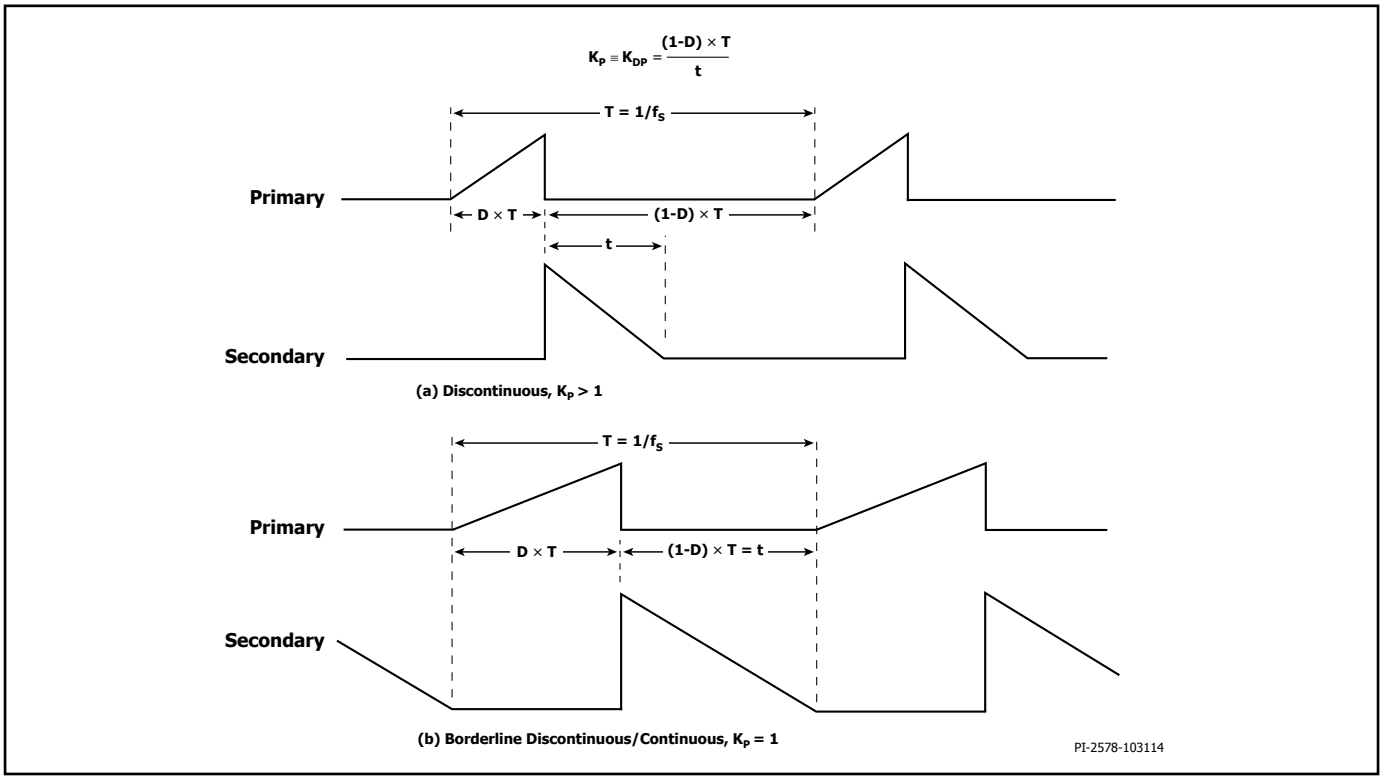


Figure 24. Discontinuous Mode Current Waveform, KP ≥ 1.

Transformer Construction for Mitigation of Audible Noise

Although InnoSwitch3-PD features audible noise reduction engine which prevents operation in the predominant audible range, application of the thixotropic epoxy glue in the transformer air gap is recommended. This helps to damp any audible noise when the power supply operates at light load which results in the low frequency operation.

Design Considerations When Using PowiGaN Devices (INN3878C, INN3879C and INN3870C)

For a flyback converter configuration, typical voltage waveform at the drain pin of the IC is shown in Figure 25.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding.

In addition to V_{BUS} + V_{OR}, the drain also sees a large voltage spike at turn off that is caused by the energy stored in the leakage inductance of the primary winding. To keep the drain voltage from exceeding the rated maximum continuous drain voltage, a clamp circuit is needed across the primary winding. The forward recovery of the clamp diode will add a spike at the instant of turn-OFF of the primary switch. V_{CLM} in Figure 25 is the combined clamp voltage including the spike. The peak drain voltage of the primary switch is the total of V_{BUS}, V_{OR} and V_{CLM}.

V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long term reliability and design margin.

V_{OR} choice will affect the operating efficiency and should be selected carefully. Table below shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for VOR
5 V	45 - 70
12 V	80 - 120
15 V	100 - 135
20 V	120 - 150
24 V	135 - 180

Table 3. Optimal Range of VOR for different Output Voltage.

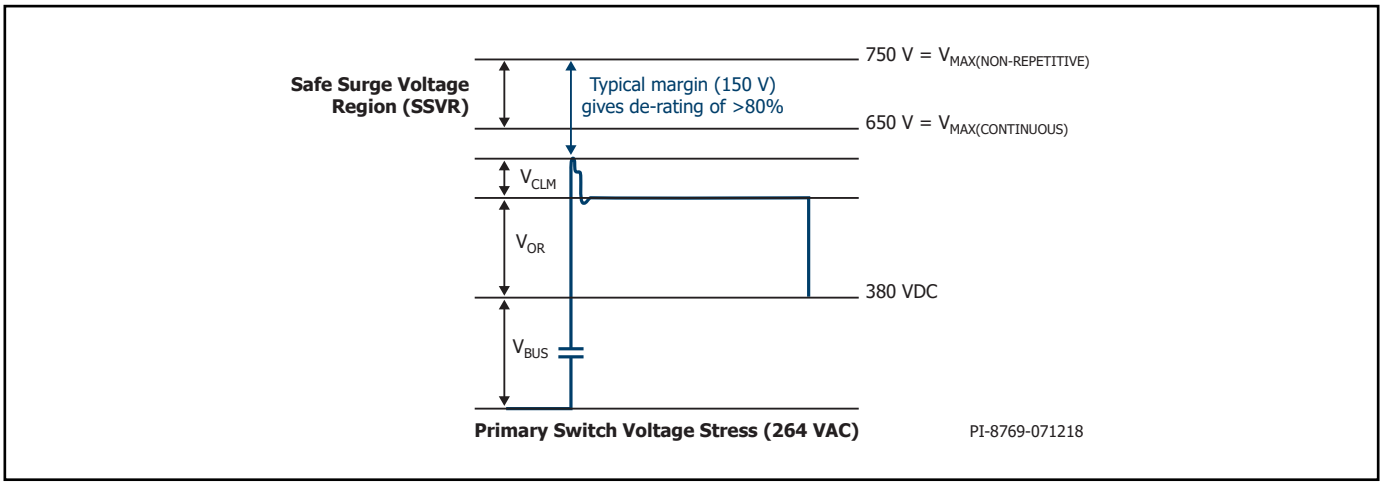


Figure 25. Peak Drain Voltage for 264 VAC Input Voltage.

Quick Design Checklist

As with any power supply design, all InnoSwitch3-PD designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch3-PD and SR FET do not exceed 90% of breakdown voltages at highest input voltage and peak (overload) output power in normal operating and start-up conditions.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady-state conditions and verify that the leading edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.

Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specification limits are not exceeded for InnoSwitch3-PD IC, transformer, output SR FET, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of InnoSwitch3-PD IC as specified in the data sheet.

Under low-line, maximum power, a maximum InnoSwitch3-PD IC SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Thermal Resistance Test Conditions for PowiGaN Devices (INN3878C, INN3879C and INN3870C)

Thermal resistance value is for primary power device junction to ambient only.

Testing performed on custom thermal test PCB as shown in Figure 26. The test board consists of 2 layers of 2 oz. Cu with the InSOP package mounted to the top surface and connected to a bottom layer Cu heat sinking area of 550 mm^2.

Connection between the two layers was made by 82 vias in a 5 x 17 matrix outside the package mounting area. Vias are spaced at 40 mils, with 12 mil diameter and plated through holes are not filled.

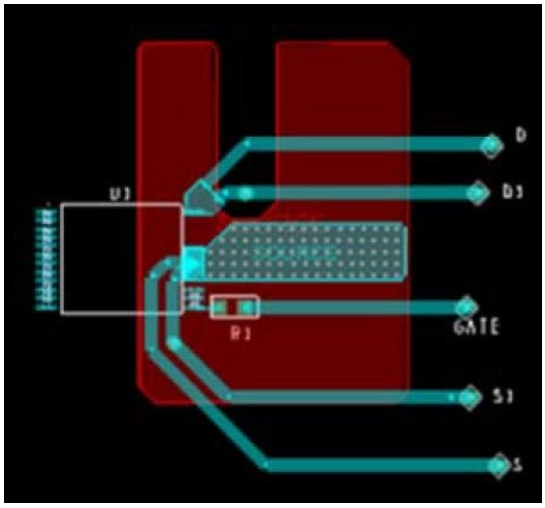


Figure 26. Thermal Resistance Test Conditions for PowiGaN Devices (INN3878C, INN3879C and INN3870C).

Firmware Configuration

Name	Function	PDO	APDO	Bus Switch Disabled State (Default)
OVA	Overvoltage Threshold	$1.1 \times V_{OUTMAX}$ [1]	$1.1 \times V_{OUTMAX}$ [1]	6.2 V
UVA	Undervoltage Threshold	3.1 V	3.1 V	3.6 V
CVO	Constant Voltage Only	Enabled	Disabled	Disabled
OVL	Overvoltage Fault Response	AR	AR	AR
UVL	Undervoltage Fault Response	AR	AR	AR
CVOL	Constant Voltage Mode Fault Response	AR	Not Applicable	NR
UVL Timer	UVL Fault Timer	8 ms	8 ms	64 ms
CVOL Timer	CVOL Fault Timer	8 ms	Not Applicable	8 ms
CDC	Cable Drop Compensation	300 mV	0 mV	0 mV
VKP	Constant Output Power Knee Voltage	24 V	24 V	24 V
CCSC	Output Short-Circuit Fault Detection	AR	AR	AR
ISSC	IS Pin Short Fault Response and Detection Frequency	NR 50 kHz	NR 50 kHz	NR 50 kHz
OTP	Secondary Over-Temperature Fault Hysteresis	40 °C	40 °C	40 °C
VCONN OCP	VCONN Over-Current Protection	Enabled	Enabled	Disabled
VCONN OCP Threshold	VCONN Over-Current Protection Threshold	40 mA	40 mA	40 mA
Type-C OTP	Connector Over-Temperature Fault Protection	Disabled	Disabled	Disabled

NOTES:
1. $V_{OUT(MAX)} = MAX \{V_{OUT(MAX)APDO}, V_{OUT(MAX)PDO}\}$

Table 4. Firmware Configuration Table (Subject to change based on Firmware).

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: INN3865C–INN3868C .. .. -0.3 V to 650 V
INN3875C–INN3877C ..... -0.3 V to 725 V
INN3896C ..... -0.3 V to 900 V
DRAIN Pin Voltage[5]: INN3878C–INN3870C..... -0.3 V to 750 V
DRAIN Pin Peak Current: INN3865C..... 3.87 A[7]
INN3875C..... 4.11 A[7]
INN3866C..... 4.88 A[7]
INN3876C..... 5.19 A[7]
INN3867C..... 5.57 A[7]
INN3896C..... 5.72 A[7]
INN3877C..... 5.92 A[7]
INN3868C..... 6.24 A[7]
PowiGaN device INN3878C ..... 6.5 A[7]
PowiGaN device INN3879C ..... 10 A[7]
PowiGaN device INN3870C ..... 14 A[7]
BPP/BPS Pin Voltage..... -0.3 to 6 V
BPP/BPS Pin Current ..... 100 mA
CC1, CC2 Pin Voltage ..... -0.3 to 28 V
NTC Pin Voltage..... -0.3 to 6 V
uVCC Pin Voltage ..... -0.3 V to 5.5 V
FWD Pin Voltage ..... -1.5 V to 150 V
SR Pin Voltage ..... -0.3 V to 6 V
V Pin Voltage ..... -0.3 V to 650 V
VOUT Pin Voltage ..... -0.3 V to 27 V
VB/D Pin Voltage ..... -0.3 V to 35 V
IS Pin Voltage ..... -0.3 V to 0.3 V[6]
Storage Temperature ..... -55 to 150 °C
Operating Junction Temperature[3]..... -40 to 150 °C
Ambient Temperature..... -40 to 105 °C
Lead Temperature[4]..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. PowiGaN devices:
   Maximum drain voltage (non-repetitive pulse) ..... -0.3 V to 750 V
   Maximum continuous drain voltage..... -0.3 V to 650 V
6. Absolute maximum voltage for less than 500 μs is 3 V.
7. Please refer to Figures 27, 33, 41 and 42 for maximum allowable voltage and current combinations.

Thermal Resistance

Thermal Resistance:
INN38x5C to INN38x7C
(θ_{JA})..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC})..... 8 °C/W[3]
PowiGaN devices INN3878C / 3879C / 3870C
(θ_{JA})..... 50 °C/W[4]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.
4. Please see Figure 26.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C		23	25		kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C f_{SW} = 100 kHz		0.7	1.15		kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C			14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}					$t_{OFF(MIN)}$	µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C	INN38x5C – INN38x7C	145	200	425	µA
			INN3878C – INN3870C	145	266	425	
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 132 kHz) T_J = 25 °C	INN3865C		0.65	1.03	mA
			INN3866C		0.86	1.21	
			INN3867C		1.03	1.38	
			INN3868C		1.20	1.75	
			INN3875C		0.79	1.10	
			INN3876C		1.02	1.38	
			INN3877C		1.20	1.73	
			INN3896C		0.90	1.35	
			INN3878C		1.24	1.79	
			INN3879C INN3870C		1.95	2.81	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35		mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65		
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.65	4.90	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.39		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.15	3.50	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C	INN38x5C – INN38x7C	23.6	25.8	28.0	µA
			INN3878C – INN3870C	22.9	24.9	27.2	
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C	INN38x5C – INN38x7C	20.0	22.0	24.5	µA
			INN3878C – INN3870C	19.0	21.7	23.6	
Brown-Out Delay Time	t_{UV-}				35		ms

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C	INN38x5C – INN38x7C	106	115	118	µA
			INN3878C – INN3870C	106	112	118	
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			8		µA
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C	INN38x5C – INN38x7C	100	106		µA
			INN3878C – INN3870C	98	104		
Line Fault Protection							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C			3		µs
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		650			V
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF See Note D	I_{LIMIT}	di/dt = 213 mA/µs T_J = 25 °C	INN38x5C	883	950	1017	mA
		di/dt = 238 mA/µs T_J = 25 °C	INN38x6C	1162	1250	1338	
		di/dt = 300 mA/µs T_J = 25 °C	INN3877C	1255	1350	1445	
			INN3867C	1348	1450	1552	
		di/dt = 375 mA/µs T_J = 25 °C	INN3868C	1534	1650	1766	
			INN3878C	1581	1700	1819	
		di/dt = 425 mA/µs T_J = 25 °C	INN3879C	1767	1900	2033	
		di/dt = 525 mA/µs T_J = 25 °C	INN3870C	2139	2300	2461	
Increased Current Limit (BPP) Capacitor = 4.7 µF See Note D	$I_{LIMIT+1}$	di/dt = 213 mA/µs T_J = 25 °C	INN38x5C	1040	1143	1246	mA
		di/dt = 238 mA/µs T_J = 25 °C	INN38x6C	1297	1425	1553	
		di/dt = 300 mA/µs T_J = 25 °C	INN3877C	1410	1550	1689	
			INN3867C	1494	1642	1790	
		di/dt = 375 mA/µs T_J = 25 °C	INN3868C	1683	1850	2017	
			INN3878C	1714	1884	2054	
		di/dt = 425 mA/µs T_J = 25 °C	INN3879C	1919	2109	2299	
		di/dt = 525 mA/µs T_J = 25 °C	INN3870C	2325	2555	2785	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		102	110		kHz

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
BYPASS Pin Fault Shutdown Threshold Current	I_{SD}	T_J = 25 °C		5.8	7.4		mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C		75	82	89	ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C			2	2.11	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C See Note A			0.20		sec
Output							
ON-State Resistance	$R_{DS(ON)}$	INN3865C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	Ω
			T_J = 100 °C		3.02	3.47	
		INN3875C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		INN3866C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.30	1.50	
			T_J = 100 °C		2.02	2.32	
		INN3876C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.34	1.54	
			T_J = 100 °C		2.08	2.39	
		INN3867C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.02	1.17	
			T_J = 100 °C		1.58	1.82	
		INN3877C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
		INN3868C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.91	1.05	
			T_J = 100 °C		1.33	1.53	
		INN3896C $I_D = I_{LIMIT+1}$	T_J = 25 °C		2.35	2.80	
			T_J = 100 °C		3.40	4.20	
		INN3878C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.52	0.68	
			T_J = 100 °C		0.78	1.02	
		INN3879C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.35	0.44	
			T_J = 100 °C		0.49	0.62	
		INN3870C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	118	132		kHz
Minimum Off-Time	$t_{OFF(MIN)}$	T_J = 25 °C	2.7	3.6	4.6	µs
BPS Pin Latch Command Shutdown Threshold Current	$I_{BPS(SD)}$		5.2	8.9		mA
Start-Up VOUT Pin Regulation Voltage	$VOUT_{REG}$	T_J = 25 °C	4.85	5	5.15	V
Output Voltage Programming Range	$V_{OUT(R)}$	Default = 5 V	3.00		24.00	V
	TOL_{VOUT}	Tolerance T_J = 25 °C	-3		+3	%
Output Voltage Step Size	ΔV_{OUT}	T_J = 25 °C		10		mV
Report-Back Output Voltage Tolerance	$V_{OUT(T)}$	T_J = 25 °C	-3		3	%
Normalized Output Current Tolerance	I_{OUT}	0.6 - 1.0 T_J = 25 °C, See Note C	-5		5	%
		0.2 T_J = 25 °C, See Note C	-15		15	
Normalized Output Current Step Size	ΔI_{OUT}	T_J = 25 °C		0.78		%
Internal Current Limit Voltage Threshold	$I_{SV(TH)}$	T_J = 25 °C Across External IS to GND Pin Resistor See Note E		32		mV
CDC Tolerance	$TOL\phi_{CD}$	100 mV ≤ CDC ≤ 400 mV T_J = 25 °C	-35		+35	mV
Output Overvoltage Programming Range	V_{OVA}	Default = 6.2 V	6.2		25	V
Output Overvoltage Tolerance	TOL_{OVA}	T_J = 25 °C	-3		3	%
Output Undervoltage Programming Range	V_{UVA}	Default = 3.6 V	3		24	V
Output Undervoltage Tolerance	TOL_{UVA}	T_J = 25 °C	-3		3	%
VB/D Drive Voltage	$V_{VB/D}$	With Respect to VOUT Pin	4		10	V
VB/D Turn-On Time	$t_{R(VB/D)}$	T_J = 25 °C C_{LOAD} = 10 nF		4	10	ms
VB/D Turn-Off Time	$t_{F(VB/D)}$	T_J = 25 °C C_{LOAD} = 10 nF		4	10	ms
VB/D Pin Load Discharge Internal On-State Resistance	$R_{B/D(ON)}$	See Note H		32		Ω

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary (cont.)						
VB/D Pin Load Discharge Internal Off-State Resistance	$R_{B/D(OFF)}$		80			kΩ
VOUT Pin Bleeder Current	IVO_{BLD}	V_{OUT} = 5 V T_J = 0 – 125 °C		270		mA
uVCC Supply Voltage	uVCC	V_{OUT} = 5 V	3.42	3.60	3.78	V
uVCC Reset Voltage Threshold	$uVCC_{RST}$	See Note B		2.8	3.0	V
BPS Pin Voltage	V_{BPS}		4.2	4.4		V
BPS Pin Current	I_{SNL}	T_J = 25 °C VBUS Switch Open		0.7	0.9	mA
		T_J = 25 °C VBUS Switch Closed		1.03	1.3	
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)TH}$		3.6	3.8	4.0	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)TH}$			0.65		V
Soft Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C		11.8		ms
FORWARD Pin Breakdown Voltage	BV_{FWD}		150			V
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}		4.2	4.4		V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-5.0	0	mV
Rise Time	$t_{R(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 10-90%		50		ns
Fall Time	$t_{F(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 90-10%		30		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} + 0.1 V I_{SR} = 30 mA		10	13	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} + 0.2 V I_{SR} = 30 mA		5.0	5.8	Ω

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
PD Controller - Type C Configuration Channels CC1 and CC2						
Source 0.5 A Current Advertisement	$I_{RP(0P5A)}$		64	80	96	µA
Source 1.5 A Current Advertisement	$I_{RP(1P5A)}$		166	180	194	µA
Source 3.0 A Current Advertisement	$I_{RP(3P0A)}$		304	330	356	µA
BMC Receiver						
RX Input Detection Threshold	V_{RXTH}	See Note F	550			mV
Receiver Input Impedance	R_{BMCRX}			1.3		MΩ
VCONN Switch						
Over Current Detection Threshold	$I_{VCONN\_OCP\_CURRENT}$	See Note G		40		mA
Total Resistance (V_{CONN} Switch + Protection Switch)	$R_{VCONN(CC)}$	V_{CONN} = V_{CC}, Current = 10 mA		6.5		Ω
NTC and Internal Temperature Sense						
NTC Pin Current Source	$I_{SOURCE(NTC)}$			45		µA
ADC Accuracy On NTC	TOL_{ADC}	T_J = 25 °C			2	%
Input Voltage Range	V_{ADC_IN}		0.25		2.20	V

NOTES:

A. This parameter is derived from characterization.

B. This parameter is guaranteed by design.

C. Use 1% tolerance resistor.

D. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

E. This parameter should be used only for calculation of typical value of current sense resistor. Firmware programs the register to regulate output current. The tolerance is specified in the Normalized Output Current parameter (I_{OUT}).

F. This parameter is indirectly tested.

G. Only at 5 V output, VCONN can supply up to 40 mA current for 0.5 seconds.

H. The current into VB/D pin during the discharge should be limited to <50 mA.

Typical Performance Curves

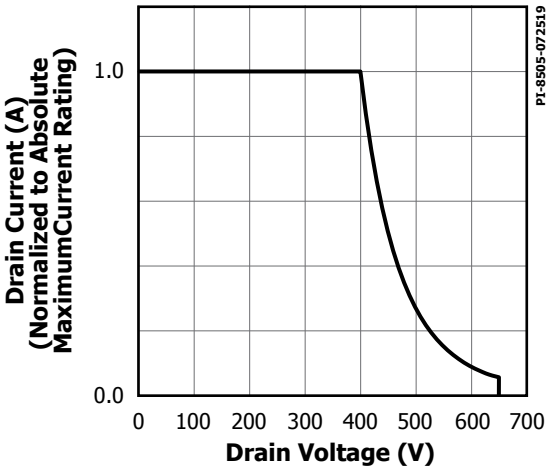


Figure 27. Maximum Allowable Drain Current vs. Drain Voltage (INN386x).

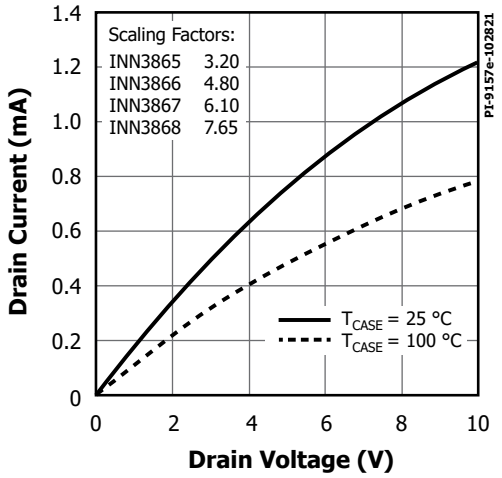


Figure 28. Output Characteristics.

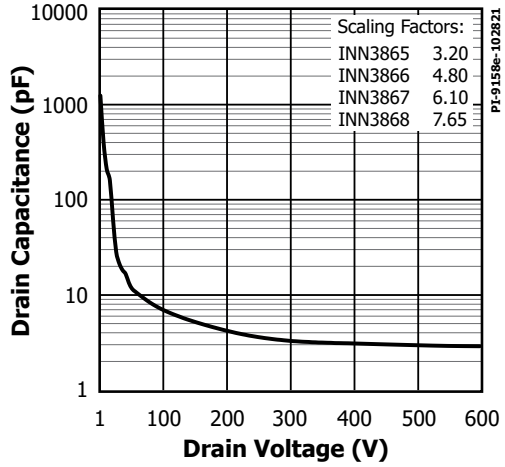


Figure 29. C_{OSS} vs. Drain Voltage.

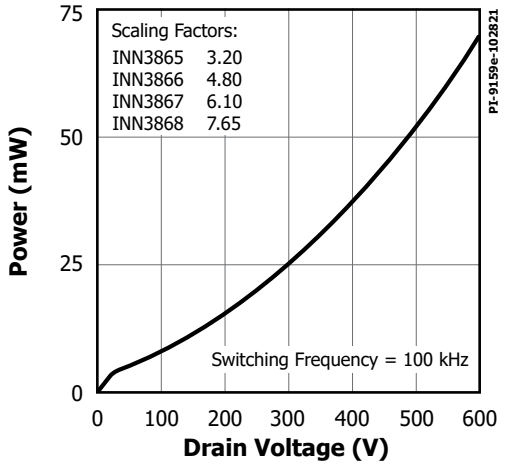


Figure 30. Drain Capacitance Power.

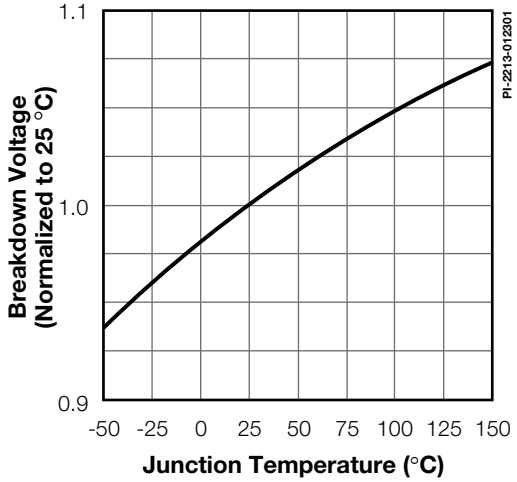


Figure 31. Breakdown vs. Temperature (Exclude INN3878C / INN3879C / INN3870C).

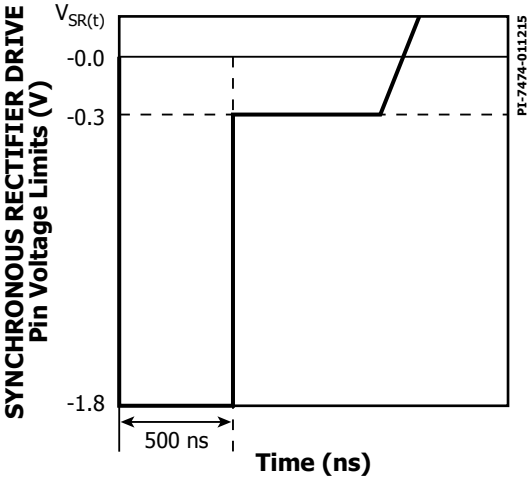


Figure 32. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

Typical Performance Curves (cont.)

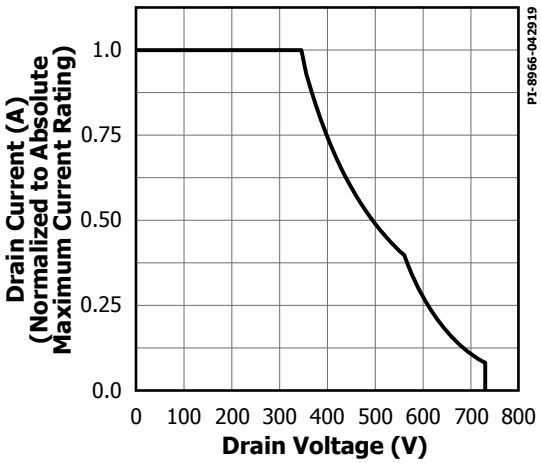


Figure 33. Maximum Allowable Drain Current vs. Drain Voltage (INN3875C / INN3876C / INN3877C).

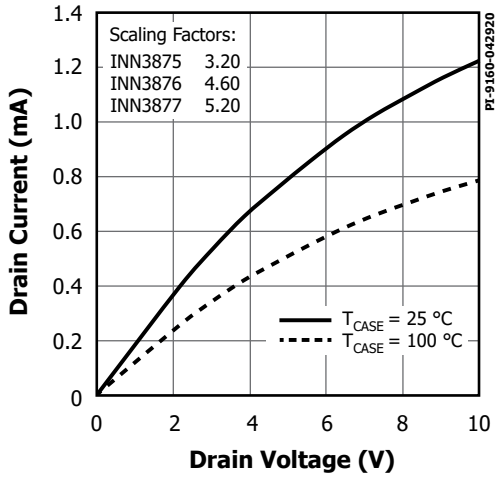


Figure 34. Output Characteristics.

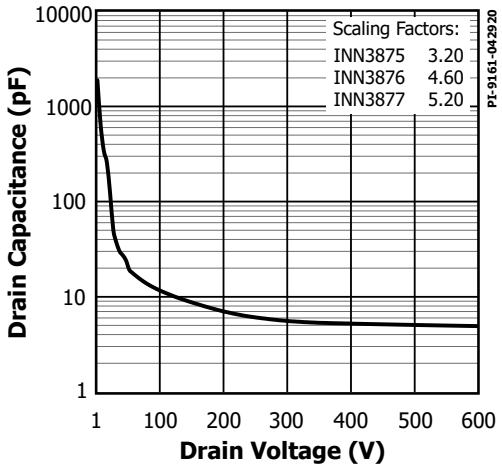


Figure 35. C_{OSS} vs. Drain Voltage.

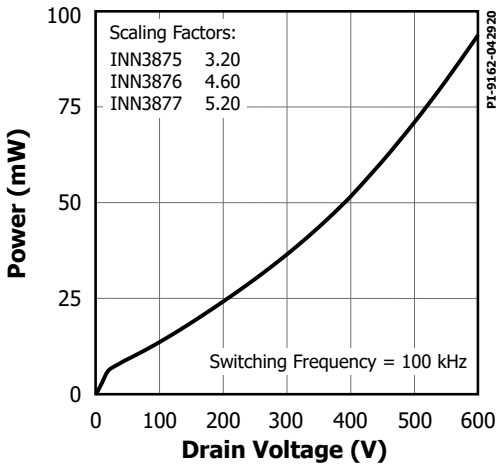


Figure 36. Drain Capacitance Power.

Typical Performance Curves (cont.)

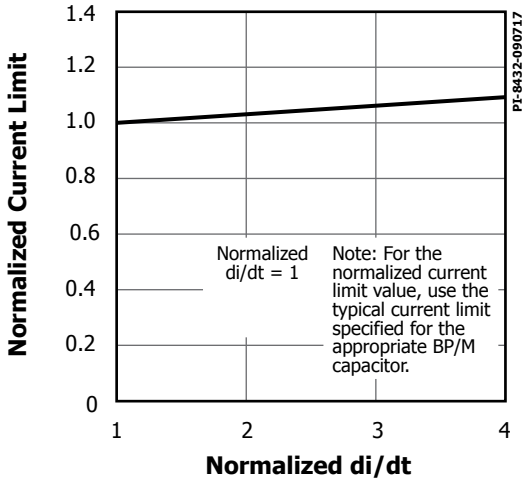


Figure 37. Standard Current Limit vs. di/dt.

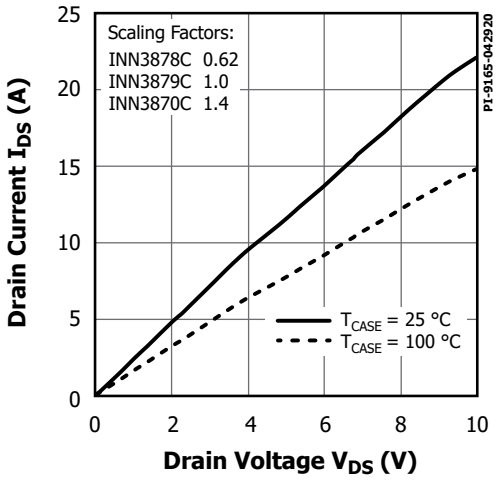


Figure 38. Output Characteristics.

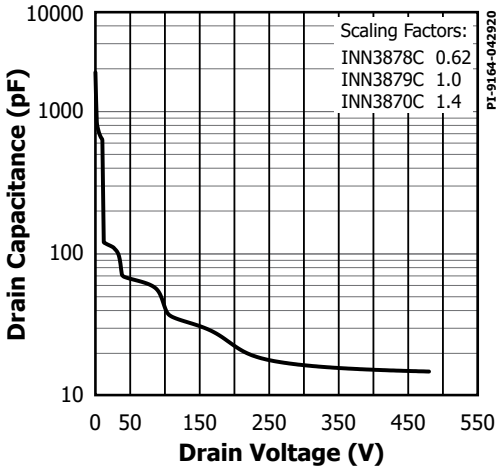


Figure 39. C_{OSS} vs. Drain Voltage.

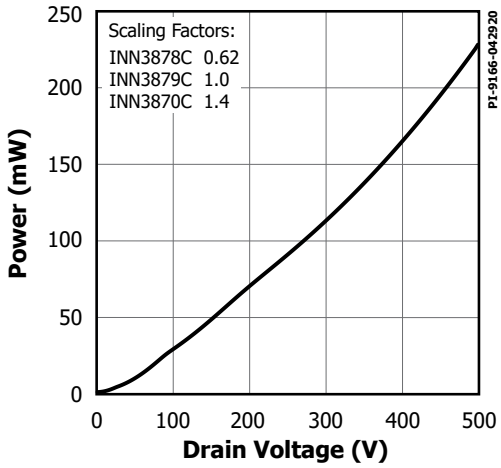


Figure 40. Drain Capacitance Power.

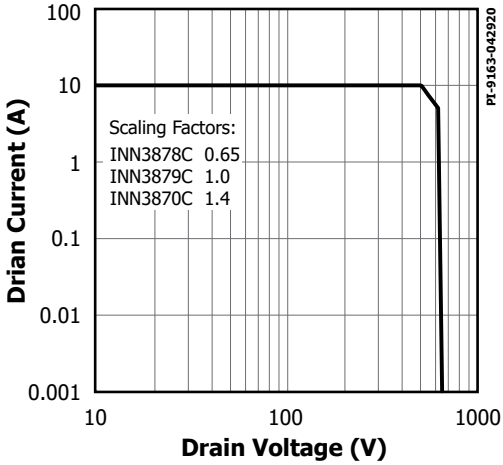


Figure 41. Maximum Allowable Drain Current vs. Drain Voltage (PowiGaN Devices INN3878-INN3870).

Typical Performance Curves (cont.)

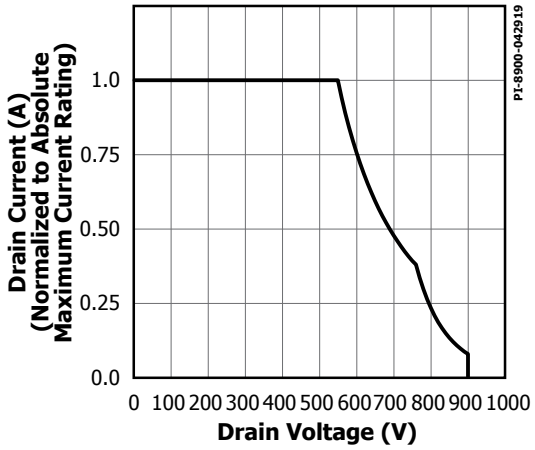


Figure 42. Maximum Allowable Drain Current vs. Drain Voltage (INN389x).

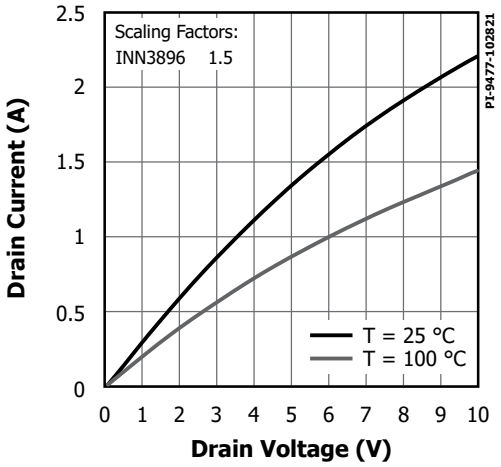


Figure 43. Output Characteristics.

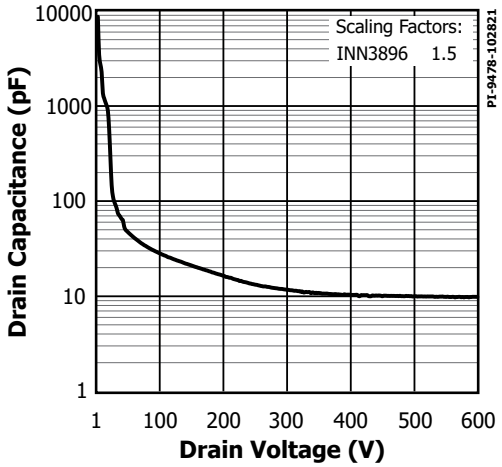


Figure 44. C_{OSS} vs. Drain Voltage.

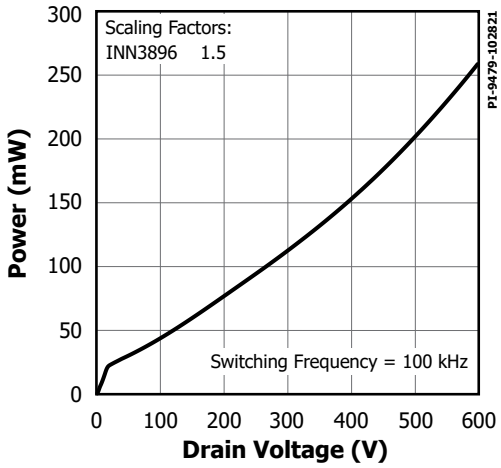
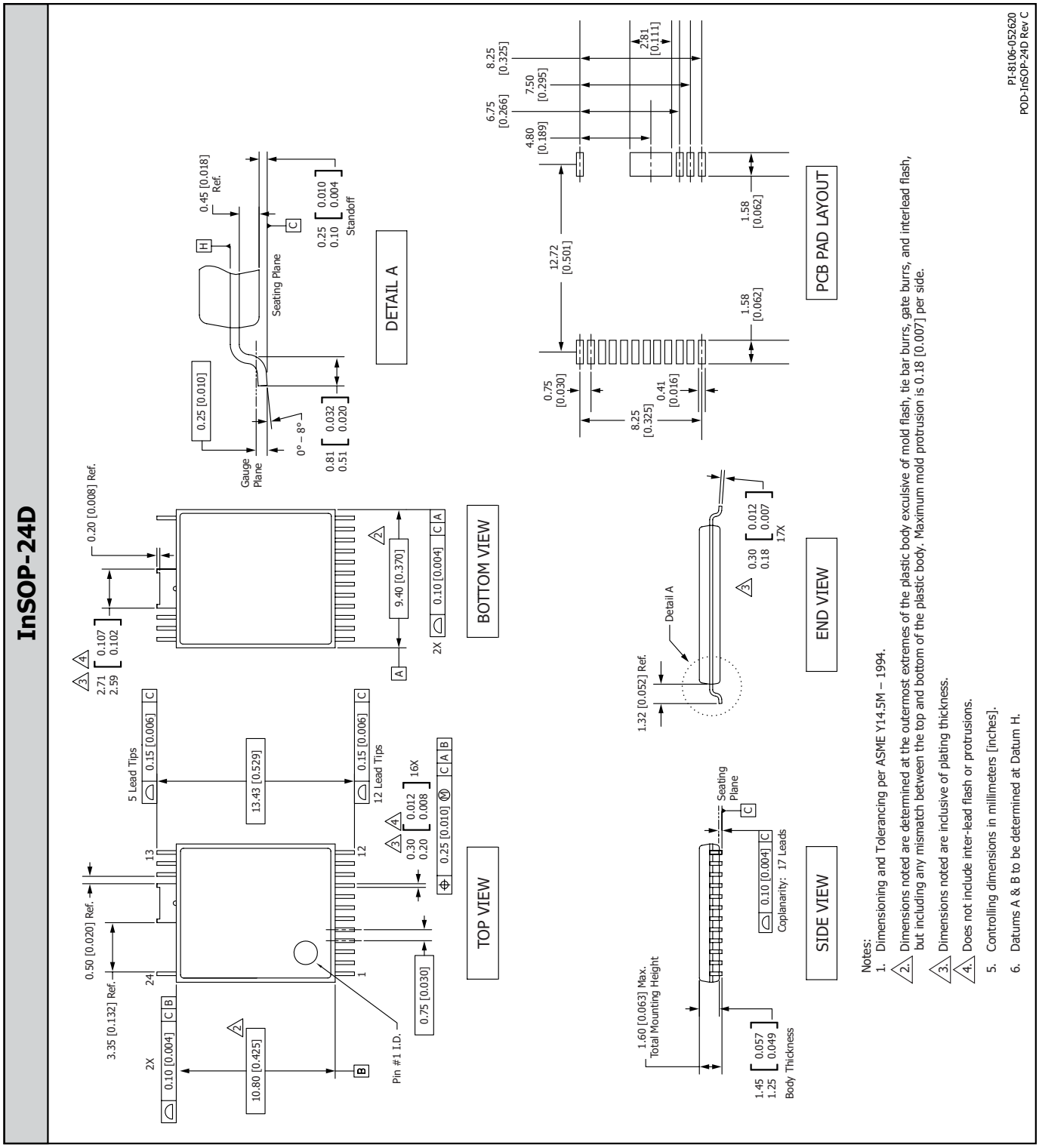
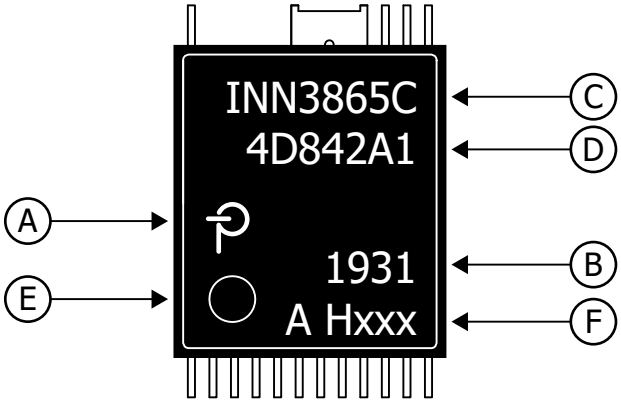


Figure 45. Drain Capacitance Power.


InSOP-24D
TOP VIEW
BOTTOM VIEW
SIDE VIEW
END VIEW
DETAIL A
PCB PAD LAYOUT
Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.
PI-8106-052620
POD-InSOP-24D Rev C

PACKAGE MARKING

InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Test Lot Information and Feature Code

PI-9156-051721

Safety Certification Specifications

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5*	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W
Package Characteristics			
Clearance		11.4	mm (min)
Creepage		11.4	mm (min)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		>600	V

*For INN3878C rating is 1.0 A.

Parameter	Symbol	Conditions		Rating	Units
Package Characteristics					
Clearance	CLR			11.4	mm (min)
Creepage	CPG			11.4	mm (min)
Distance Through Insulation	DTI			0.4	mm
Comparative Tracking Index	CTI			>600	V
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, T_J = 25 °C (See Note 1)		10^{12}	Ω (min)
		V_{IO} = 500 V, 100 °C ≤ T_J ≤ 125 °C (See Note 1)		10^{11}	
Isolation Capacitance, Input to Output	C_{IO}	(See Note 1)		1	pF
Package Insulation Characteristics (See Note 2)					
Maximum RMS Working Isolation Voltage	$V_{IORM(RMS)}$	INN386xC		512	V_{RMS} (max)
		INN387xC		530	
		INN389xC		636	
Maximum Repetitive Peak Isolation Voltage	$V_{IORM(PK)}$	INN386xC		650	V_{PK} (max)
		INN387xC		725	
		INN389xC		900	
Maximum Transient Peak Isolation Voltage	V_{IOTM}	Test Voltage = V_{IOTM}, t = 60 s (Qualification)		6.6	kV_{PK} (max)
		t = 1 s (100% Production)		8	
Maximum Surge Isolation Voltage	V_{IOSM}	Surge Test 1.2/50 usec Table 2 IEC 60747-17		10.4	kV_{PK} (max)
Input to Output Test Peak Voltage	V_{PD}	Method A, After Environmental Tests Subgroup 1, V_{PD} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial Discharge < 5 pC	INN386xC	1040	V_{PEAK}(min)
			INN387xC	1160	
			INN389xC	1440	
		Method A, After Input / Output Safety Test Subgroup 2/3, V_{PD} = 1.2 × V_{IORM}, t = 10 s, (qualification) Partial Discharge < 5 pC	INN386xC	780	
			INN387xC	870	
			INN389xC	1080	
		Method B1, 100% Production Test, V_{PD} = 1.875 × V_{IORM}, t = 1 s Partial Discharge < 5 pC	INN386xC	1220	
			INN387xC	1360	
			INN389xC	1688	
Insulation Resistance	R_S	V_{IO} = 500 V at T_S		>10^9	Ω
Climatic Category				40/125/21	

Parameter	Conditions	Specifications
IEC 60664-1 Rating Table		
Basic Isolation Group	Material Group	I
Insulation Classification	Rated Mains RMS voltage ≤ 150 V	I - IV
	Rated Mains RMS voltage ≤ 300 V	I - IV
	Rated Mains RMS voltage ≤ 600V	I - IV
	Rated Mains RMS voltage ≤ 1000 V	I - III

Note 1: All pins on each side of the barrier tied together creating a two-terminal device
Note 2: VDE 0884-11 only applies to devices with following H-codes: -H608, -H609, -H610, -H611 and –H612
Note 3: VDE 0884-11 certification is pending for INN369x devices.

Feature Code Table

Summary Features	H801
I_{LIM} Selectable	Yes
Over-Temperature Protection	Hysteretic
Line OV/UV	Enabled
Line UV Timer (35 ms or 400 ms)	35 ms
Primary Bypass Output Overvoltage Protection	Latch-Off

Part Ordering Table – Standard Offering

Part Number	Feature Code	P_{OUT} (W)	PDOs & APDOs						
INN3865C/ INN3875C	H801	20	5 V / 3 A	9 V / 2.22 A	12 V / 1.67 A	3.3-5.9 V / 3 A	3.3-11 V / 2.2 A		
INN3866C/ INN3876C	H801	30	5 V / 3 A	9 V / 3 A	12 V / 2.5 A	15 V / 2 A	20 V / 1.5 A	3.3-11 V / 3 A	3.3-16 V / 2 A
INN3867C/ INN3877C	H801	33	5 V / 3 A	9 V / 3 A	12 V / 2.75 A	15 V / 2.2 A	20 V / 1.65 A	3.3-11 V / 3 A	3.3-16 V / 2.05 A
INN3878C/ INN3868C	H801	45	5 V / 3 A	9 V / 3 A	12 V / 3 A	15 V / 3 A	20 V / 2.25 A	3.3-16 V / 3 A	3.3-21 V / 2.25 A
INN3879C	H801	60	5 V / 3 A	9 V / 3 A	15 V / 3 A	20 V / 3 A	3.3-21 V / 3 A		
INN3870C	H801	65	5 V / 3 A	9 V / 3 A	12 V / 3 A	15 V / 3 A	20 V / 3.25 A	3.3-21 V / 3 A	

Parts listed above meet standard USB Type-C and PD3.0 requirements.
Please contact Power Integrations Factory or local Sales Office for availability of additional part numbers.

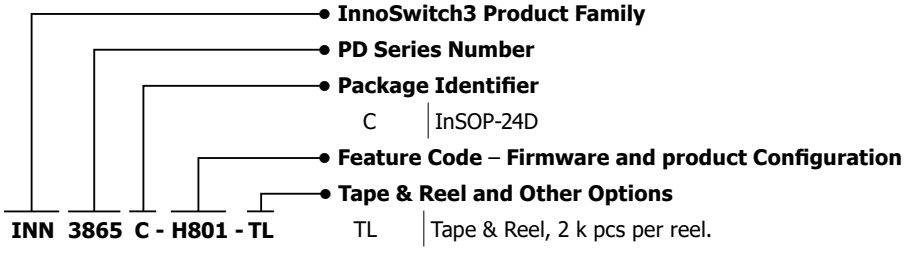
MSL Table

Part Number	MSL Rating
INN38xxC	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±1 kV on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±2 kV on all pins, except on VB/D pin > ±1 kV on VB/D pin

Part Ordering Information



Notes

Revision	Notes	Date
C	Code A release.	09/21
D	Added par numbers: INN3875/3876/3877/3868/3896.	12/21
E	Updated UL1577 isolation voltage on page 1. Updated Package and Insulation Characteristics Parameter Table and IEC 60664-1 Rating Table Notes 2 and 3.	11/22

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany (AC-DC/LED Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com