Enpirion EN5337QI 3A DCDC Converter w/Integrated Inductor Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

- The EN5337QI features integrated inductor, power MOSFETS, Controller, a bulk of the compensation Network, and protection circuitry against system faults. This level of integration delivers a substantial reduction in footprint and part count over competing solutions. However, the evaluation board is not optimized for minimum footprint; rather for engineering ease of evaluation through programming options, clip leads, test points etc.

- The EN5337QI features a customer programmable output voltage by means of a resistor divider. The resistor divider allows the user to set the output voltage to any value within the range 0.75V to (V_{IN}-$V_{DROPOUT}$). The evaluation board, as shipped is populated with a 4 resistor divider option. The upper resistor is fixed (150kΩ) and has a phase lead capacitor (27pF) in parallel. One of 4 lower resistors is selected with the jumper option for output voltages of 1.0V, 1.2V, 1.55V and 2.5V. To change any of the output voltages, retain the upper resistor and capacitor values and change only the lower resistor.

- This device has no over-voltage protection feature. We strongly recommend the customer to ensure the feedback loop is truly closed before powering up the device especially if the load can not withstand the input voltage.

- The input capacitor is a 10V rated 22uF X5R MLCC. The output filter section is populated with 1 x 47uF and 1 x10uF, 6.3V rated X5R MLC capacitors to achieve the required ~50uF of output capacitance. This combination of output caps yields very low ESR and hence low output ripple. A single 47uF capacitor may be substituted if minimizing footprint is important. The Soft-start capacitor is a small 10V rated 15nF X5R MLCC.

- Pads are available to add an additional input capacitor, and there are a total of 5 pads to accommodate the output capacitor(s). This allows for evaluation of performance over a wide range of input/output capacitor combinations.

- Clip on terminals are provided for ENA, SS, POK, VIN and VOUT. Other test points are also made available.

- A jumper is provided for controlling the Enable signal. Enable may also be controlled using an external switching source by removing the jumper and applying the enable signal to the middle pin and ground.

- A jumper is also provided to connect a resistor load to POK pin. This jumper is especially useful to measure the disable current and eliminates having to subtract the current drawn by the POK resistor.

- Foot print is also provided for a SMA connector to SYNC input. The SYNC input allows the device switching to be phase locked to an external clock signal. This external clock synchronization allows for moving any offending beat frequency to be moved out-of-band. A swept frequency applied to this pin results in spread spectrum operation and reduces the peaks in the noise spectrum of emitted EMI.

- Numerous test points are provided as well as banana plugs for input and output connections. Input / Output ripple are best measured directly across the appropriate capacitors. The switching waveform may be viewed between test points labeled SW and GND.

- The board comes with input decoupling and reverse polarity protection to guard the device against common setup mishaps.

Quick Start Guide

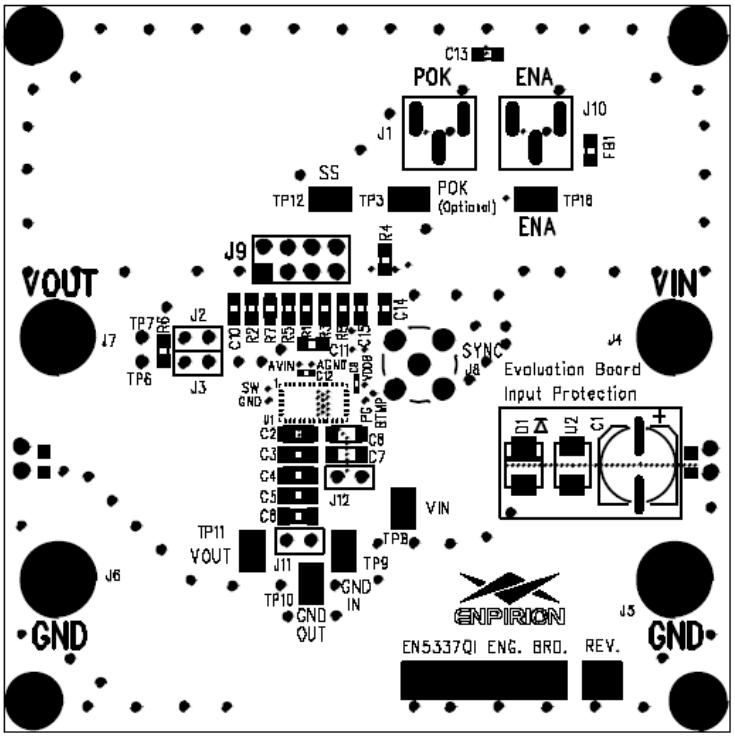


Figure 1 shows a top view evaluation board.

WARNING: complete steps 1 through 4 before applying power to the EN5337QI evaluation board.

STEP 1: Set the "ENABLE" jumper to the Disable Position.

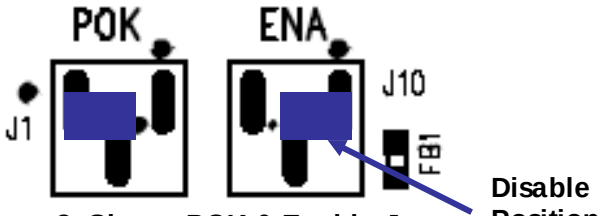


Figure 2: Shows POK & Enable Jumpers
(POK jumper as shown connects pull-up resistor to VIN.
Enable jumper shown in DISABLE position.)

STEP 2: Connect Power Supply to the input power connectors, VIN (+) and GND (-) as indicated in Figure 1 and set the supply to the desired voltage. The device disable current may be measured in this configuration.

CAUTION: be mindful of the polarity. Even though the evaluation board comes with reverse polarity protection diodes, it is rarely a good idea to reverse the input polarity.

STEP 3: Connect the load to the output connectors VOUT (+) and GND (-), as indicated in Figure 1.

STEP 4: Select the output voltage setting jumper. You may also set the POK jumper to include the POK load if POK signal monitoring is intended. The only time to disable POK is when measuring the absolute Disable current.

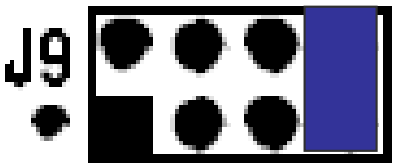


Figure 3: Output Voltage selection jumpers
Jumper shown selects 1.2V output
(Jumper positions from left are: 2.5V, 1.55V, 1.0V and 1.2V)

STEP 5: Apply V_{IN} to the board and move the ENABLE jumper to the enabled position. The EN5337QI is now powered up! Various measurements such as efficiency, line and load regulation, input / output ripple, load transient, drop-out voltage measurements may be made at this point. The over current trip level, short circuit protection, under voltage lock out thresholds, temperature coefficient of the output voltage may also be measured in this configuration.

STEP 5A: Power Up/Down Behavior – Remove ENA jumper and connect a pulse generator (output disabled) signal to the middle pin of ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec. and duty cycle to 50%. Hook up oscilloscope probes to ENA, SS, POK and VOUT with clean ground returns. Apply power to evaluation board. Enable pulse generator output. Observe the SS capacitor and VOUT voltage ramps as ENA goes high and again as ENA goes low. The device when powered down ramps down the output voltage in a controlled manner before fully shutting down. The output voltage level when POK is asserted /de-asserted as the device is powered up / down may be observed as well as the clean output voltage ramp and POK signals.

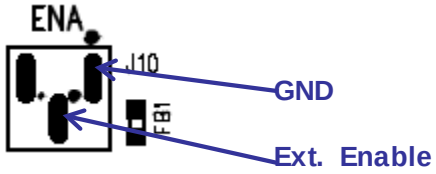


Figure 4: Means to Pulse Enable

STEP 6: External Clock Synchronization / Spread Spectrum Modes: In order to activate this mode, it may be necessary to a solder a SMA connector at J8.

Alternately the input clock signal leads may be directly soldered to the through holes of J8 as shown below.

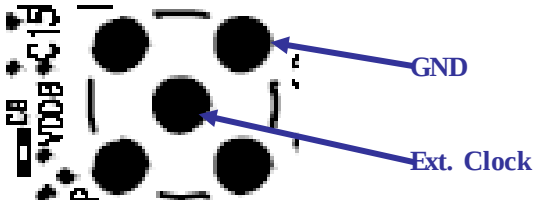


Figure 4: SMA Connector for External Clock Input

Power down the device. Move ENA into disable position. Connect the clock signal as just indicated. The clock signal should be clean and have a frequency in the range of 4.5 to 5.5MHz; amplitude 0 to 2.5 volts with a duty cycle between 20 and 80%.

With SYNC signal disabled, power up the device and move ENA jumper to Enabled position. The device is now powered up and outputting the desired voltage. The device is switching at its free running frequency. The switching waveform may be observed between test points SW and GND. Now enabling the SYNC signal will automatically phase lock the internal switching frequency to the externally applied frequency as long as the external clock parameters are within the specified range. To observe phase-lock connect oscilloscope probes to the input clock as well as to the SW test point. Phase lock range can be determined by sweeping the external clock frequency up / down until the device just goes out of lock at the two extremes of its range.

For spread spectrum operation the input clock frequency may be swept between two frequencies that are within the lock range. The sweep (jitter) repetition rate should be limited to 10kHz. The radiated EMI spectrum may be now measured in various states – free running, phase locked to a fixed frequency and spread spectrum.

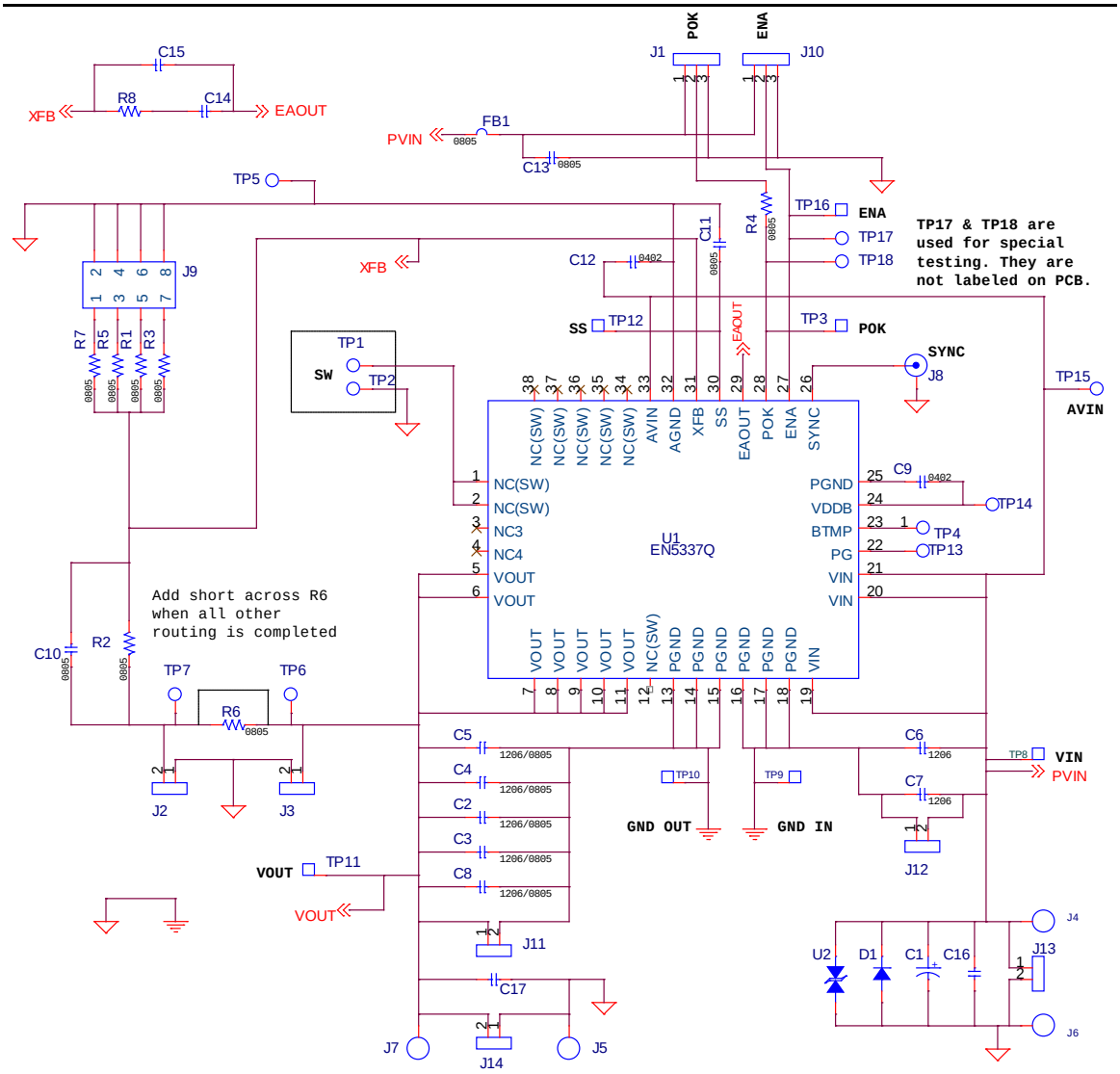


Figure 5: EN5337 Evaluation Board Schematic

Output Voltage Select

Programming the Output Voltage.

The EN5337QI output voltage is programmed using a simple resistor divider network. Figure 6 shows a schematic view of the resistor divider configuration.

The EN5337QI output voltage is determined by the voltage presented at the XFB pin. The voltage is set by way of a resistor divider between V_{OUT} and AGND with the midpoint going to XFB. A phase lead capacitor is also required across the upper resistor – the one between VOUT and XFB.

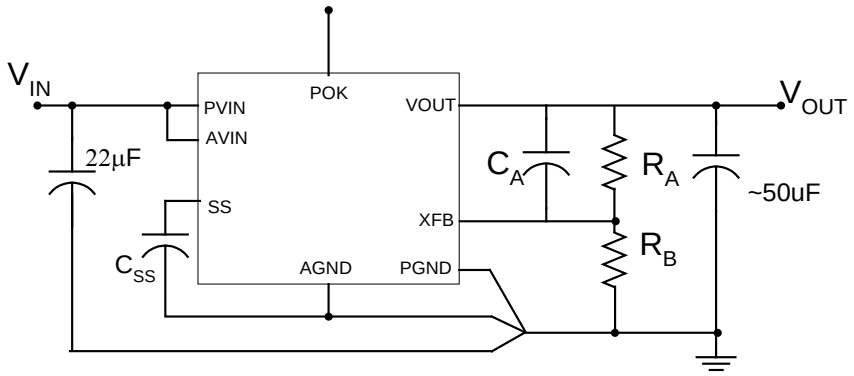


Figure 6: V_{OUT} resistor divider network and Phase lead Details.

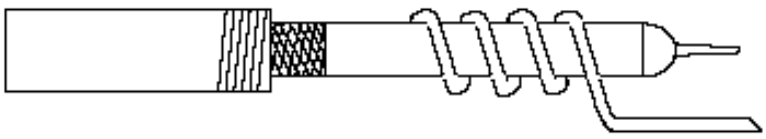
$$RA = 150k\Omega,\ CA = 27pF$$

$$RB = \frac{0.75V * RA}{(VOUT - 0.75V)}$$

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the test points provided. This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with series ammeters or accurate shunt resistors. This is especially important when measuring efficiency.
3. Use a balanced impedance probe tip shown below to measure switching signals and input / output ripple to avoid noise coupling into the probe ground lead. Input ripple, output ripple, and load transient deviation are best measured at the respective input / output capacitors.



4. The board includes a pull-up resistor for the POK signal and ready to monitor the power OK status. The POK signal may be viewed at clip lead marked POK.

5. A 15nF soft-start capacitor is populated on the board for ~1msec soft-start time.
6. The over-current protection circuit typically limits the maximum load current to approximately 1.5X the rated value – nominally 4.5A.

Input and Output Capacitors

The **input** capacitance requirement is between 10-20uF X5R/X7R for the EN5337QI. Altera recommends that a low ESR MLC capacitor be used. The voltage rating should be rated high enough to provide adequate margin for your application. There is a pre-tinned pad for one additional 1206 capacitor to experiment with input filter performance.

The **output** capacitance requirement is approximately 50uF of X5R/X7R capacitance. The EN5337QI-E evaluation board comes populated with 1 x 47uF 1206 and 1 x 10uF 0805, 6.3V MLC capacitors. The 2 parallel capacitors provide reduced ESR and hence lower output ripple voltage. If a minimum footprint configuration is desired, a single 47uF MLC capacitor can be used.

NOTE: Please refer to product datasheet for specific recommendations.

Contact Information

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Phone: 408-544-7000
www.altera.com/

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