EEC1005

Enterprise Storage Backplane Management Processor

- Complete Universal Storage Backplane Management Processor
  - SFF-TA-1005 Universal Backplane Management (UBM) over I2C
  - Provides SFF-8654 compliant Host Facing Connector (HFC) communication support over I2C
  - HFC connection responds to all standard UBM commands from the host
  - Integrates the UBM FRU non-volatile memory on the UBM FRU I2C Address
  - Provides SFF-8639 compliant U.2 Drive Facing Connector (DFC) Support
  - Provides SFF-TA-1001 compliant U.3 Drive Facing Connector (DFC) Support
  - Support for SES over UBM
- Supports I2C communication to Baseboard Management Controller
- Up to 8 I2C ports for UBM and BMC host interfaces
- SFF-8485 Support
  - Implements up to 4 Hardware Accelerated SGPIO Legacy Interfaces for SAS/SATA backplane implementations
- Secure Boot
  - EEC1005 code is authenticated by a secure boot loader prior to loading from internal flash
  - Hardware accelerated crypto blocks provide fast secure boot
  - Secure Firmware update
  - Key revocation
- Supports Storage LED Management as per SFF-8489 IBPI specifications by default
- Custom LED patterns can be configured
- Scalable Solution for up to 16 Hard Drives on a Single Device
  - SGPIO Host Interfaces support up to 16 drives (SAS/SATA drive types)
  - UBM Host Interfaces support up to 12 drives (NVMe drive types)
  - Up to 6 HFCs
- Supports multiple backplanes on a single chassis
- Support for NVME Hot plug and Power Disable for drives
- Integrated NV Memory for:
  - UBM FRU (Field Replaceable Unit) for every HFC
  - General Purpose FRU
  - NV Configuration Memory
- Configurable Interfaces using a single analog configuration pin
  - Host interface (SGPIO vs UBM)
  - Number of HFCs and Drive Facing Connectors (DFCs)
  - Other supported features
- Monitors system PERST
  - One pin per DFC for PERST support
- Monitors for drive insertion from IFDET and PRSNT signals
  - IFDET2 support (for SFF-TA-1001)
- Package Options
  - 144 pin WFBGA RoHS Compliant package
  - 84 pin WFBGA RoHS Compliant package

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1.0 GENERAL DESCRIPTION

EEC1005 is a generic, easily configurable, True Universal Backplane Management (UBM) device that can be used on hard drive backplanes to provide complete storage enclosure management and reporting to computing host systems using industry standard communication protocols.

EEC1005 supports a variety of host interfaces to accommodate SAS/SATS/NVMe backplane. The SFF-8654 slimline connector (Host facing Connector) can be used to route SAS signals in which case the HBA will manage SAS/SATA drives, the same connector protocol (physically a different connector) can be used to route PCIe signals in which case the HBA will manage NVME drives. In both cases UBM will be used as management protocol with support of SGPIO as well on SAS Slimline (Configuration dependent).The device supports using U.2 and U.3 Drive facing Connectors. EEC1005 also supports Multiple Backplanes on a single chassis.

EEC1005 supports 2 or 3 LED IBPI blinking patterns for up to 16 drives. Customized LED blink pattern can also be programmed through the FRU.

The EEC1005 has a secure boot loader that authenticates and decrypts the Flash boot image (UBM application) using the AES-256, ECDSA P-256, SHA-256 cryptographic hardware accelerators. EEC1005 hardware accelerators support 128-bit and 256-bit AES encryption, ECDSA and EC_KCDSA signing algorithms, 1024-bits to 4096-bits RSA and Elliptic asymmetric public key algorithms, and a True Random Number Generator (TRNG). Additionally, the device offers lockable OTP storage for private keys and IDs.

EEC1005 is available in 84 pin and 144 pin WFBGA packages.

1.1 References

1. SFF-TA-1005 Universal Backplane Management Specification
2. SFF-8485 Serial General-Purpose Input/output (SGPIO) Specification
3. SFF-8448 SAS Sideband Signal Assignment
4. SFF-8489 Serial GPIO (International Blinking Pattern Interpretation)
5. Enterprise SSD Form Factor Version 1.0a
6. SFF-TA-1001 (U.3 Drive Connector) Specification
7. SFF-8639 (U.2 Drive Connector) Specification
8. SFF-9639 (U.2 Connector Pinout) Specification
9. SFF-8654 Slimline Connector Specification
10. SFF-9402 Multi-Protocol Internal Cables for SAS and/or PCIe (Slimline Connector Pinout) Specification
11. SCSI Enclosure Services -4 Specification

2.0 UBM BACKPLANE ARCHITECTURE

EEC1005 on the back plane communicates to the Host through SGPIO or I2C interface over the Host facing Connector (Host attach configuration) or dedicated cable (Direct attach configuration). It detects hard drive being installed in the backplane and notifies the host of the insertion/removal/failure of the drive. It also blinks Leds for each hard drive's status as explained in Section 8.0, "LED Specifications".

There are different types of Backplanes based on:

1. Number of drives the back plane supports
2. Type of host communication (For eg. I2C or SGPIO)
3. Type of Drive slots (For eg. U.2 or U.3)

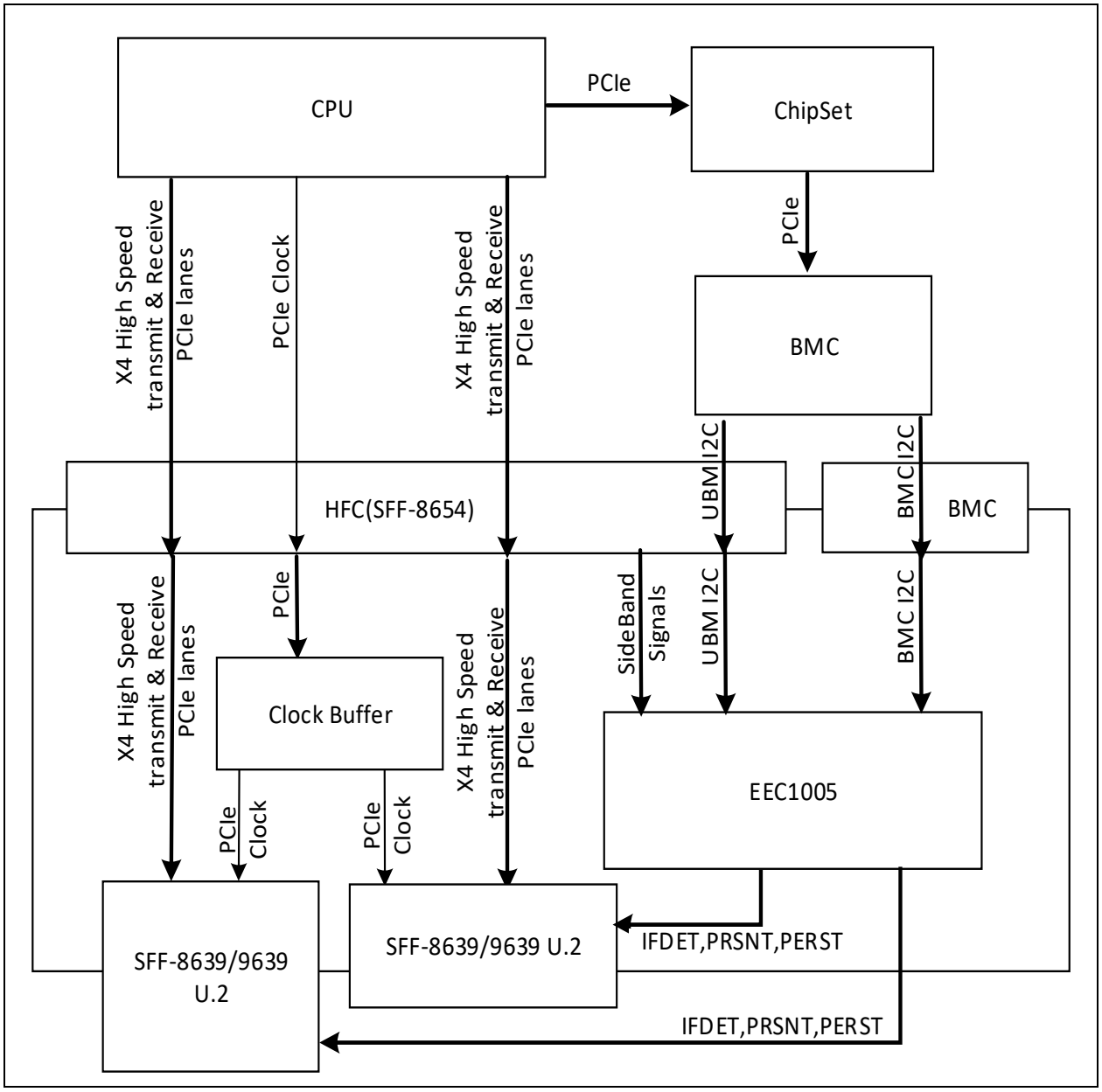
The different configurations of the backplane that EEC1005 supports is covered in Section 3.0, "Configurations".

2.1 Direct Attach UBM Backplane

A direct attach configuration is enabled when user connects the backplane directly to mother board and the drives are not managed by an HBA. In this case the drives are managed either by BMC or PCIe Switch/Expander for switch-based configurations.EEC1005 can be used in Direct attach configurations using UBM as the management protocol from BMC (BMC Emulation) or Switch/Expander.

EEC1005 based backplane architectures are capable of supporting Y-cable configurations where the PCIe lanes from a single Host HFC will be split into 2x backplane HFC's, this allows splitting on PCIe clocks using clock buffers as shown in the following diagram.

FIGURE 2-1: DIRECT ATTACH CONFIGURATION



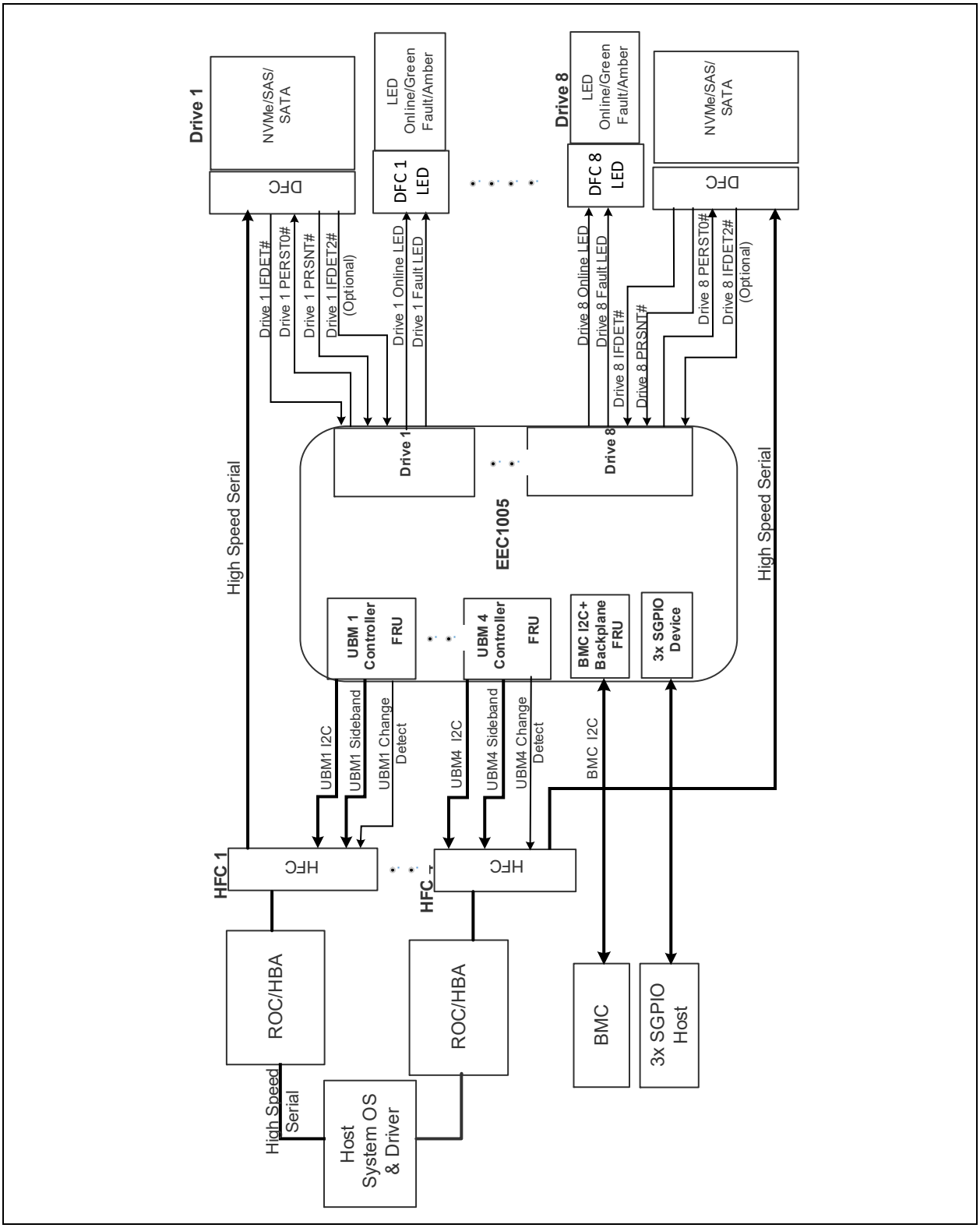
2.2 Host Attach UBM Backplane

A Host attach configuration is enabled when user connects the backplane directly to SMARTROC/HBA and the drives are managed by an HBA. EEC1005 can be used in Host attach configuration as in FIGURE 2-2: “Host Attach Configuration”. Each HFC is connected to a Host through a cable to communicate with EEC1005.

EEC1005 based backplane architecture supports NVME PERST functionality by allowing the Host to directly control the PERST signal. This allows the Host to directly control the reset behavior of NVME drive without adding any latency. The PERST signal will be driven from HFC and then split into 2 signals to control 2 drives from a single signal.

Note:	The hardware bifurcation of the PCIe lanes is application dependent. Usually each HFC bifurcates x8 lanes into two x4 connections.

FIGURE 2-2: HOST ATTACH CONFIGURATION



3.0 CONFIGURATIONS

Multiple Backplane architectures are supported using EEC1005 that are configured by firmware based on an analog value sampled at one of EEC1005 input ADC pin (Config Pin) at startup. Table 3-1, “EEC1005 Configuration Select” provides the complete list of Configurations selectable based on the analog value on CONFIG_PIN. The analog value can be set by a resistor divider network as in Figure 3-1, the values of the resistors are user defined.The configuration is fixed for a Backplane and is not runtime modified. The recommendations on the resistor values are provided in Table 3-2, “Recommended Resistor Values,” on page 9.

TABLE 3-1: EEC1005 CONFIGURATION SELECT

EEC1005 Config[a]	Pin Count	ID	Config (V)	Pinout	HFC Total[b]	HFC - SAS	HFC - PCIe	DFC Total	DFC SAS/ SATA	DFC PCIe
4 Drive SGPIO	84	01	0.1	Table 10-3, “SGPIO Controller - 84 Pin Package”	1	1	0	4	4	0
8 Drive SGPIO	84	02	0.2	Table 10-3, “SGPIO Controller - 84 Pin Package”	1	1	0	8	8	0
12 Drive SPGIO	144	03	0.3	Table 10-1, “SGPIO Controller - 144 Pin Package”	2	2	0	12	12	0
16 Drive SPGIO	144	04	0.4	Table 10-1, “SGPIO Controller - 144 Pin Package”	2	2	0	16	16	0
4 Drive UBM U.2	84	05	0.5	Table 10-4, “UBM Controller - 84 Pin Package”	3	1	2	4	4	4
8 Drive UBM U.2	84	06	0.6	Table 10-4, “UBM Controller - 84 Pin Package”	5	1	4	8	8	8
8 Drive UBM U.2 (Full Feature)	144	07	0.7	Table 10-2, “UBM Controller - 144 Pin Package”	5	1	4	8	8	8
8 Drive UBM U.3 (Minimum Feature)	84	08	0.8	Table 10-4, “UBM Controller - 84 Pin Package”	4	4	4	8	8	8
8 Drive UBM U.3 (Full Feature)	144	09	0.9	Table 10-2, “UBM Controller - 144 Pin Package”	4	4	4	8	8	8
12 Drive UBM U.2 PCIe Only (Full Featured)	144	0A	1.0	Table 10-2, “UBM Controller - 144 Pin Package”	6	0	6	12	0	12
12 Drive UBM U.3 PCIe Only (Full Featured)	144	0B	1.1	Table 10-2, “UBM Controller - 144 Pin Package”	6	0	6	12	0	12
8 Drive UBM+SGPIO U.2	144	0D	1.3	Table 10-5, “UBM_SGPIO Controller - 144 Pin Package”	5	1	4	8	8	8

a. Configurations not mentioned in the above table are not supported by EEC1005.

b. HFC Total is the number of host facing connectors required for a particular configuration.

FIGURE 3-1: VOLTAGE DIVIDER AT ADC INPUT

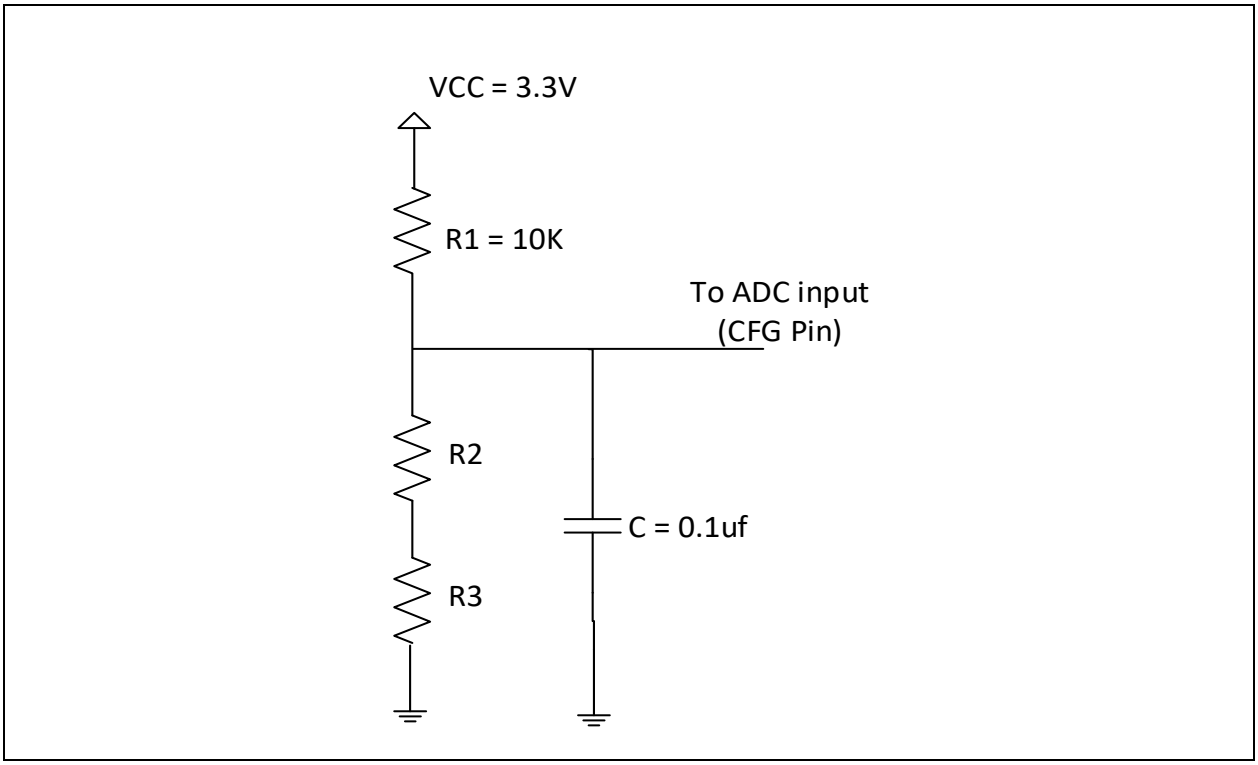


TABLE 3-2: RECOMMENDED RESISTOR VALUES

EEC1005 Config	Config (V)	Pinout	R2 (in Ohms)	R3(in Ohms)
4 Drive SGPIO	0.1	Table 10-3, “SGPIO Controller - 84 Pin Package”	301	11.5
8 Drive SGPIO	0.2	Table 10-3, “SGPIO Controller - 84 Pin Package”	634	11
12 Drive SPGIO	0.3	Table 10-1, “SGPIO Controller - 144 Pin Package”	1000	0
16 Drive SPGIO	0.4	Table 10-1, “SGPIO Controller - 144 Pin Package”	1370	9.31
4 Drive UBM U.2	0.5	Table 10-4, “UBM Controller - 84 Pin Package”	1780	5.76
8 Drive UBM U.2	0.6	Table 10-4, “UBM Controller - 84 Pin Package”	2210	12.1
8 Drive UBM U.2 (Full Feature)	0.7	Table 10-2, “UBM Controller - 144 Pin Package”	2670	40.2

TABLE 3-2: RECOMMENDED RESISTOR VALUES (CONTINUED)

EEC1005 Config	Config (V)	Pinout	R2 (in Ohms)	R3(in Ohms)
8 Drive UBM U.3 (Minimum Feature)	0.8	Table 10-4, "UBM Controller - 84 Pin Package"	3160	40.2
8 Drive UBM U.3 (Full Feature)	0.9	Table 10-2, "UBM Controller - 144 Pin Package"	3740	10
12 Drive UBM U.2 PCIe Only (Full Featured)	1.0	Table 10-2, "UBM Controller - 144 Pin Package"	4320	28
12 Drive UBM U.3 PCIe Only (Full Featured)	1.1	Table 10-2, "UBM Controller - 144 Pin Package"	4990	10
8 Drive UBM+SGPIO U.2	1.3	Table 10-5, "UBM_SGPIO Controller - 144 Pin Package"	5490	1000

Note 1: The resistor values suggested are based on the standard value resistors available @1% tolerance.

2: It is highly recommended to use 1% tolerant resistors at ADC input.

3: The ADC input capacitor should be 0.1uF.

4: The resistor R1 should be fixed at 10K.

5: The Config values not mentioned in the above table is not supported by EEC1005.

4.0 CONFIGURATION FRU

EEC1005 supports a 256-byte FRU (Field Replaceable Unit) that is used to initialize/input the parameters which are client specific. These parameters are read on power up as well as run time to initialize the firmware accordingly. This 256-byte FRU is accessible over BMC I2C segment, if used in an architecture where BMC exists.

TABLE 4-1: CONFIGURATION FRU TABLE

Address	Group	Field Name	Pattern	LED Name	Parameters
0x00	Global	ACTIVITY/2WIRE_RESET OPTION			
0x01	Global	IBPI PATTERN 2/3 LED			
0x02	Global	Backplane HFC Count			
0x03	Global	Backplane DFC Count			
0x04	Global	Backplane Physical Location			
0x05	Global	RSVD			
0x06	Global	RSVD			
0x07	Global	RSVD			
0x08	Global	RSVD			
0x09	Global	RSVD			
0x0A	Global	RSVD			
0x0B	Global	RSVD			
0x0C	Global	RSVD			
0x0D	Global	RSVD			
0x0E	Global	RSVD			
0x0F	Global	RSVD			
0x10	Global	RSVD			
0x11	Global	RSVD			
0x12	Global	RSVD			
0x13	Global	RSVD			
0x14	Global	CHECKSUM			
0x15	HFC0	UBM CONTROLLER DEVICE CODE MSB			
0x16	HFC0	UBM CONTROLLER DEVICE CODE			
0x17	HFC0	UBM CONTROLLER DEVICE CODE			
0x18	HFC0	UBM CONTROLLER DEVICE CODE LSB			
0x19	HFC0	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x1A	HFC0	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x1B	HFC0	HFC IDENTITY			
0x1C	HFC0	CPRSNT# or CHANGE_DETECT#			
0x1D	HFC0	RSVD			
0x1E	HFC0	RSVD			
0x1F	HFC0	RSVD			
0x20	HFC0	RSVD			
0x21	HFC0	RSVD			
0x22	HFC0	RSVD			
0x23	HFC0	RSVD			
0x24	HFC0	RSVD			
0x25	HFC0	RSVD			

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0x26	HFC0	RSVD			
0x27	HFC0	RSVD			
0x28	HFC0	RSVD			
0x29	HFC0	RSVD			
0x2A	HFC0	RSVD			
0x2B	HFC0	RSVD			
0x2C	HFC0	CHECKSUM			
0x2D	HFC1	UBM CONTROLLER DEVICE CODE MSB			
0x2E	HFC1	UBM CONTROLLER DEVICE CODE			
0x2F	HFC1	UBM CONTROLLER DEVICE CODE			
0x30	HFC1	UBM CONTROLLER DEVICE CODE LSB			
0x31	HFC1	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x32	HFC1	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x33	HFC1	HFC IDENTITY			
0x34	HFC1	CPRSNT# or CHANGE_DETECT#			
0x35	HFC1	RSVD			
0x36	HFC1	RSVD			
0x37	HFC1	RSVD			
0x38	HFC1	RSVD			
0x39	HFC1	RSVD			
0x3A	HFC1	RSVD			
0x3B	HFC1	RSVD			
0x3C	HFC1	RSVD			
0x3D	HFC1	RSVD			
0x3E	HFC1	RSVD			
0x3F	HFC1	RSVD			
0x40	HFC1	RSVD			
0x41	HFC1	RSVD			
0x42	HFC1	RSVD			
0x43	HFC1	RSVD			
0x44	HFC1	CHECKSUM			
0x45	HFC2	UBM CONTROLLER DEVICE CODE MSB			
0x46	HFC2	UBM CONTROLLER DEVICE CODE			
0x47	HFC2	UBM CONTROLLER DEVICE CODE			
0x48	HFC2	UBM CONTROLLER DEVICE CODE LSB			
0x49	HFC2	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x4A	HFC2	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x4B	HFC2	HFC IDENTITY			
0x4C	HFC2	CPRSNT# or CHANGE_DETECT#			
0x4D	HFC2	RSVD			
0x4E	HFC2	RSVD			

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0x4F	HFC2	RSVD			
0x50	HFC2	RSVD			
0x51	HFC2	RSVD			
0x52	HFC2	RSVD			
0x53	HFC2	RSVD			
0x54	HFC2	RSVD			
0x55	HFC2	RSVD			
0x56	HFC2	RSVD			
0x57	HFC2	RSVD			
0x58	HFC2	RSVD			
0x59	HFC2	RSVD			
0x5A	HFC2	RSVD			
0x5B	HFC2	RSVD			
0x5C	HFC2	CHECKSUM			
0x5D	HFC3	UBM CONTROLLER DEVICE CODE MSB			
0x5E	HFC3	UBM CONTROLLER DEVICE CODE			
0x5F	HFC3	UBM CONTROLLER DEVICE CODE			
0x60	HFC3	UBM CONTROLLER DEVICE CODE LSB			
0x61	HFC3	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x62	HFC3	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x63	HFC3	HFC IDENTITY			
0x64	HFC3	CPRSNT# or CHANGE_DETECT#			
0x65	HFC3	RSVD			
0x66	HFC3	RSVD			
0x67	HFC3	RSVD			
0x68	HFC3	RSVD			
0x69	HFC3	RSVD			
0x6A	HFC3	RSVD			
0x6B	HFC3	RSVD			
0x6C	HFC3	RSVD			
0x6D	HFC3	RSVD			
0x6E	HFC3	RSVD			
0x6F	HFC3	RSVD			
0x70	HFC3	RSVD			
0x71	HFC3	RSVD			
0x72	HFC3	RSVD			
0x73	HFC3	RSVD			
0x74	HFC3	CHECKSUM			
0x75	HFC4	UBM CONTROLLER DEVICE CODE MSB			
0x76	HFC4	UBM CONTROLLER DEVICE CODE			
0x77	HFC4	UBM CONTROLLER DEVICE CODE			
0x78	HFC4	UBM CONTROLLER DEVICE CODE LSB			

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0x79	HFC4	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x7A	HFC4	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x7B	HFC4	HFC IDENTITY			
0x7C	HFC4	CPRSNT# or CHANGE_DETECT#			
0x7D	HFC4	RSVD			
0x7E	HFC4	RSVD			
0x7F	HFC4	RSVD			
0x80	HFC4	RSVD			
0x81	HFC4	RSVD			
0x82	HFC4	RSVD			
0x83	HFC4	RSVD			
0x84	HFC4	RSVD			
0x85	HFC4	RSVD			
0x86	HFC4	RSVD			
0x87	HFC4	RSVD			
0x88	HFC4	RSVD			
0x89	HFC4	RSVD			
0x8A	HFC4	RSVD			
0x8B	HFC4	RSVD			
0x8C	HFC4	CHECKSUM			
0x8D	HFC5	UBM CONTROLLER DEVICE CODE MSB			
0x8E	HFC5	UBM CONTROLLER DEVICE CODE			
0x8F	HFC5	UBM CONTROLLER DEVICE CODE			
0x90	HFC5	UBM CONTROLLER DEVICE CODE LSB			
0x91	HFC5	SILICON VENDOR ID VENDOR SPECIFIC 0			
0x92	HFC5	SILICON VENDOR ID VENDOR SPECIFIC 1			
0x93	HFC5	HFC IDENTITY			
0x94	HFC5	CPRSNT# or CHANGE_DETECT#			
0x95	HFC5	RSVD			
0x96	HFC5	RSVD			
0x97	HFC5	RSVD			
0x98	HFC5	RSVD			
0x99	HFC5	RSVD			
0x9A	HFC5	RSVD			
0x9B	HFC5	RSVD			
0x9C	HFC5	RSVD			
0x9D	HFC5	RSVD			
0x9E	HFC5	RSVD			
0x9F	HFC5	RSVD			
0xA0	HFC5	RSVD			
0xA1	HFC5	RSVD			

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0xA2	HFC5	RSVD			
0xA3	HFC5	RSVD			
0xA4	HFC5	CHECKSUM			
0xA5	HFC6	UBM CONTROLLER DEVICE CODE MSB			
0xA6	HFC6	UBM CONTROLLER DEVICE CODE			
0xA7	HFC6	UBM CONTROLLER DEVICE CODE			
0xA8	HFC6	UBM CONTROLLER DEVICE CODE LSB			
0xA9	HFC6	SILICON VENDOR ID VENDOR SPECIFIC 0			
0xAA	HFC6	SILICON VENDOR ID VENDOR SPECIFIC 1			
0xAB	HFC6	HFC IDENTITY			
0xAC	HFC6	CPRSNT# or CHANGE_DETECT#			
0xAD	HFC6	RSVD			
0xAE	HFC6	RSVD			
0xAF	HFC6	RSVD			
0xB0	HFC6	RSVD			
0xB1	HFC6	RSVD			
0xB2	HFC6	RSVD			
0xB3	HFC6	RSVD			
0xB4	HFC6	RSVD			
0xB5	HFC6	RSVD			
0xB6	HFC6	RSVD			
0xB7	HFC6	RSVD			
0xB8	HFC6	RSVD			
0xB9	HFC6	RSVD			
0xBA	HFC6	RSVD			
0xBB	HFC6	RSVD			
0xBC	HFC6	CHECKSUM			
0xBD	LED PATTERN	NOT_PRES_LED_ACT_BLINKP_REP	NOT_PRES	LED_ACT	BLINKP_REP
0xBE	LED PATTERN	NOT_PRES_LED_ACT_PAT_PERIOD	NOT_PRES	LED_ACT	PAT_PERIOD
0xBF	LED PATTERN	NOT_PRES_LED_STAorLOC_BLINKP_REP	NOT_PRES	LED_STAorLOC	BLINKP_REP
0xC0	LED PATTERN	NOT_PRES_LED_STAorLOC_PAT_PERIOD	NOT_PRES	LED_STAorLOC	PAT_PERIOD
0xC1	LED PATTERN	NOT_PRES_LED_FAIL_BLINKP_REP	NOT_PRES	LED_FAIL	BLINKP_REP
0xC2	LED PATTERN	NOT_PRES_LED_FAIL_PAT_PERIOD	NOT_PRES	LED_FAIL	PAT_PERIOD
0xC3	LED PATTERN	PRES_NO_ACT_LED_ACT_BLINKP_REP	PRES_NO_ACT	LED_ACT	BLINKP_REP
0xC4	LED PATTERN	PRES_NO_ACT_LED_ACT_PAT_PERIOD	PRES_NO_ACT	LED_ACT	PAT_PERIOD
0xC5	LED PATTERN	PRES_NO_ACT_LED_STAorLOC_BLINKP_REP	PRES_NO_ACT	LED_STAorLOC	BLINKP_REP

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0xC6	LED PAT-TERN	PRES_NO_ACT_LED_STAor-LOC_PAT_PERIOD	PRES_NO_AC T	LED_STAor-LOC	PAT_PE-RIOD
0xC7	LED PAT-TERN	PRES_NO_ACT_LED_FAIL_BLINKP_REP	PRES_NO_AC T	LED_FAIL	BLINK-P_REP
0xC8	LED PAT-TERN	PRES_NO_ACT_LED_FAIL_PAT_PE-RIOD	PRES_NO_AC T	LED_FAIL	PAT_PE-RIOD
0xC9	LED PAT-TERN	PRES_ACT_LED_ACT_BLINKP_REP	PRES_ACT	LED_ACT	BLINK-P_REP
0xCA	LED PAT-TERN	PRES_ACT_LED_ACT_PAT_PERIOD	PRES_ACT	LED_ACT	PAT_PE-RIOD
0xCB	LED PAT-TERN	PRES_ACT_LED_STAorLOC_BLINK-P_REP	PRES_ACT	LED_STAor-LOC	BLINK-P_REP
0xCC	LED PAT-TERN	PRES_ACT_LED_STAorLOC_PAT_PE-RIOD	PRES_ACT	LED_STAor-LOC	PAT_PE-RIOD
0xCD	LED PAT-TERN	PRES_ACT_LED_FAIL_BLINKP_REP	PRES_ACT	LED_FAIL	BLINK-P_REP
0xCE	LED PAT-TERN	PRES_ACT_LED_FAIL_PAT_PERIOD	PRES_ACT	LED_FAIL	PAT_PE-RIOD
0xCF	LED PAT-TERN	LOCATE_LED_ACT_BLINKP_REP	LOCATE	LED_ACT	BLINK-P_REP
0xD0	LED PAT-TERN	LOCATE_LED_ACT_PAT_PERIOD	LOCATE	LED_ACT	PAT_PE-RIOD
0xD1	LED PAT-TERN	LOCATE_LED_STAorLOC_BLINKP_REP	LOCATE	LED_STAor-LOC	BLINK-P_REP
0xD2	LED PAT-TERN	LOCATE_LED_STAorLOC_PAT_PERIOD	LOCATE	LED_STAor-LOC	PAT_PE-RIOD
0xD3	LED PAT-TERN	LOCATE_LED_FAIL_BLINKP_REP	LOCATE	LED_FAIL	BLINK-P_REP
0xD4	LED PAT-TERN	LOCATE_LED_FAIL_PAT_PERIOD	LOCATE	LED_FAIL	PAT_PE-RIOD
0xD5	LED PAT-TERN	FAIL_LED_ACT_BLINKP_REP	FAIL	LED_ACT	BLINK-P_REP
0xD6	LED PAT-TERN	FAIL_LED_ACT_PAT_PERIOD	FAIL	LED_ACT	PAT_PE-RIOD
0xD7	LED PAT-TERN	FAIL_LED_STAorLOC_BLINKP_REP	FAIL	LED_STAor-LOC	BLINK-P_REP
0xD8	LED PAT-TERN	FAIL_LED_STAorLOC_PAT_PERIOD	FAIL	LED_STAor-LOC	PAT_PE-RIOD
0xD9	LED PAT-TERN	FAIL_LED_FAIL_BLINKP_REP	FAIL	LED_FAIL	BLINK-P_REP
0xDA	LED PAT-TERN	FAIL_LED_FAIL_PAT_PERIOD	FAIL	LED_FAIL	PAT_PE-RIOD
0xDB	LED PAT-TERN	REBUILD_LED_ACT_BLINKP_REP	REBUILD	LED_ACT	BLINK-P_REP
0xDC	LED PAT-TERN	REBUILD_LED_ACT_PAT_PERIOD	REBUILD	LED_ACT	PAT_PE-RIOD
0xDD	LED PAT-TERN	REBUILD_LED_STAorLOC_BLINKP_REP	REBUILD	LED_STAor-LOC	BLINK-P_REP
0xDE	LED PAT-TERN	REBUILD_LED_STAorLOC_PAT_PERIOD	REBUILD	LED_STAor-LOC	PAT_PE-RIOD

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0xDF	LED PATTERN	REBUILD_LED_FAIL_BLINKP_REP	REBUILD	LED_FAIL	BLINKP_REP
0xE0	LED PATTERN	REBUILD_LED_FAIL_PAT_PERIOD	REBUILD	LED_FAIL	PAT_PERIOD
0xE1	LED PATTERN	PFA_LED_ACT_BLINKP_REP	PFA	LED_ACT	BLINKP_REP
0xE2	LED PATTERN	PFA_LED_ACT_PAT_PERIOD	PFA	LED_ACT	PAT_PERIOD
0xE3	LED PATTERN	PFA_LED_STAorLOC_BLINKP_REP	PFA	LED_STAorLOC	BLINKP_REP
0xE4	LED PATTERN	PFA_LED_STAorLOC_PAT_PERIOD	PFA	LED_STAorLOC	PAT_PERIOD
0xE5	LED PATTERN	PFA_LED_FAIL_BLINKP_REP	PFA	LED_FAIL	BLINKP_REP
0xE6	LED PATTERN	PFA_LED_FAIL_PAT_PERIOD	PFA	LED_FAIL	PAT_PERIOD
0xE7	LED PATTERN	RSVD			
0xE8	LED PATTERN	RSVD			
0xE9	LED PATTERN	RSVD			
0xEA	LED PATTERN	RSVD			
0xEB	LED PATTERN	RSVD			
0xEC	LED PATTERN	RSVD			
0xED	LED PATTERN	RSVD			
0xEE	LED PATTERN	RSVD			
0xEF	LED PATTERN	RSVD			
0xF0	LED PATTERN	RSVD			
0xF1	LED PATTERN	RSVD			
0xF2	LED PATTERN	RSVD			
0xF3	LED PATTERN	RSVD			
0xF4	LED PATTERN	RSVD			
0xF5	LED PATTERN	RSVD			
0xF6	LED PATTERN	RSVD			
0xF7	LED PATTERN	RSVD			

TABLE 4-1: CONFIGURATION FRU TABLE (CONTINUED)

Address	Group	Field Name	Pattern	LED Name	Parameters
0xF8	LED PATTERN	RSVD			
0xF9	LED PATTERN	RSVD			
0xFA	LED PATTERN	RSVD			
0xFB	LED PATTERN	RSVD			
0xFC	LED PATTERN	RSVD			
0xFD	LED PATTERN	RSVD			
0xFE	LED PATTERN	RSVD			
0xFF	LED PATTERN	CHECKSUM			

5.0 GENERIC FRU

EEC1005 has a Generic FRU space which customer can use as non volatile storage. 256 bytes are allocated for this Customer defined Generic FRU. This memory emulates AT24C02 256 byte I2C EEPROM.Read and write of data to this FRU space can be done by host over the same physical I2C interface connected to BMC/Host at I2C slave address 0x54 (7-bit address).

6.0 UBM FRU

The SFF-TA-1005 (UBM) Specification calls out for an external Field Replaceable Unit (FRU) per every UBM Controller.

EEC1005 incorporates a UBM FRU for every UBM Controller as per the spec requirement within EEC1005 Memory space. This saves board space and cost.

The UBM FRU on backplane is a 256 byte read-only NVRAM with IPMI FRU formatted content and is responsible for reporting static backplane information.

FIGURE 6-1: UBM FRU FORMAT

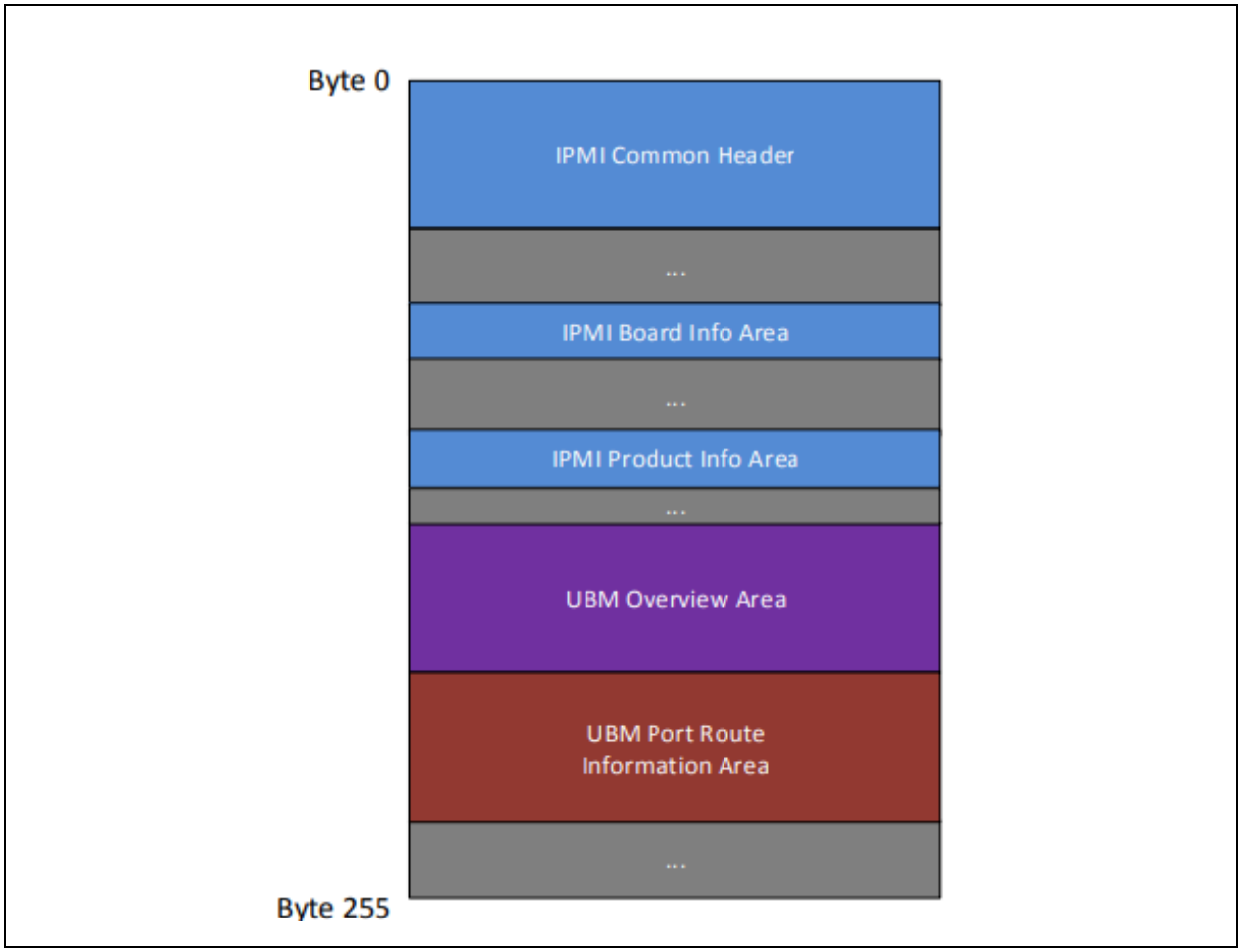
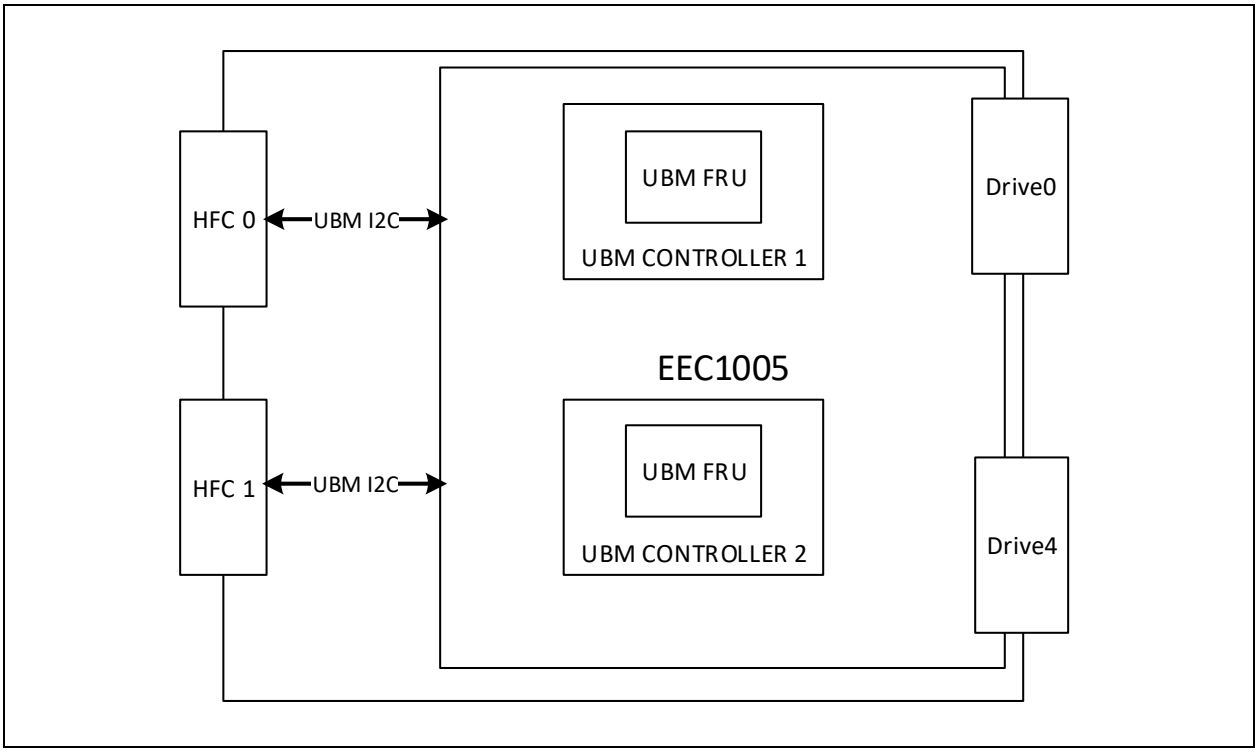


FIGURE 6-2: UBM FRU



The UBM FRU is addressed as specified by SFF-TA-1005, over Slave Address (0xAE).

7.0 UBM CONTROLLER COMMANDS

The UBM Controller manages the Host facing Connector sideband I/O signaling, the Drive facing connector I/O signaling and the LED states for the DFC. It provides backplane implementation features and options for the initialization of the devices. These features are selected for the device through the CONFIG_PIN (Section 10.2, "Pin List") as explained in Section 3.0, "Configurations".

The below are the supported UBM controller command set for EEC1005. There are variables in UBM that are client specific for example “Vendor Specific” bytes of Silicon Identity and Revision Command. EEC 1005 allows clients to initialize those variables from FRU, the UBM registers are initialized to these values on power up.

7.1 Silicon Identity and Revision (0x02)

Byte/Bit	7	6	5	4	3	2	1	0
0	UBM Spec Major Version = **1**				UBM Spec Minor Version = **3**			
1	PCIE Vendor ID (LSB) = 0x54							
2	PCIE Vendor ID (MSB) = 0x00							
3	**RESERVED = 0x00**							
4	UMB Controller Device Code (LSB) = Configuration FRU							
5	UBM Controller Device Code = Configuration FRU							
6								
7	UBM Controller Device Code (MSB) = Configuration FRU							
8	**RESERVED = 0x0000**							
9								
10	UBM Controller Image Version Minor = Backplane FW Minor Version							
11	UBM Controller Image Version Major = Backplane FW Major Version							
12	Vendor Specific = Configuration FRU							
13								

7.2 Programming Update Mode Capabilities (0x03)

Byte/Bit	7	6	5	4	3	2	1	0
0	RSVD						Update Mode = 0x01	

Update Mode: The update mode will be set to 0x01 to indicate that update is supported while the device remains online. In order to support the non-destructive status of NVME drives while the update is being performed the GPIOs status will remain consistent across a firmware reset.

7.3 Host Facing Connector Info (0x30)

Byte/Bit	7	6	5	4	3	2	1	0
0	Port Type = 1 (PCIe) = 0 (SAS)	RSVD = 0x0			Host Facing Connector Identity = Configuration FRU			

Host Facing Connector ID will start from 0 and will report SAS HFC first followed by NVME HFC

PORT TYPE: HFCs that are SAS/SATA shall report Port Type = 0. HFCs that are PCIe shall report Port Type = 1.

7.4 Backplane Info (0x31)

Byte/Bit	7	6	5	4	3	2	1	0
0	Backplane Type			RSVD = 0	Backplane Number = Configuration FRU			

The Backplane Type will represent the Configuration selected from Config Pin.The Backplane Number will be read from Configuration FRU or configured based on input voltage on CONFIG_BPNUM_PIN.

7.5 Starting Slot (0x32)

Byte/Bit	7	6		5	4	3	2	1	0
0		Starting Slot = 0x00							

Starting Slot is fixed to 0x0.

7.6 Capabilities (0x33)

Byte/Bit	7	6	5	4	3	2	1	0
0	DFC Change Count = 1	Change Detect Int = 1	2-Wire Reset = 02h		Dual Port = 0b	PCIe Reset Control =0	Slot Power Control = 1	Clock Routing = Configuration FRU
1	RSVD = 00h				DFC PERST# Management Override support =1	IFDET2 = 0 or 1*	IFDET1 = 1 P4	PRSNT = 1 P10

CLOCK ROUTING: Set to 0 for SAS HFCS. Set to 1 for PCIe HFCs.

SLOT POWER CONTROL: Set to 0. DFCs with SAS drives will support Slot Power Control if a backplane configuration supports Power Disable Pin

PCIE RESET CONTROL: Set to 0.

DUAL PORT: Set to 0. Single ported only.

2WIRE RESET: Set to 0. 2-wire reset is not supported.

CHANGE DETECT: Set to 1. One Change Detect interrupt supported per backplane HFC.

DFC CHANGE COUNT : Set to 1. Indicates if a change count is maintained per an individual DFC Status and Control Command Descriptor.

PRSNT: Set to 1. Indicates that the DFCs connected to this HFC support the PRSNT signal.

IFDET1: Set to 1. Indicates that the DFCs connected to this HFC support the IFDET1 signal.

*IFDET2: This bit will be set to 1 if it is a U.3 backplane and to 0 if it is a U.2 backplane

DFC PERST# MANAGEMENT OVERRIDE : Set to 1, Override supported

7.7 Features (0x34)

Byte/Bit	7	6	5	4	3	2	1	0
0	DFC PERST# Management Override		Operational State Mask = 1b	Drive Type Change Mask = 1b	PCIE Reset Change Mask = 1b	CPRSTN = Configuration FRU	Write Checksum = 1b	Read Checksum = 1b
1	RSVD = 0x00							

READ CHECKSUM: Set to 1.

WRITE CHECKSUM CHECKING: Set to 1.

CPRSNT LEGACY MODE: Set to 0.

PCIE RESET CHANGE MASK: Set to 1.

DRIVE TYPE INSTALLED CHANGE COUNT MASK: Set to 1

OPERATIONAL STATE CHANGE COUNT MASK: Set to 1.

DFC PERST# MANAGEMENT OVERRIDE : Indicates the DFC_PERST# behaviour when a drive has been installed

0 = No override

1 = DFC PERST# Managed upon install

2 = DFC PERST# Automatically released upon install

3 = Reserved

8.0 LED SPECIFICATIONS

EEC1005 supports three LED's per every DFC (Activity, Fail, Locate).The Drive Activity LED can be controlled directly from Host or from EEC1005 which is selected using Configuration FRU (Configuration address 0x01), the Fail (Amber) and Locate (Green) are supported as a bi color LED on backplane and controlled by EEC1005.

In order to prevent any current leakage, the LED pins will remain tri-stated till the backplane is initialized and the default state for all the LED's will be off on power up after initialization is complete.

The table below summarizes the LED patterns as per International Blinking Pattern Interpretation defined in SFF-8489.

TABLE 8-1: IBPI LED BLINK PATTERN

Drive State	Locate/Identify LED (Green)	Fail LED (Amber)
Drive Not Present	OFF	OFF
Drive Present, No Activity	ON	OFF
Drive Present, Activity	ON	OFF
Locate (Identify)	4Hz	OFF
Fail	OFF	ON
Rebuild	OFF	1Hz
Rebuild Abort	OFF	1Hz
Predicted Failure (PFA)	OFF	2 Blinks at 4Hz & Pause for 0.5sec
Hot spare	Not Supported	Not Supported
In A Critical Array	Not Supported	Not Supported
In a Failed Array	Not Supported	Not Supported

If a Host sets multiple drive states at the same time, then backplane controller will follow a priority as defined in the below. Configurable LED blink frequency/duty cycle are also supported via FRU in order to support blink patterns that are not IBPI complaint.

TABLE 8-2: LED PRIORITY

Drive State	Priority
Locate (Identify)	1
Fault	2
Predicted Failure	3
Rebuild Abort	4
Drive Present, Activity	5
Drive Present, No Activity	6

9.0 MULTIPLE CHASSIS CONFIGURATION

When multiple Backplanes are used in a single system, the Backplane Number in the Backplane Info (0x31) UBM register is used by host to determine the physical backplane location of a given backplane.

The Backplane Number is populates with the values of Table 9-1, " Backplane number vs Resistor select" as a function of the voltage on pin CONFIG_BPNUM_PIN. This voltage can be provided by a fixed voltage divider on the backplane or by mating with the backplane power cable. Alternatively, the Configuration FRU can be used to overwrite the Backplane Number value. This is done by writing a value different than 0xFF to offset 0x04 of the Configuration FRU, Backplane Physical Location.

FIGURE 9-1: MULTIPLE CHASSIS CONFIGURATION

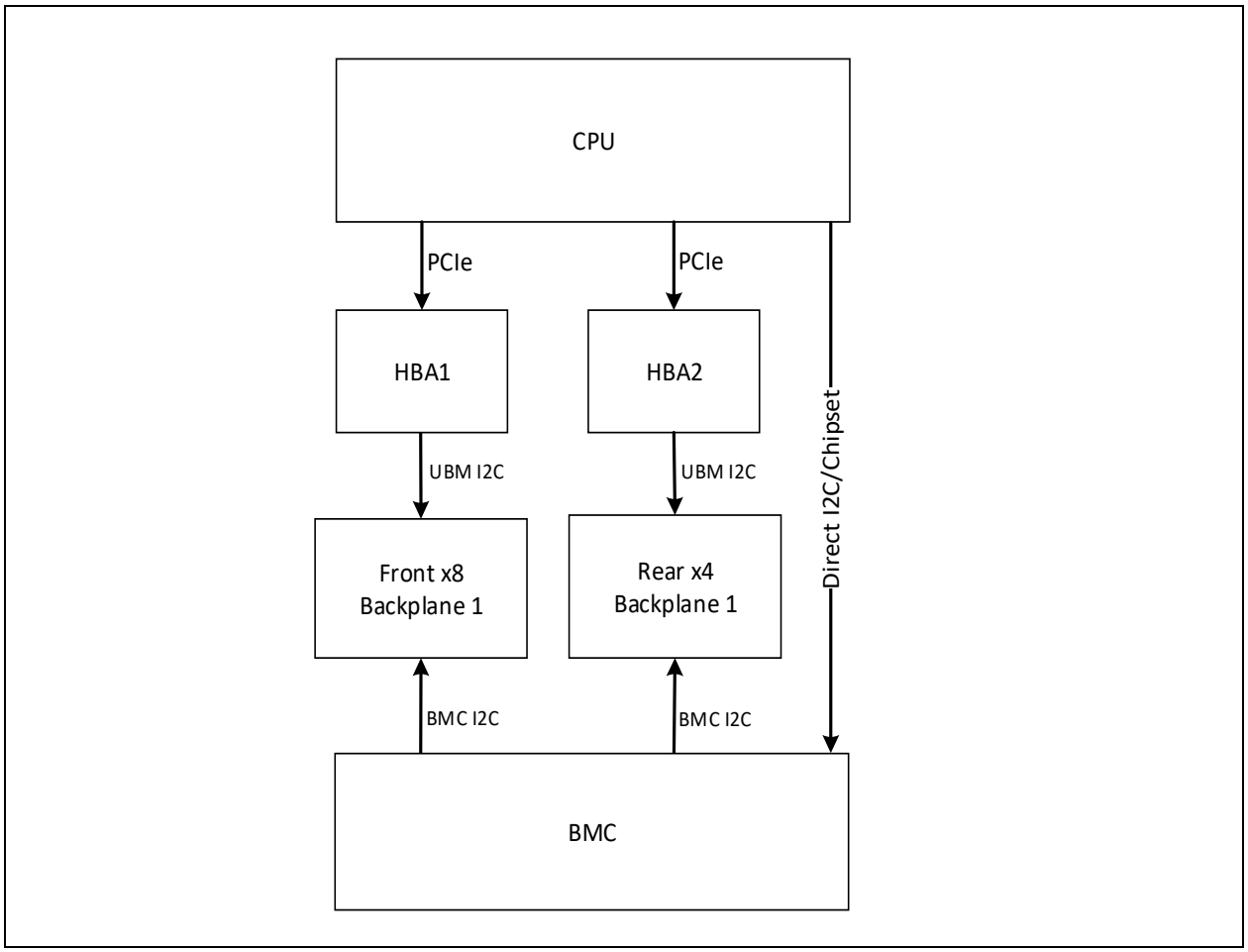


FIGURE 9-2: BACKPLANE NUMBER SELECT ADC INPUT

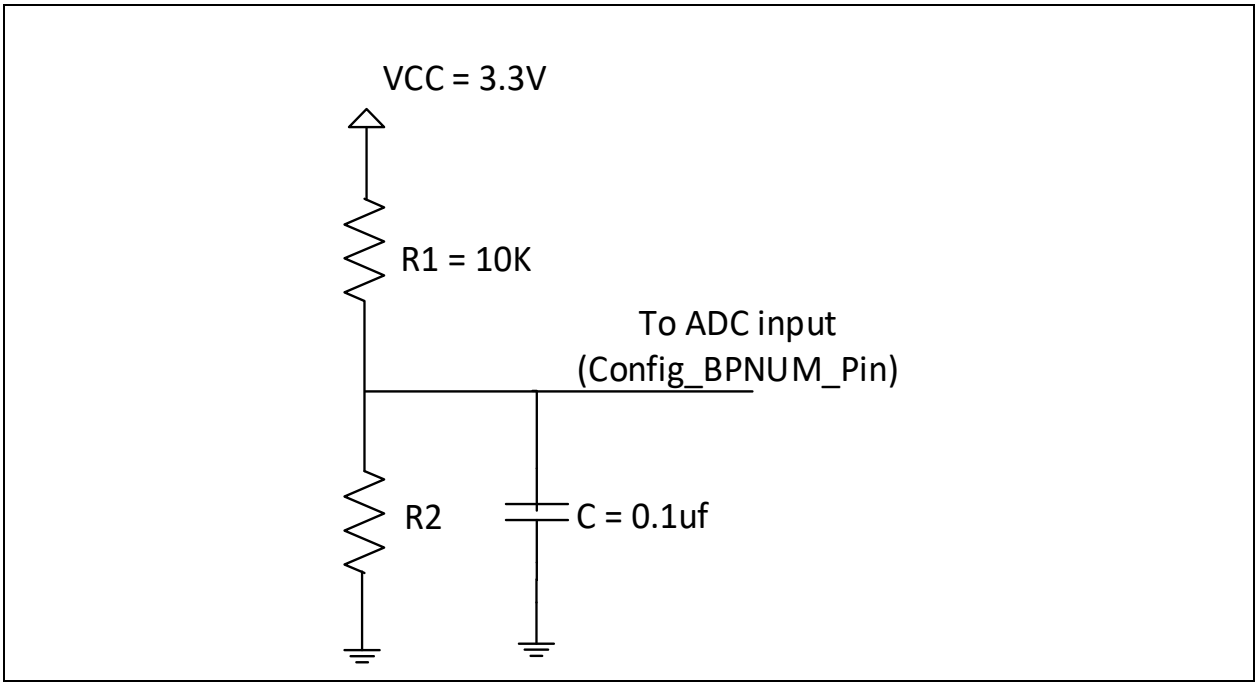


TABLE 9-1: BACKPLANE NUMBER VS RESISTOR SELECT

Backplane Number	Pull Down Resistor (R2) in Ohms	Voltage at the Config_BPNUM_Pin
0	0	0.000
1	470	0.148
2	820	0.250
3	1200	0.354
4	1800	0.503
5	2700	0.702
6	3600	0.874
7	4700	1.055
8	5600	1.185
9	6800	1.336
10	8200	1.487
11	10000	1.650
12	12000	1.800
13	15000	1.980
14	18000	2.121
15	22000	2.269

Note 1: The resistor values suggested are based on the standard value resistors available @1% tolerance

2: It is highly recommended to use 1% tolerant resistors at ADC input

3: The ADC input capacitor should be 0.1uF

4: The resistor R1 should be fixed at 10K

5: The Backplane Number values not mentioned in the above table is not supported by EEC1005

10.0 PIN CONFIGURATION

10.1 Description

Section 10.0 “Pin Configuration” consists of the Pin Lists and Package Drawings.

10.2 Pin List

TABLE 10-1: SGPIO CONTROLLER - 144 PIN PACKAGE

Ball Number	Function
A1	DFC_00_PWR_DISABLE
A2	BMC_I2C_SDA
A3	BMC_I2C_SCL
A4	DFC_14_IFDET_N
A5	DFC_13_IFDET_N
A6	RSVD
A7	NC
A8	SGPIO_03_DATAOUT
A9	DFC_07_IFDET_N
A10	DFC_13_ACTIVITY_N
A11	DFC_08_PWR_DISABLE
A12	DFC_02_LED_STA_N
B1	DFC_06_ACTIVITY_N
B2	SGPIO_00_CLOCK
B3	DFC_05_LED_STA_N
B4	DFC_01_IFDET_N
B5	DFC_12_IFDET_N
B6	NC
B7	DFC_09_PRSNT_N
B8	DFC_03_PWR_DISABLE
B9	DFC_05_PWR_DISABLE
B10	DFC_04_PWR_DISABLE
B11	DFC_14_ACTIVITY_N
B12	SGPIO_03_CTRL_TYPE
C1	DFC_01_PWR_DISABLE
C2	SGPIO_03_CLOCK
C3	SGPIO_01_CLOCK
C4	SGPIO_02_CLOCK
C5	DFC_13_PRSNT_N
C6	RSVD
C7	DFC_10_PRSNT_N
C8	DFC_07_LED_STA_N
C9	DFC_02_ACTIVITY_N
C10	DFC_10_ACTIVITY_N
C11	DFC_07_PWR_DISABLE
C12	DFC_03_ACTIVITY_N
D1	VCC

TABLE 10-1: SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
D2	DFC_07_ACTIVITY_N
D3	DFC_02_IFDET_N
D4	nRESET_IN
D5	SGPIO_02_LOAD
D6	DFC_12_PWR_DISABLE
D7	NC
D8	DFC_11_PWR_DISABLE
D9	DFC_08_IFDET_N
D10	DFC_11_ACTIVITY_N
D11	DFC_14_PWR_DISABLE
D12	DFC_13_PWR_DISABLE
E1	BMC_2WIRE_RESET
E2	DFC_15_ACTIVITY_N
E3	DFC_02_PWR_DISABLE
E4	SGPIO_00_DATAOUT
E5	VCC
E6	VSS
E7	VCC
E8	VSS
E9	SGPIO_01_DATAOUT
E10	DFC_09_ACTIVITY_N
E11	DFC_00_LED_ACT_N
E12	SGPIO_02_CTRL_TYPE
F1	VR_CAP
F2	DFC_06_PWR_DISABLE
F3	SGPIO_03_DATAIN
F4	SGPIO_01_LOAD
F5	VCC
F6	DFC_06_IFDET_N
F7	DFC_04_LED_STA_N
F8	VSS
F9	DFC_07_PRSNT_N
F10	nSTRAP_IN
F11	DFC_08_ACTIVITY_N
F12	DFC_06_LED_STA_N
G1	DFC_15_PWR_DISABLE
G2	VREF_ADC
G3	SGPIO_03_LOAD
G4	DFC_12_ACTIVITY_N
G5	VSS
G6	VSS
G7	DFC_04_ACTIVITY_N
G8	VCC

TABLE 10-1: SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
G9	HEARTBEAT_PIN
G10	DFC_08_LED_STA_N
G11	DFC_03_LED_STA_N
G12	DFC_05_ACTIVITY_N
H1	CONFIG_PIN
H2	DFC_05_IFDET_N
H3	DFC_09_PWR_DISABLE
H4	DFC_01_LED_ACT_N
H5	DFC_10_PWR_DISABLE
H6	VCC
H7	VCC
H8	DFC_00_ACTIVITY_N
H9	DFC_09_LED_STA_N
H10	DFC_10_LED_STA_N
H11	DFC_11_LED_STA_N
H12	DFC_11_LED_ACT_N
J1	DFC_04_IFDET_N
J2	DFC_00_IFDET_N
J3	DFC_03_IFDET_N
J4	DFC_10_IFDET_N
J5	DFC_03_LED_ACT_N
J6	DFC_15_LED_ACT_N
J7	DFC_12_LED_ACT_N
J8	SGPIO_02_DATAIN
J9	NC
J10	DFC_12_PRSNT_N
J11	DFC_11_PRSNT_N
J12	SGPIO_00_CTRL_TYPE
K1	CONFIG_BPNUM_PIN
K2	DFC_00_PRSNT_N
K3	DFC_15_PRSNT_N
K4	DFC_02_LED_ACT_N
K5	DFC_13_LED_ACT_N
K6	DFC_12_LED_STA_N
K7	DFC_06_LED_ACT_N
K8	DFC_07_LED_ACT_N
K9	DFC_09_LED_ACT_N
K10	DFC_08_LED_ACT_N
K11	SGPIO_00_DATAIN
K12	DFC_15_IFDET_N
L1	DFC_01_PRSNT_N
L2	SGPIO_00_LOAD
L3	DFC_14_PRSNT_N

TABLE 10-1: SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
L4	SGPIO_01_DATAIN
L5	DFC_14_LED_ACT_N
L6	DFC_14_LED_STA_N
L7	DFC_05_LED_ACT_N
L8	DFC_04_PRSNT_N
L9	DFC_01_LED_STA_N
L10	SGPIO_01_CTRL_TYPE
L11	DFC_05_PRSNT_N
L12	DFC_10_LED_ACT_N
M1	DFC_09_IFDET_N
M2	DFC_02_PRSNT_N
M3	DFC_11_IFDET_N
M4	DFC_03_PRSNT_N
M5	DFC_08_PRSNT_N
M6	DFC_04_LED_ACT_N
M7	DFC_13_LED_STA_N
M8	DFC_00_LED_STA_N
M9	DFC_15_LED_STA_N
M10	DFC_01_ACTIVITY_N
M11	SGPIO_02_DATAOUT
M12	DFC_06_PRSNT_N

TABLE 10-2: UBM CONTROLLER - 144 PIN PACKAGE

Ball Number	Function
A1	DFC_02_IFDET2_N
A2	BMC_I2C_SDA
A3	BMC_I2C_SCL
A4	HFC_04_SCL
A5	HFC_04_SDA
A6	RSVD
A7	HFC_01_SDA
A8	DFC_06_ACTIVITY_N
A9	DFC_07_IFDET_N
A10	DFC_10_IFDET2_N
A11	DFC_09_IFDET2_N
A12	DFC_02_LED_STA_N
B1	DFC_01_IFDET2_N
B2	HFC_00_SCL
B3	DFC_05_LED_STA_N
B4	DFC_01_IFDET_N
B5	HFC_02_SCL
B6	HFC_02_SDA

TABLE 10-2: UBM CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
B7	DFC_09_PRSNT_N
B8	DFC_04_PERST_N
B9	DFC_06_IFDET2_N
B10	DFC_05_IFDET2_N
B11	DFC_11_IFDET2_N
B12	DFC_11_PWR_DISABLE
C1	DFC_03_IFDET2_N
C2	DFC_09_PERST_N
C3	DFC_05_PERST_N
C4	DFC_08_PERST_N
C5	DFC_10_PERST_N
C6	RSVD
C7	DFC_10_PRSNT_N
C8	DFC_07_LED_STA_N
C9	DFC_02_ACTIVITY_N
C10	DFC_10_ACTIVITY_N
C11	DFC_08_IFDET2_N
C12	DFC_08_PWR_DISABLE
D1	VCC
D2	DFC_00_PERST_N
D3	DFC_02_IFDET_N
D4	nRESET_IN
D5	DFC_00_IFDET2_N
D6	HFC_03_CHNG_DET_N
D7	HFC_01_SCL
D8	HFC_01_CHNG_DET_N
D9	DFC_08_IFDET_N
D10	DFC_11_ACTIVITY_N
D11	HFC_05_2WIRE_RESET
D12	HFC_04_2WIRE_RESET
E1	BMC_2WIRE_RESET
E2	DFC_11_PERST_N
E3	DFC_04_IFDET2_N
E4	DFC_03_ACTIVITY_N
E5	VCC
E6	VSS
E7	VCC
E8	VSS
E9	DFC_02_PERST_N
E10	DFC_09_ACTIVITY_N
E11	DFC_00_LED_ACT_N
E12	DFC_10_PWR_DISABLE
F1	VR_CAP

TABLE 10-2: UBM CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
F2	DFC_07_IFDET2_N
F3	DFC_07_ACTIVITY_N
F4	DFC_03_PERST_N
F5	VCC
F6	DFC_06_IFDET_N
F7	DFC_04_LED_STA_N
F8	VSS
F9	DFC_07_PRSNT_N
F10	nSTRAP_IN
F11	DFC_01_PERST_N
F12	DFC_06_LED_STA_N
G1	HFC_05_CHNG_DET_N
G2	VREF_ADC
G3	DFC_08_ACTIVITY_N
G4	DFC_09_PWR_DISABLE
G5	VSS
G6	VSS
G7	DFC_04_ACTIVITY_N
G8	VCC
G9	HEARTBEAT_PIN
G10	DFC_08_LED_STA_N
G11	DFC_03_LED_STA_N
G12	DFC_05_ACTIVITY_N
H1	CONFIG_PIN
H2	DFC_05_IFDET_N
H3	HFC_00_2WIRE_RESET
H4	DFC_01_LED_ACT_N
H5	HFC_01_2WIRE_RESET
H6	VCC
H7	VCC
H8	DFC_00_ACTIVITY_N
H9	DFC_09_LED_STA_N
H10	DFC_10_LED_STA_N
H11	DFC_11_LED_STA_N
H12	DFC_11_LED_ACT_N
J1	DFC_04_IFDET_N
J2	DFC_00_IFDET_N
J3	DFC_03_IFDET_N
J4	DFC_10_IFDET_N
J5	DFC_03_LED_ACT_N
J6	DFC_01_PWR_DISABLE
J7	HFC_02_2WIRE_RESET
J8	DFC_06_PWR_DISABLE

TABLE 10-2: UBM CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
J9	HFC_03_SCL
J10	HFC_05_SCL
J11	DFC_11_PRSNT_N
J12	HFC_03_SDA
K1	CONFIG_BPNUM_PIN
K2	DFC_00_PRSNT_N
K3	DFC_07_PERST_N
K4	DFC_02_LED_ACT_N
K5	HFC_03_2WIRE_RESET
K6	DFC_02_PWR_DISABLE
K7	DFC_06_LED_ACT_N
K8	DFC_07_LED_ACT_N
K9	DFC_09_LED_ACT_N
K10	DFC_08_LED_ACT_N
K11	HFC_00_CHNG_DET_N
K12	HFC_05_SDA
L1	DFC_01_PRSNT_N
L2	HFC_00_SDA
L3	DFC_06_PERST_N
L4	HFC_04_CHNG_DET_N
L5	DFC_00_PWR_DISABLE
L6	DFC_04_PWR_DISABLE
L7	DFC_05_LED_ACT_N
L8	DFC_04_PRSNT_N
L9	DFC_01_LED_STA_N
L10	HFC_02_CHNG_DET_N
L11	DFC_05_PRSNT_N
L12	DFC_10_LED_ACT_N
M1	DFC_09_IFDET_N
M2	DFC_02_PRSNT_N
M3	DFC_11_IFDET_N
M4	DFC_03_PRSNT_N
M5	DFC_08_PRSNT_N
M6	DFC_04_LED_ACT_N
M7	DFC_03_PWR_DISABLE
M8	DFC_00_LED_STA_N
M9	DFC_07_PWR_DISABLE
M10	DFC_01_ACTIVITY_N
M11	DFC_05_PWR_DISABLE
M12	DFC_06_PRSNT_N

TABLE 10-3: SGPIO CONTROLLER - 84 PIN PACKAGE

Ball Number	Function
A1	DFC_07_ACTIVITY_N
A2	DFC_00_IFDET_N
A3	DFC_05_LED_STA_N
A4	BMC_I2C_SDA
A5	BMC_I2C_SCL
A6	DFC_03_ACTIVITY_N
A7	DFC_00_PRSNT_N
A8	RSVD
A9	DFC_06_PWR_DISABLE
A10	DFC_05_PWR_DISABLE
B1	VCC
B2	nRESET_IN
B3	SGPIO_01_CLOCK
B4	SGPIO_00_CLOCK
B5	DFC_01_IFDET_N
B6	DFC_02_ACTIVITY_N
B7	NC
B8	DFC_07_LED_STA_N
B9	DFC_03_PWR_DISABLE
B10	DFC_07_IFDET_N
C1	SGPIO_00_LOAD
C2	SGPIO_00_DATAOUT
C5	DFC_02_PWR_DISABLE
C6	RSVD
C9	DFC_01_PWR_DISABLE
C10	DFC_02_IFDET_N
D1	VR_CAP
D2	SGPIO_01_LOAD
D4	VCC
D5	VCC
D6	VSS
D7	VSS
D9	DFC_06_LED_STA_N
D10	DFC_02_LED_STA_N
E1	CONFIG_PIN
E2	DFC_04_PWR_DISABLE
E3	BMC_2WIRE_RESET
E4	VCC
E7	VSS
E8	SGPIO_01_DATAOUT
E9	DFC_00_LED_ACT_N
E10	nSTRAP_IN
F1	VREF_ADC

TABLE 10-3: SGPIO CONTROLLER - 84 PIN PACKAGE (CONTINUED)

Ball Number	Function
F2	DFC_01_LED_ACT_N
F3	DFC_06_IFDET_N
F4	VSS
F7	VSS
F8	DFC_07_PRSNT_N
F9	DFC_00_PWR_DISABLE
F10	DFC_04_ACTIVITY_N
G1	DFC_04_IFDET_N
G2	DFC_05_ACTIVITY_N
G4	RSVD
G5	VCC
G6	VCC
G7	VCC
G9	DFC_04_LED_STA_N
G10	DFC_03_LED_STA_N
H1	DFC_05_IFDET_N
H2	SPARE
H5	DFC_03_LED_ACT_N
H6	DFC_01_ACTIVITY_N
H9	DFC_00_ACTIVITY_N
H10	DFC_07_PWR_DISABLE
J1	DFC_03_IFDET_N
J2	CONFIG_BPNUM_PIN
J3	SGPIO_01_DATAIN
J4	DFC_02_PRSNT_N
J5	DFC_04_LED_ACT_N
J6	DFC_04_PRSNT_N
J7	DFC_00_LED_STA_N
J8	DFC_06_PRSNT_N
J9	SGPIO_00_DATAIN
J10	SGPIO_00_CTRL_TYPE
K1	DFC_06_ACTIVITY_N
K2	DFC_01_PRSNT_N
K3	DFC_02_LED_ACT_N
K4	DFC_03_PRSNT_N
K5	DFC_06_LED_ACT_N
K6	DFC_07_LED_ACT_N
K7	DFC_05_LED_ACT_N
K8	DFC_01_LED_STA_N
K9	SGPIO_01_CTRL_TYPE
K10	DFC_05_PRSNT_N

TABLE 10-4: UBM CONTROLLER - 84 PIN PACKAGE

Ball Number	Function
A1	DFC_00_PERST_N
A2	DFC_02_IFDET_N
A3	DFC_05_LED_STA_N
A4	BMC_I2C_SDA
A5	BMC_I2C_SCL
A6	HFC_04_SCL
A7	HFC_02_SCL
A8	DFC_05_ACTIVITY_N
A9	HFC_01_SDA
A10	HFC_01_SCL
B1	VCC
B2	nRESET_IN
B3	DFC_05_PERST_N
B4	HFC_00_SCL
B5	DFC_01_IFDET_N
B6	HFC_04_SDA
B7	HFC_02_SDA
B8	DFC_07_LED_STA_N
B9	DFC_04_PERST_N
B10	DFC_07_IFDET_N
C1	HFC_00_SDA
C2	DFC_03_ACTIVITY_N/HFC_03_2WIRE_RESET
C5	HFC_03_CHNG_DET_N
C6	DFC_06_ACTIVITY_N
C9	HFC_01_CHNG_DET_N
C10	DFC_02_ACTIVITY_N/HFC_02_2WIRE_RESET
D1	VR_CAP
D2	DFC_03_PERST_N
D4	VCC
D5	VCC
D6	VSS
D7	VSS
D9	DFC_06_LED_STA_N
D10	DFC_02_LED_STA_N
E1	CONFIG_PIN
E2	DFC_07_ACTIVITY_N
E3	BMC_2WIRE_RESET
E4	VCC
E7	VSS
E8	DFC_02_PERST_N
E9	DFC_00_LED_ACT_N
E10	nSTRAP_IN
F1	VREF_ADC

TABLE 10-4: UBM CONTROLLER - 84 PIN PACKAGE (CONTINUED)

Ball Number	Function
F2	DFC_01_LED_ACT_N
F3	DFC_06_IFDET_N
F4	VSS
F7	VSS
F8	DFC_07_PRSNT_N
F9	DFC_01_PERST_N
F10	DFC_04_ACTIVITY_N/HFC_04_2WIRE_RESET
G1	DFC_04_IFDET_N
G2	DFC_07_PERST_N
G4	DFC_07_PRSNT_N
G5	VCC
G6	VCC
G7	VCC
G9	DFC_04_LED_STA_N
G10	DFC_03_LED_STA_N
H1	DFC_05_IFDET_N
H2	DFC_00_IFDET_N
H5	DFC_03_LED_ACT_N
H6	DFC_01_ACTIVITY_N/HFC_01_2WIRE_RESET
H9	DFC_00_ACTIVITY_N/HFC_00_2WIRE_RESET
H10	HFC_03_SCL
J1	DFC_03_IFDET_N
J2	CONFIG_BPNUM_PIN
J3	HFC_04_CHNG_DET_N
J4	DFC_02_PRSNT_N
J5	DFC_04_LED_ACT_N
J6	DFC_04_PRSNT_N
J7	DFC_00_LED_STA_N
J8	DFC_06_PRSNT_N
J9	HFC_00_CHNG_DET_N
J10	HFC_03_SDA
K1	DFC_06_PERST_N
K2	DFC_01_PRSNT_N
K3	DFC_02_LED_ACT_N
K4	DFC_03_PRSNT_N
K5	DFC_06_LED_ACT_N
K6	DFC_07_LED_ACT_N
K7	DFC_05_LED_ACT_N
K8	DFC_01_LED_STA_N
K9	HFC_02_CHNG_DET_N
K10	DFC_05_PRSNT_N

TABLE 10-5: UBM_SGPIO CONTROLLER - 144 PIN PACKAGE

Ball Number	Function
A1	DFC_02_IFDET2_N
A2	BMC_I2C_SDA
A3	BMC_I2C_SCL
A4	NC
A5	NC
A6	RSVD
A7	HFC_02_SDA
A8	DFC_06_ACTIVITY_N
A9	DFC_07_IFDET_N
A10	NC
A11	DFC_05_PERST_N
A12	DFC_02_LED_STA_N
B1	DFC_01_IFDET2_N
B2	SGPIO_00_CLOCK/HFC_00_SCL
B3	DFC_05_LED_STA_N
B4	DFC_01_IFDET_N
B5	HFC_03_SCL
B6	HFC_03_SDA
B7	DFC_03_PERST_N
B8	DFC_04_PERST_N
B9	DFC_06_IFDET2_N
B10	DFC_05_IFDET2_N
B11	HFC_04_SDA
B12	HFC_00_CHNG_DET_N
C1	DFC_03_IFDET2_N
C2	NC
C3	SGPIO_01_CLOCK
C4	NC
C5	NC
C6	RSVD
C7	NC
C8	DFC_07_LED_STA_N
C9	DFC_02_ACTIVITY_N
C10	HFC_01_SCL
C11	DFC_03_ACTIVITY_N
C12	HFC_01_CHNG_DET_N
D1	VCC
D2	DFC_00_PERST_N
D3	DFC_02_IFDET_N
D4	nRESET_IN
D5	DFC_00_IFDET2_N
D6	HFC_04_CHNG_DET_N
D7	HFC_02_SCL

TABLE 10-5: UBM_SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
D8	HFC_02_CHNG_DET_N
D9	HFC_04_SCL
D10	HFC_01_SDA
D11	NC
D12	HFC_00_2WIRE_RESET
E1	BMC_2WIRE_RESET
E2	NC
E3	DFC_04_IFDET2_N
E4	SGPIO_00_DATAOUT
E5	VCC
E6	VSS
E7	VCC
E8	VSS
E9	SGPIO_01_DATAOUT
E10	HFC_03_CHNG_DET_N
E11	DFC_00_LED_ACT_N
E12	NC
F1	VR_CAP
F2	DFC_07_IFDET2_N
F3	DFC_07_ACTIVITY_N
F4	SGPIO_01_LOAD
F5	VCC
F6	DFC_06_IFDET_N
F7	DFC_04_LED_STA_N
F8	VSS
F9	DFC_07_PRSNT_N
F10	nSTRAP_IN
F11	DFC_01_PERST_N
F12	DFC_06_LED_STA_N
G1	NC
G2	VREF_ADC
G3	NC
G4	NC
G5	VSS
G6	VSS
G7	DFC_04_ACTIVITY_N
G8	VCC
G9	HEARTBEAT_PIN
G10	NC
G11	DFC_03_LED_STA_N
G12	DFC_05_ACTIVITY_N
H1	CONFIG_PIN
H2	DFC_05_IFDET_N

TABLE 10-5: UBM_SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
H3	HFC_01_2WIRE_RESET
H4	DFC_01_LED_ACT_N
H5	HFC_02_2WIRE_RESET
H6	VCC
H7	VCC
H8	DFC_00_ACTIVITY_N
H9	NC
H10	NC
H11	NC
H12	NC
J1	DFC_04_IFDET_N
J2	DFC_00_IFDET_N
J3	DFC_03_IFDET_N
J4	NC
J5	DFC_03_LED_ACT_N
J6	DFC_01_PWR_DISABLE
J7	HFC_03_2WIRE_RESET
J8	DFC_06_PWR_DISABLE
J9	NC
J10	NC
J11	NC
J12	SGPIO_00_CTRL_TYPE
K1	CONFIG_BPNUM_PIN
K2	DFC_00_PRSNT_N
K3	DFC_07_PERST_N
K4	DFC_02_LED_ACT_N
K5	HFC_04_2WIRE_RESET
K6	DFC_02_PWR_DISABLE
K7	DFC_06_LED_ACT_N
K8	DFC_07_LED_ACT_N
K9	NC
K10	NC
K11	SGPIO_00_DATAIN
K12	NC
L1	DFC_01_PRSNT_N
L2	SGPIO_00_LOAD/HFC_00_SDA
L3	DFC_06_PERST_N
L4	SGPIO_01_DATAIN
L5	DFC_00_PWR_DISABLE
L6	DFC_04_PWR_DISABLE
L7	DFC_05_LED_ACT_N
L8	DFC_04_PRSNT_N
L9	DFC_01_LED_STA_N

TABLE 10-5: UBM_SGPIO CONTROLLER - 144 PIN PACKAGE (CONTINUED)

Ball Number	Function
L10	SGPIO_01_CTRL_TYPE
L11	DFC_05_PRSNT_N
L12	NC
M1	DFC_02_PERST_N
M2	DFC_02_PRSNT_N
M3	NC
M4	DFC_03_PRSNT_N
M5	NC
M6	DFC_04_LED_ACT_N
M7	DFC_03_PWR_DISABLE
M8	DFC_00_LED_STA_N
M9	DFC_07_PWR_DISABLE
M10	DFC_01_ACTIVITY_N
M11	DFC_05_PWR_DISABLE
M12	DFC_06_PRSNT_N

11.0 ELECTRICAL SPECIFICATIONS

11.1 Maximum Ratings*

*Stresses exceeding those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note:	When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

11.1.1 ABSOLUTE MAXIMUM THERMAL RATINGS

Parameter	Maximum Limits
Operating Temperature Range	-40°C to +85°C Industrial
Storage Temperature Range	-55° to +150°C
Lead Temperature Range	Refer to JEDEC Spec J-STD-020B

11.1.2 ABSOLUTE MAXIMUM SUPPLY VOLTAGE RATINGS

Symbol	Parameter	Maximum Limits
VCC	3.3V Power Supply with respect to ground	-0.3V to +3.63V

11.1.3 ABSOLUTE MAXIMUM I/O VOLTAGE RATINGS

Parameter	Maximum Limits
Voltage on any Digital Pin with respect to ground	Determined by Power Supply of I/O Buffer and Pad Type

11.2 Operational Specifications

11.2.1 POWER SUPPLY OPERATIONAL CHARACTERISTICS

TABLE 11-1: POWER SUPPLY OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	Units
VCC	3.3V Power Supply	3.135	3.3	3.465	V

11.2.2 CAPACITIVE LOADING SPECIFICATIONS

The following table defines the maximum capacitive load validated for the buffer characteristics listed in Table 11-4, "DC Electrical Characteristics".

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{cc} = 3.3 VDC

Note:	All output pins, except pin under test, tied to AC ground.

TABLE 11-2: MAXIMUM CAPACITIVE LOADING

Parameter	Symbol	Limits			Unit	Notes
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	Note 1
Output Capacitance	C_{OUT}			20	pF	Note 2

Note 1: All input buffers can be characterized by this capacitance unless otherwise specified.

2: All output buffers can be characterized by this capacitance unless otherwise specified.

11.2.3 DC ELECTRICAL CHARACTERISTICS FOR I/O BUFFERS

TABLE 11-3: BUFFER TYPE

Signal Name	Buffer Type
DFC_xx_ACTIVITY_N	I
DFC_xx_IFDET_N	I
DFC_xx_IFDET2_N	I
DFC_xx_PRSNT_N	I
HFC_xx_2WIRE_RESET	I
DFC_xx_LED_ACT_N	OD-2mA
DFC_xx_LED_STA_N	OD-2mA
DFC_xx_PERST_N	OD-2mA
DFC_xx_CHNG_DET_N	OD-2mA
DFC_xx_PWR_DISABLE_N	PIO
CONFIG_PIN	I_AN
CONFIG_BPNUM_PIN	I_AN

Note: xx is the instance/port number

TABLE 11-4: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
PIO Type Buffer						
All PIO Buffers Pull-up Resistor @3.3V	R_{PU}	34	52	95	KΩ	Internal PU selected via the GPIO Pin Control Register.
All PIO Buffers Pull-down Resistor @3.3V	R_{PD}	38	63	127	KΩ	Internal PD selected via the GPIO Pin Control Register.
PIO	V_{OL}			0.4	V	I_{OL} = 4 mA (min)
	V_{OH}	VCC-0.4			V	I_{OH} = -4 mA (min)
OD-2mA						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 2mA (min)
I Type Input Buffer						TTL Compatible Schmitt Trigger Input
Low Input Level	V_{ILI}			0.3x VCC	V	
High Input Level	V_{IHI}		0.7x VCC		V	
Schmitt Trigger Hysteresis	V_{HYS}		400		mV	
I_AN Type Buffer						
I_AN Type Buffer (Analog Input Buffer)	I_AN	Voltage range on pins: -0.3V to +3.63V				These buffers are not 5V tolerant buffers and they are not back-drive protected
ADC Reference Pins						
VREF_ADC						
Voltage (Option A)	V		VCC		V	Connect to same power supply as VCC
Voltage (Option B)	V	2.97	3.0	3.03	V	
Input Impedance	R_{REF}		75		KΩ	
Input Low Current	ILEAK	-0.05		+0.05	µA	This buffer is not 5V tolerant This buffer is not backdrive protected.

11.2.3.1 Pin Leakage

Leakage characteristics for all digital I/O pins is shown in the following Pin Leakage table, unless otherwise specified. Two exceptions are pins with Over-voltage protection and Backdrive protection (**10.2 "Pin List"**). Leakage characteristics for Over-Voltage protected pins and Backdrive protected pins are shown in the two sub-sections following the Pin Leakage table.

TABLE 11-5: PIN LEAKAGE (VCC=3.3V + 5%; VCC = 1.8V +5%)

(T_A = -40°C to +85°C)						
Leakage Current	I_{IL}			+/-2	µA	VIN=0V to VCC

11.2.4 ADC ELECTRICAL CHARACTERISTICS

TABLE 11-6: ADC CHARACTERISTICS

Symbol	Parameter	MIN	TYP	MAX	Units	Comments
VCC	Analog Supply Voltage	3.135	3.3	3.465	V	
V_{RNG}	Input Voltage Range	0		VREF_ADC	V	Range of VREF_ADC input to ADC ground
RES	Resolution	–	–	10/12	Bits	Guaranteed Monotonic
ACC	Absolute Accuracy	–	2	4	LSB	
DNL	Differential Non Linearity, DNL	-1	–	+1	LSB	Guaranteed Monotonic
INL	Integral Non Linearity, INL	-3.0	–	+3	LSB	Guaranteed Monotonic
E_{GAIN}	Gain Error, E_{GAIN}	-2	–	2	LSB	
E_{OFFSET}	Offset Error, E_{OFFSET}	-2	–	2	LSB	
CONV	Conversion Time		1.125		µS/channel	
II	Input Impedance	4	4.5	5.3	MΩ	

11.2.5 THERMAL CHARACTERISTICS

TABLE 11-7: THERMAL OPERATING CONDITIONS

Rating	Symbol	MIN	TYP	MAX	Unit
Consumer Temperature Devices					
Operating Junction Temperature Range	T_J	0	—	125	°C
Operating Ambient Temperature Range - Industrial	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - S\ I_{OH})$ I/O Pin Power Dissipation: $I/O = S\ (\{V_{DD} - V_{OH}\} \times I_{OH}) + S\ (V_{OL} \times I_{OL})$	P_D	69.3 (P_{INT} + $P_{I/O}$)			mW
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J{}^a - T_A)/\theta_{JA}$			W

a. Tj Max value is at ambient of 70°C

11.3 Power Consumption

TABLE 11-9: VCC SUPPLY CURRENT, I_VCC

48 MHz Clock	Typical (3.3V, 25C)	Max (3.45V, 70C)	Max (3.45V, 85C)	Unit	Comments
48MHz	9.41	13.79	15.8	mA	Full On

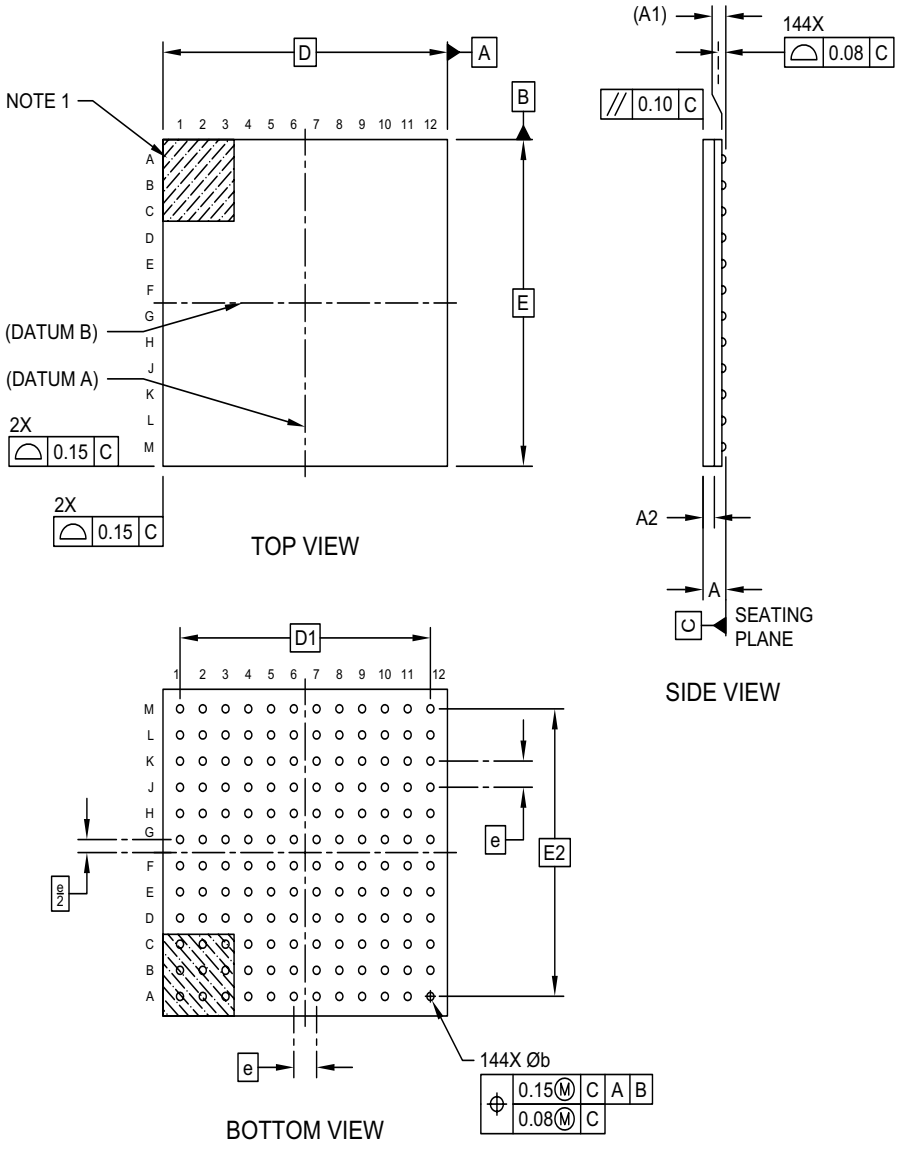
12.0 PACKAGE INFORMATION

12.1 144 Pin WFBGA/WC Package

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

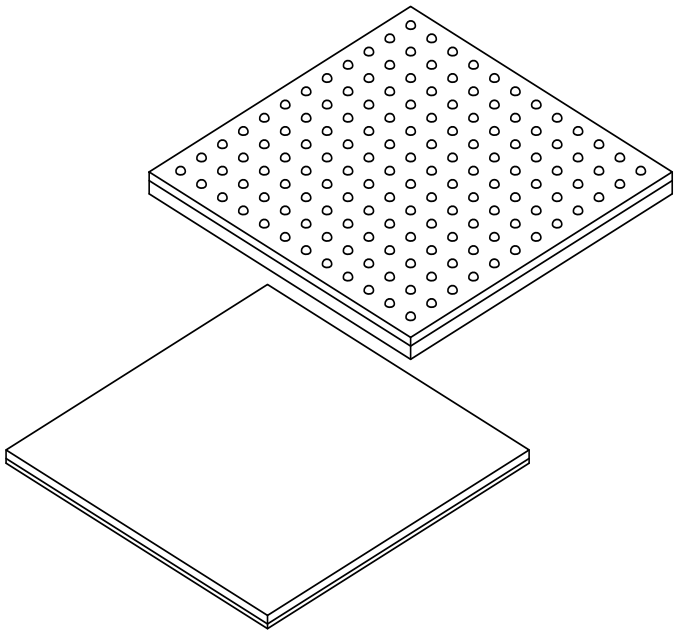
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-416A Sheet 1 of 2

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		144	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	0.80
Standoff	A1		0.17 REF	
Mold Package Thickness	A2	0.35	0.40	0.45
Overall Length	D		10.00 BSC	
Exposed Pad Length	D1		8.80 BSC	
Overall Width	E		10.00 BSC	
Exposed Pad Width	E1		8.80 BSC	
Terminal Diameter	b	0.20	0.25	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

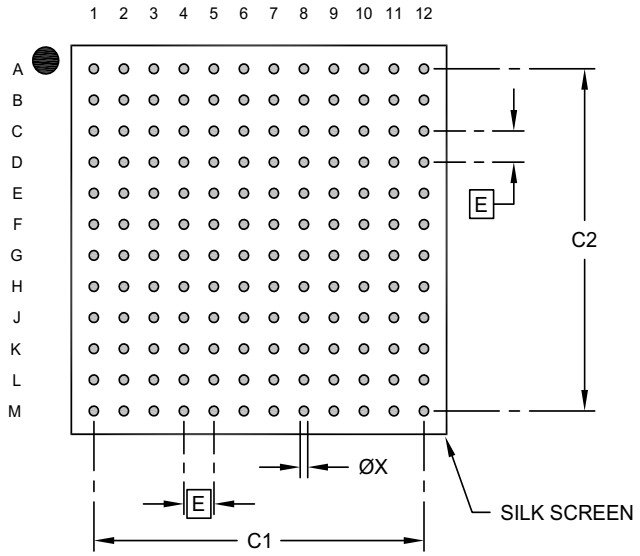
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-416A Sheet 2 of 2

144-Ball Very, Very Thin Fine Pitch Ball Grid Array (WCX) - 10x10 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		8.80	
Contact Pad Spacing	C2		8.80	
Contact Pad Width (X20)	X		0.25	

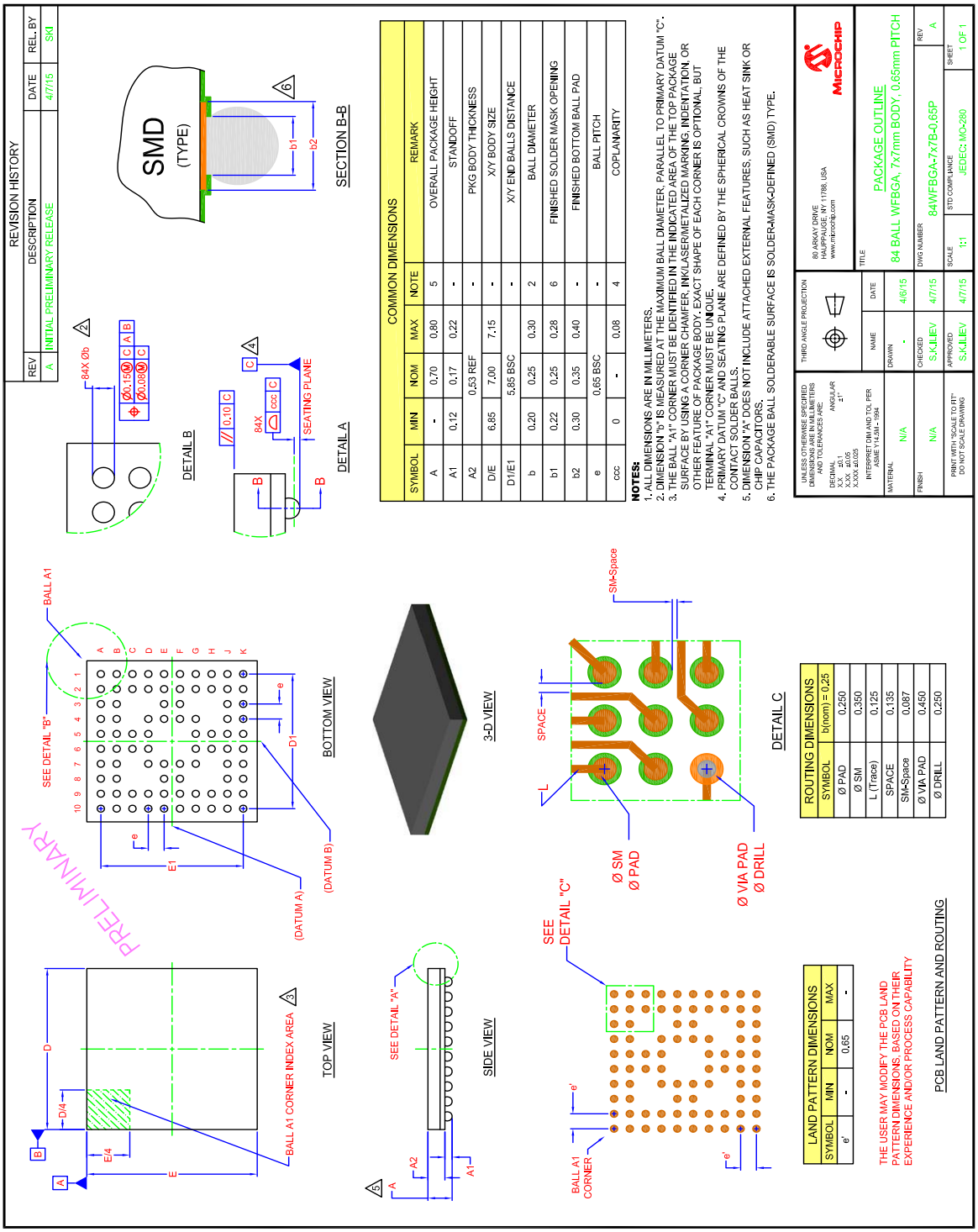
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2416A

12.2 84 Pin WFBGA/SX1 Package

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003392B (05-06-20)	Section 7.6, "Capabilities (0x33)"	Register bits "2-Wire Reset" updated to 02h.
	Section 11.0, "Electrical Specifications"	Chapter added
DS00003392A (02-26-20)	Initial document	

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PRODUCT IDENTIFICATION SYSTEM

Not all of the possible combinations of Device, Temperature Range and Package may be offered for sale. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.[1]	-	X	-	XX	-	X/XXX[2]	-	[X][3]
Device		Total SRAM		Version/ Revision		Temp Range/ Package		Tape and Reel Option

Device:	EEC1005[1]	UBM Controller
Total SRAM:	H	256KB
Version/ Revision:	B#	B = Version, # = Version Revision Number
Temperature Range:	I/	= -40°C to +85°C (Industrial)
Package:	WC	144 pin WFBGA 10x10mm body, 0.80mm pitch
	SX1	84 pin WFBGA 7x7mm body, 0.65mm pitch
Tape and Reel Option:	Blank	= Tray packaging
	TR	= Tape and Reel[3]

Example:

a) EEC1005-I/WC = EEC1005 with 12-drive UBM solution provided with FW

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html

3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option

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ISBN: 9781522458968

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