Description

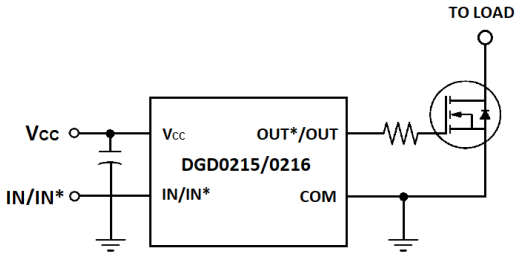
The DIODES™ DGD0215 and DIODES™ DGD0216 high speed / low side MOSFET and IGBT drivers are capable of driving 1.9A of peak current. The DGD0215 and DGD0216 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. Fast and well matched propagation delays allow high speed operation, enabling a smaller and more compact power switching design using smaller associated components.

The DGD0215 and DGD0216 are highly resistant to noise, and are able to withstand up to 5V positive or negative on the ground pin without damage. The devices can also withstand 500mA of reverse current forced back into the outputs without damage or logic change. The DGD0215 provides an inverted output and the DGD0216 provides a non-inverting ouput.

The DGD0215 and DGD0216 are offered in TSOT25 (Standard) package and the operating temperature extends from -40°C to +125°C.

Applications

- DC-DC converters
- Line drivers
- Motor controls
- Switch mode power supplies



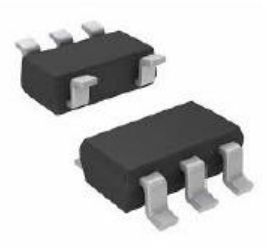
Typical Configuration

Features

- Efficient Low Cost Solution for Driving MOSFETs and IGBTs
- Wide Supply Voltage Operating Range: 4.5V to 18V
- 1.9A Source / 1.8A Sink Output Current Capability
- Inverting and Non-Inverting Input Configurations
- Fast Propagation Delay (35ns typ)
- Fast Rise and Fall Times (15ns typ)
- Logic Input (IN and IN*) 3.3V Capability
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Mechanical Data

- Package: TSOT25
- Package Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.012 grams (Approximate)



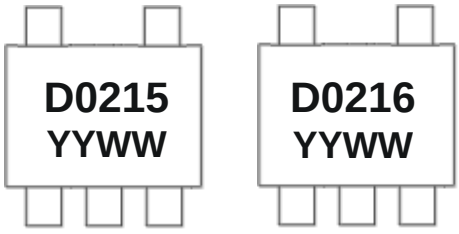
TSOT25 (Standard)

Ordering Information (Note 4)

Part Number	Package	Marking	Reel Size (inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
DGD0215WT-7	TSOT25 (Standard)	D0215	7	8	3,000	Reel
DGD0216WT-7	TSOT25 (Standard)	D0216	7	8	3,000	Reel

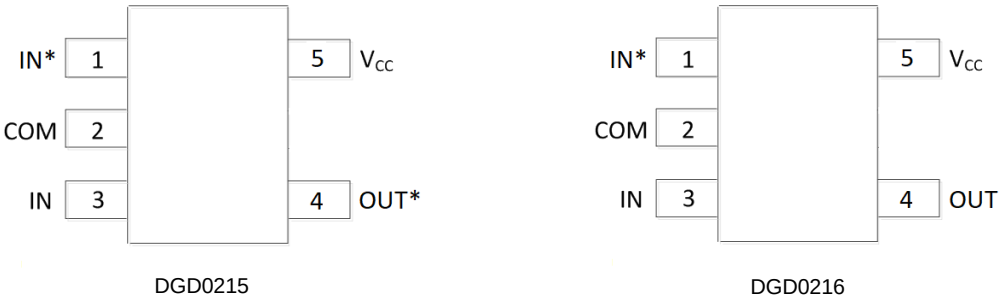
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



D0215/D0216 = Product Type Marking Code
YY = Year (ex: 22 = 2022)
WW = Week (01 to 53)

Pin Diagrams

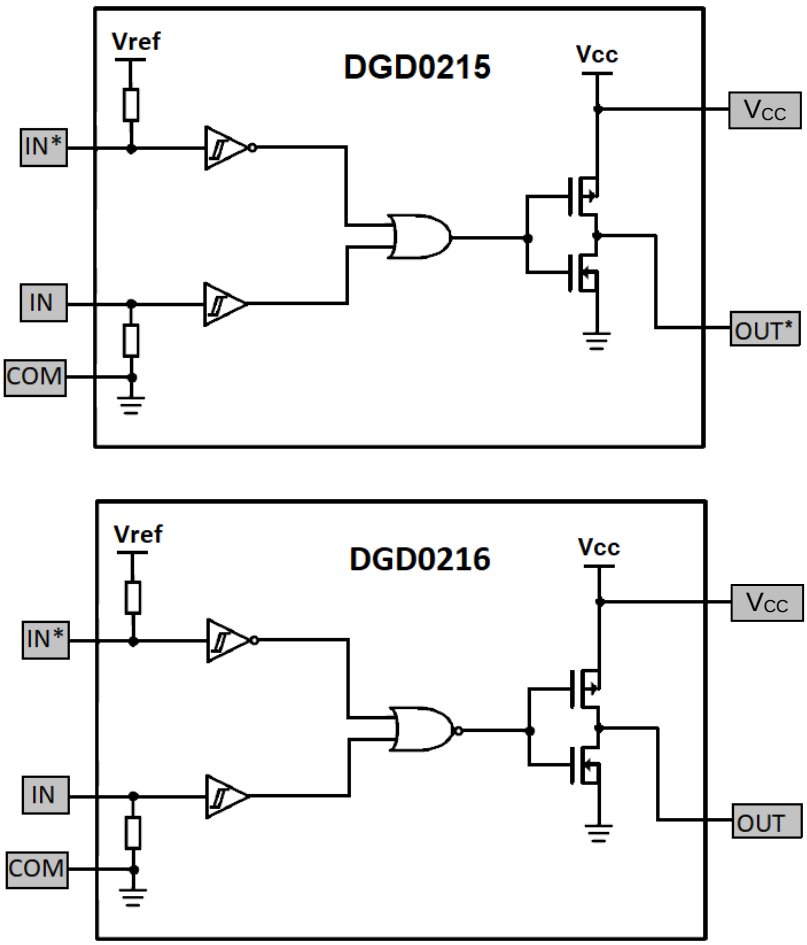


Top View: TSOT25 (Standard)

Pin Descriptions

Pin Number	Pin Name	Function
1	IN*	Logic Input, In Phase with OUT* (DGD0215), Out of Phase with OUT (DGD0216), leave open when not in use.
2	COM	Supply Return
3	IN	Logic Input, Out of Phase with OUT* (DGD0215), In Phase with OUT (DGD0216), leave open when not in use.
4	OUT*/OUT	Gate Drive Output
5	V_{CC}	Supply Input

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Low-Side Fixed Supply Voltage	V_{CC}	-0.3 to 22	V
Output Voltage (OUT/OUT*)	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Logic Input Voltage (IN and IN*)	V_{IN}	-5 to V_{CC} + 0.3	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P_D	0.54	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	188	°C/W
Operating Temperature	T_J	+150	°C
Lead Temperature (Soldering, 10s)	T_L	+300	
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

ESD Ratings (Note 6)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	2,000	V	2

Note: 6. Refer to JEDEC specification JESD22-A114.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_B	4.5	18	V
Output Voltage (OUT/OUT*)	V_S	0	V_{CC}	V
Logic Input Voltage (IN and IN*)	V_{IN}	0	5	V
Ambient Temperature	T_A	-40	+125	°C

DC Electrical Characteristics (V_{BIAS} (4.5V < V_{CC} < 18V), @T_A = +25°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic “1” Input Voltage	V_{IH}	2.4	1.6	—	V	—
Logic “0” Input Voltage	V_{IL}	—	1.3	0.8	V	—
Logic “1” Input Bias Current	I_{IN+}	—	—	5	µA	V_{IN} = 3V, V_{IN*} = 0V
Logic “0” Input Bias Current	I_{IN-}	—	—	2	µA	V_{IN} = 0V, V_{IN*} = 3V
High Level Output Voltage, V_{BIAS} - V_O	V_{OH}	—	25	—	mV	—
Low Level Output Voltage	V_{OL}	—	25	—	mV	—
Quiescent V_{CC} Supply Current	I_{CCQ}	—	50	100	µA	V_{IN} = 0V or 3V
Output High Short Circuit Pulsed Current	I_{O+}	—	1.9	—	A	V_{CC} = 12V
Output Low Short Circuit Pulsed Current	I_{O-}	—	1.8	—	A	V_{CC} = 12V
Output Resistance, High	R_{OH}	—	3.3	—	Ω	I_{OUT} = 10mA, V_{CC} = 12V
Output Resistance, Low	R_{OL}	—	2.3	—	Ω	I_{OUT} = 10mA, V_{CC} = 12V

AC Electrical Characteristics (V_{BIAS} (4.5V < V_{CC} < 18V), @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Rise Time	t_r	—	15	25	ns	C_L = 1000pF, V_{CC} = 12V
Turn-Off Fall Time	t_f	—	15	25	ns	C_L = 1000pF, V_{CC} = 12V
Turn-On Propagation Delay	t_{ON}	—	35	50	ns	V_{CC} = 12V
Turn-Off Propagation Delay	t_{OFF}	—	35	55	ns	V_{CC} = 12V

DC Electrical Characteristics (V_{BIAS} (4.5V < V_{CC} < 18V), @T_C = -40°C to +125°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic “1” Input Voltage	V_{IH}	2.4	—	—	V	—
Logic “0” Input Voltage	V_{IL}	—	—	0.8	V	—
Logic “1” Input Bias Current	I_{IN+}	—	—	10	µA	V_{IN} = 3V
Logic “0” Input Bias Current	I_{IN-}	—	0	5	µA	V_{IN} = 0V
High Level Output Voltage, V_{BIAS} - V_O	V_{OH}	—	25	—	mV	—
Low Level Output Voltage	V_{OL}	—	25	—	mV	—
Quiescent V_{CC} Supply Current	I_{CCQ}	—	0.1	0.2	mA	V_{IN} = 0V or 3V
Output Resistance, High	R_{OH}	—	—	10	Ω	I_{OUT} = 10mA, V_{CC} = 12V
Output Resistance, Low	R_{OL}	—	—	7	Ω	I_{OUT} = 10mA, V_{CC} = 12V

Note: 7. The V_{IN} and I_{IN} parameters are applicable to the logic input pins: IN and IN*. The V_O and I_O parameters are applicable to the output pins: OUT and OUT*.

AC Electrical Characteristics (V_{BIAS} (4.5V < V_{CC} < 18V), @T_C = -40°C to +125°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Rise Time	t_r	—	30	40	ns	C_L = 1000pF, V_{CC} = 12V
Turn-Off Fall Time	t_f	—	30	40	ns	C_L = 1000pF, V_{CC} = 12V
Turn-On Propagation Delay	t_{ON}	—	45	55	ns	V_{CC} = 12V
Turn-Off Propagation Delay	t_{OFF}	—	50	60	ns	V_{CC} = 12V

Timing Waveforms

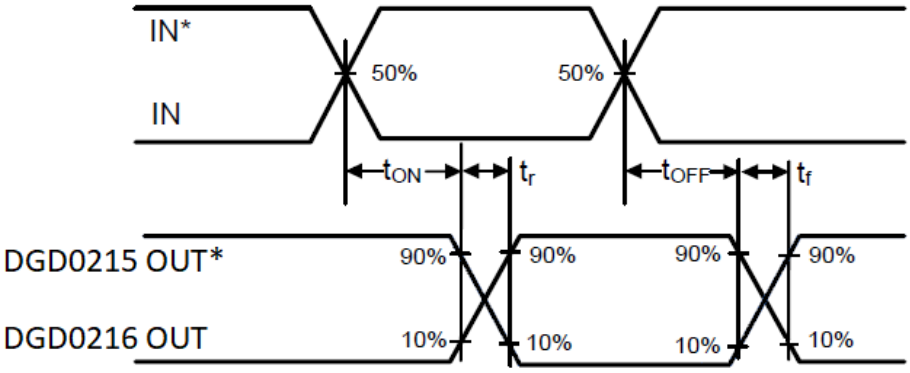


Figure 1. Switching Time Waveform Definitions

Input/Output Response Table

IN	IN*	DGD0215 (OUT*)	DGD0216 (OUT)
H	H (Open)	L	H
L	H (Open)	H	L
L (Open)	H	H	L
L (Open)	L	L	H

Typical Performance Characteristics (V_{CC} = 12V, @T_A = +25°C, unless otherwise specified.)

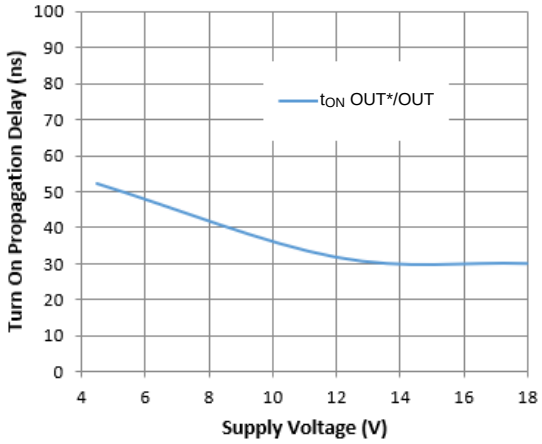


Figure 2. Turn-on Propagation Delay vs. Supply Voltage

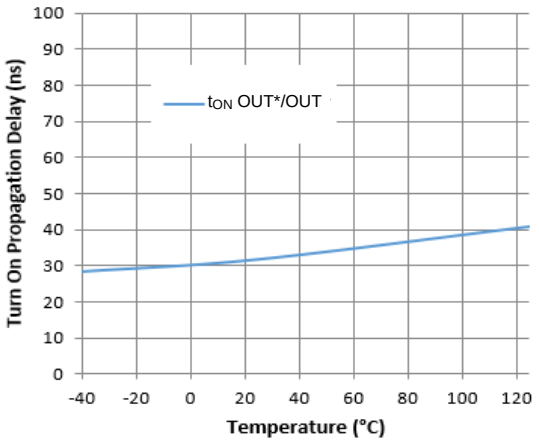


Figure 3. Turn-on Propagation Delay vs. Temperature

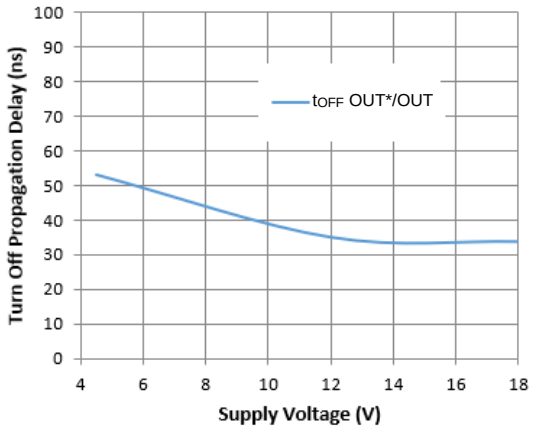


Figure 4. Turn-off Propagation Delay vs. Supply Voltage

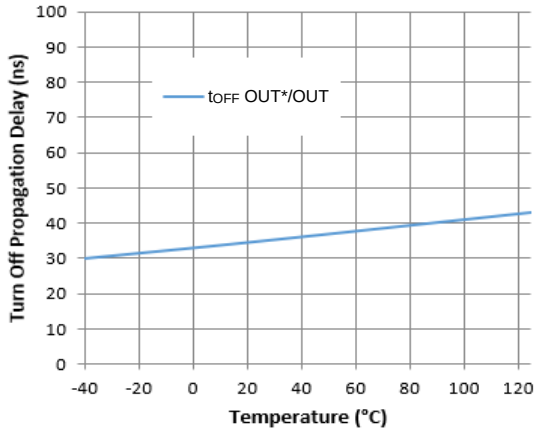


Figure 5. Turn-off Propagation Delay vs. Temperature

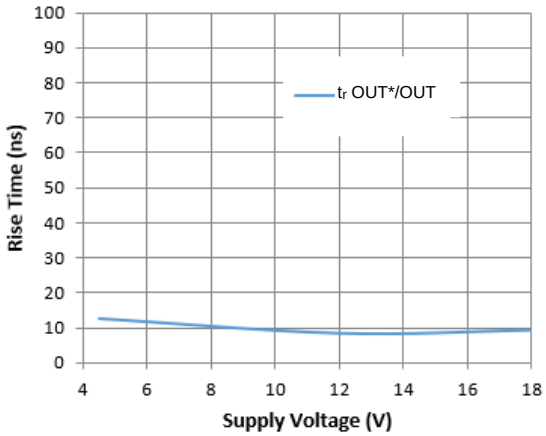


Figure 6. Rise Time vs. Supply Voltage

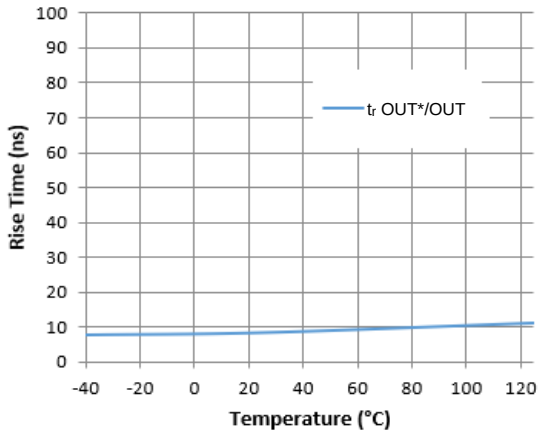


Figure 7. Rise Time vs. Temperature

Typical Performance Characteristics (continued)

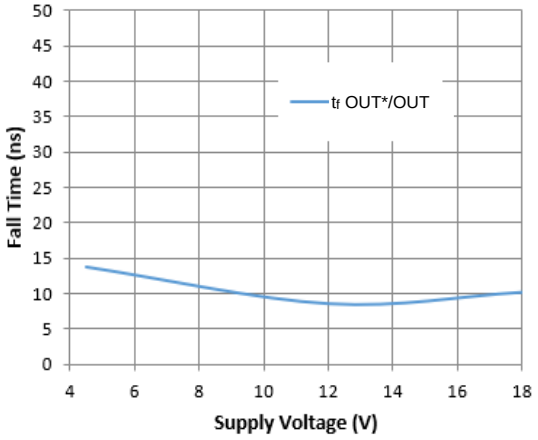


Figure 8. Fall Time vs. Supply Voltage

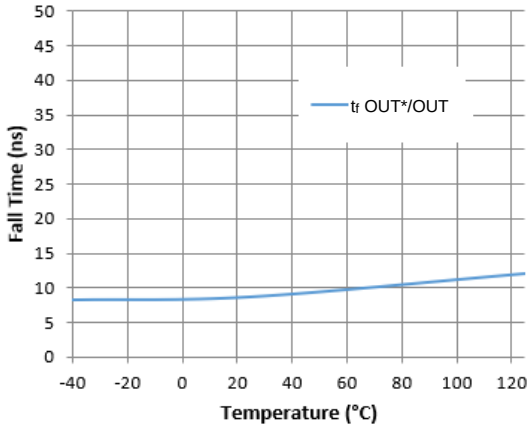


Figure 9. Fall Time vs. Temperature

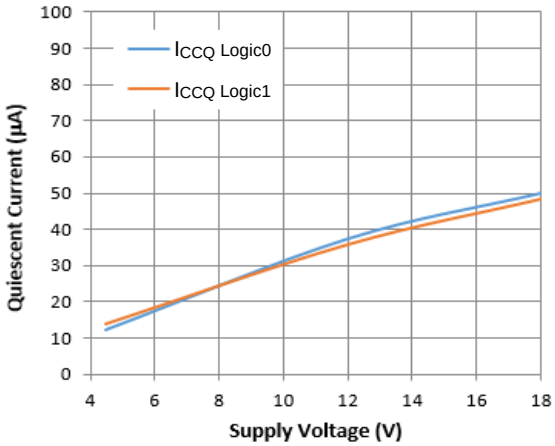


Figure 10. Quiescent Current vs. Supply Voltage

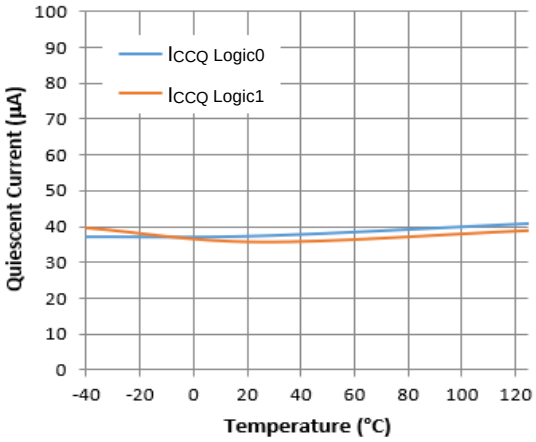


Figure 11. Quiescent Current vs. Temperature

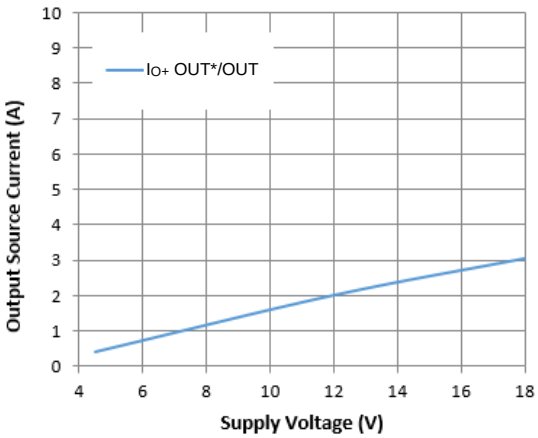


Figure 12. Output Source Current vs. Supply Voltage

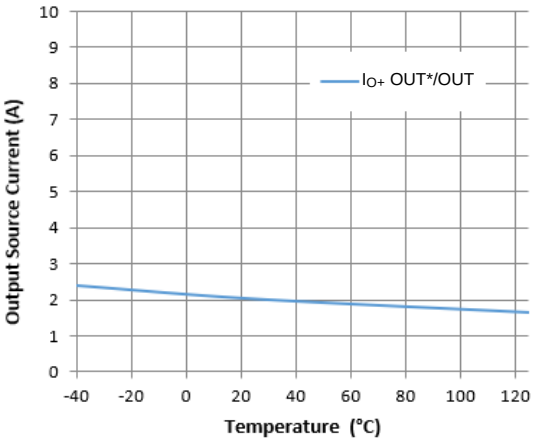


Figure 13. Output Source Current vs. Temperature

Typical Performance Characteristics (continued)

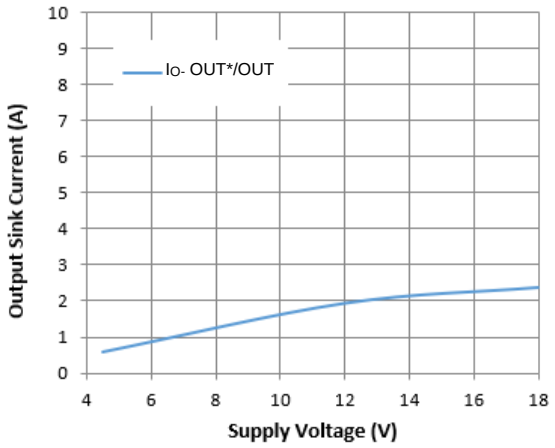


Figure 14. Output Sink Current vs. Supply Voltage

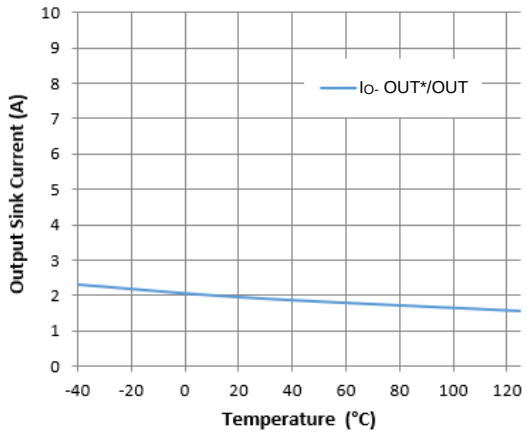


Figure 15. Output Sink Current vs. Temperature

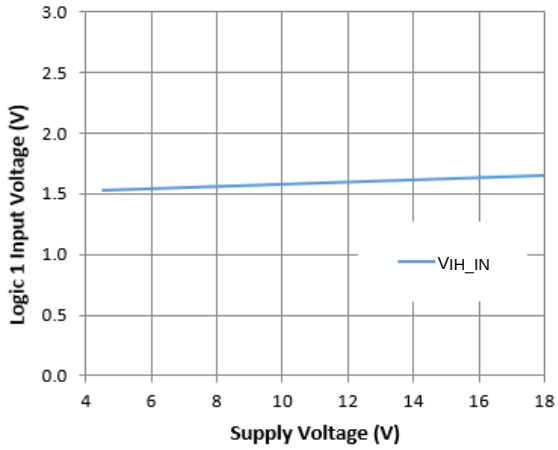


Figure 16. Logic 1 Input Voltage vs. Supply Voltage

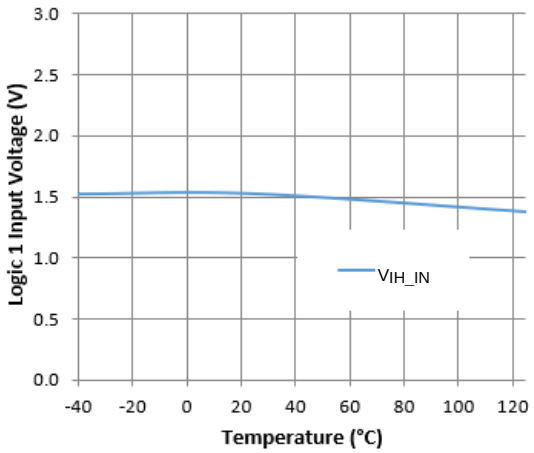


Figure 17. Logic 1 Input Voltage vs. Temperature

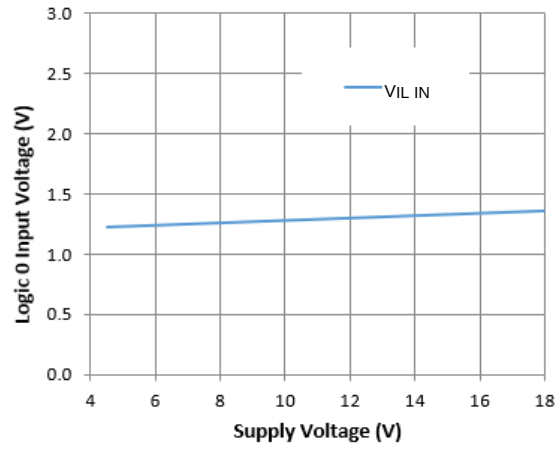


Figure 18. Logic 0 Input Voltage vs. Supply Voltage

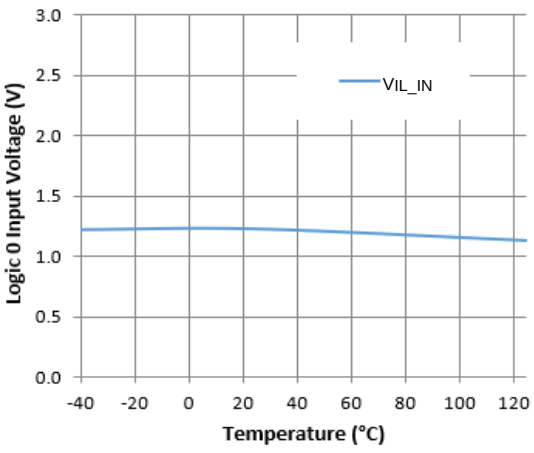


Figure 19. Logic 0 Input Voltage vs. Temperature

PCB Layout Information

The DGD0215 and DGD0216 High Speed, Low-Side, single Gate Drivers demand a fast switching current through V_{CC}, and in the power switching circuit a much larger current will be switched through the MOSFET. Typical applications are PFC or boost converter. Particular consideration for layout is key to ensuring optimal operation of the Gate Driver IC as well as to minimizing ringing and noise on the power line (VBUS) and ground. Figure 20 shows an example layout of the DGD0216 in the Low-Side power switching of a PFC circuit. Figure 21 shows the schematic of the layout shown in Figure 20, followed by a description of layout considerations for the DGD0215 and DGD0216.

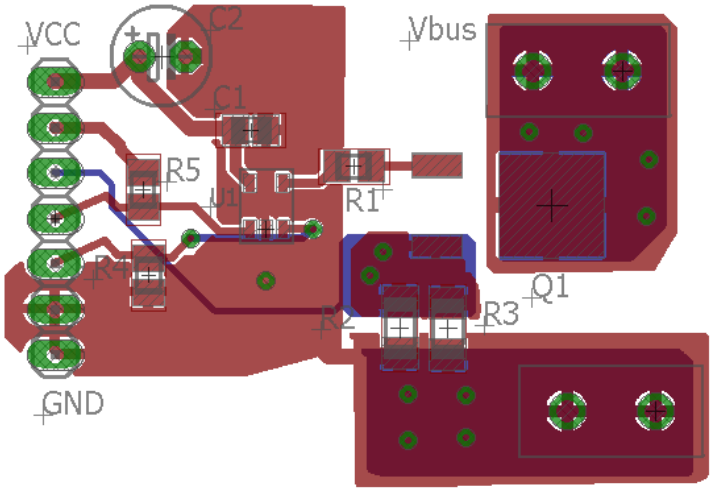


Figure 20. Example Layout of DGD0216 Driving a Low-Side MOSFET (For Example PFC Circuit)

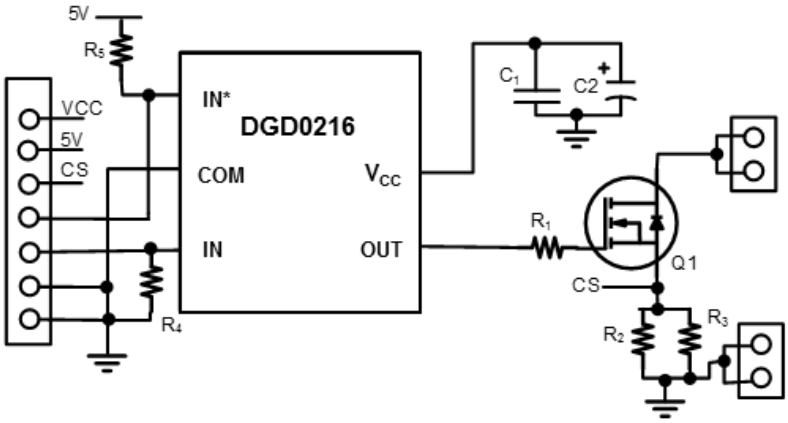


Figure 21. Schematic for Layout Example Circuit Shown in Figure 20

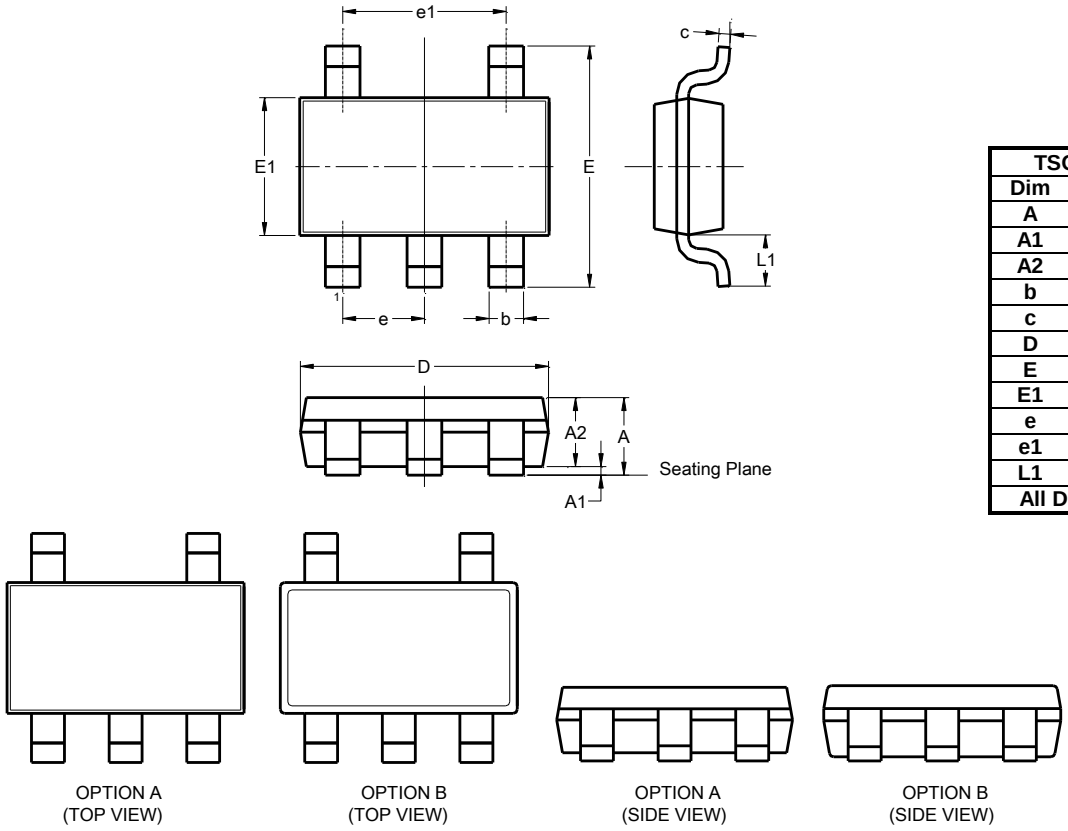
In Gate Driver circuits, most of the current occurs during turning on/off, so when designing optimal layout, it is best to consider the charge transfer during turn on/off.

When the DGD0216 turns on, charge will flow from C_1/C_2 through the logic circuits in the Gate Driver IC and directly to GND. But the majority of the charge will flow from C_1/C_2 via the internal P-channel MOSFET (see Functional Block Diagram Output Stage), through the OUT pin to charge the Gate of the MOSFET, Q1; the return is from the Source of Q1 through the current sense resistors (R_2 and R_3) and to GND (back to C_1/C_2). **Hence this loop must be as short as possible to minimize stray inductance**. C_1 should be a low ESR ceramic capacitor and along with gate resistor (R_1) and MOSFET (Q1) should be located close to the DGD0216 to minimize the inductance of that loop. When the device turns off, the charge on the MOSFET Gate sinks current into the IC through the internal N-channel MOSFET to GND.

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT25 (Standard)

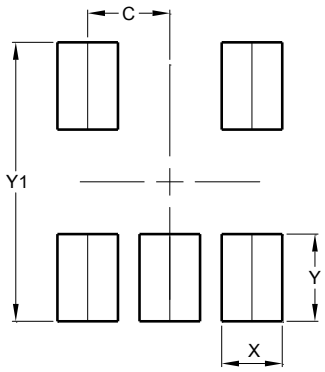


TSOT25 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	--	1.10	--
A1	0.01	0.10	--
A2	0.70	1.00	0.90
b	0.30	0.50	--
c	0.08	0.20	--
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

TSOT25 (Standard)



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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