QUAD/DUAL DSPLL
ANY-FREQUENCY, ANY-OUTPUT JITTER ATTENUATORS
Si5347, Si5346
FAMILY REFERENCE MANUAL

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1. Scope

This Family Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5347/46 devices in end applications. The official device specifications can be found in the Si5347/46 data sheets.

1.1. Related Documents

- Si5347/46 Data Sheet
- Si5347/46 Device Errata
- Si5347/46-EVB User Guide

2. Overview

The Si5347 is a high performance jitter attenuating clock multiplier that integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5346 is a dual DSPLL version in a smaller package. Each DSPLL has access to any of the four inputs and can provide low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency conversion with typical jitter performance of <100 fs in integer mode or <150 fs in fractional frequency synthesis mode. Each DSPLL supports independent free-run, holdover modes of operation, and offers automatic and hitless input clock switching. The Si5347/46 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5347/46 is made easy with Silicon Labs' ClockBuilder Pro software. Factory preprogrammed devices are available.

2.1. Work Flow Using ClockBuilder Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is to enable use of the device without an in-depth understanding of its complexities. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

2.2. Family Product Comparison

Table 1 lists the differences between the devices in this family.

Table 1. Device Selector Guide

Grade	PLLs/OUTs	Max Output Freq	Frequency Synthesis Modes
Si5347A	4/8	712.5 MHz	Integer + Fractional
Si5347C	4/4	712.5 MHz	Integer + Fractional
Si5346A	2/4	712.5 MHz	Integer + Fractional
Si5347B	4/8	350 MHz	Integer + Fractional
Si5347D	4/4	350 MHz	Integer + Fractional
Si5346B	2/4	350 MHz	Integer + Fractional

3. Functional Description

The Si5347 takes advantage of Silicon Labs fourth-generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. Each DSPLL has access to any of the four inputs (IN0 to IN3) after having been divided down by the P dividers, which are either fractional or integer. Clock selection can be either manual or automatic. Any of the output clocks can be configured to any of the DSPLLs using a flexible crosspoint connection. The Si5346 is a smaller form factor dual DSPLL version with four inputs and four outputs.

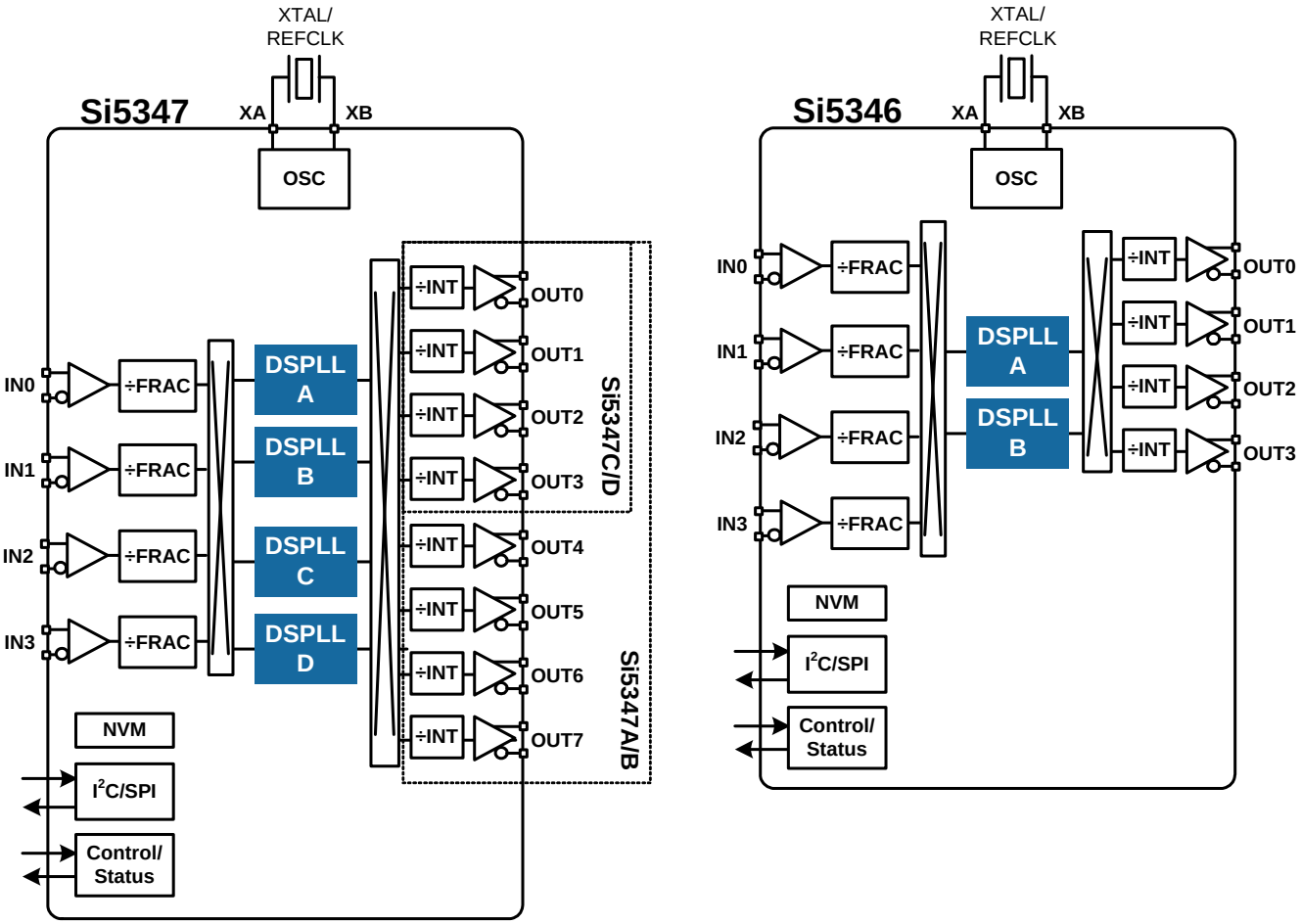


Figure 1. Block Diagrams

3.1. DSPLL

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pxn/Pdc) allow the DSPLL to perform hitless switching between input clocks (INx). Input switching is controlled manually or automatically using an internal state machine. The oscillator circuit (OSC) provides a frequency reference that determines output frequency stability and accuracy while the device is in free-run or holdover mode. A crosspoint switch connects any of the DSPLLs to any of the outputs. An additional integer divisor (R) determines the final output frequency.

The frequency configuration of the DSPLL is programmable through the SPI or I2C serial interface and can also be storied in non-volatile memory or RAM. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md) and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined by using the ClockBuilder Pro software.

Because a jitter reference is required for all applications, either a crystal or an external clock source needs to be connected to the XAXB pins. See "10.Recommended Crystals and External Oscillators" on page 57 and "11.Crystal and Device Circuit Layout Recommendations" on page 63 for more information.

3.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings of from 0.1 Hz up to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414, 0x0514, 0x0614, 0x0715) must be set high to latch the new values into operation. Note that each of these update bits will latch both loop and fastlock bandwidths.

Table 2. DSPLL Loop Bandwidth Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
BW_PLLA	0408[7:0] - 040D[7:0]	0408[7:0] - 040D[7:0]	This group of registers determine the loop bandwidth for DSPLL A, B, C, D. They are all independently selectable in the range from 0.1 Hz up to 4 kHz. Register values determined by ClockBuilderPro.
BW_PLLB	0508[7:0] - 050D[7:0]	0508[7:0] - 050D[7:0]	
BW_PLLC	0608[7:0] - 060D[7:0]	—	
BW_PLLD	0709[7:0] - 070E[7:0]	—	

3.2.1. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range from 100 Hz up to 4 kHz are available for selection. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs. If enabled, when LOL is asserted, Fastlock is enabled. When LOL is not asserted, Fastlock is disabled. Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414, 0x0514, 0x0614, 0x0715) must be set high to latch the new values into operation. Note that each of these update bits will latch both loop and fastlock bandwidths.

Table 3. Fastlock Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
FASTLOCK_AUTO_EN_PLLA	042B[0]	042B[0]	Fastlock enable/disable. Fastlock is enabled by default with a bandwidth of 4 kHz.
FASTLOCK_AUTO_EN_PLLB	052B[0]	052B[0]	
FASTLOCK_AUTO_EN_PLLC	062B[0]	—	
FASTLOCK_AUTO_EN_PLLD	072C[0]	—	
FAST_BW_PLLA	040E[7:0] - 0413[7:0]	040E[7:0] - 0413[7:0]	Fastlock bandwidth is selectable in the range of 100 Hz up to 4 kHz. Register values determined using ClockBuilder Pro.
FAST_BW_PLLB	050E[7:0] - 0513[7:0]	050E[7:0] - 0513[7:0]	
FAST_BW_PLLC	060E[7:0] - 0613[7:0]	—	
FAST_BW_PLLD	070F[7:0] - 0714[7:0]	—	

3.3. Dividers Overview

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

There are four main divider classes within the Si5347/46. See Figure 1 for a block diagram that shows them. Additionally, the DCO step word is used to scale the nominal output frequency in DCO mode. See "7.Digitally Controlled Oscillator (DCO) Mode" on page 43 for more information and block diagrams on DCO mode.

- PXAXB: Reference input divider (0x0206)
  - Divide reference clock by 1, 2, 4, or 8 to obtain an internal reference < 125 MHz
- P0-P3: Input clock wide range dividers (0x0208-0x022F)
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24}
  - 48-bit numerator, 32-bit denominator
  - Practical P divider range of (Fin / 2 MHz) < P < (Fin / 8 kHz)
  - Each P divider has a separate update bit for the new divider value to take effect
- MA-MD: DSPLL feedback dividers (0x0415-0x041F, 0x0515-0x051F, 0x0615-0x061F, 0x0716-0x0720)
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24}
  - 56-bit numerator, 32-bit denominator
  - Practical M divider range of (Fdco / 2 MHz) < M < (Fdco / 8 kHz)
  - Each M divider has a separate update bit for the new divider value to take effect
  - Soft reset will also update M divider values
- FSTEPW: DSPLL DCO step words (0x0423-0x0429, 0x0523-0x0529, 0x0623-0x0629, 0x0724-0x072A)
  - Positive Integers, where FINC/FDEC select direction
  - Min. value is 0, Max. value is 2^{24}
  - 56-bit step size, relative to 32-bit M numerator
- R0-R7: Output dividers (0x024A-0x026A)
  - Even integer divide values: 2, 4, 6, etc.
  - Min. value is 2, Max. value is 2^{24}
  - 24-bit word where Value = 2 x (Word + 1), for example Word = 3 gives an R value of 8

4. Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 2. The following sections describe each of these modes in greater detail.

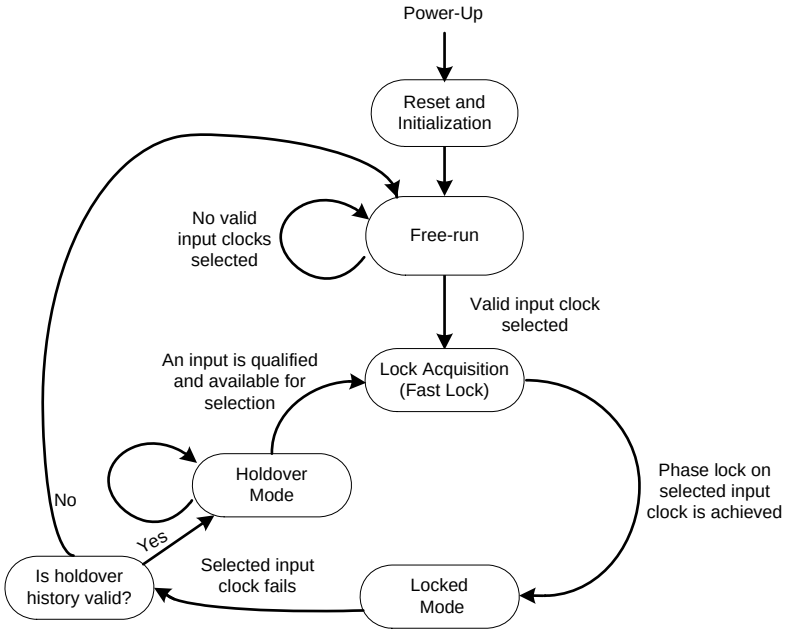


Figure 2. Modes of Operation

4.1. Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the $\overline{\text{RST}}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can affect all or each DSPLL individually.

Table 4. Reset Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
HARD_RST	001E[1]	001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST_ALL	001C[0]	001C[0]	Resets the device without re-downloading the register configuration from NVM.
SOFT_RST_PLLA	001C[1]	001C[1]	Performs a soft reset on DSPLL A only.
SOFT_RST_PLLB	001C[2]	001C[2]	Performs a soft reset on DSPLL B only.
SOFT_RST_PLLC	001C[3]	—	Performs a soft reset on DSPLL C only.
SOFT_RST_PLLD	001C[4]	—	Performs a soft reset on DSPLL D only.

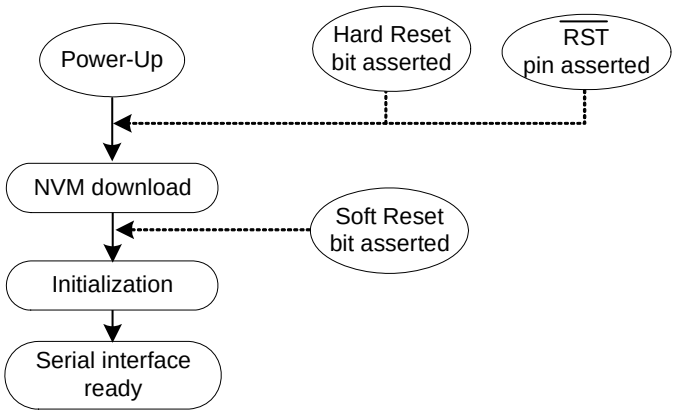


Figure 3. Initialization from Hard Reset and Soft Reset

The Si547/46 is fully configurable using the serial interface (I^2C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins. Neither VDDOx or VDDS supplies are required to write the NVM.

4.1.1. Updating Registers during Device Operation

ClockBuilder Pro generates all necessary control register writes to update settings for the entire device, including the ones described below. This is the case for both “Export” generated files as well as when using the GUI. This is sufficient to cover most applications. However, in some applications it is desirable to modify only certain sections of the device while maintaining unaffected clocks on the remaining outputs. If this is the case, please contact Silicon Labs Technical Support for further information.

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). Additionally, making single frequency step changes greater than ±350 ppm, either by using the DCO or by directly updating the M dividers, may also cause the PLL to become responsive. The following are the affected registers:

Control	Register(s)
XAXB_FREQ_OFFSET	0x0202 – 0x0205
PXAXB	0x0206[1:0]
MXAXB_NUM	0x0235 – 0x023A
MXAXB_DEN	0x023B – 0x023E

PLL lockup can easily be avoided by using the following the preamble and postamble write sequence below when one of these registers is modified or large frequency steps are made. Clockbuilder Pro software adds these writes to the output file by default when Exporting Register Files.

1. To start, write the preamble by updating the following control bits using Read/Modify/Write sequences:

Register	Decimal
0x0B24	0xD8
0x0B25	0x00

2. Then, modify all desired control registers.
3. Write 0x01 to Register 0x001C (SOFT_RST_ALL) to perform a Soft Reset once modifications are complete.
4. Write the postamble by updating the following control bits using Read/Modify/Write sequences:

Register	Decimal
0x0B24	0xDB
0x0B25	0x02

Note, however, that this procedure affects all DSPLLs and outputs on the device. For cases where it is desired to change only certain portions of the device without affecting the other outputs while the device is operating, please contact Silicon Labs technical support using the link on the last page of this document.

4.1.2. NVM Programming

The NVM is two-time writable for a base part (no set frequency plan) and one-time writable for a part with a factory pre-programmed frequency plan. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Note: In-circuit programming is supported over the temperature range of 0 to 80 °C.

The procedure for writing registers into NVM is as follows:

1. Ensure the part is configured correctly before proceeding.
2. Write 0xC7 to NVM_WRITE register.
3. Wait until DEVICE_READY = 0x0F.
4. Set NVM_READ_BANK 0x00E4[0] = “1”.
5. Wait until DEVICE_READY = 0x0F.
6. Steps 3 and 4 can be replaced by simply powering down and then powering up the device. Note that this process writes the current values in the device to the NVM. A hard reset by either RSTB pin or register bit may be used to reload the registers using the NVM values.

Table 5. NVM Programming Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
NVM_WRITE	0x00E3[7:0]	0x00E3[7:0]	Initiates an NVM write when written with 0xC7.
ACTIVE_NVM_BANK	0x00E2[5:0]	0x00E2[5:0]	Identifies the active NVM bank.
NVM_READ_BANK	0x00E4[0]	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	0x00FE[7:0]	Indicates that the device serial interface is ready to accept commands.

4.2. Free Run Mode

Once power is applied to the Si5347 and initialization is complete, all DSPLLs will automatically enter freerun mode, generating the frequencies determined by the NVM. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun or holdover modes.

4.3. Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process. If the fast lock feature is enabled, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.4. Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL frequency drift will not affect the output frequency. Each DSPLL has its own $\overline{\text{LOL}}$ pin and status bit to indicate when lock is achieved. See section 5.3.4 for more details on the operation of the loss of lock circuit.

4.5. Holdover Mode

Any of the DSPLLs will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each DSPLL stores up to 120 seconds of historical frequency data while the locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in Figure 4. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

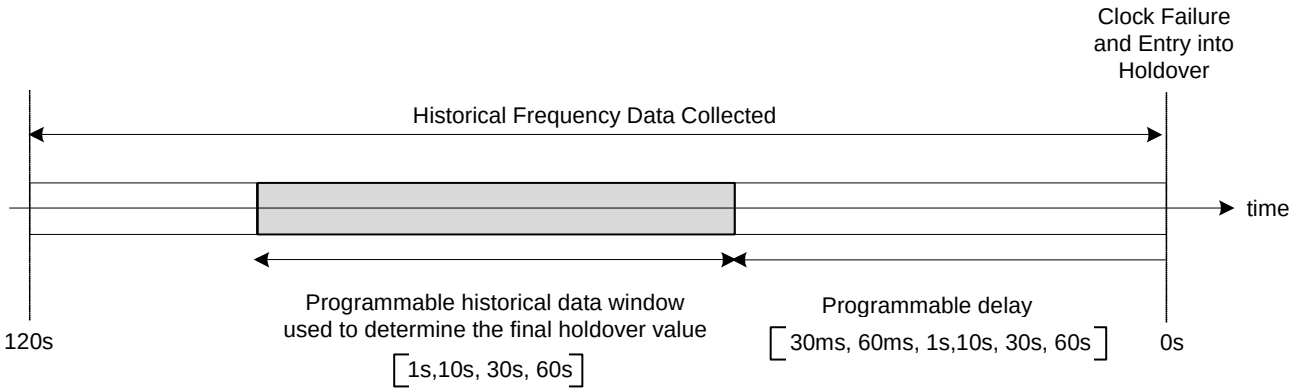


Figure 4. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth. These options are register-programmable.

Table 6. DSPLL Holdover Control and Status Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
Holdover Status			
HOLD_PLL(D,C,B,A)	000E[7:4]	000E[5:4]	Holdover status indicator. Indicates when a DSPLL is in holdover or free-run mode and is not synchronized to the input reference. The DSPLL goes into holdover only when the historical frequency data is valid, otherwise the DSPLL will be in free-run mode.
HOLD_FLG_PLL(D,C,B,A)	0013[7:4]	0013[5:4]	Holdover status monitor sticky bits. Sticky bits will remain asserted when an holdover event occurs until cleared. Writing a zero to a sticky bit will clear it.
HOLD_HIST_VALID_PLLA	043F[1]	043F[1]	Holdover historical frequency data valid. Indicates if there is enough historical frequency data collected for valid holdover value.
HOLD_HIST_VALID_PLLB	053F[1]	053F[1]	
HOLD_HIST_VALID_PLLC	063F[1]	—	
HOLD_HIST_VALID_PLLD	0740[1]	—	
Holdover Control and Settings			
HOLD_HIST_LEN_PLLA	042E[4:0]	042E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $((2^{HOLD_HIST\text{-}LEN_PLLx}) – 1 \times 8/3/(10^7)$Win
HOLD_HIST_LEN_PLLB	052E[4:0]	052E[4:0]	
HOLD_HIST_LEN_PLLC	062E[4:0]	—	
HOLD_HIST_LEN_PLLD	072F[4:0]	—	
HOLD_HIST_DELAY_PLLA	042F[4:0]	042F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $(2^{HOLD\_HIST\text{-}DELAY\_PLLx}) \times 2/3/(10^7)$
HOLD_HIST_DELAY_PLLB	052F[4:0]	052F[4:0]	
HOLD_HIST_DELAY_PLLC	062F[4:0]	—	
HOLD_HIST_DELAY_PLLD	0730[4:0]	—	
FORCE_HOLD_PLLA	0435[0]	0435[0]	These bits allow forcing any of the DSPLLs into holdover
FORCE_HOLD_PLLB	0535[0]	0535[0]	
FORCE_HOLD_PLLC	0635[0]	—	
FORCE_HOLD_PLLD	0736[0]	—	
HOLD_EXIT_BW_SEL_PLLA	042C[4]	042C[4]	Selects the exit from holdover bandwidth. Options are: 0: Exit of holdover using the fastlock bandwidth 1: Exit of holdover using the DSPLL loop bandwidth
HOLD_EXIT_BW_SEL_PLLB	052C[4]	052C[4]	
HOLD_EXIT_BW_SEL_PLLC	062C[4]	—	
HOLD_EXIT_BW_SEL_PLLD	072D[4]	—	
HOLD_RAMP_EN_PLLA	042C[3]	042C[3]	Must be set to 1 for normal operation.
HOLD_RAMP_EN_PLLB	052C[3]	052C[3]	
HOLD_RAMP_EN_PLLC	062C[3]	—	
HOLD_RAMP_EN_PLLD	072D[3]	—	

5. Clock Inputs

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both standard format inputs and low duty cycle pulsed CMOS clocks. The input P dividers can be either fractional or integer. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in Figure 5.

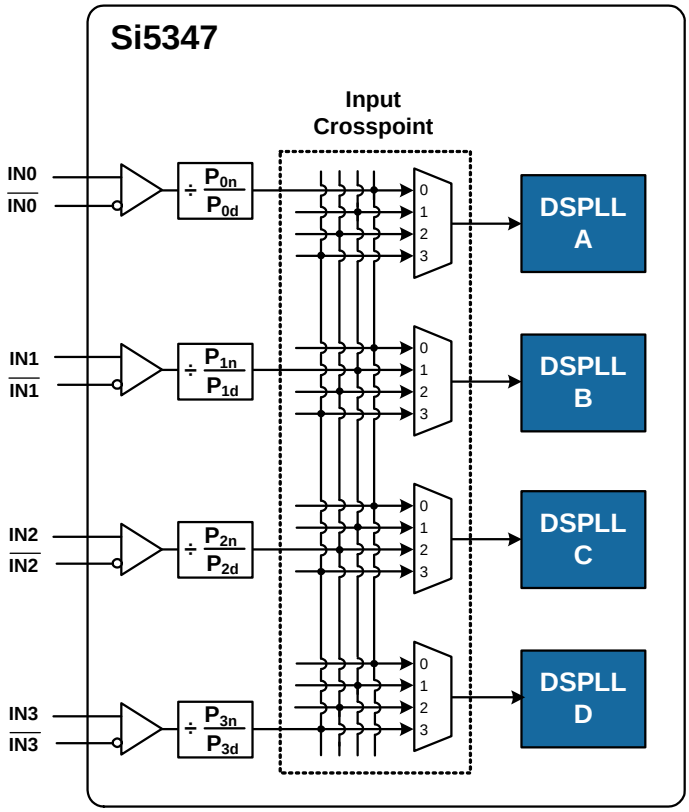


Figure 5. DSPLL Input Selection Crosspoint

5.1. Input Source Selection

Input source selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

Table 7. Manual or Automatic Input Clock Selection Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
CLK_SWITCH_MODE_PLLA	0436[1:0]	0436[1:0]	Selects manual or automatic switching mode for DSPLL A, B, C, D. 0: For manual 1: For automatic, non-revertive 2: For automatic, revertive 3: Reserved
CLK_SWITCH_MODE_PLLB	0536[1:0]	0536[1:0]	
CLK_SWITCH_MODE_PLLC	0636[1:0]	—	
CLK_SWITCH_MODE_PLLD	0737[1:0]	—	

In manual mode the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode if the holdover history is valid or Freerun if it is not.

Table 8. Manual Input Select Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
IN_SEL_PLLA	042A[3:1]	042A[3:1]	Selects the clock input used to synchronize DSPLL A, B, C, or D. Selections are: IN0, IN1, IN2, IN3, corresponding to the values 0, 1, 2, and 3. Selections 4–7 are reserved.
IN_SEL_PLLB	052A[3:1]	052A[3:1]	
IN_SEL_PLLC	062A[3:1]	—	
IN_SEL_PLLD	072B[3:1]	—	

When configured in automatic mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority arrangement is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). By default, inputs asserting either or both LOS or OOF cannot be selected as a source for any DSPLL. However, these restrictions may be removed by writing to the registers described below. If there is no valid input clock, the DSP will enter either Holdover or Free Run mode depending on whether the holdover history is valid at that time or not.

Table 9. Automatic Input Select Control Registers

Setting Name	Hex Address		Function
	Si5347	Si5346	
IN(3,2,1,0)_PRIORITY_PLLA	0x0438–0x0439	0x0438–0x0439	Selects the automatic selection priority for [IN3, IN2, IN1, IN0] for each DSPLL A, B, C, D. Selections are: 1st, 2nd, 3rd, 4th, or never select. Default is IN0=1st, IN1=2nd, IN2=3rd, IN3=4th.
IN(3,2,1,0)_PRIORITY_PLLB	0x0538–0x0539	0x0538–0x0539	
IN(3,2,1,0)_PRIORITY_PLLC	0x0638–0x0639	—	
IN(3,2,1,0)_PRIORITY_PLLD	0x0739–0x073A	—	
IN(3,2,1,0)_LOS_MSK_PLLA	0x0437	0x0437	Determines if the LOS status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is LOS is enabled (unmasked).
IN(3,2,1,0)_LOS_MSK_PLLB	0x0537	0x0537	
IN(3,2,1,0)_LOS_MSK_PLLC	0x0637	—	
IN(3,2,1,0)_LOS_MSK_PLLD	0x0738	—	
IN(3,2,1,0)_OOF_MSK_PLLA	0x0437	0x0437	Determines if the OOF status for [IN3, IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, B, C, D. Default is OOF enabled (unmasked).
IN(3,2,1,0)_OOF_MSK_PLLB	0x0537	0x0537	
IN(3,2,1,0)_OOF_MSK_PLLC	0x0637	—	
IN(3,2,1,0)_OOF_MSK_PLLD	0x0738	—	

5.2. Types of Inputs

Each of the four different inputs IN0-IN3 can be configured as standard LVDS, LVPECL, HCL, CML, and single-ended LVCMOS formats, or as a low duty cycle pulsed CMOS format. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc-biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown below in Figure 6. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance.

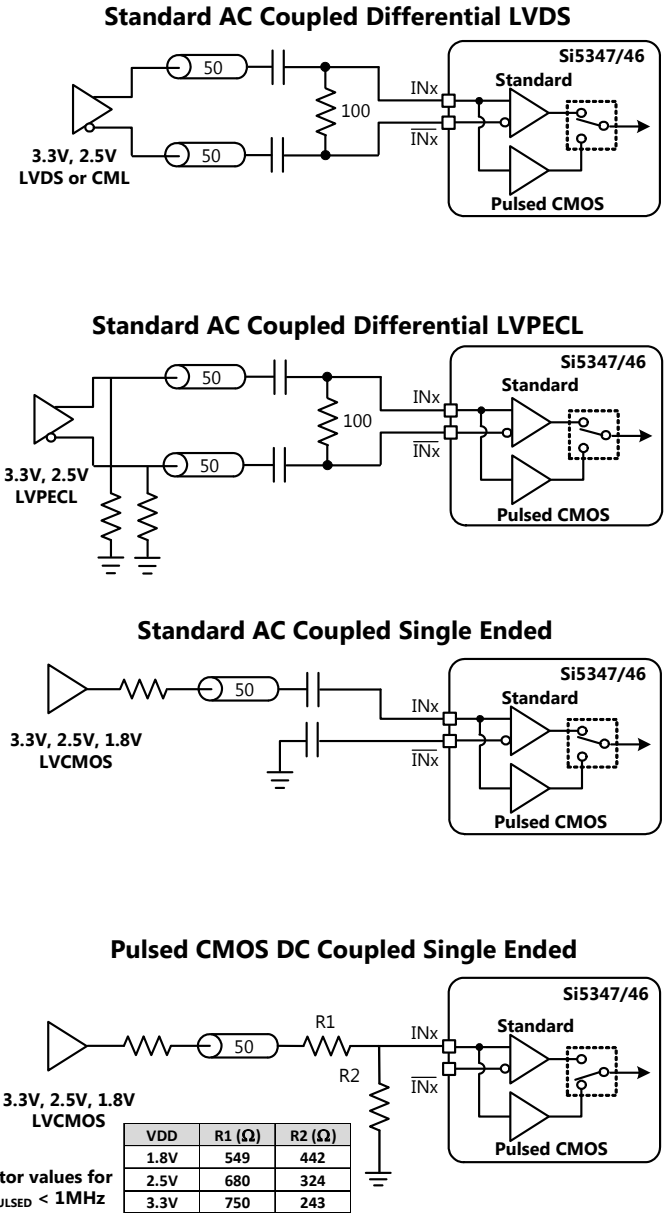


Figure 6. Input Termination for Standard and Pulsed CMOS Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for IN3 through IN0. Unused clock inputs may be powered down and left unconnected at the system level. For standard mode inputs, both input pins must be properly connected as shown in Figure 6, including the "Standard AC Coupled Single Ended" case. In Pulsed CMOS mode, it is not necessary to connect the inverting INx input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4] for IN3 through IN0.

Table 10. Input Clock Control and Configuration Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
IN_EN	0x0949[3:0]	0x0949[3:0]	Enable each of the input clock buffers for IN3 through IN0.
IN_PULSED_CMOS_EN	0x0949[7:4]	0x0949[7:4]	Enable Pulsed CMOS mode for each input IN3 through IN0.

5.2.1. Hitless Input Switching

Hitless switching is a feature that prevents a phase change from propagating to the output when switching between two clock inputs that have exactly the same frequency and a fixed phase relationship. In practice, this means that either one of the clocks must be frequency-locked to the other or that both must be frequency-locked to the same source. When hitless switching is enabled, the DSPLL absorbs the phase difference between the two input clocks during a input switch by enabling phase buildout. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis. If a fractional P divider is used on an input, the input frequency must be 300 MHz or higher in order to ensure proper hitless switching.

Table 11. DSPLL Hitless Switching Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
HSW_EN_PLLA	0436[2]	0436[2]	Hitless Switching Enable/Disable for DSPLL A, B, C, D. Hitless switching is enabled by default.
HSW_EN_PLLB	0536[2]	0536[2]	
HSW_EN_PLLC	0636[2]	—	
HSW_EN_PLLD	0737[2]	—	

5.2.2. Glitchless Input Switching

The DSPLLs have the ability to switch between two input clock frequencies that are up to ±500 ppm apart. The DSPLLs will pull-in to the new frequency at a rate determined by the DSPLLs' loop bandwidth. The DSPLLs loop bandwidth is set using registers 0x0408 to 0x040D for DSPLL A, 0x0508 to 0x050D for DSPLL B, 0x0608 to 0x060D for DSPLL C and 0x0709 to 0x070E for DSPLL D. Note that if "Fastlock" is enabled, then the DSPLL will pull-in to the new frequency using the Fastlock Loop Bandwidth. Depending on the LOL configuration settings, the loss of lock (LOL) indicator may assert while the DSPLL is pulling-in to the new clock frequency. However, there will never be output runt pulses generated at the output during the transition.

5.2.3. Synchronizing to Gapped Input Clocks

The DSPLL supports locking to a gapped input clock with missing clock edges. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its edges. Gapping a clock significantly increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of 2 missing cycles out of every 8.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification of up to 1.5 ns for a maximum phase transient, when the switch occurs during a gap in either input clocks. Figure 7 shows a 100 MHz clock with one cycle removed every 10 cycles that results in a 90 MHz periodic non-gapped output clock.

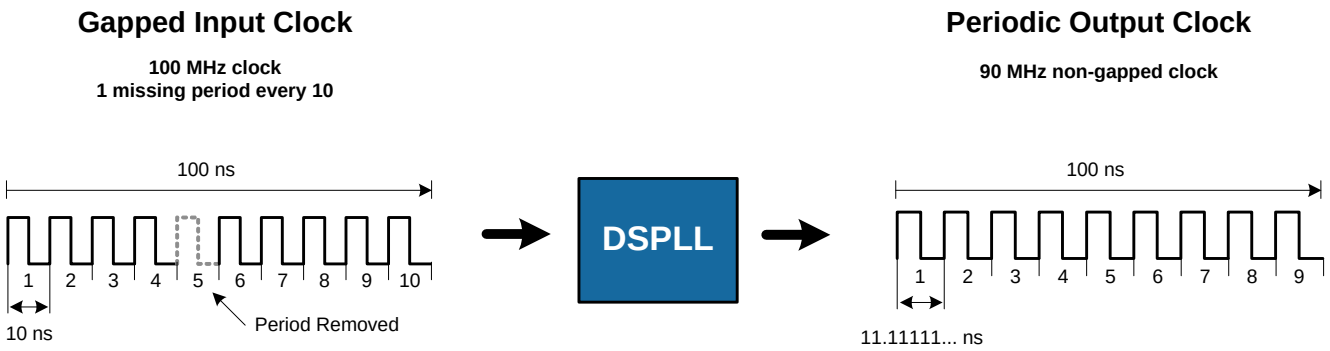


Figure 7. Gapped Input Clock Use

5.3. Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in Figure 8. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has a Loss Of Lock (LOL) indicator which is asserted when synchronization is lost with their selected input clock.

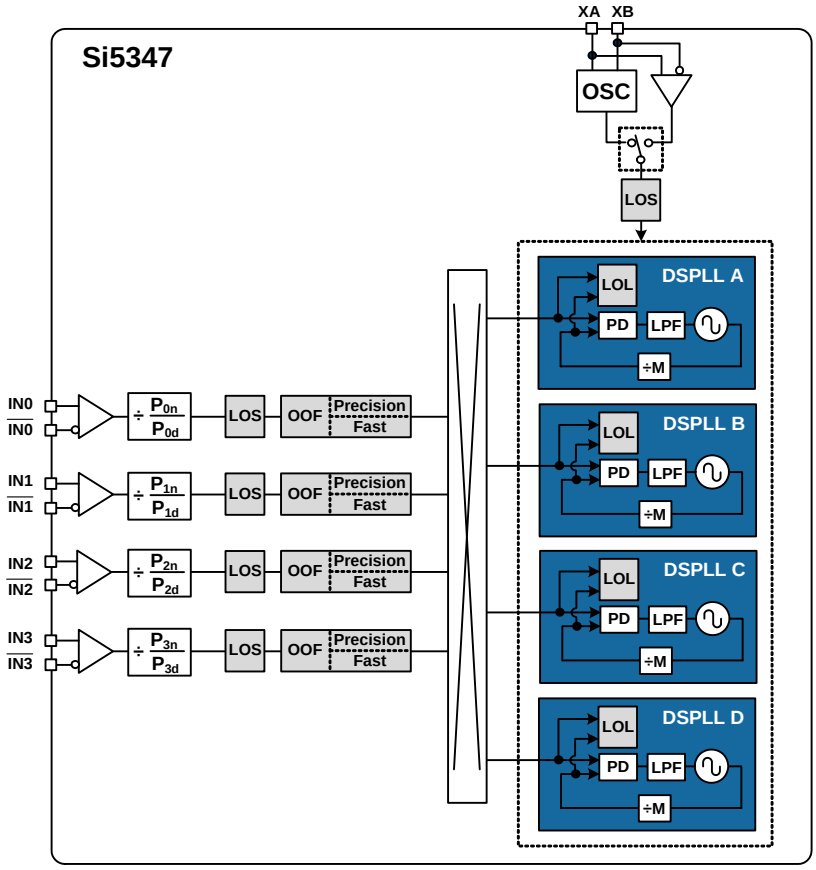


Figure 8. Fault Monitors

5.3.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register, when set, always stays asserted until cleared.

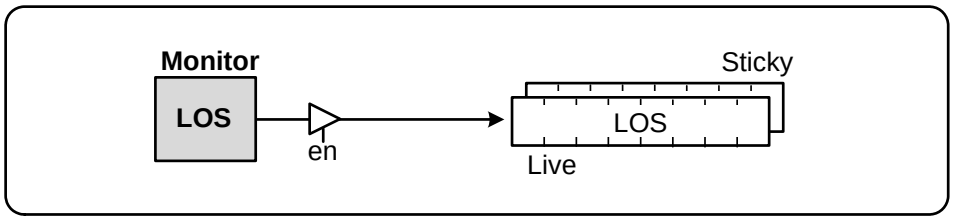


Figure 9. LOS Status Indicator

5.3.2. XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

Table 12. LOS Status Monitor Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
LOS Status Indicators			
LOS(3,2,1,0)	000D[3:0]	000D[3:0]	LOS status monitor for IN3, IN2, IN1, IN0. Indicates if a valid clock is detected or if a LOS condition is present.
LOSXAXB	000C[1]	000C[1]	LOS status monitor for the XTAL or REFCLK at the XA/XB pins.
LOS(3,2,1,0)_FLG	0012[3:0]	0012[3:0]	LOS status monitor sticky bits for IN3, IN2, IN1, IN0. Sticky bits will remain asserted when an LOS event occurs until they are cleared. Writing a zero to a sticky bit will clear it.
LOSXAXB_FLG	0011[1]	0011[1]	LOS status monitor sticky bits for XAXB. Sticky bits will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS Fault Monitor Controls and Settings			
LOS(3,2,1,0)_EN	002C[3:0]	002C[3:0]	LOS monitor enable for IN3, IN2, IN1, IN0. Allows disabling the monitor if unused.
LOS(3,2,1,0)_TRIG_THR	002E[7:0] - 0035[7:0]	002E[7:0] - 0035[7:0]	Sets the LOS trigger threshold and clear sensitivity for IN3, IN2, IN1, IN0. These 16-bit values are determined with the ClockBuilder Pro utility.
LOS(3,2,1,0)_CLR_THR	0036[7:0] - 003D[7:0]	0036[7:0] - 003D[7:0]	
LOS(3,2,1,0)_VAL_TIME	002D[7:0]	002D[7:0]	LOS clear validation time for IN3, IN2, IN1, IN0. This sets the time that an input must have a valid clock before the LOS condition is cleared. Settings of 2 ms, 100 ms, 200 ms, and 1 s are available.

5.3.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0 ppm” reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in Figure 10. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

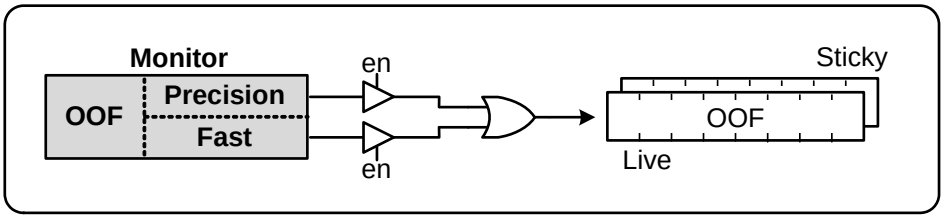


Figure 10. OOF Status Indicator

5.3.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±2 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the register-programmable OOF frequency range of ±2 ppm to ±500 ppm in steps of 2 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in Figure 11. In this case the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 - IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register configurable.

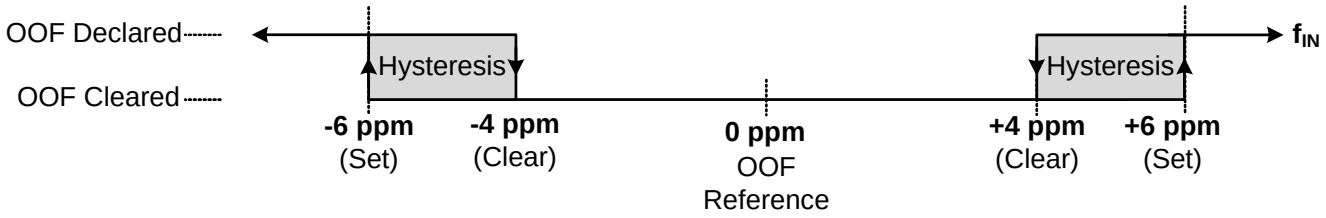


Figure 11. Example of Precise OOF Monitor Assertion and Deassertion Triggers

5.3.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

Table 13. OOF Status Monitor Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
OOF Status Indicators			
OOF(3,2,1,0)	000D[7:4]	000D[7:4]	OOF status monitor for IN3, IN2, IN1, IN0. Indicates if a valid clock is detected or if a OOF condition is detected.
OOF(3,2,1,0)_FLG	0012[7:4]	0012[7:4]	OOF status monitor sticky bits for IN3, IN2, IN1, IN0. Sticky bits will remain asserted when an OOF event occurs until cleared. Writing a zero to a sticky bit will clear it.
OOF Monitor Control and Settings			
OOF_REF_SEL	0040[2:0]	0040[2:0]	This selects the clock that the OOF monitors use as their “0 ppm” reference. Selections are: XA/XB, IN0, IN1, IN2, IN3.
OOF(3,2,1,0)_EN	003F[3:0]	003F[3:0]	This allows to enable/disable the precision OOF monitor for IN3, IN2, IN1, IN0.
FAST_OOF(3,2,1,0)_EN	003F[7:4]	003F[7:4]	To enable/disable the fast OOF monitor for IN3, IN2, IN1, IN0.
OOF(3,2,1,0)_SET_THR	0046[7:0] - 0049[7:0]	0046[7:0] - 0049[7:0]	Determines the OOF alarm set threshold for IN3, IN2, IN1, IN0. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm
OOF(3,2,1,0)_CLR_THR	004A[7:0] - 004D[7:0]	004A[7:0] - 004D[7:0]	Determines the OOF alarm clear threshold for INx. Range is from ±2 ppm to ±500 ppm in steps of 2 ppm

5.3.4. LOL Detection

There is a loss of lock (LOL) monitor for each of the DSPLLs. The LOL monitor asserts a LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs ($\overline{\text{LOL\_A}}$, $\overline{\text{LOL\_B}}$, $\overline{\text{LOL\_C}}$, $\overline{\text{LOL\_D}}$). The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in Figure 12. The live $\underline{\text{LOL}}$ register always displays the current LOL state and a sticky register always stays asserted until cleared. The $\overline{\text{LOL}}$ pin reflects the current state of the LOL monitor.

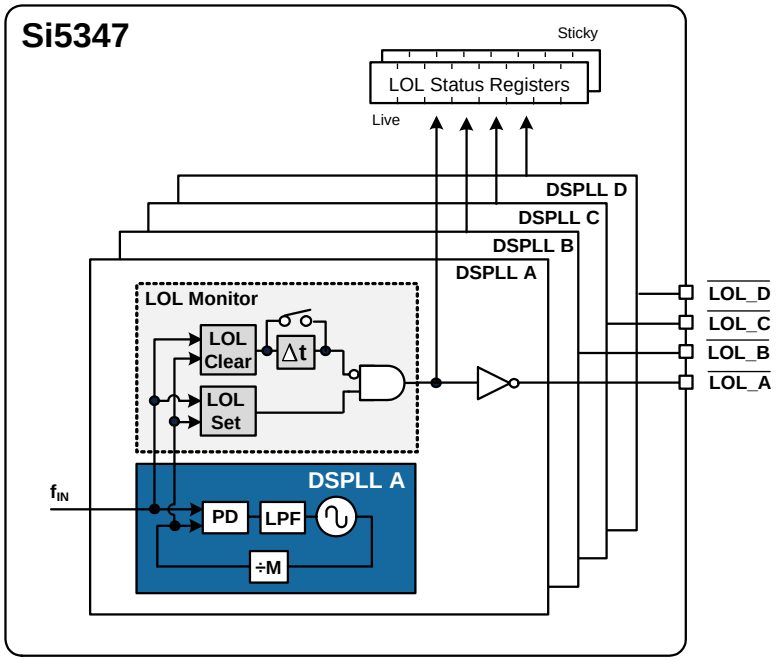


Figure 12. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity which is register configurable from 0.2 ppm to 20000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 0.2 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 2 ppm frequency difference is shown in Figure 13.

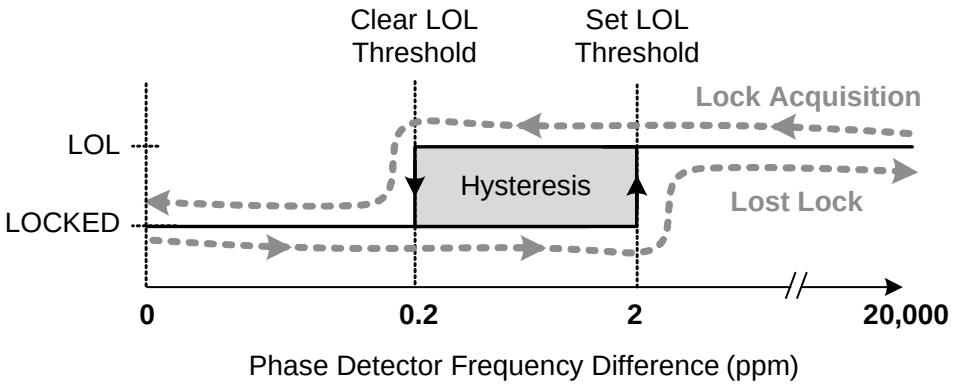


Figure 13. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

It is important to know that, in addition to being status bits, LOL enables Fastlock.

Table 14. LOL Status Monitor Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
LOL Status Indicators			
LOL_PLL(D,C,B,A)	000E[3:0]	000E[1:0]	Status bit that indicates if DSPLL A, B, C, or D is locked to an input clock.
LOL_FLG_PLL(D,C,B,A)	0013[3:0]	0013[1:0]	Sticky bits for LOL_[D,C,B,A]_STATUS register. Writing a zero to a sticky bit will clear it.
LOL Fault Monitor Controls and Settings			
LOL_SET_THR_PLL(D,C,B,A)	009E[7:0] - 009F[7:0]	009E[7:0]	Configures the loss of lock set thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 0.2 ppm.
LOL_CLR_THR_PLL(D,C,B,A)	00A0[7:0] - 00A1[7:0]	00A0[7:0]	Configures the loss of lock clear thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 2 ppm.
LOL_CLR_DELAY_PLL(D,C,B,A)	00A3[7:0] - 00B6[7:0]	00A3[7:0] - 00AC[7:0]	This is a 35-bit register that configures the delay value for the LOL Clear delay. Selectable from 4 ns over 500 seconds. This value depends on the DSPLL frequency configuration and loop bandwidth. It is calculated using ClockBuilder Pro utility.
LOL_TIMER_EN_PLL(D,C,B,A)	00A2[3:0]	00A2[1:0]	Allows bypassing the LOL Clear timer for DSPLL A, B, C, D. 0- bypassed, 1-enabled

The settings in Table 14 are handled by ClockBuilder Pro. Manual settings should be avoided.

5.3.5. Interrupt pin (INTR)

An interrupt pin (INTR) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTR pin is reset by clearing the sticky status registers.

Table 15. Interrupt Mask Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
LOS(3, 2, 1, 0)_INTR_MSK	0018[3:0]	0018[1:0]	Prevents IN3, IN2, IN1, IN0 LOS from asserting the INTR pin
OOF(3, 2, 1, 0)_INTR_MSK	0018[7:4]	0018[5:4]	Prevents IN3, IN2, IN1, IN0 OOF from asserting the INTR pin
LOSXAXB_INTR_MSK	0017[1]	0017[1]	Prevents XAXB LOS from asserting the INTR pin
LOL_INTR_MSK_PLL(D,C,B,A)	0019[3:0]	0019[1:0]	Prevents DSPLL D, C, B, A LOL from asserting the INTR pin
HOLD_INTR_MSK_PLL(D,C,B,A)	0019[7:4]	0019[5:4]	Prevents DSPLL D, C, B, A HOLD from asserting the INTR pin

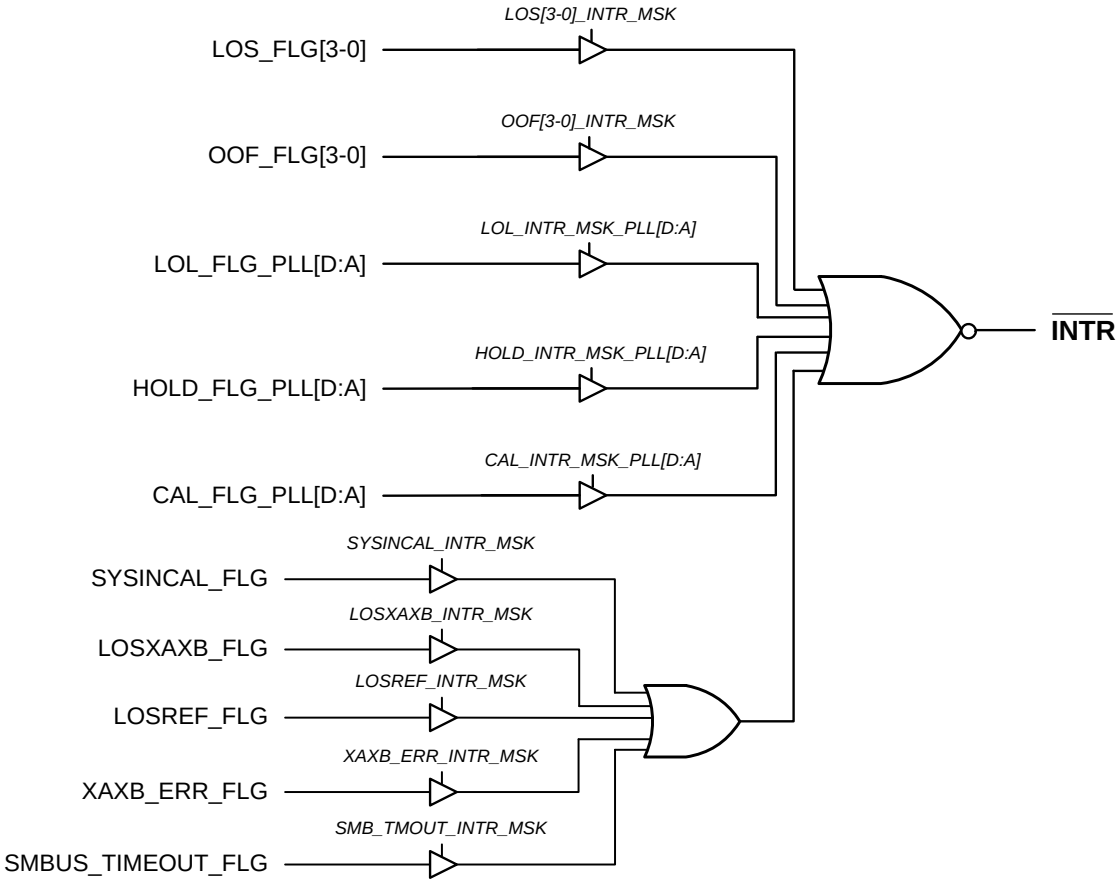


Figure 14. Interrupt Triggers and Masks

The _FLG bits are “sticky” versions of the alarm bits and will stay high until cleared. A _FLG bit can be cleared by writing a zero to the _FLG bit. When a _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTR pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannot be cleared.

6. Output Clocks

6.1. Outputs

The Si5347 supports up to eight differential output drivers and the Si5346 supports four. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, with CML-compatible amplitudes. In addition to supporting differential signals, any of the outputs can be configured as dual single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 16 single-ended outputs, or any combination of differential and single-ended outputs.

6.1.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in Figure 15. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

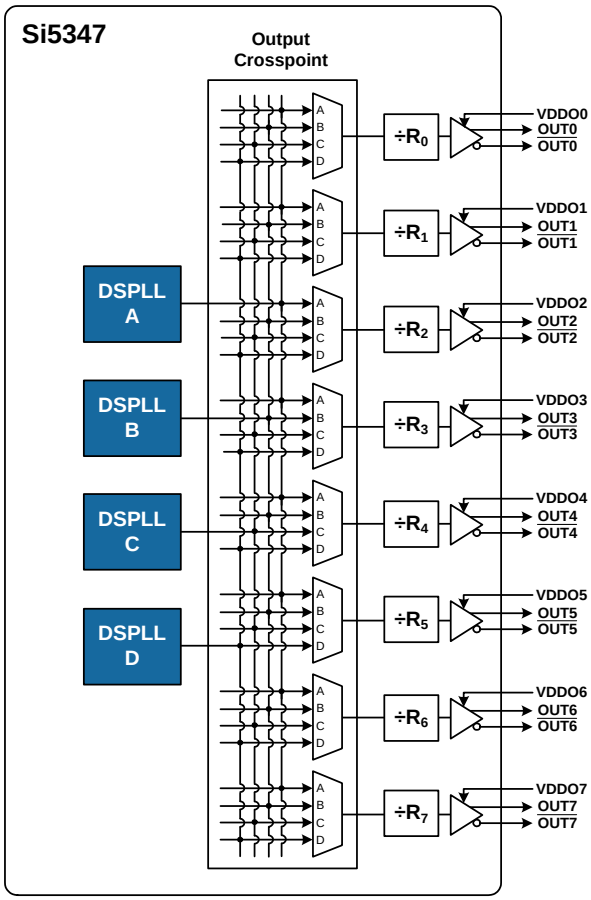


Figure 15. DSPLL to Output Driver Crosspoint

6.1.2. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment. Resetting the device using the $\overline{\text{RST}}$ pin or asserting the hard reset bit 0x001E[1] will give the same result. Soft reset does not affect output alignment.

6.2. Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter generation of the Si5347/46 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the crosstalk will come from the Si5347/46, and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources since the Si5347/46 must be attached to a board in order to measure jitter.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in Table 16.

Table 16. Example of Output Clock Placement

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	622.08	Not used
5	625	156.25
6	Not used	156.25
7	Not used	625

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. For example, a 155.52 MHz clock should not be placed next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are allowed, and these outputs should be grouped together when possible. Noting that because 155.52 MHz x 4 = 622.08 MHz and 156.25 MHz x 4 = 625 MHz, it is okay to place each pair of these frequency values close to one another.
3. Unused outputs can be used to separate clock outputs that might otherwise interfere with one another. In this case, see OUT3 and OUT4.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided in jitter-sensitive applications. When CMOS clocks are unavoidable, even greater care must be taken with respect to the above guidelines. For more information on these issues, see AN862: “Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems.”

The ClockBuilder Pro Clock Placement Wizard is an easy way to reduce crosstalk for a given frequency plan. This feature can be accessed on the “Define Output Frequencies” page of ClockBuilder Pro in the lower left hand corner of the GUI. It is recommended to use this tool after each project frequency plan change.

6.2.1. Output Crosspoint and Differential Signal Format Selection

The differential output swing and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS, LVPECL, HCSL, and CML. The differential formats can be either normal- or low-power mode. Low-power format uses less power for the same amplitude but has the drawback of slower rise/fall times. See "Appendix A—Custom Differential Amplitude Controls" on page 239 for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs or any combination of differential and single-ended outputs. Note also that CMOS can create much more crosstalk than differential outputs, so extra care must be taken in their pin placement so that other clocks that need the lowest jitter are not on nearby pins. With all outputs, see “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for additional information on frequency planning considerations.

Table 17. Output Crosspoint Selection Registers

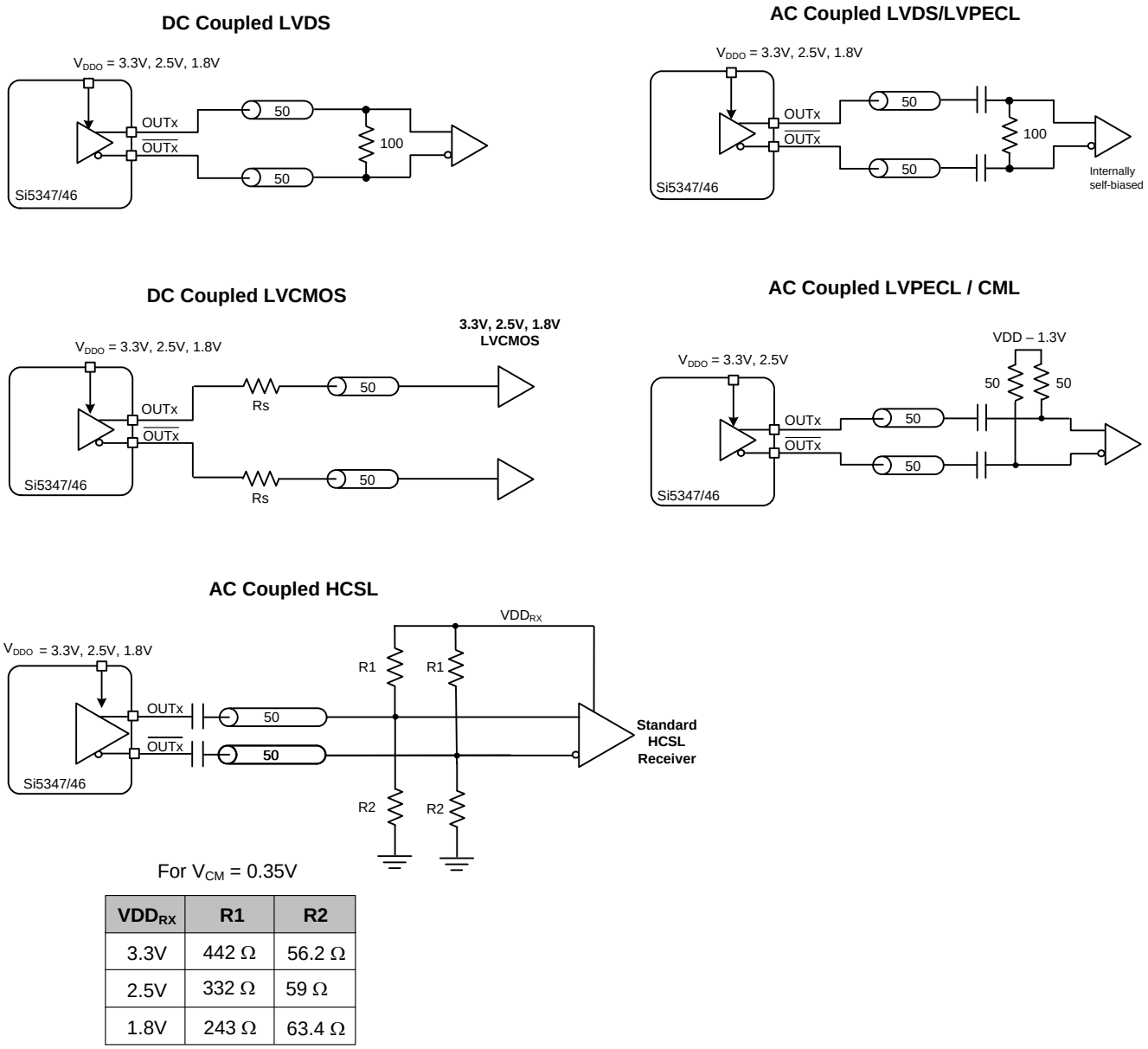
Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_MUX_SEL	010B[2:0]	010B[2:0]	0115[2:0]	Selects the DSPLL that each of the outputs are connected to. Options are DSPLL_A, DSPLL_B, DSPLL_C, or DSPLL_D.
OUT1_MUX_SEL	0115[2:0]	011F[2:0]	011A[2:0]	
OUT2_MUX_SEL	011A[2:0]	0129[2:0]	0129[2:0]	
OUT3_MUX_SEL	011F[2:0]	012E[2:0]	012E[2:0]	
OUT4_MUX_SEL	0129[2:0]	—	—	
OUT5_MUX_SEL	012E[2:0]	—	—	
OUT6_MUX_SEL	0133[2:0]	—	—	
OUT7_MUX_SEL	013D[2:0]	—	—	

Table 18. Output Signal Format Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_FORMAT	0109[2:0]	0109[2:0]	0113[2:0]	Selects the output signal format as differential or LVCMOS.
OUT1_FORMAT	0113[2:0]	011D[2:0]	0118[2:0]	
OUT2_FORMAT	0118[2:0]	0127[2:0]	0127[2:0]	
OUT3_FORMAT	011D[2:0]	012C[2:0]	012C[2:0]	
OUT4_FORMAT	0127[2:0]	—	—	
OUT5_FORMAT	012C[2:0]	—	—	
OUT6_FORMAT	0131[2:0]	—	—	
OUT7_FORMAT	013B[2:0]	—	—	

6.2.2. Output Terminations

The differential output drivers support both ac coupled and dc coupled terminations as shown in Figure 16.



For V_{CM} = 0.35V

VDD_{RX}	R1	R2
3.3V	442 Ω	56.2 Ω
2.5V	332 Ω	59 Ω
1.8V	243 Ω	63.4 Ω

Figure 16. Output Terminations for Differential and LVCMOS Outputs

6.3. Differential Outputs

6.3.1. Differential Output Amplitude Controls

The differential amplitude of each output can be controlled with the following registers. See "Appendix A—Custom Differential Amplitude Controls" on page 239 for register settings for non-standard amplitudes.

Table 19. Differential Output Voltage Amplitude (Swing) Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_AMPL	010A[6:4]	010A[6:4]	0114[6:4]	Sets the differential voltage swing (amplitude) for the output drivers in both normal and low-power modes. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36 for more information.
OUT1_AMPL	0114[6:4]	011E[6:4]	0119[6:4]	
OUT2_AMPL	0119[6:4]	0128[6:4]	0128[6:4]	
OUT3_AMPL	011E[6:4]	012D[6:4]	012D[6:4]	
OUT4_AMPL	0128[6:4]	—	—	
OUT5_AMPL	012D[6:4]	—	—	
OUT6_AMPL	0132[6:4]	—	—	
OUT7_AMPL	013C[6:4]	—	—	

6.3.2. Differential Output Common Mode Voltage Selection

The common mode voltage (VCM) for differential output normal and low-power modes is selectable depending on the supply voltage provided at the output’s VDDO pin. See Table 21. for recommended OUTx_CM settings for common signal formats. See “ Appendix A—Custom Differential Amplitude Controls” for recommended OUTx_CM settings when using custom output amplitude.

Table 20. Differential Output Common Mode Voltage Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_CM	010A[3:0]	010A[3:0]	0114[3:0]	Sets the common mode voltage for the differential output driver. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36 for more information.
OUT1_CM	0114[3:0]	011E[3:0]	0119[3:0]	
OUT2_CM	0119[3:0]	0128[3:0]	0128[3:0]	
OUT3_CM	011E[3:0]	012D[3:0]	012D[3:0]	
OUT4_CM	0128[3:0]	—	—	
OUT5_CM	012D[3:0]	—	—	
OUT6_CM	0132[3:0]	—	—	
OUT7_CM	013C[3:0]	—	—	

6.3.3. Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low

The Normal mode setting includes an internal 100 Ω resistor between the OUTx pins. In Low Power mode, this resistor is removed, resulting in a higher output impedance. The increased impedance creates larger amplitudes for the same power while reducing edge rates that may increase jitter or phase noise. In either mode, the differential receiver must be properly terminated to the PCB trace impedance for good system signal integrity. Note that ClockBuilder Pro does not provide low-power mode settings. Contact Silicon Labs Technical Support for assistance with low-power mode use.

Amplitude controls are as described in the previous section and also in more detail in "Appendix A—Custom Differential Amplitude Controls" on page 239. Common mode voltage selection is also described in more detail in Appendix A. The Stop High or Stop Low choice is described above.

Table 21. Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML

Standard	VDDOx	Mode	OUTx_FORMAT	OUTx_CM	OUTx_AMPL
	(V)		(dec)	(dec)	(dec)
LVPECL	3.3	Normal	1	11	6
LVPECL	2.5	Normal	1	11	6
LVPECL	3.3	Low-Power	2	11	3
LVPECL	2.5	Low-Power	2	11	3
LVDS	3.3	Normal	1	3	3
LVDS	2.5	Normal	1	11	3
Sub-LVDS[1]	1.8	Normal	1	13	3
LVDS	3.3	Low-Power	2	3	1
LVDS	2.5	Low-Power	2	11	1
Sub-LVDS[1]	1.8	Low-Power	2	13	1
HCSL[2]	3.3	Low-Power	2	11	3
HCSL[2]	2.5	Low-Power	2	11	3
HCSL[2]	1.8	Low-Power	2	13	3

Notes:
1. The Sub-LVDS common mode voltage is not compliant with LVDS standards. Therefore, AC coupling the driver to an LVDS receiver is highly recommended.
2. Creates HCSL compatible signals, see HCSL receiver biasing network in Figure 16.

The output differential driver can also produce a wide range of CML compatible output amplitudes. See "Appendix A—Custom Differential Amplitude Controls" on page 239 for additional information.

6.4. LVCMOS Outputs

6.4.1. LVCMOS Output Terminations

LVCMOS outputs may be ac- or dc-coupled, as shown in Figure 16. AC coupling is recommended for best jitter and phase noise performance. For dc-coupled LVCMOS, as shown again in Figure 17 below, series termination resistors are required in order to increase the total source resistance to match the trace impedance of the circuit board.

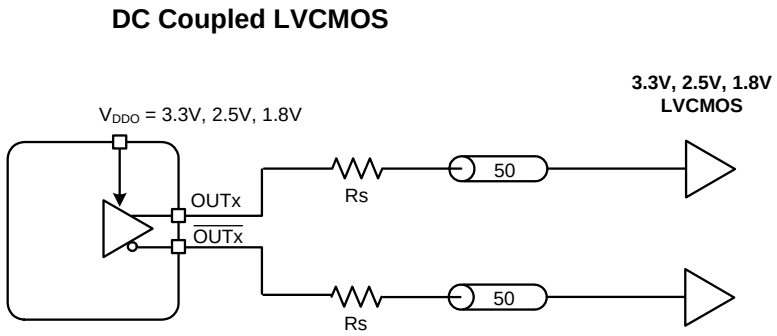


Figure 17. LVCMOS Output Terminations

6.4.2. LVCMOS Output Impedance And Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A series source termination resistor (Rs) is recommended close to the output to match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance – Zs). There are multiple programmable output impedance selections for each VDDO option as shown in Table 22. Generally, the lowest impedance for a given supply voltage is preferable, since it will give the fastest edge rates.

Table 22. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA
***Note:** Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.			

Table 23. LVCMOS Drive Strength Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_CMOS_DRV	0109[7:6]	0109[7:6]	0118[7:6]	LVCMOS output impedance. See Table 22.
OUT1_CMOS_DRV	0113[7:6]	011D[7:6]	011D[7:6]	
OUT2_CMOS_DRV	0118[7:6]	0127[7:6]	0127[7:6]	
OUT3_CMOS_DRV	011D[7:6]	012C[7:6]	012C[7:6]	
OUT4_CMOS_DRV	0127[7:6]	—	—	
OUT5_CMOS_DRV	012C[7:6]	—	—	
OUT6_CMOS_DRV	0131[7:6]	—	—	
OUT7_CMOS_DRV	013B[7:6]	—	—	

6.4.3. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver automatically detects the voltage on the VDDO pin to properly determine the correct output voltage.

6.4.4. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and $\overline{\text{OUTx}}$). By default the clock on the $\overline{\text{OUTx}}$ pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

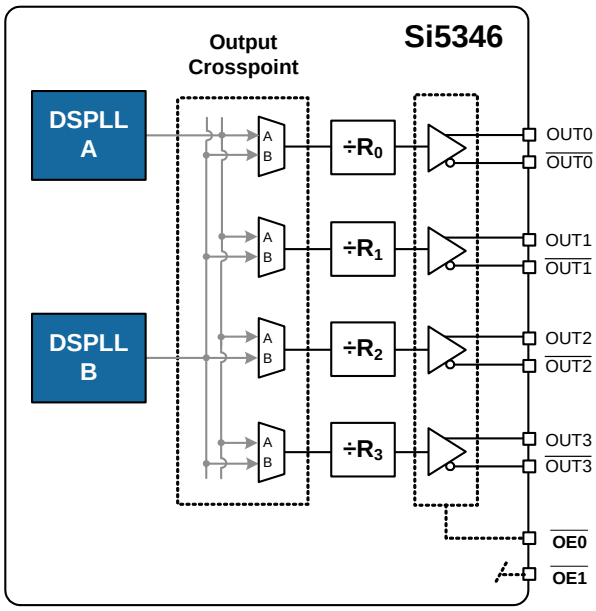
Table 24. LVCMOS Output Polarity Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_INV	010B[7:6]	010B[7:6]	0115[7:6]	Controls output polarity of the OUTx and $\overline{\text{OUTx}}$ pins when in LVCMOS mode. Selections are:
OUT1_INV	0115[7:6]	011F[7:6]	011A[7:6]	
OUT2_INV	011A[7:6]	0129[7:6]	0129[7:6]	
OUT3_INV	011F[7:6]	012E[7:6]	012E[7:6]	
OUT4_INV	0129[7:6]	—	—	
OUT5_INV	012E[7:6]	—	—	
OUT6_INV	0133[7:6]	—	—	
OUT7_INV	013D[7:6]	—	—	

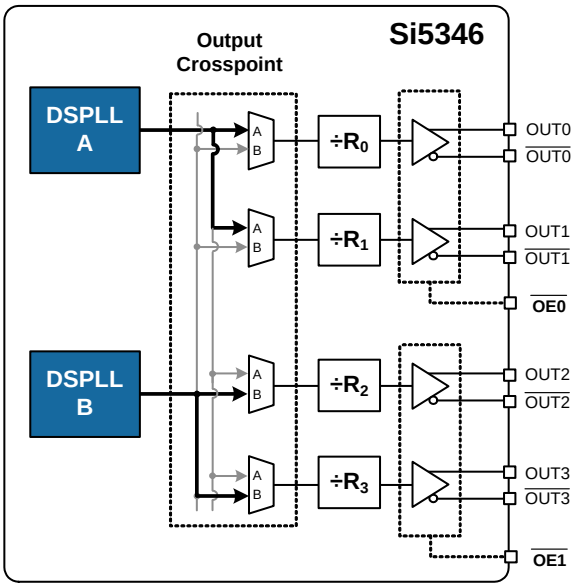
OUTx_INV	OUTx	$\overline{\text{OUTx}}$	Comment
0 0	CLK	CLK	Both in phase (default)
0 1	CLK	$\overline{\text{CLK}}$	Non-inverted
1 0	$\overline{\text{CLK}}$	CLK	Inverted
1 1	$\overline{\text{CLK}}$	$\overline{\text{CLK}}$	Both out of phase

6.5. Output Enable/Disable

The Si5347/46 allows enabling/disabling outputs by either pin, register control, or a combination of both. Two output enable pins are available (OE0, OE1). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0 controls all of the outputs while OE1 remains unmapped and has no affect until configured. Figure 18 shows an example of a output enable mapping scheme that is register configurable and can be stored in NVM as the default at power-up.



In its default state the OE0 pin enables/ disables all outputs. The OE1 pin is not mapped and has no effect on outputs.



An example of an configurable output enable scheme. In this case OE0 controls the outputs associated with DSPLL A, while OE1 controls the outputs of DSPLL B.

Figure 18. Example of Configuring Output Enable Pins

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OE pin(s) has them enabled. By default the output enable register settings are configured to allow the OE pins to have full control.

6.5.1. Output Disable State Selection

When the output driver is disabled, the outputs will drive either logic high or logic low, selectable by the user. The output common mode voltage is maintained while the driver is disabled, reducing enable/disable transients.

By contrast, powering down the driver rather than disabling it increases output impedance and shuts off the output common mode voltage. For all output drivers connected in the system, it is recommended to use Disable rather than Powerdown to reduce enable/disable common mode transients. Unused outputs may be left unconnected, powered down to reduce current draw, and, with the corresponding VDDOx, left unconnected.

6.5.2. Output Disable During LOL

By default a DSPLL that is out of lock will generate an output clock. There is an option to disable the outputs when a DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into holdover.

6.5.3. Output Disable During XAXB_LOS

The internal oscillator circuit, in combination with the external crystal, provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm.

6.5.4. Output Driver State When Disabled

The disabled state of an output driver is register-configurable as disable low or disable high.

Table 25. Output Enable/Disable Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUTALL_DISABLE_LOW	0102[0]	0102[0]	0102[0]	Allows disabling all output drivers: 0 - all outputs disabled, 1 - all outputs controlled by the OUTx_OE bits. Note that if the $\overline{OE}$ pin is held high (disabled), then all assigned outputs will be disabled regardless of the state of this register bit.
OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE OUT7_OE	0108[1] 0112[1] 0117[1] 011C[1] 0126[1] 012B[1] 0130[1] 013A[1]	0108[1] 011C[1] 0126[1] 012B[1] — — — —	0012[1] 0117[1] 0126[1] 012B[1] — — — —	Allows enabling/disabling individual output drivers. Note that the $\overline{OE}$ pin must be held low in order to enable an output with these register bits.
OUT_DIS_MASK_LOL_PLL(D,C,B,A)	0142[3:0]	0142[3:0]	0142[1:0]	Determines if the outputs are disabled during an LOL condition. 0 = outputs disable on LOL, 1 = outputs remain enabled during LOL (default). This option is independently configured for each DSPLL. See DRVx_DIS_SRC registers.
OUT_DIS_MSK_LOSXAXB	0141[6]	0141[6]	0141[6]	Determines if outputs are disabled during an LOSXAXB condition. 0 = all outputs disabled on LOSXAXB (default), 1 = outputs remain enabled during LOSXAXB condition.
OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE OUT4_DIS_STATE OUT5_DIS_STATE OUT6_DIS_STATE OUT7_DIS_STATE	0109[5:4] 0113[5:4] 0118[5:4] 011D[5:4] 0127[5:4] 012C[5:4] 0131[5:4] 013B[5:4]	0109[5:4] 011D[5:4] 0127[5:4] 012C[5:4] — — — —	0113[5:4] 0118[5:4] 0127[5:4] 012C[5:4] — — — —	Sets the state for the outputs when they are disabled.

6.5.5. Synchronous/Asynchronous Output Selection

Outputs can be configured to enable and disable either synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

Table 26. Synchronous/Asynchronous Disable Control Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
OUT0_SYNC_EN	0109[3]	0109[3]	0113[3]	Selects Synchronous or Asynchronous output disable. 1= synchronous, 0 = asynchronous. Default is asynchronous mode.
OUT1_SYNC_EN	0113[3]	011D[3]	0118[3]	
OUT2_SYNC_EN	0118[3]	0127[3]	0127[3]	
OUT3_SYNC_EN	011D[3]	012C[3]	012C[3]	
OUT4_SYNC_EN	0127[3]	—	—	
OUT5_SYNC_EN	012C[3]	—	—	
OUT6_SYNC_EN	0131[3]	—	—	
OUT7_SYNC_EN	013B[3]	—	—	

6.5.6. Output Driver Disable Source Summary

There are a number of conditions that may cause the outputs to be automatically disabled. The user may mask out unnecessary disable sources to match the system requirements. Any one of the unmasked sources may cause the outputs to be disabled; this is more powerful but similar in concept to open source “wired-OR” configurations. Table 27 summarizes the output disable sources with additional information for each source.

Table 27. Output Driver Disable Sources Summary

Output Driver Disable Source	Disable Outputs when Source	Individually Assignable?	Maskable?	Related Registers[Bits] (Hex)			Comments
				Si5347A/B	Si5347C/D	Si5346	
OUTALL_DISABLE_LOW	Low	N	N	0102[0]	0102[0]	0102[0]	User Controllable
OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE OUT7_OE	Low	Y	N	0108[1] 0112[1] 0117[1] 011C[1] 0126[1] 012B[1] 0130[1] 013A[1]	0108[1] 011C[1] 0126[1] 012B[1] — — — —	0112[1] 0117[1] 0126[1] 012B[1] — — — —	User Controllable
OE0 (pin)	High	Y	N	0022[1:0], 0023-0024	0022[1:0], 0023-0024	0022[1:0], 0023-0024	User Controllable
OE0 (register)	Low						
OE1 (pin)	High	Y	N	0022[2,0], 0025, 0026	0022[2,0], 0025, 0026	0022[2,0], 0025, 0026	User Controllable
OE1 (register)	Low						
LOL_PLL[D:A]	High	Y	Y	000D[3:0], 0142[3:0]	000D[3:0], 0142[3:0]	000D[1:0], 0142[1:0]	Maskable separately for each DSPLL

Table 27. Output Driver Disable Sources Summary

Output Driver Disable Source	Disable Outputs when Source	Individually Assignable?	Maskable?	Related Registers[Bits] (Hex)			Comments
				Si5347A/B	Si5347C/D	Si5346	
LOS_XAXB	High	N	Y	000C[1], 0141[6]	000C[1], 0141[6]	000C[1], 0141[6]	Maskable
SYSINCAL	High	N	N	000C[0]	000C[0]	000C[0]	Automatic, not user-controllable or maskable

7. Digitally Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in pre-defined steps given by frequency step words (FSTEPW). The frequency adjustments are controlled through the serial interface or by pin control using frequency increments (FINC) or decrements (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it. The DCO mode is available when the DSPLL is operating in locked mode. Note that the maximum FINC/FDEC update rate, by either hardware or software, is 1 MHz. Each DSPLL being used in DCO mode should have fractional M division enabled by setting the appropriate M_FRAC_EN_PLLx = 0x31 for proper operation.

Table 28. Fractional M Divider Enable Controls

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
M_FRAC_EN_PLLA	0x0421[5:0]	0x0421[5:0]	DSPLL feedback M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.
M_FRAC_EN_PLLB	0x0521[5:0]	0x0521[5:0]	
M_FRAC_EN_PLLC	0x0621[5:0]	—	
M_FRAC_EN_PLLD	0x0721[5:0]	—	

7.1. Frequency Increment/Decrement Using Pin Controls

Controlling the output frequency with pin controls is available on the Si5347. This feature involves asserting the FINC or FDEC pins to increment or decrement the DSPLL frequency. The DSPLL_SEL pins select which DSPLL output frequency is affected by the frequency change. The frequency step words (FSTEPW) define the amount of frequency change for each FINC or FDEC. The FSTEPW may be written once or may be changed after every FINC/FDEC assertion. Note that the DSPLL_SEL pins are not available on the Si5346. Both the FINC and FDEC inputs are rising-edge-triggered and must meet the data sheet minimum pulse width (PW) specifications.

Note: When the FINC/FDEC pins on the Si5347 are unused, the FDEC pin must be pulled down with an external pull-down resistor or jumper. The FINC pin has an internal pull-down and may be left unconnected when not in use.

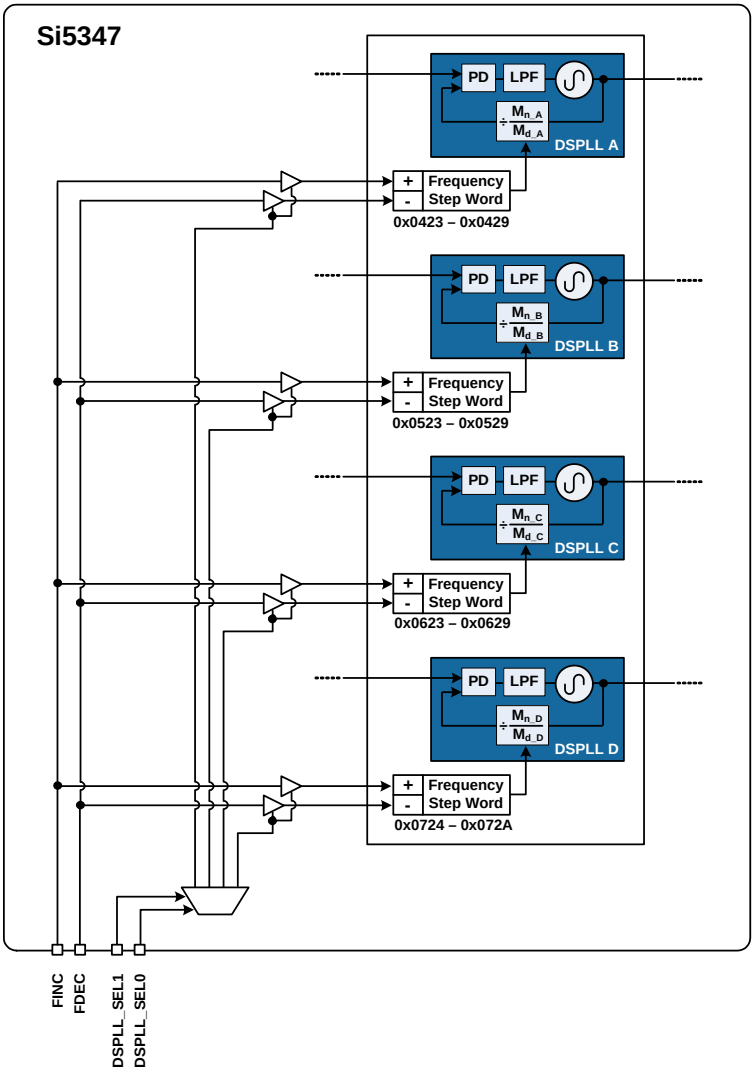


Figure 19. Controlling the DCO Mode By Pin Control

7.2. Frequency Increment/Decrement Using the Serial Interface

Controlling the DSPLL frequency through the serial interface is available on both the Si5347 and Si5346. This can be performed by asserting the FINC or FDEC bits to activate the frequency change defined by the frequency step word. A set of mask bits selects the DSPLL(s) that is affect by the frequency change. The FINC and FDEC pins can also be used to trigger a frequency change. Note that both the FINC and FDEC register bits are rising-edge-triggered and self-clearing.

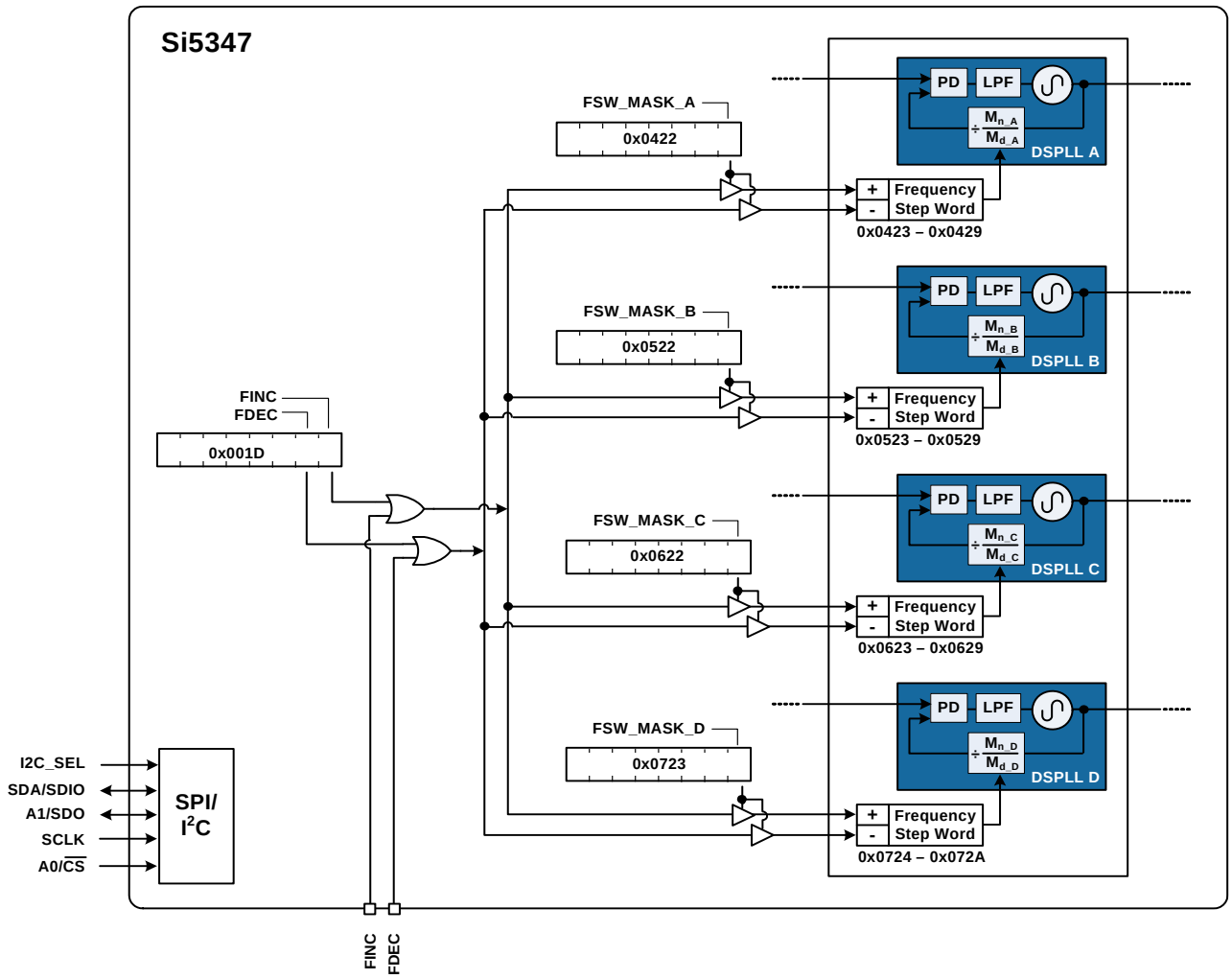


Figure 20. Controlling The DCO Mode Using the Serial Interface

Table 29. Frequency Increment/Decrement Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
FINC	001D[0]	001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	001D[1]	001D[1]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
M_FSTEPW_PLLA	0423[7:0] - 0429[7:0]	0423[7:0] - 0429[7:0]	This is a 56-bit frequency step word for DSPLL A, B, C, D. The FSTEPW will be added or subtracted to the DSPLL output frequency during assertion of the FINC/FDEC bits or pins. The FSTEPW is calculated based on the frequency configuration and is easily calculated using ClockBuilder Pro utility.
M_FSTEPW_PLLB	0523[7:0] - 0529[7:0]	0523[7:0] - 0529[7:0]	
M_FSTEPW_PLLC	0623[7:0] - 0629[7:0]	—	
M_FSTEPW_PLLD	0724[7:0] - 072A[7:0]	—	
M_FSTEP_MSK_PLLA	0422[0]	0422[0]	This mask bit determines if a FINC or FDEC affects DSPLL A, B, C, D. 0 = FINC/FDEC will increment/decrement the FSTEPW to the DSPLL. 1 = Ignores FINC/FDEC.
M_FSTEP_MSK_PLLB	0522[0]	0522[0]	
M_FSTEP_MSK_PLLC	0622[0]	—	
M_FSTEP_MSK_PLLD	0723[0]	—	

7.2.1. DCO with Direct Register Writes

In addition to the register-based FINC/FDEC described above, updated values for the DSPLL feedback M divider value may be updated directly by the user. When the M divider numerator (Mx_NUM) and its corresponding update bit (Mx_UPDATE) is written, the new numerator value will take effect and the output frequency will change without any glitches. The M divider numerator and denominator terms (Mx_NUM and Mx_DEN) can be left and right-shifted so that the least significant bit of the numerator word represents the exact step resolution that is needed for your application. Each individual M divider has its own update bit (Mx_UPDATE) that must be written to cause the new numerator value to take effect. All M dividers can be updated at the same time by issuing a Soft Reset.

Changing the DSPLL feedback M divider value while the device is operating will not generate any glitches on affected outputs. The frequency settling to the new value will be determined by the Loop BW of the DSPLL. All other outputs generated by other DSPLLs will be unaffected by this update. It is generally recommended to avoid dynamically changing the M divider denominator (Mx_DEN) as, in some cases, a small output phase hit of approximately 550 fs may be observed when the update becomes active. However, by using the proper combination of settings for the particular frequency plan, it is possible to avoid this entirely. If your application requires dynamic changes to an M divider denominator, contact Silicon Labs at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx.

Table 30. Direct DCO Control Registers

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
M_NUM_PLLA	0x0415–0x041B	0x0415–0x041B	56-bit DSPLL feedback M divider Numerator.
M_NUM_PLLB	0x0515–0x051B	0x0515–0x051B	
M_NUM_PLLC	0x0615–0x061B	—	
M_NUM_PLLD	0x0716–0x071C	—	
M_DEN_PLLA	0x041C–0x041F	0x041C–0x041F	32-bit DSPLL feedback M divider Denominator.
M_DEN_PLLB	0x051C–0x051F	0x051C–0x051F	
M_DEN_PLLC	0x061C–0x061F	—	
M_DEN_PLLD	0x071D–0x0720	—	
M_UPDATE_PLLA	0x0420[0]	0x0420[0]	Must write a 1 to this bit to cause the individual M divider changes to take effect.
M_UPDATE_PLLB	0x0520[0]	0x0520[0]	
M_UPDATE_PLLC	0x0620[0]	—	
M_UPDATE_PLLD	0x0721[0]	—	

8. Serial Interface

Configuration and operation of the Si5347/46 is controlled by reading and writing registers using the I2C or SPI serial interface. The I2C_SEL pin selects between I2C or SPI operation. The Si5347/46 supports communication with either a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit. See Figure 21 for supported modes of operation and settings. The I2C pins are open drain and are ESD clamped to 3.3 V, regardless of the host supply level. The I2C pins are clamped to 3.3 V so that they may be externally pulled up to 3.3 V regardless of IO_VDD_SEL (in register 0x0943).

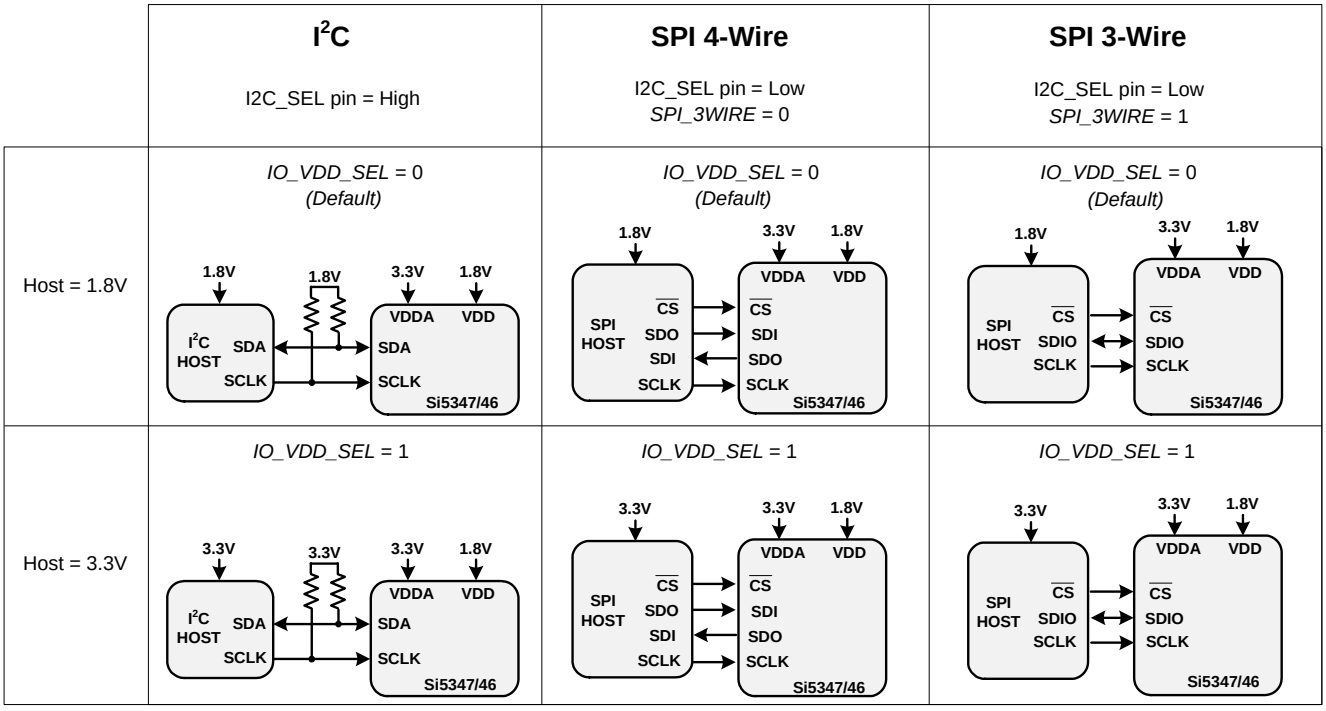


Figure 21. I2C/SPI Device Connectivity Configurations

Table 31 lists register settings of interest for the I2C/SPI.

If neither serial interface is used, leave I2C_SEL unconnected. Pull pins SDA/SDIO, SCLK, A1/SDO, and A0/CS all low.

Note that the Si5347/46 is not I2C fail-safe upon loss of power. Applications that require fail-safe operation should isolate the device from a shared I2C bus.

Table 31. I²C/SPI Register Settings

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
IO_VDD_SEL	0x0943[0]	0x0943[0]	The IO_VDD_SEL configuration bit optimizes the V_{IL}, V_{IH}, V_{OL}, and V_{OH} thresholds to match the VDDS voltage. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I²C or SPI host is operating at 3.3 V and the Si5347/46 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.
SPI_3WIRE	0x002B[3]	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default, this configuration bit is set to the 4-wire option. In this mode the Si5347/46 will accept write commands from a 4-wire or 3- wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to “1”.

8.1. I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 24. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I²C specification as shown in Figure 22. Two address select bits (A0, A1) are provided allowing up to four Si5347/46 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

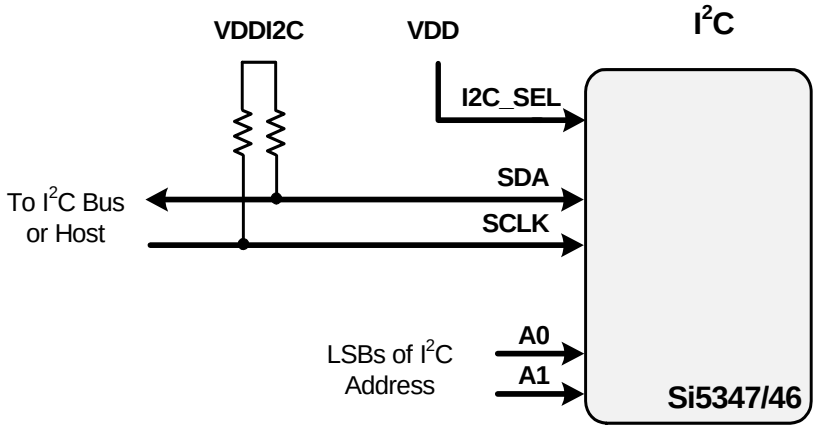


Figure 22. I²C Configuration

The 7-bit slave device address of the Si5347/46 consists of a 5-bit fixed address plus 2 pins which are selectable for the last two bits, as shown in Figure 23.

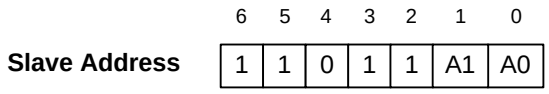


Figure 23. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 26. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

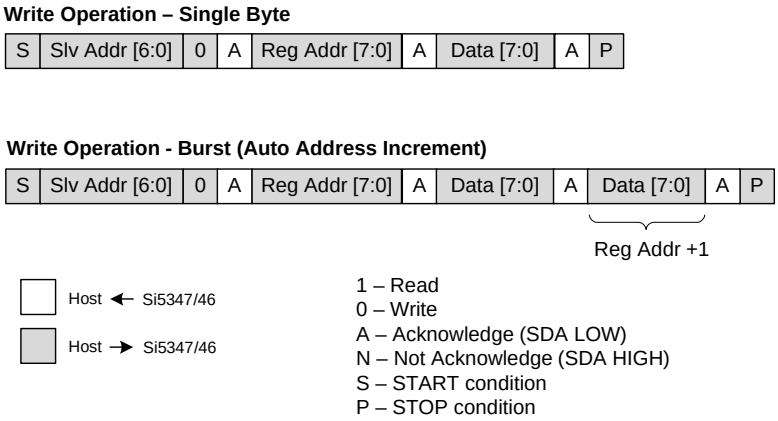


Figure 24. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 25.

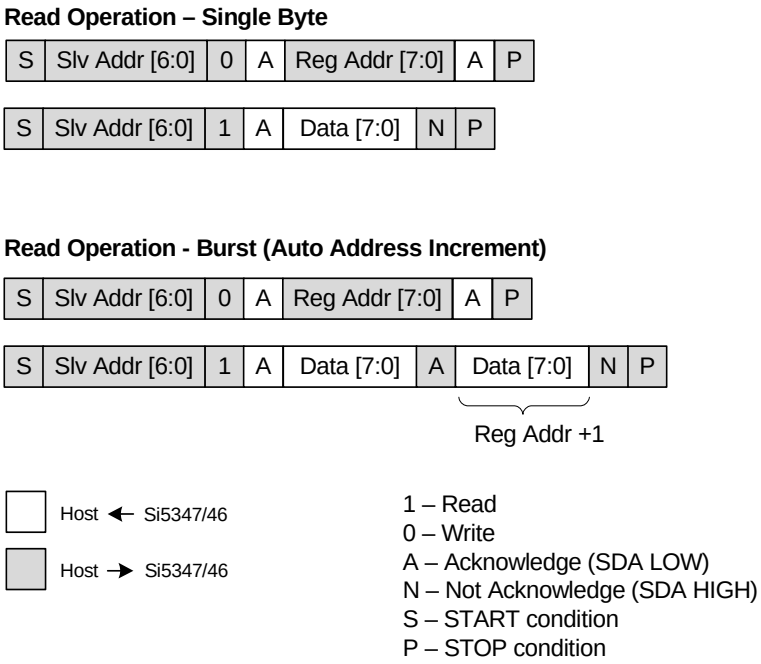


Figure 25. I²C Read Operation

8.2. SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CS), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in Figure 26.

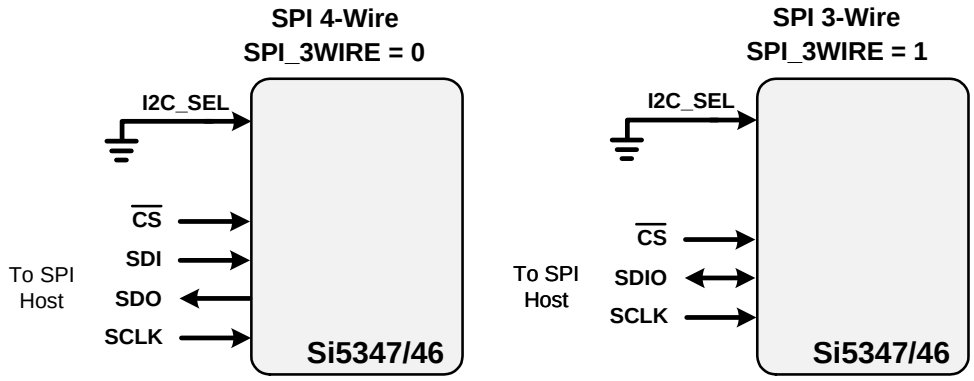


Figure 26. SPI Interface Connections

Table 32. SPI Command Format

Instruction	Ist Byte[1]	2nd Byte	3rd Byte	Nth Byte[2,3]
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Notes:
1. X = don't care (1 or 0).
2. The Burst Write Command is terminated by de-asserting /CS (/CS = high).
3. There is no limit to the number of data bytes that follow the Burst Write Command, but the address will wrap around to zero in the byte after address 255 is written.

Writing or reading data consist of sending a "Set Address" command followed by a "Write Data" or "Read Data" command. The 'Write Data + Address Increment' or "Read Data + Address Increment" commands are available for cases where multiple byte operations in sequential address locations is necessary. The "Burst Write Data" instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. Figure 27 shows an example of writing three bytes of data using the write commands. As can be seen, the "Write Burst Data" command is the most efficient method for writing data to sequential address locations. Figure 28 provides a similar comparison for reading data with the read commands. Note that there is no equivalent burst read; the read increment function is used in this case.

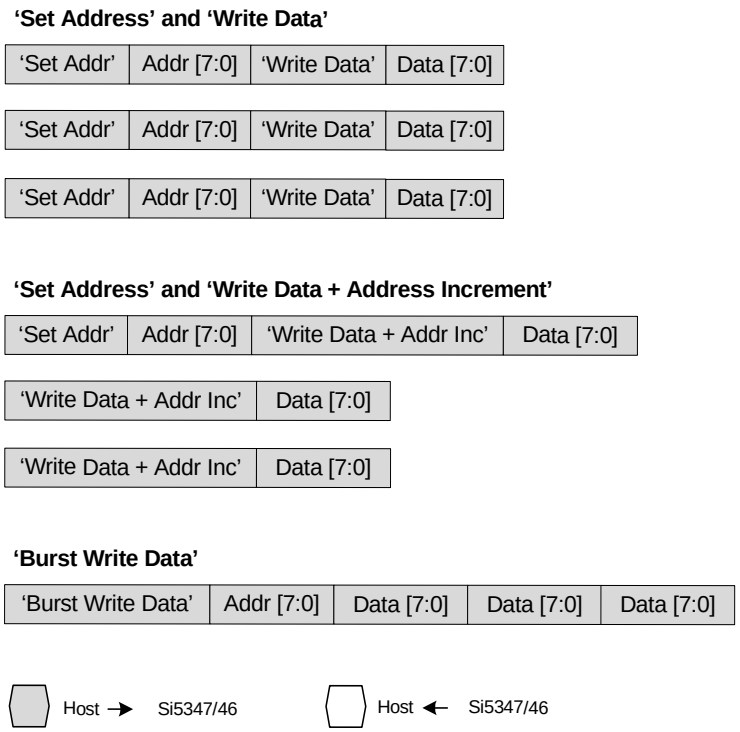


Figure 27. Example Writing Three Data Bytes using the SPI Write Commands

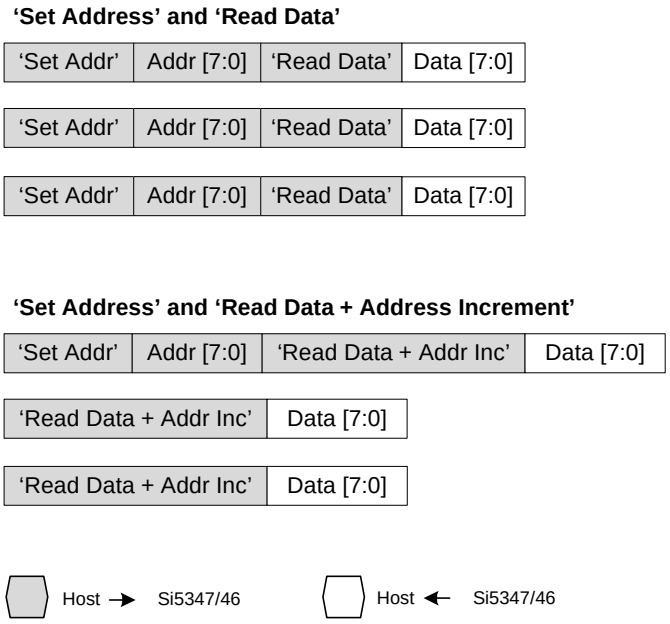


Figure 28. Example of Reading Three Data Bytes Using the SPI Read Commands

The timing diagrams for the SPI commands are shown in Figures 29, 30, 31, and 32.

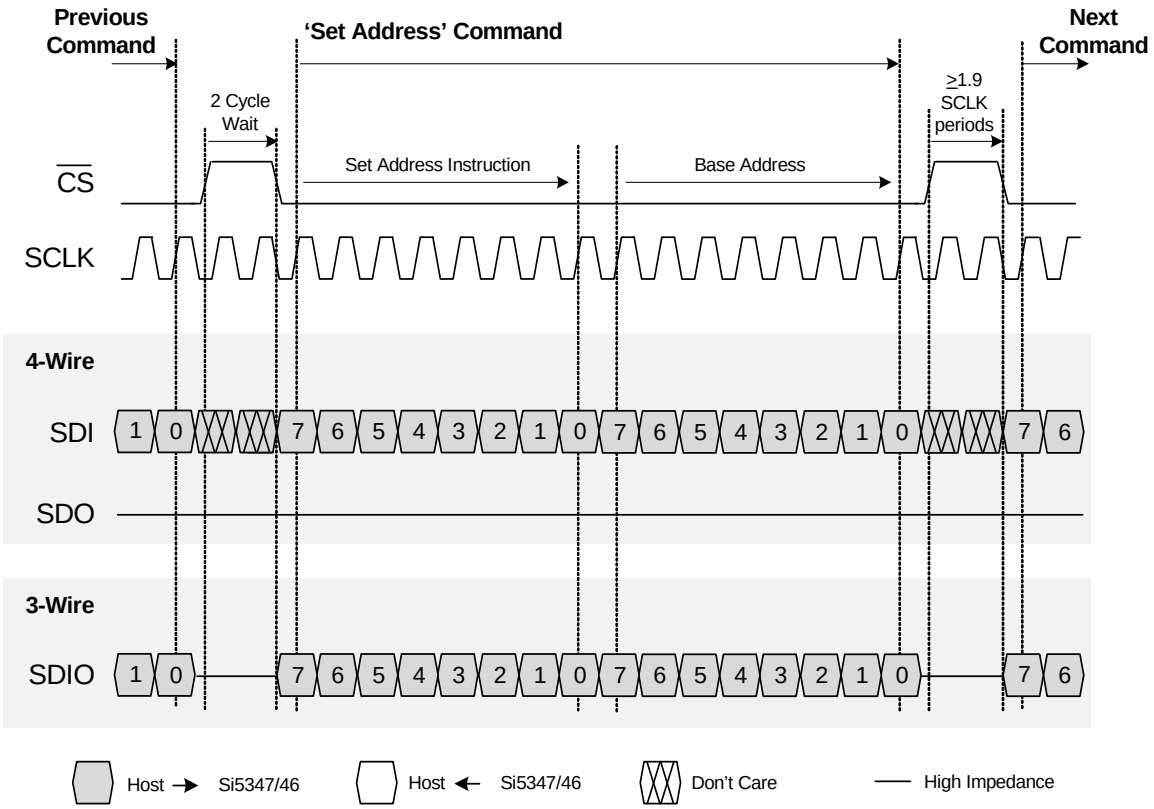


Figure 29. SPI "Set Address" Command Timing

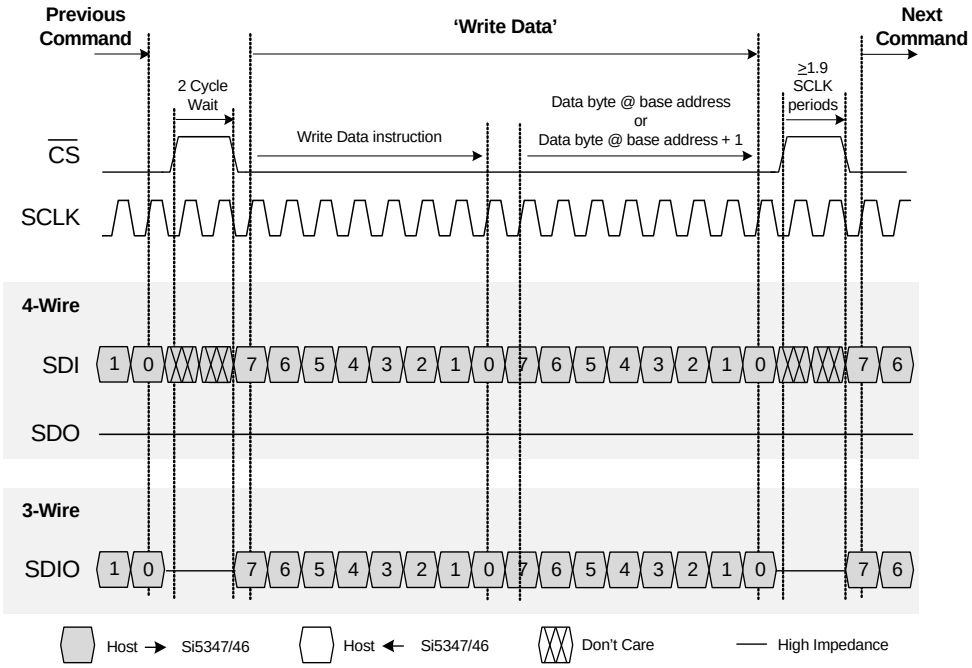


Figure 30. SPI "Write Data" and "Write Data+ Address Increment" Instruction Timing

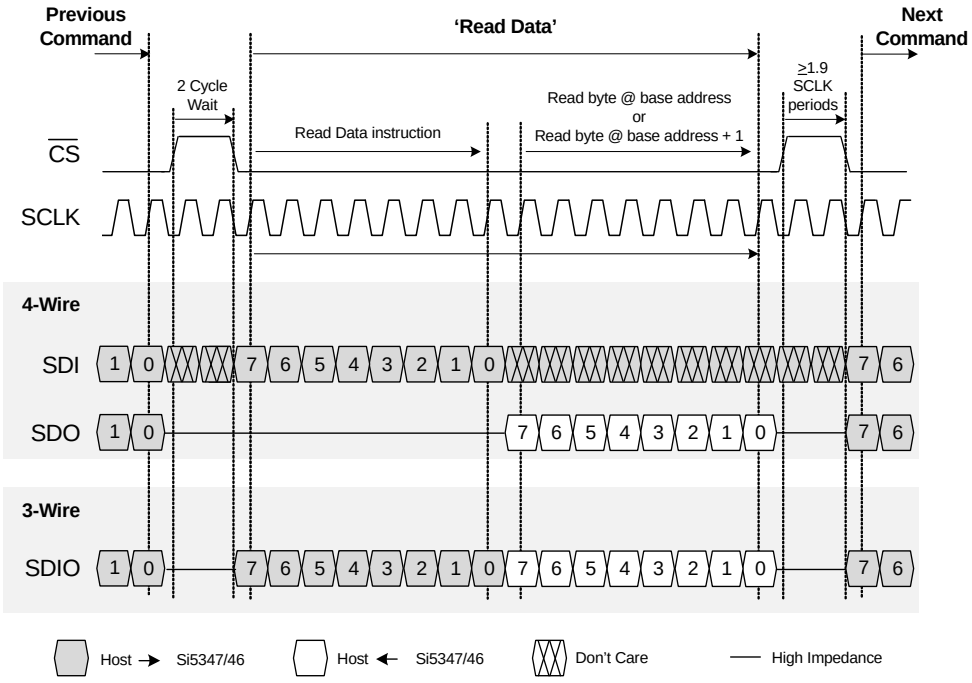


Figure 31. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

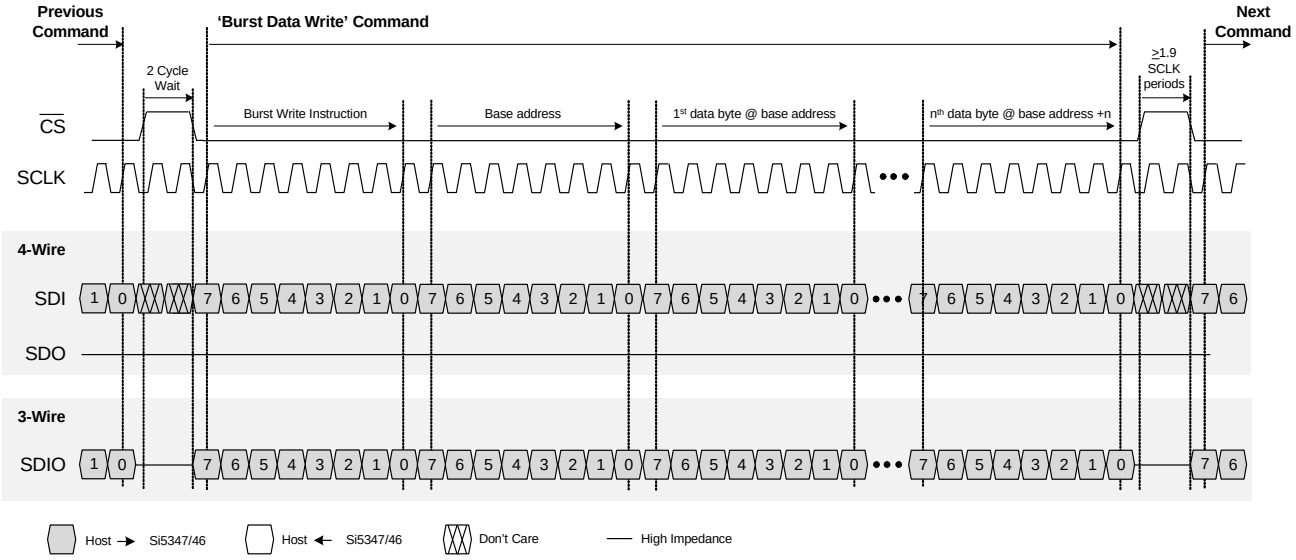


Figure 32. SPI "Burst Data Write" Instruction Timing

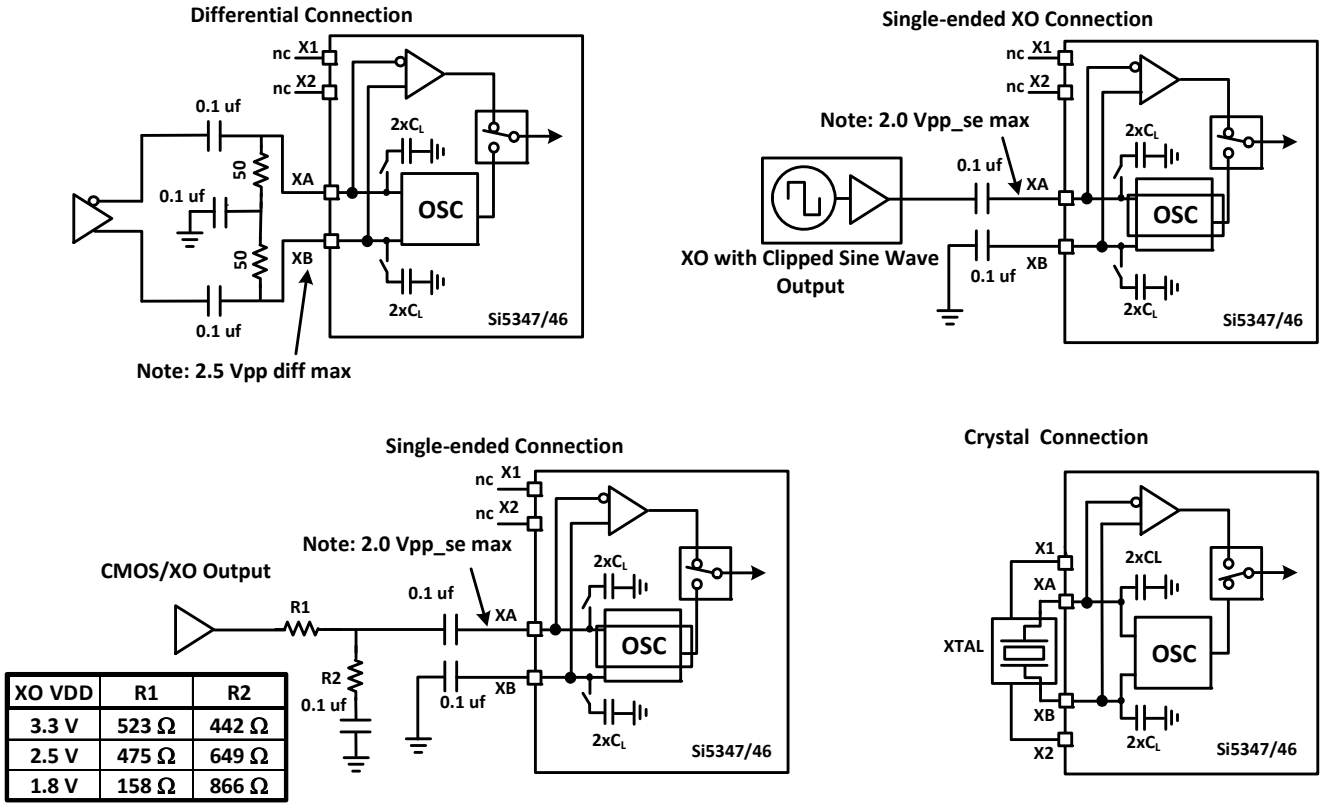
9. Field Programming

To simplify design and software development of systems using the Si5347/46, a field programmer is available in addition to the evaluation board. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5347/46 sample devices. Refer to www.silabs.com/CBProgrammer for information about this kit.

10. Recommended Crystals and External Oscillators

10.1. Performance of External References

An external standard non-pullable crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. A simplified diagram is shown in Figure 33. The device includes internal XTAL loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. Frequency offsets due to CL mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±200 ppm. The recommended crystal suppliers are listed in Table 33 with PCB layout recommendations for the crystal to ensure optimum jitter performance in "11.Crystal and Device Circuit Layout Recommendations" on page 63.



XO VDD	R1	R2
3.3 V	523 Ω	442 Ω
2.5 V	475 Ω	649 Ω
1.8 V	158 Ω	866 Ω

Figure 33. XAXB Crystal Resonator and External Reference Clock Connection Options

The Si5347/46 accepts a clipped sine wave, CMOS, or differential reference clock on the XA/XB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 100 Ω or 50 Ω load. For this reason, place the TCXO as close to the Si5347/46 as possible to minimize PCB trace length. In addition, ensure that both the Si5347/46 and the TCXO are both connected directly to the ground plane. Figure 33 shows the recommended method of connecting a clipped sine wave TCXO to the Si5347/46. Because the Si5347/46 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into the XA interface of the Si5347/46 once it has been ac-coupled. Because the signal is single-ended, the XB input is ac-coupled to ground. Figure 33 illustrates the recommended method of connecting a CMOS rail-to-rail output to the XA/XB inputs of the Si5347/46. The resistor network attenuates the rail-to-rail output swing to ensure that the maximum input voltage swing at the XA pin is less than the data sheet specification. The signal is ac-coupled before connecting it to the Si5347/46 XA input. Again, since the signal is single-ended, the XB input should be ac-coupled to ground.

If an external oscillator is used as the XAXB reference, it is important to use a low jitter source because there is effectively no jitter attenuation from the XAXB pins to the outputs.

For best jitter performance, use a XAXB frequency above 40 MHz. Also, for XAXB frequencies higher than 125 MHz, the PXAXB control must be used to divide the input frequency down below 125 MHz.

For applications that have low wander requirements and are using a loop BW less than 10 Hz, it is recommended that an external TXCO or OCXO be used to avoid the wander inherent in the XTAL.

10.2. Recommended Crystals

Table 33 lists the presently recommended crystals. Other vendors can also supply crystals which meet the specifications given in Figures 34 and 35.

Table 33. Recommended Crystals

Supplier	Part Number	Frequency	Initial Tolerance in ± ppm	Accuracy over –40 °C to +85 °C in ± ppm	C0, Max pF	ESR Max Ω	CL pF	Tested over Temp for Activity Dips?	Drive Level µW	Case Size mm x mm
Connor Winfield	CS-043	48 MHz	15	25	2.0	20	8	No	200	3.2 x 2.5
Connor Winfield	CS-044	54 MHz	15	25	2.0	20	8	No	200	3.2 x 2.5
Hosonic	E3S48.000F08M22SI	48 MHz	20	20	1.5	25	8	No	200	3.2 x 2.5
Hosonic	E2S48.000F08M22SI	48 MHz	20	20	1.5	25	8	No	200	2.5 x 2.0
Hosonic	E3S54.000F08M22SI	54 MHz	20	20	2.0	22	8	No	200	3.2 x 2.5
Hosonic	E2S54.000F08M22SI	54 MHz	20	20	1.5	25	8	No	200	2.5 x 2.0
Kyocera	CX3225SB48000D0FP-JC1	48 MHz	10	15	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB48000D0WP-SC1	48 MHz	15	30	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB48000D0WPTC1	48 MHz	30	60	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB54000D0FP-JC1	54 MHz	10	15	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WP-SC1	54 MHz	15	30	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WPTC1	54 MHz	30	60	2.0	23	8	No	200	3.2 x 2.5
Kyocera	CX3225SB48000D0FP-JC2	48 MHz	10	15	2.0	23	8	Yes	200	3.2 x 2.5
Kyocera	CX3225SB48000D0WP-SC2	48 MHz	15	30	2.0	23	8	Yes	200	3.2 x 2.5

Table 33. Recommended Crystals (Continued)

Supplier	Part Number	Frequency	Initial Tolerance in ± ppm	Accuracy over –40 °C to +85 °C in ± ppm	C0, Max pF	ESR Max Ω	CL pF	Tested over Temp for Activity Dips?	Drive Level µW	Case Size mm x mm
Kyocera	CX3225SB54000D0FP-JC2	54 MHz	10	15	2.0	23	8	Yes	200	3.2 x 2.5
Kyocera	CX3225SB54000D0WP-SC2	54 MHz	15	30	2.0	23	8	Yes	200	3.2 x 2.5
NDK	NX3225SA-48.000M-CS07559	48 MHz	20	30	1.8	23	8	No	200	3.2 x 2.5
NDK	NX3225SA-54.000M-CS07551	54 MHz	20	30	1.8	23	8	No	200	3.2 x 2.5
Siward	XTL571500-S315-006	54 MHz	50	50	2.0	20	8	No	200	3.2 x 2.5
Siward	XTL571500-S315-007	54 MHz	50	50	2.0	20	8	No	200	2.5 x 2.0
Taitien	S0242-X-001-3	54 MHz	20	20	2.0	23	8	No	200	3.2 x 2.5
Taitien	S0242-X-002-3	48 MHz	20	20	2.0	23	8	No	200	3.2 x 2.5
TXC	7M48070012	48 MHz	10	15	2.0	22	8	No	200	3.2 x 2.5
TXC	7M54070010	54 MHz	10	15	2.0	22	8	No	200	3.2 x 2.5
TXC	7M48072001	48 MHz	20	30	2.0	22	8	Yes	200	3.2 x 2.5
TXC	7M54072001	54 MHz	20	30	2.0	22	8	Yes	200	3.2 x 2.5
TXC	7M48072002	48 MHz	10	15	2.0	22	8	Yes	200	3.2 x 2.5
TXC	7M54072002	54 MHz	10	15	2.0	22	8	Yes	200	3.2 x 2.5

In general, a crystal meeting the requirements of Figure 34 or Figure 35 and having a max power rating of at least 200 µW is guaranteed to oscillate. It is preferred that a crystal have a CL rating of 8 pF. Crystals with CL not equal to 8 pF can be used; however, the XAXB_FREQ_OFFSET register word may be needed to compensate for oscillation frequency error. 25 MHz crystals must also meet the 200 mW maximum power rating. Generally, lower crystal frequencies give higher jitter. For example, 25 MHz crystals typically cause the output jitter to increase by approximately 10–40% versus a 48 MHz or 54 MHz crystal.

Some applications may require crystals that have been tested incrementally over the entire temperature range to ensure that the change in crystal resonant frequency over any 2 °C temperature difference is bounded. This is called testing for activity dips. This additional testing adds cost to the crystal. The Si534x products are designed to work with both normally-tested crystals as well as activity dip-tested crystals.

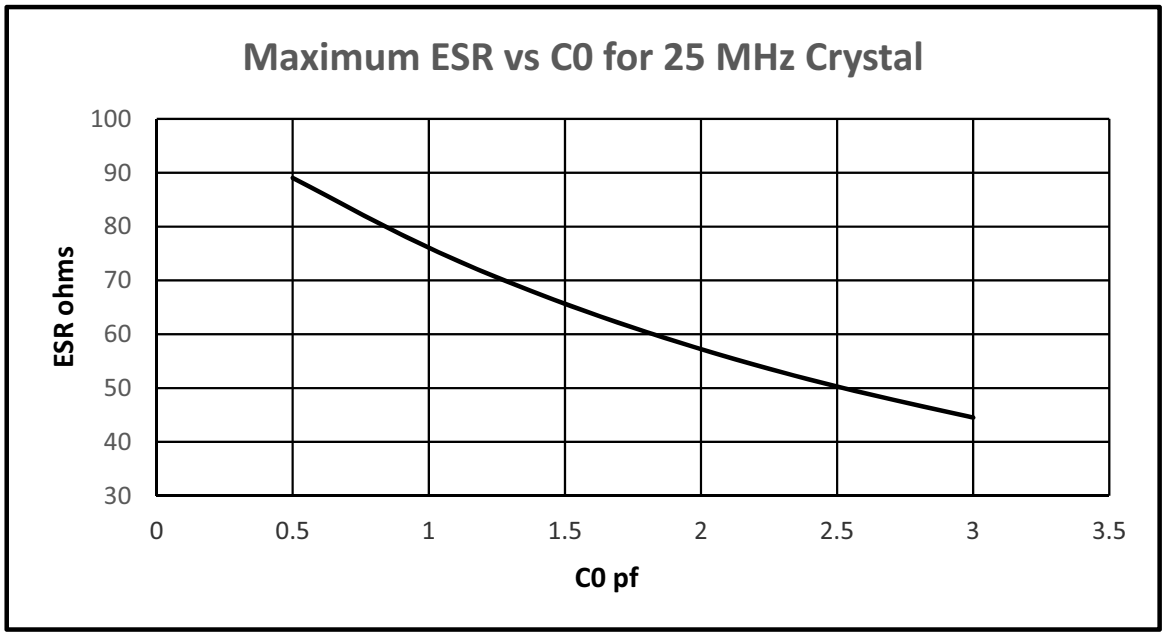


Figure 34. Maximum ESR vs. C0 for 25 MHz Crystal

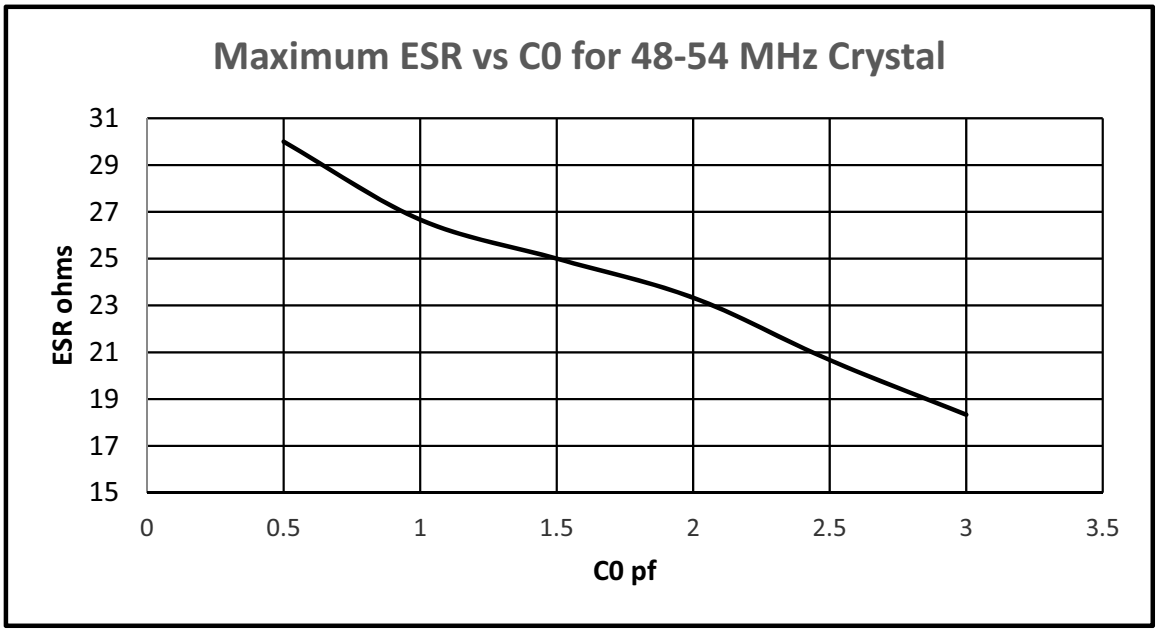


Figure 35. Maximum ESR vs. C0 for 48–54 MHz Crystal

10.3. Recommended Oscillators

Table 34 lists recommended TCXO part numbers for various frequencies.

Table 34. Recommended Oscillator Suppliers

Supplier	Part Number	TCXO/ OCXO	Frequency	Case Size (mm x mm)
Rakon	513872 (40MHz RTX7050A HCMOS)	TCXO	40.000	5x7
NDK	NT7050BB-40.000M-ENA4199B	TCXO	40.000	5x7
Vectron	VT-803-EAH-2870-40M0000	TCXO	40.000	5x3.2
Vectron	VT-803-EAH-2870-49M1520	TCXO	49.152	5x3.2
Vectron	VT-803-EAH-2870-50M0000	TCXO	50.000	5x3.2

10.3.1. Recommended Stratum 3/3E Oscillators

Table 35 lists the recommended suppliers of Stratum 3/3E-capable oscillators.

Table 35. Recommended Stratum 3/3E Oscillator Suppliers

Supplier	Part Number	TCXO/ OCXO	Frequency	Stability over Temp	Temp	Stratum	Package
AVX	OO12.8000000M14070AT	OCXO	12.000	±10	–40/+85 °C	3E	22x25.4
Connor Winfield	OH300-50503CF-012.8M	OCXO	12.800	±5	–20/+70 °C	3E	22x25.4
Connor Winfield	OH300-61003CF-012.8M	OCXO	12.800	±10	–40/+85 °C	3E	22x25.4
NDK	NH14M09WA-12M80-NSA3540A	OCXO	12.800	±10	–20/+70 °C	3E	9x15
NDK	NT14M09TA-12M80-NSA3543A	OCXO	12.800	±20	–40/+85 °C	3E	9x15
Rakon	STP3158	OCXO	12.800	±10	–40/+85 °C	3E	22x25.4
Vectron	OX-2022-EAE-1080-12M8000	OCXO	12.800	±5	–40/+85 °C	3E	25x25
Vectron	OX-4033-EAE-1080-12M8000	OCXO	12.800	±10	–40/+85 °C	3E	12.7x20.3
Connor Winfield	T100F-012.8M	TCXO	12.800	±100	0/+70 °C	3	5x7
Connor Winfield	T200F-012.8M	TCXO	12.800	±200	–40/+85 °C	3	5x7
NDK	NT7050BC-12M800-NSA3517A	TCXO	12.800	±280	–40/+85 °C	3	5x7
Rakon	E6127LF	TCXO	12.800	±280	–20/+70 °C	3	5x7
Rakon	E6518LF	TCXO	12.800	±280	–40/+85 °C	3	5x7
Vectron	VT-803-EAH-2870-12M800	TCXO	12.800	±280	–30/+85 °C	3	5x3

10.4. Register Settings to Configure for External XTAL Reference

The following registers can be used to control and make adjustments for the external reference source used.

10.4.1. XAXB_FREQ_OFFSET Frequency Offset Register

Table 36. XAXB Frequency Offset Register

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
XAXB_FREQ_OFFSET	0202[7:0]-0205[7:0]	0202[7:0]-0205[7:0]	32-bit number adjusts the center frequency of the XTAL in the range of ±1000 ppm.

The VCO locks to the frequency input to the XAXB pins. When an external reference is used, this setting may be used to correct for static frequency offset in the source. It is a 32-bit 2s complement number. The Default value is 0.

10.4.2. XAXB_EXTCLK_EN Reference Clock Selection Register

Table 37. XAXB External Clock Selection Register

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
XAXB_EXTCLK_EN	090E[0]	090E[0]	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

The internal crystal loading capacitors (CL) are disabled when an external clock source is selected.

10.4.3. PXAXB Pre-scale Divide Ratio for Reference Clock Register

Table 38. XAXB Pre-Scale Divide Ratio Register

Setting Name	Hex Address [Bit Field]		Function
	Si5347	Si5346	
PXAXB	0206[1:0]	0206[1:0]	Sets the XAXB input divider value according to Table 39 below.

Table 39 lists the values, along with the corresponding divider ratio.

Table 39. XAXB Pre-Scale Divide Values

Value (Decimal)	PXAXB Divider Value
0	1
1	2
2	4
3	8

11. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered include the following:

- Number and size of the ground vias for the Epad (see "12.4.Grounding Vias" on page 73.)
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace coupling
- Xtal signal coupling
- Xtal layout

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins to provide the best possible performance. The shield should *not* be connected to the ground plane(s), and the layers underneath should have as little area under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

Go to www.silabs.com/Si538x-4x-EVB to obtain Si5347-EVB and Si5346-EVB schematics, layouts, and component BOM files.

11.1. 64-Pin QFN Si5347 Layout Recommendations

This section details the recommended guidelines for the crystal layout of the 64-pin Si5347 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals
- Layer 2: crystal shield
- Layer 3: ground plane
- Layer 4: power distribution
- Layer 5: power routing layer
- Layer 6: input clocks
- Layer 7: output clocks layer
- Layer 8: ground layer

Figure 36 shows the top layer layout of the Si5347 device mounted on the top PCB layer. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. The crystal/ oscillator area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

11.1.1. Si5347 Applications without a Crystal

For applications that do not use a crystal, leave X1 and X2 pins as "no connect". Do not tie to ground. In this case, there is no need for a crystal shield or the voids underneath the shield. The XAXB connection should be treated as a high speed critical path that is ac coupled and terminated at the end of the etch run. The layout should minimize the stray capacitance from the XA pin to the XB pin. Jitter is very critical at the XAXB pins and therefore split termination and differential signaling should be used whenever possible.

11.1.2. Si5347 Crystal Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. *Do not* connect the crystal's X1 or X2 pins to PCB ground.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal shield placed around and under the crystal. See Figure 36 at the bottom left for an illustration of how to create a crystal shield by placing vias connecting the top layer traces to the shield layer underneath. Note the zoom view of the crystal shield layer on the next layer down is shown in Figure 37.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.

5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5347 should have all layers underneath the ground shield removed.

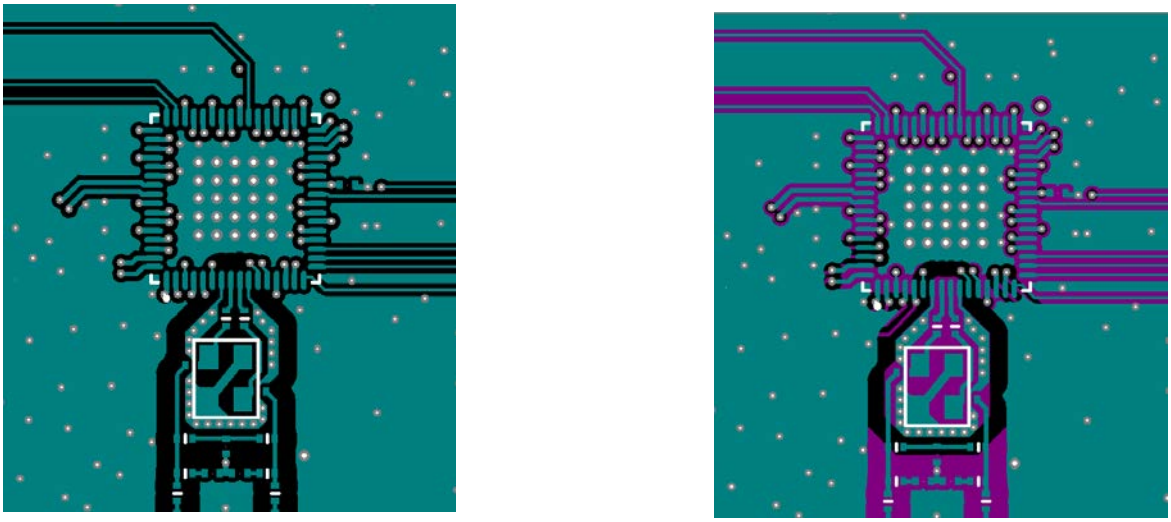


Figure 36. 64-pin Si5347 Crystal Layout Recommendations Top Layer (Layer 1)

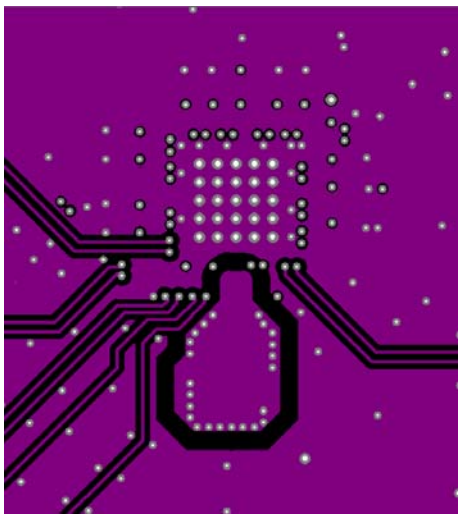


Figure 37. Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2)

Figure 37 shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2 they have a ground shield above below and on the sides for protection.

Figure 38 is the ground plane and shows a void underneath the crystal shield. Figure 39 is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

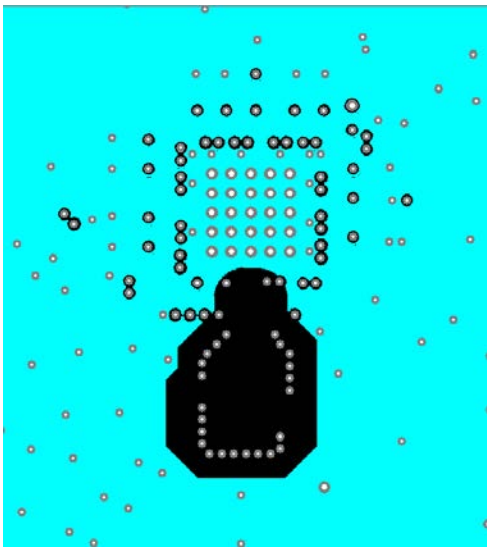


Figure 38. Crystal Ground Plane (Layer 3)

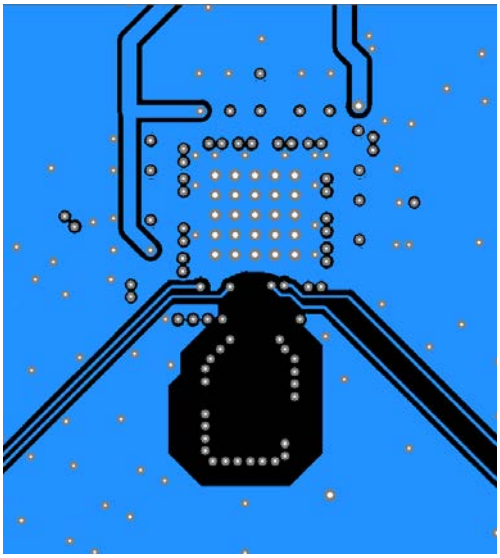


Figure 39. Power Plane (Layer 4)

Figure 40 shows layer 5, which is the power plane with the power routed to the clock output power pins.

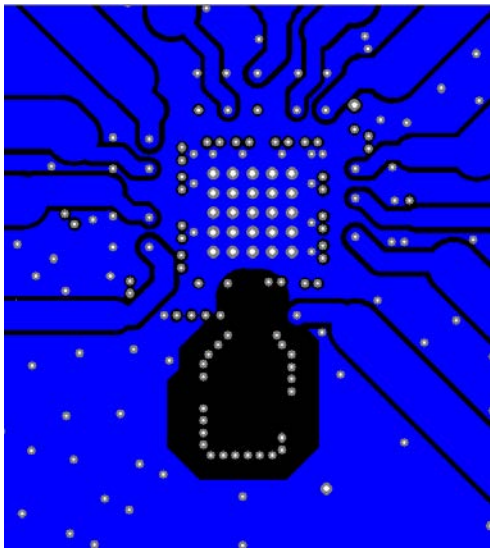


Figure 40. Layer 5 Power Routing on Power Plane (Layer 5)

Figure 41 is another ground plane similar to layer 3.

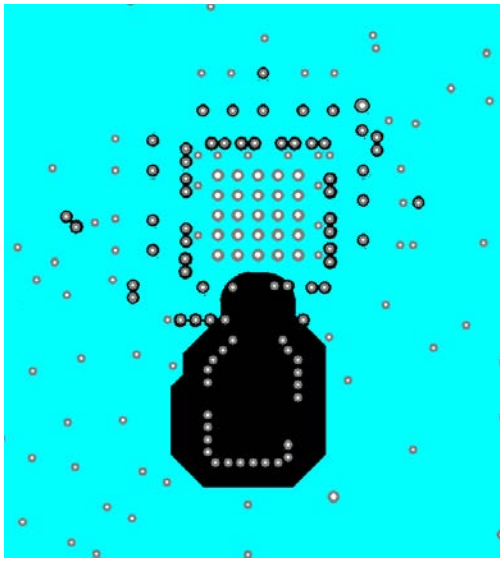


Figure 41. Ground Plane (Layer 6)

11.1.3. Si5347 Output Clocks

Figure 42 shows the output clocks. Similar to the input clocks the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

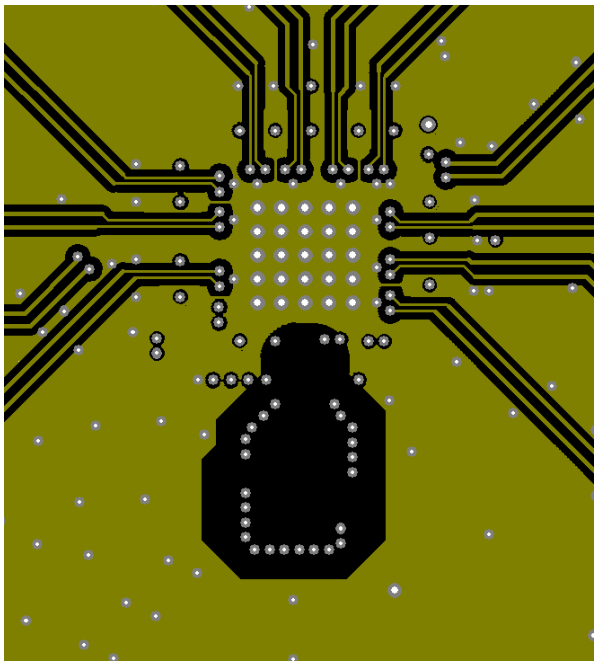


Figure 42. Output Clock Layer (Layer 7)

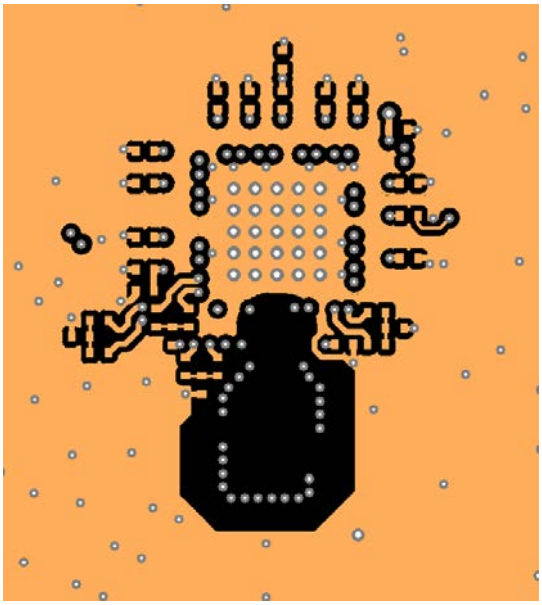


Figure 43. Bottom Layer Ground Flooded (Layer 8)

11.2. 44-Pin QFN Si5346 Layout Recommendations

This section details the layout recommendations for the 44-pin Si5346 device using an example 6-layer PCB.

The following guidelines details images of a six layer board with the following stack:

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: crystal shield, output clocks, ground flooded
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: input clocks, ground flooded
- Layer 6: low-speed CMOS control/status signals, ground flooded

This layout was designed to implement either a crystal or an external oscillator as the XAXB reference. The top layer is flooded with ground. The clock output pins go to layer 2 using vias to avoid crosstalk during transit. When the clock output signals are on layer 2 there is a ground shield above, below and on all sides for protection. Output clocks should always be routed on an internal layer with ground reference planes directly above and below. The plane that has the routing for the output clocks should have ground flooded near the clock traces to further isolate the clocks from noise and other signals.

11.2.1. Si5346 Applications without a Crystal

If the application does not use a crystal, then the X1 and X2 pins should be left as “no connect” and should *not* be tied to ground. In addition, there is no need for a crystal shield or the voids underneath the shield. If there is a differential external clock input on XAXB there should be a termination circuit near the XA and XB pins. This termination circuit should be two 50 Ω resistors and one 0.1 µF cap connected in the same manner as on the other clock inputs (IN0, IN1 and IN2). The clock input on XAXB must be ac-coupled. Care should be taken to keep all clock inputs well isolated from each other as well as any other dynamic signal.

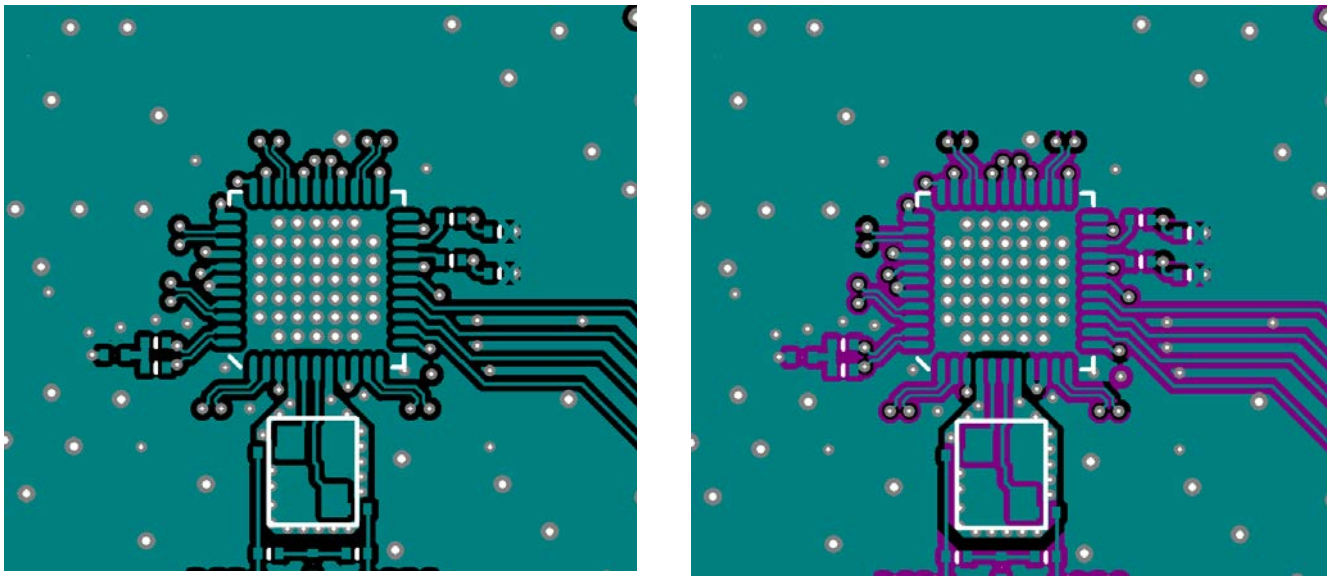


Figure 44. 44-Pin Si5346 Device Layer (Layer 1)

11.2.2. Si5346 Crystal Guidelines

Figure 45 is the second layer. The second layer implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. There should be no less than 12 vias to connect the X1 and X2 planes on layers 1 and 2. These vias are not shown in any other figures. All traces with signals that are not static must be kept well away from the crystal and the X1 and X2 plane.

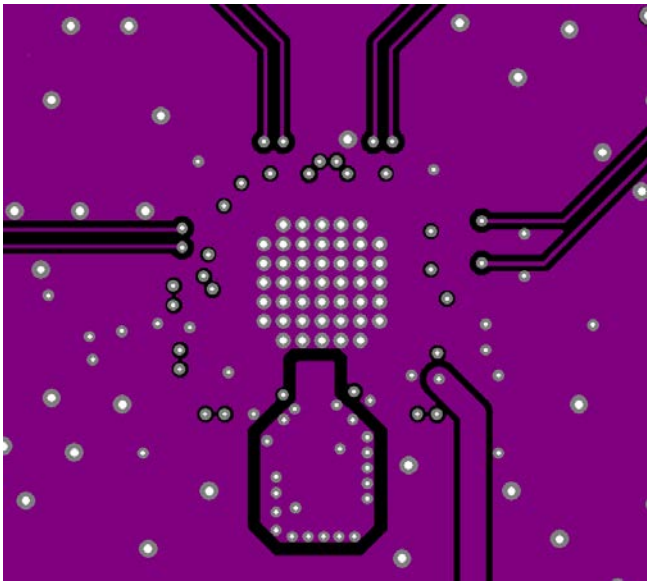


Figure 45. Crystal Shield Layer 2

Figure 46 is the ground plane and shows a void underneath the crystal shield.

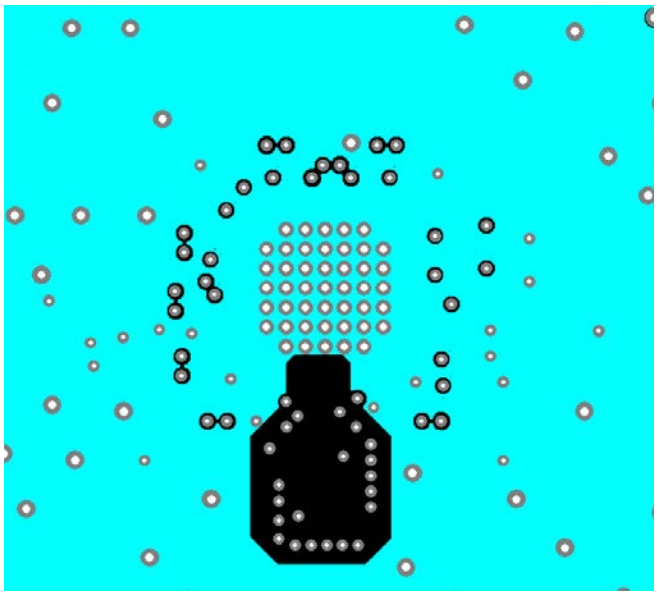


Figure 46. Ground Plane (Layer 3)

Figure 47 is a power plane showing the clock output power supply traces. The void underneath the crystal shield is continued.

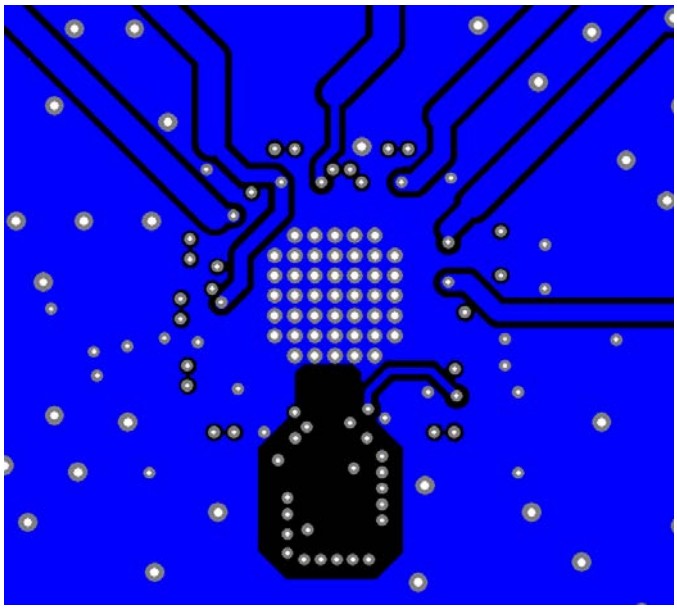


Figure 47. Power Plane and Clock Output Power Supply Traces (Layer 4)

Figure 48 shows layer 5 and the clock input traces. Similar to the clock output traces, they are routed to an inner layer and surrounded by ground to avoid crosstalk.

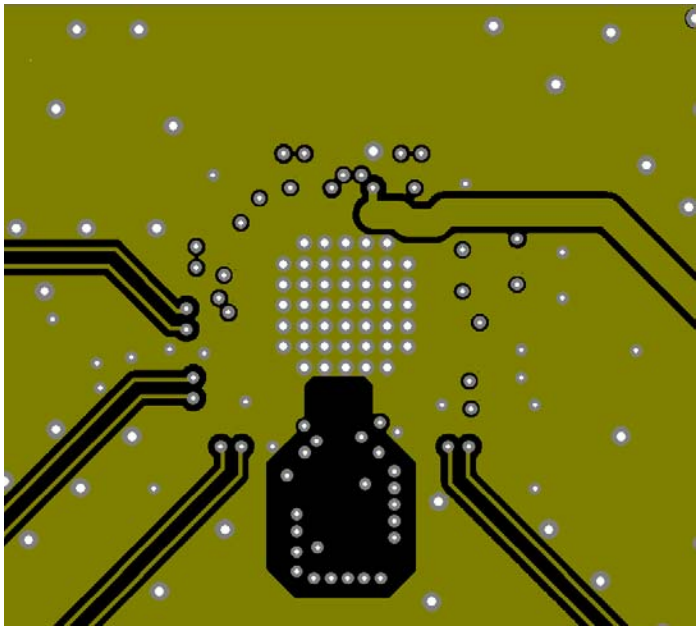


Figure 48. Clock Input Traces (Layer 5)

Figure 49 shows the bottom layer, which continues the void underneath the shield. Layer 6 and layer 1 are mainly used for low speed CMOS control and status signals for which crosstalk is not a significant issue. PCB ground can be placed under the X1 and X2 shield as long as the PCB ground is at least 0.05 inches below it.

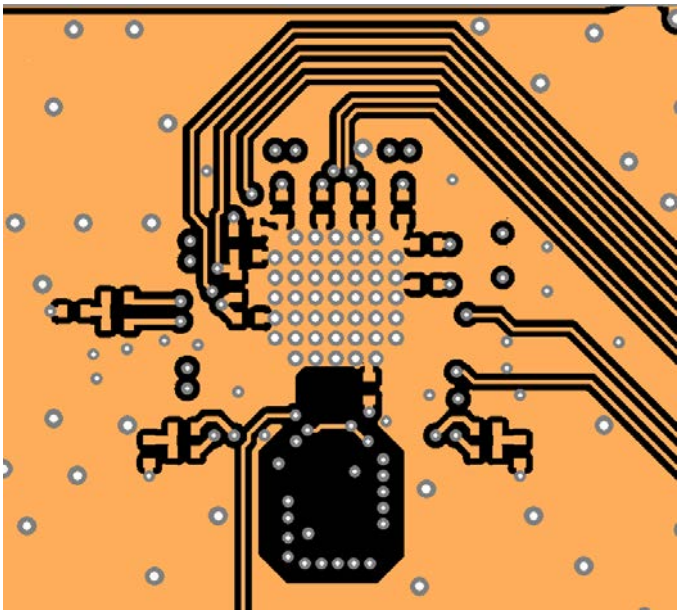


Figure 49. Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer)

For any high-speed, low-jitter application, the clock signal runs should be impedance-controlled to 100 Ω differential or 50 Ω single-ended. Differential signaling is preferred because of its increased immunity to common-mode noise. All clock I/O runs should be properly terminated.

12. Power Management

12.1. Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed in Table 40 are used for powering down different features.

Table 40. Power Management Registers

Setting Name	Hex Address [Bit Field]			Function
	Si5347A/B	Si5347C/D	Si5346	
PDN	0x001E[0]			This bit allows powering down the device. The serial interface remains powered during power down mode and the registers are available to be read and written.
OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN OUT4_PDN OUT5_PDN OUT6_PDN OUT7_PDN	0x0108[0] 0x0112[0] 0x0117[0] 0x011C[0] 0x0126[0] 0x012B[0] 0x0130[0] 0x013A[0]	0x0108[0] 0x011C[0] 0x0126[0] 0x012B[0] — — — —	0x0112[0] 0x0117[0] 0x0126[0] 0x012B[0] — — — —	Powers down unused clock outputs. When powered down, output pins will be high-impedance with a light pull-down effect.
OUT_PDN_ALL	0x0145[0]			Power down all output drivers

12.2. Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5347/46 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 1 µF 0402 ceramic capacitor on each VDD for optimal performance. It is also suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed.

12.3. Power Supply Sequencing

Four classes of supply voltages exist on the Si5347/46:

1. VDD = 1.8 V (Core digital supply)
2. VDDA = 3.3 V (Analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)
4. VDDS = 1.8/3.3 V ± 5% (Digital I/O supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. VDDS has no effect on output clock alignment.

If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST 0x001C[0] or Hard Reset 0x001E[1] register bits or driving the RSTB pin. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

12.4. Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground and primary heat transfer path. Hence it is important to minimize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

13. Base vs. Factory Preprogrammed Devices

The Si5347/46 devices can be ordered as “base” or “factory-preprogrammed” (also known as “custom OPN”) versions.

13.1. ”Base” Devices (Also Known as “Blank” Devices)

- Example “base” orderable part numbers (OPNs) are of the form “Si5341A-A-GM” or “Si5340B-A-GM”.
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 48 MHz crystal on the XAXB reference and a 1.8 V compatible I/O voltage setting for the host I2C/SPI interface.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the on-line lookup utility at: www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx to access the default configuration plan and register settings for any base OPN.

13.2. “Factory Preprogrammed” (Custom OPN) Devices

- Factory preprogammed devices use a “custom OPN”, such as Si5341A-A-xxxxx-GM, where “xxxxx” is a sequence of characters assigned by Silicon Labs for each customer-specific configuration. These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder software is required to select among all of these options and to produce a project file that Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx.
- Custom OPN devices include a device top mark that includes the unique OPN ID. Refer to the device data sheet’s Ordering Guide and Top Mark sections for more details.

Both “base” and “factory preprogrammed” devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see "4.1.2.NVM Programming" on page 16).

14. Register Map

14.1. Register Map Overview and Default Settings Values

The Si5347/46 family parts have large register maps that are divided into separate “Pages” of register banks. This allows more register addresses than either the I^2C or SPI serial interface standards 8-bit addressing provide. Each page has a maximum of 256 addresses, however not all addresses are used on every page. Every register has a maximum data size of 8-bits, or 1 byte. Writing the page number to the 8-bit serial interface address of 0x01 on any page (0x0001, 0x0101, 0x0201, etc.) updates the page selection for subsequent register reads and writes. For example, to access the value in register 0x040E, it is first necessary to write the page value 0x04 to serial interface register address 0x01. At this point, the value of serial interface address 0x0E (0x040E) may be read or written. Note that is it not necessary to write the page select register again when accessing other registers on the same page. Similarly, the read-only DEVICE_READY status is available from every page at serial interface address 0xFE (0x00FE, 0x01FE, 0x02FE, etc.).

It is recommended to use dynamic Read-Modify-Write methods when writing to registers which contain multiple settings, such as register 0x0011. To do this, first read the current contents of the register. Next, update only the select bit or bits that are being modified. This may involve using both logical AND and logical OR operations. Finally, write the updated contents back to the register. Writing to pages, registers, or bits not documented below may cause undesired behavior in the device.

Details of the register and settings information are organized hierarchically below. To find the relevant information for your application, first choose the section corresponding to the base part number, Si5347 or Si5346, for your design. Then, choose the section under that for the page containing the desired register(s). For example, to find information on Page 2 register 0x02030 for the Si5346, see "14.4.3.Page 2 Registers Si5346" on page 215.

Default register contents and settings differ for each device part number, or OPN. This information may be found by searching for the Custom OPN for your device using the link below. Both Base/Blank and Custom OPNs are available there. See the previous section on “Base vs. Factory Preprogrammed Devices" for more information on part numbers. The Private Addendum to the datasheet lists the default settings and frequency plan information. You must be logged into the Silicon Labs website to access this information. The Public addendum gives only the general frequency plan information (www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx).

Table 41. Register Map Page Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, and other configuration
Page 1	0100h	256	Output clock configuration
Page 2	0200h	512	P and R dividers, user scratch area
Page 3	0300h	768	Internal divider value updates
Page 4	0400h	1024	DSPLLA
Page 5	0500h	1280	DSPLLB
Page 6	0600h	1536	DSPLLC, Si5347 only
Page 7	0700h	1792	DSPLLD, Si5347 only
Page 9	0900h	2304	Control IO configuration
Page A	0A00h	2560	Internal divider enables
Page B	0B00h	2816	Internal clock disables and control

R = Read Only

R/W = Read Write

S = Self Clearing

A self-clearing bit will be cleared by the device once the operation initiated by this bit is complete. Registers with “sticky” flag bits, such as LOS0_FLG, are cleared by writing “0” to the bit that has been automatically set high by the device.

14.2. Si5347A/B Register Map

14.2.1. Page 0 Registers Si5347A/B

Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Register 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Register 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x47	Four-digit “base” part number, one nibble per digit Example: Si5347A-A-GM. The base part number (OPN) is 5347, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/synthesis mode. 0 = A 1 = B 2 = C 3 = D

Refer to the device data sheet Ordering Guide section for more information about device grades.

Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5347C-**A**12345-GM, the device revision is “A” and stored as 0

Register 0x0006–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0006	3:0	R	SPECIAL	ClockBuilder Pro version that was used to generate the NVM image Major.Minor.Revision.Special
0x0006	7:4	R	REVISION	
0x0007	7:0	R	MINOR	
0x0008	0	R	MINOR	
0x0008	4:1	R	MAJOR	
0x0008	7:5	R	TOOL	
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5347C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5347C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5347 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Register 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address

Register 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if there is no signal detected on the XAXB input signal.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Register 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [3 2 1 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [3 2 1 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Register 0x000EHoldover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Register 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4
DSPLL_B corresponds to bit 5
DSPLL_C corresponds to bit 6
DSPLL_D corresponds to bit 7

Register 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to clear the flag.
0x0011	3	R	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Register 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]
- Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Register 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Register 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Register 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOSREF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	LOL_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this register is 0x035.

Register 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1: To mask the clock input OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]
- Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]
- DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019 [2], HOLD_INTR_MSK_PLL 0x0019 [6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019 [3], HOLD_INTR_MSK_PLL 0x0019 [7]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: Initialize and calibrate the entire device. This will also align the outputs from the four DSPLLs.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB
0x001C	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715.

Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1: To put the device into low power mode
0x001E	1	S	HARD_RST	Perform hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Resets all output R dividers to the same state.

Register 0x0020 DSPLL_SEL0,1 Control of FINC/FDEC

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	DSPLL_SELx_EN	0: DSPLL_SEL0,1 pins and bits are disabled. 1: DSPLL_SEL0,1 pins or DSPLL_SELx_REG bits are enabled. See DSPLL_SELX_REG_EN.
0x0020	1	R/W	DSPLL_SELx_REG_EN	Only functions when DSPLL_SELx_EN = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	2	R/W	DSPLL_SEL0_REG	Register version of the pin DSPLL_SEL0. Used to select which PLL (M divider) is affected by FINC/FDEC.
0x0020	3	R/W	DSPLL_SEL1_REG	Register version of the pin DSPLL_SEL1. Used to select which PLL (M divider) is affected by FINC/FDEC.

Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	0: $\overline{OE0}$ and $\overline{OE1}$ pins disable 1: OE0 and OE1 register disable
0x0022	1	R/W	OE0_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE0 selected outputs 1: Enable OE0 selected outputs
0x0022	2	R/W	OE1_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE1 selected outputs 1: Enable OE1 selected outputs

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Register 0x0023-0x0024 OE0 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description

Register 0x0023-0x0024 OE0 Output Disable Selection

0x0023	1 3 4 5 7	R/W	OE0_OUT0_SEL OE0_OUT1_SEL OE0_OUT2_SEL OE0_OUT3_SEL OE0_OUT4_SEL	0: Output ignores OE0 1: Output disabled by OE0 See Table 27, “Output Driver Disable Sources Summary,” on page 41 for additional information.
0x0024	0 1 3	R/W	OE0_OUT5_SEL OE0_OUT6_SEL OE0_OUT7_SEL	

Register 0x0025-0x0026 OE1 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0025	1 3 4 5 7	R/W	OE1_OUT0_SEL OE1_OUT1_SEL OE1_OUT2_SEL OE1_OUT3_SEL OE1_OUT4_SEL	0: Output ignores OE1 1: Output disabled by OE1 See Table 27, “Output Driver Disable Sources Summary,” on page 41 for additional information.
0x0026	0 1 3	R/W	OE1_OUT5_SEL OE1_OUT6_SEL OE1_OUT7_SEL	

Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI.

Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Input 3 (IN3): LOS_EN[3]

Register 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Register 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Register 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Register 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Register 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable 1: To enable
0x003F	7:4	R/W	FAST_OOF_EN	

Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Register 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0048	7:0	R/W	OOF2_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0049	7:0	R/W	OOF3_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Register 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004C	7:0	R/W	OOF2_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004D	7:0	R/W	OOF3_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Register 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	7:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	7:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	7:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Register 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	7:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	7:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	3:0	R/W	LOL_SLW_EN_PLL[D:A]	0: To disable fast LOL. 1: To enable fast LOL.

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Register 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.

Register 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm.

The following are the thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm
- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

Register 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

The following are the thresholds for the value that is placed in the four bits of the DSPLLs. ClockBuilder Pro sets these values.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm
- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	3:0	R/W	LOL_TIMER_EN_PLL	0: To disable 1: To enable

LOL_TIMER extends the time after the LOL clear threshold has been met that LOL stays active.

DSPLL A bit 0

DSPLL B bit 1

DSPLL C bit 2

DSPLL D bit 3

Register 0x00A3-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A3	7:0	R/W	LOL_CLR_DELAY_PLLA	35-bit value
0x00A4	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A5	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A6	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A7	2:0	R/W	LOL_CLR_DELAY_PLLA	

Register 0x00A8-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY_PLLB	35-bit value
0x00A9	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AA	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AB	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AC	2:0	R/W	LOL_CLR_DELAY_PLLB	

Register 0x00AD-0x00B1 LOL Clear Delay DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x00AD	7:0	R/W	LOL_CLR_DELAY_PLLC	35-bit value
0x00AE	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00AF	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00B0	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00B1	2:0	R/W	LOL_CLR_DELAY_PLLC	

Register 0x00B2-0x00B6 LOL Clear Delay DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x00B2	7:0	R/W	LOL_CLR_DELAY_PLLD	35-bit value
0x00B3	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B4	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B5	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B6	2:0	R/W	LOL_CLR_DELAY_PLLD	

Register 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	5:0	R	ACTIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See “4.1.1. Updating Registers during Device Operation” for a detailed description of how to program the NVM.

Register 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See "4.1.2.NVM Programming" on page 16.

Register 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	1: To download NVM.

When set, this bit will read the NVM down into the volatile memory.

Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is most useful after powerup, after a hard reset 0x001E[1], or after an NVM write 0x00E3 to determine when the operation is complete. The “Device Ready” register is available on every page in the device at 0x##FE, where “##” represents the page address.

14.2.2. Page 1 Registers Si5347A/B

Register 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers 1: Pass through the output enables.

Register 0x0108, 0x0112, 0x0117, 0x011C, 0x0126, 0x012B, 0x0130, 0x013A
Clock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0108 0x0112 0x0117 0x011C 0x0126 0x012B 0x0130 0x013A	0	R/W	OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN OUT4_PDN OUT5_PDN OUT6_PDN OUT7_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pull-down effect.
0x0108 0x0112 0x0117 0x011C 0x0126 0x012B 0x0130 0x013A	1	R/W	OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE OUT7_OE	0: To disable the output 1: To enable the output
0x0108 0x0112 0x0117 0x011C 0x0126 0x012B 0x0130 0x013A	2	R/W	OUT0_RDIV_FORCE OUT1_RDIV_FORCE OUT2_RDIV_FORCE OUT3_RDIV_FORCE OUT4_RDIV_FORCE OUT5_RDIV_FORCE OUT6_RDIV_FORCE OUT7_RDIV_FORCE	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2

The output drivers are all identical. See "6.2.Performance Guidelines for Outputs" on page 32.

Register 0x0109, 0x0113, 0x0118, 0x011D, 0x0127, 0x012C, 0x0131, 0x013B Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT OUT4_FORMAT OUT5_FORMAT OUT6_FORMAT OUT7_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN OUT4_SYNC_EN OUT5_SYNC_EN OUT6_SYNC_EN OUT7_SYNC_EN	0: Disable 1: Enable
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE OUT4_DIS_STATE OUT5_DIS_STATE OUT6_DIS_STATE OUT7_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high
0x0109 0x0113 0x0118 0x011D 0x0127 0x012C 0x0131 0x013B	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV OUT4_CMOS_DRV OUT5_CMOS_DRV OUT6_CMOS_DRV OUT7_CMOS_DRV	LVCMOS output impedance drive strength see "Table 23.LVCMOS Drive Strength Control Registers" on page 38.

The output drivers are all identical.

Register 0x010A, 0x0114, 0x0119, 0x011E, 0x0128, 0x012D, 0x0132, 0x0137 Output Amplitude and Common Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x010A 0x0114 0x0119 0x011E 0x0128 0x012D 0x0132 0x013C	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM OUT4_CM OUT5_CM OUT6_CM OUT7_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.
0x010A 0x0114 0x0119 0x011E 0x0128 0x012D 0x0132 0x013C	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL OUT4_AMPL OUT5_AMPL OUT6_AMPL OUT7_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Register 0x010B, 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133, 0x0138 Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x010B 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x0138	1:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL OUT4_MUX_SEL OUT5_MUX_SEL OUT6_MUX_SEL OUT7_MUX_SEL	Output driver 0 input mux select.This selects the source of the output clock. 0: DSPLL A 1: DSPLL B 2: DSPLL C 3: DSPLL D
0x010B 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133 0x0138	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV OUT4_INV OUT5_INV OUT6_INV OUT7_INV	0: CLK and $\overline{\text{CLK}}$ not inverted 1: $\overline{\text{CLK}}$ inverted 2: CLK and $\overline{\text{CLK}}$ inverted 3: CLK inverted These bits have no effect on differential outputs.

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical.

Register 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	6	R/W	OUT_DIS_MSK_LOSXAXB	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition

Register 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MASK_LOL_PLL[D:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs

Bit 0 LOL_DSPLL_A mask
Bit 1 LOL_DSPLL_B mask
Bit 2 LOL_DSPLL_C mask
Bit 3 LOL_DSPLL_D mask

Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Setting Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0: No effect 1: All drivers powered down

14.2.3. Page 2 Registers Si5347A/B

Register 0x0202-0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Setting Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this frequency reference with high resolution. XAXB_FREQ_OFFSET can be used to compensate for the XTAL frequency error. This will cause the free run frequency to be more accurate. It is programmed as a two's complement number. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This valid with external clock sources, not crystals.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 3 = pre-scale value 8
- Note that changing this register furing operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Table 42. Si5347A/B P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values.

Register 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x024A	7:0	R/W	R0_REG	24-bit Integer output divider divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 43. Si5347A/B R1–R7 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0250-0x0252	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0253-0x0255	R2_REG	24-bit Integer Number	0x024A-0x024C
0x0256-0x0258	R3_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R4_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R5_REG	24-bit Integer Number	0x024A-0x024C
0x0262-0x0264	R6_REG	24-bit Integer Number	0x024A-0x024C
0x0268-0x026A	R7_REG	24-bit Integer Number	0x024A-0x024C

Register 0x026B–0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5347C-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5347C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5347C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5347 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

14.2.4. Page 3 Registers Si5347A/B

Register 0x030C DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE_PLLA	Must write a 1 to this bit to cause DSPLLA internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0317 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0317	0	S	N1_UPDATE_PLLB	Must write a 1 to this bit to cause DSPLL B internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0322 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0322	0	S	N2_UPDATE_PLLC	Must write a 1 to this bit to cause DSPLL C internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x032D DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x032D	0	S	N3_UPDATE_PLLD	Must write a 1 to this bit to cause DSPLL D internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.2.5. Page 4 Registers Si5347A/B

Register 0x0407

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL A is currently using.

Register 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	7:0	R/W	BW0_PLLA	48 bit integer number
0x0409	15:8	R/W	BW1_PLLA	
0x040A	23:16	R/W	BW2_PLLA	
0x040B	31:24	R/W	BW3_PLLA	
0x040C	39:32	R/W	BW4_PLLA	
0x040D	47:40	R/W	BW5_PLLA	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	7:0	R/W	FAST_BW0_PLLA	48-bit integer number
0x040F	15:8	R/W	FAST_BW1_PLLA	
0x0410	23:16	R/W	FAST_BW2_PLLA	
0x0411	31:24	R/W	FAST_BW3_PLLA	
0x0412	39:32	R/W	FAST_BW4_PLLA	
0x0413	47:40	R/W	FAST_BW5_PLLA	
0x0414	0	S	BW_UPDATE_PLLA	0: No effect 1: Update both the Normal and Fast-lock BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56- bit number.
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	5:0	R/W	M_FRAC_EN_PLLA	DSPLL A M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.

Register 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Register 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register-based clock selection.

Register 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FAST-LOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Register 0x042C DSPLL A Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Must be set to 1 for normal operation.
0x042C	4	R/W	HOLD_EXIT_BW_SEL_PLLA	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Register 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x043F	2	R	FASTLOCK_STATUS_PLLA	0: Not in Fastlock 1: Fastlock active

14.2.6. Page 5 Registers Si5347A/B

Register 0x0507

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL B is currently using.

Register 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	7:0	R/W	BW0_PLLB	48 bit integer number
0x0509	15:8	R/W	BW1_PLLB	
0x050A	23:16	R/W	BW2_PLLB	
0x050B	31:24	R/W	BW3_PLLB	
0x050C	39:32	R/W	BW4_PLLB	
0x050D	47:40	R/W	BW5_PLLB	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.The BW_UPDATE bit (register 0x0514[0] must be set to cause the normal and fast bandwidth parameters to be active.

Register 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	7:0	R/W	FAST_BW0_PLLB	48-bit integer number
0x050F	15:8	R/W	FAST_BW1_PLLB	
0x0510	23:16	R/W	FAST_BW2_PLLB	
0x0511	31:24	R/W	FAST_BW3_PLLB	
0x0512	39:32	R/W	FAST_BW4_PLLB	
0x0513	47:40	R/W	FAST_BW5_PLLB	
0x0514	0	S	BW_UPDATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLB to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	5:0	R/W	M_FRAC_EN_PLLB	DSPLL B M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEPW_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEPW_PLLB	
0x0525	23:16	R/W	M_FSTEPW_PLLB	
0x0526	31:24	R/W	M_FSTEPW_PLLB	
0x0527	39:32	R/W	M_FSTEPW_PLLB	
0x0528	47:40	R/W	M_FSTEPW_PLLB	
0x0529	55:48	R/W	M_FSTEPW_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0515–0x051F.

Register 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FAST-LOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Register 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL_PLLB	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x052F DSPLLB Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY_PLLB	5-bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Register 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	IN_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.
IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]
IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]
IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]
IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Register 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x053F DSPLL B Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x053F	2	R	FASTLOCK_STATUS_PLLB	0: Not in Fastlock 1: Fastlock active

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Register 0x0607

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL C is currently using.

Register 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	7:0	R/W	BW0_PLLC	48-bit integer number
0x0609	15:8	R/W	BW1_PLLC	
0x060A	23:16	R/W	BW2_PLLC	
0x060B	31:24	R/W	BW3_PLLC	
0x060C	39:32	R/W	BW4_PLLC	
0x060D	47:40	R/W	BW5_PLLC	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	7:0	R/W	FAST_BW0_PLLC	48-bit integer number
0x060F	15:8	R/W	FAST_BW1_PLLC	
0x0610	23:16	R/W	FAST_BW2_PLLC	
0x0611	31:24	R/W	FAST_BW3_PLLC	
0x0612	39:32	R/W	FAST_BW4_PLLC	
0x0613	47:40	R/W	FAST_BW5_PLLC	
0x0614	0	S	BW_UPDATE_PLLC	0: No effect. 1: Update both the Normal and Fastback BWs for PLL C.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLC to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	56-bit number
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	32-bit number
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UPDATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0621 DSPLL C M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	5:0	R/W	M_FRAC_EN_PLLC	DSPLL C M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.

Register 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	56-bit number
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F.

Register 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLC is out of lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Register 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	Must be set to 1 for normal operation.
0x062C	4	R/W	HOLD_EXIT_BW_SEL_PLLC	0: to use the fastlock loop BW when exiting from holdover 1: to use the normal loop BW when exiting from holdover

Register 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Register 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Register 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN2 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

IN3 Input 3 applies to LOS alarm 0x0637[3], OOF alarm 0x0637[7]

Register 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0639	6:4	R/W	IN3_PRIORITY_PLLC	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid

14.2.8. Page 7 Registers Si5347A/B

Note that register addresses for Page 7 DSPLL D Registers 0x0709–0x074D are incremented relative to similar DSPLL A/B/C addresses on Pages 4, 5, and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0508/0x0608.

Register 0x0708

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	1:0	R	IN_PLLD_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL D is currently using.

Register 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	7:0	R/W	BW0_PLLD	48 bit integer number
0x070A	15:8	R/W	BW1_PLLD	
0x070B	23:16	R/W	BW2_PLLD	
0x070C	31:24	R/W	BW3_PLLD	
0x070D	39:32	R/W	BW4_PLLD	
0x070E	47:40	R/W	BW5_PLLD	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	7:0	R/W	FAST_BW0_PLLD	48-bit integer number
0x0710	15:8	R/W	FAST_BW_1PLLD	
0x0711	23:16	R/W	FAST_BW2_PLLD	
0x0712	31:24	R/W	FAST_BW3_PLLD	
0x0713	39:32	R/W	FAST_BW_4PLLD	
0x0714	47:40	R/W	FAST_BW5_PLLD	
0x0715	0	S	BW_UPDATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers.

Register 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	56- bit number
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	32-bit number
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0722 DSPLL D M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	5:0	R/W	M_FRAC_EN_PLLD	DSPLL D M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_PLLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	56-bit number
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716–0x0720.

Register 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLD is out of lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Register 0x072 DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	Must be set to 1 for normal operation.
0x072D	4	R/W	HOLD_EXIT_BW_SEL_PLLD	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover

Register 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applies to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

IN3 Input 3 applies to LOS alarm 0x0738[3], OOF alarm 0x0738[7]

Register 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x073A	6:4	R/W	IN3_PRIORITY_PLLD	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x0740	2	R	FASTLOCK_STATUS_PLLD	0: Not in Fastlock 1: Fastlock active

14.2.9. Page 9 Registers Si5347A/B

Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit optimizes the Vil, Vih, Vol, and Voh thresholds to match the VDDS voltage. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5347/46 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit high. This will ensure that both the host and the serial interfaces are operating at the optimum voltage thresholds.

Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See "5.Clock Inputs" on page 19 for more information.

When a clock is disabled, it is powered down.

- Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]
- Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]
- Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]
- Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

14.2.10. Page A Registers Si5347A/B

Register 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	3:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	3:0	R/W	N_PIBYP	Bypass the fractional part of the internal divider for PLLs (D C B A). Set to a 1 when the value is integer, as this may give slightly lower phase noise. May be set to 0 when the value is either fractional or integer.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	3:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.2.11. Page B Registers Si5347A/B

Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Register 0x0B44 Clock Control for Fractional Dividers

0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Register 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (IN3 IN2 IN1 IN0). Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B49 Calibration Bits

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	3:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (D C B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.3. Si5347C/D Register Map

14.3.1. Page 0 Registers Si5347C/D

Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Register 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Register 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x47	Four-digit “base” part number, one nibble per digit Example: Si5347A-A-GM. The base part number (OPN) is 5347, which is stored in this register
0x0003	15:8	R	PN_BASE	0x53	

Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/synthesis mode. 0 = A 1 = B 2 = C 3 = D

Refer to the device data sheet Ordering Guide section for more information about device grades.

Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5347C-**A**12345-GM, the device revision is “A” and stored as 0

Register 0x0006–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0006	3:0	R	SPECIAL	ClockBuilder Pro version that was used to generate the NVM image Major.Minor.Revision.Special
0x0006	7:4	R	REVISION	
0x0007	7:0	R	MINOR	
0x0008	0	R	MINOR	
0x0008	4:1	R	MAJOR	
0x0008	7:5	R	TOOL	
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5347C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5347C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5347 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Register 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address

Register 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if there is no signal detected on the XAXB input signal.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Register 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [3 2 1 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [3 2 1 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Register 0x000EHoldover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Register 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4
DSPLL_B corresponds to bit 5
DSPLL_C corresponds to bit 6
DSPLL_D corresponds to bit 7

Register 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to clear the flag.
0x0011	3	R	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Register 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]
- Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Register 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

DSPLL_C corresponds to bit 2,6

DSPLL_D corresponds to bit 3,7

Register 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Register 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W	LOSREF_INTR_MSK	1 to mask LOSREF_FLG from causing an interrupt
0x0017	3	R/W	LOL_INTR_MSK	1 to mask LOL_FLG from causing an interrupt
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this register is 0x035.

Register 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1: To mask the clock input OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]
- Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]
- DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019 [2], HOLD_INTR_MSK_PLL 0x0019 [6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019 [3], HOLD_INTR_MSK_PLL 0x0019 [7]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: Initialize and calibrate the entire device. This will also align the outputs from the four DSPLLs.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB
0x001C	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715.

Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1: To put the device into low power mode
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Resets all output R dividers to the same state.

Register 0x0020 DSPLL_SEL0,1 Control of FINC/FDEC

Reg Address	Bit Field	Type	Name	Description
0x0020	0	R/W	DSPLL_SELx_EN	0: DSPLL_SEL0,1 pins and bits are disabled. 1: DSPLL_SEL0,1 pins or DSPLL_SELx_REG bits are enabled. See DSPLL_SELX_REG_EN.
0x0020	1	R/W	DSPLL_SELx_REG_EN	Only functions when DSPLL_SELx_EN = 1. 0: DSPLL_SELx pins are enabled, and the corresponding register bits are disabled. 1: DSPLL_SELx_REG register bits are enabled, and the corresponding pins are disabled.
0x0020	2	R/W	DSPLL_SEL0_REG	Register version of the pin DSPLL_SEL0. Used to select which PLL (M divider) is affected by FINC/FDEC.
0x0020	3	R/W	DSPLL_SEL1_REG	Register version of the pin DSPLL_SEL1. Used to select which PLL (M divider) is affected by FINC/FDEC.

Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	0: $\overline{OE0}$ and $\overline{OE1}$ pins disable 1: OE0 and OE1 register disable
0x0022	1	R/W	OE0_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE0 selected outputs 1: Enable OE0 selected outputs
0x0022	2	R/W	OE1_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE1 selected outputs 1: Enable OE1 selected outputs

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Register 0x0023-0x0024 OE0 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0023	1 3 4 5 7	R/W	OE0_OUT0_SEL OE0_OUT1_SEL OE0_OUT2_SEL OE0_OUT3_SEL OE0_OUT4_SEL	0: Output ignores OE0 1: Output disabled by OE0 See Table 27, “Output Driver Disable Sources Summary,” on page 41 for additional information.
0x0024	0 1 3	R/W	OE0_OUT5_SEL OE0_OUT6_SEL OE0_OUT7_SEL	

Register 0x0025-0x0026 OE1 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0025	1 3 4 5 7	R/W	OE1_OUT0_SEL OE1_OUT1_SEL OE1_OUT2_SEL OE1_OUT3_SEL OE1_OUT4_SEL	0: Output ignores OE1 1: Output disabled by OE1 See Table 27, “Output Driver Disable Sources Summary,” on page 41 for additional information.
0x0026	0 1 3	R/W	OE1_OUT5_SEL OE1_OUT6_SEL OE1_OUT7_SEL	

Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI.

Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Input 3 (IN3): LOS_EN[3]

Register 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Register 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Register 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Register 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Register 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable 1: To enable
0x003F	7:4	R/W	FAST_OOF_EN	

Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Register 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0048	7:0	R/W	OOF2_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0049	7:0	R/W	OOF3_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Register 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004C	7:0	R/W	OOF2_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004D	7:0	R/W	OOF3_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Register 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	7:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	7:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	7:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	7:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Register 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	7:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	7:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm
0x0057	7:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	7:0	R/W	FAST_OOF3_CLR_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	3:0	R/W	LOL_SLW_EN_PLL[D:A]	0: To disable fast LOL. 1: To enable fast LOL.

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Register 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.

Register 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2,6,20,60,200,600,2000,6000,20000. Values are in ppm.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm.

The following are the thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm
- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

Register 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

The following are the thresholds for the value that is placed in the four bits of the DSPLLs. ClockBuilder Pro sets these values.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm
- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	3:0	R/W	LOL_TIMER_EN_PLL	0: To disable 1: To enable

LOL_TIMER extends the time after the LOL clear threshold has been met that LOL stays active.

DSPLL A bit 0

DSPLL B bit 1

DSPLL C bit 2

DSPLL D bit 3

Register 0x00A3-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A3	7:0	R/W	LOL_CLR_DELAY_PLLA	35-bit value
0x00A4	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A5	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A6	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A7	2:0	R/W	LOL_CLR_DELAY_PLLA	

Register 0x00A8-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY_PLLB	35-bit value
0x00A9	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AA	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AB	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AC	2:0	R/W	LOL_CLR_DELAY_PLLB	

Register 0x00AD-0x00B1 LOL Clear Delay DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x00AD	7:0	R/W	LOL_CLR_DELAY_PLLC	35-bit value
0x00AE	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00AF	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00B0	7:0	R/W	LOL_CLR_DELAY_PLLC	
0x00B1	2:0	R/W	LOL_CLR_DELAY_PLLC	

Register 0x00B2-0x00B6 LOL Clear Delay DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x00B2	7:0	R/W	LOL_CLR_DELAY_PLLD	35-bit value
0x00B3	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B4	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B5	7:0	R/W	LOL_CLR_DELAY_PLLD	
0x00B6	2:0	R/W	LOL_CLR_DELAY_PLLD	

Register 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	5:0	R	ACTIVE_NVM_BANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See “4.1.1. Updating Registers during Device Operation” for a detailed description of how to program the NVM.

Register 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See "4.1.2.NVM Programming" on page 16.

Register 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	1: To download NVM.

When set, this bit will read the NVM down into the volatile memory.

Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is most useful after powerup, after a hard reset 0x001E[1], or after an NVM write 0x00E3 to determine when the operation is complete. The “Device Ready” register is available on every page in the device at 0x##FE, where “##” represents the page address.

14.3.2. Page 1 Registers Si5347C/D

Register 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers 1: Pass through the output enables.

Register 0x0108, 0x011C, 0x0126, 0x012B Clock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0108 0x011C 0x0126 0x012B	0	R/W	OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pull-down effect.
0x0108 0x011C 0x0126 0x012B	1	R/W	OUT0_OE OUT1_OE OUT2_OE OUT3_OE	0: To disable the output 1: To enable the output
0x0108 0x011C 0x0126 0x012B	2	R/W	OUT0_RDIV_FORCE OUT1_RDIV_FORCE OUT2_RDIV_FORCE OUT3_RDIV_FORCE	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2

The output drivers are all identical. See "6.2.Performance Guidelines for Outputs" on page 32.

Register 0x0109, 0x011D, 0x0127, 0x012C Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0109 0x011D 0x0127 0x012C	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved
0x0109 0x011D 0x0127 0x012C	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN	0: Disable 1: Enable
0x0109 0x011D 0x0127 0x012C	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high
0x0109 0x011D 0x0127 0x012C	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV	LVCMOS output impedance drive strength see "Table 23.LVCMOS Drive Strength Control Registers" on page 38.

The output drivers are all identical.

Register 0x010A, 0x011E, 0x0128, 0x012D Output Amplitude and Common Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x010A 0x011E 0x0128 0x012D	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.
0x010A 0x011E 0x0128 0x012D	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Register 0x010B, 0x011F, 0x0129, 0x012E Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x010B 0x011F 0x0129 0x012E	1:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL	Output driver 0 input mux select.This selects the source of the output clock. 0: DSPLL A 1: DSPLL B 2: DSPLL C 3: DSPLL D
0x010B 0x011F 0x0129 0x012E	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV	0: CLK and $\overline{\text{CLK}}$ not inverted 1: $\overline{\text{CLK}}$ inverted 2: CLK and $\overline{\text{CLK}}$ inverted 3: CLK inverted These bits have no effect on differential outputs.

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical.

Register 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	6	R/W	OUT_DIS_MSK_LOSXAXB	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition

Register 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MASK_LOL_PLL[D:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs

Bit 0 LOL_DSPLL_A mask
Bit 1 LOL_DSPLL_B mask
Bit 2 LOL_DSPLL_C mask
Bit 3 LOL_DSPLL_D mask

Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Setting Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0: No effect 1: All drivers powered down

14.3.3. Page 2 Registers Si5347C/D

Register 0x0202-0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Setting Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this frequency reference with high resolution. XAXB_FREQ_OFFSET can be used to compensate for the XTAL frequency error. This will cause the free run frequency to be more accurate. It is programmed as a two's complement number. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This valid with external clock sources, not crystals.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 3 = pre-scale value 8
- Note that changing this register furing operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Table 44. Si5347C/D P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values.

Register 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x024A	7:0	R/W	R0_REG	24-bit Integer output divider divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 45. Si5347C/D R1–R3 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0256-0x0258	R1_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R2_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R3_REG	24-bit Integer Number	0x024A-0x024C

Register 0x026B–0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5347C-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5347C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5347C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5347 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

14.3.4. Page 3 Registers Si5347C/D

Register 0x030C DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE_PLLA	Must write a 1 to this bit to cause DSPLLA internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0317 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0317	0	S	N1_UPDATE_PLLB	Must write a 1 to this bit to cause DSPLL B internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0322 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0322	0	S	N2_UPDATE_PLLC	Must write a 1 to this bit to cause DSPLL C internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x032D DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x032D	0	S	N3_UPDATE_PLLD	Must write a 1 to this bit to cause DSPLL D internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Register 0x0407

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL A is currently using.

Register 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	7:0	R/W	BW0_PLLA	48 bit integer number
0x0409	15:8	R/W	BW1_PLLA	
0x040A	23:16	R/W	BW2_PLLA	
0x040B	31:24	R/W	BW3_PLLA	
0x040C	39:32	R/W	BW4_PLLA	
0x040D	47:40	R/W	BW5_PLLA	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	7:0	R/W	FAST_BW0_PLLA	48-bit integer number
0x040F	15:8	R/W	FAST_BW1_PLLA	
0x0410	23:16	R/W	FAST_BW2_PLLA	
0x0411	31:24	R/W	FAST_BW3_PLLA	
0x0412	39:32	R/W	FAST_BW4_PLLA	
0x0413	47:40	R/W	FAST_BW5_PLLA	
0x0414	0	S	BW_UPDATE_PLLA	0: No effect 1: Update both the Normal and Fast-lock BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56- bit number.
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	5:0	R/W	M_FRAC_EN_PLLA	DSPLL A M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.

Register 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Register 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register-based clock selection.

Register 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FAST-LOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Register 0x042C DSPLL A Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Must be set to 1 for normal operation.
0x042C	4	R/W	HOLD_EXIT_BW_SEL_PLLA	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Register 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x043F	2	R	FASTLOCK_STATUS_PLLA	0: Not in Fastlock 1: Fastlock active

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Register 0x0507

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL B is currently using.

Register 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	7:0	R/W	BW0_PLLB	48 bit integer number
0x0509	15:8	R/W	BW1_PLLB	
0x050A	23:16	R/W	BW2_PLLB	
0x050B	31:24	R/W	BW3_PLLB	
0x050C	39:32	R/W	BW4_PLLB	
0x050D	47:40	R/W	BW5_PLLB	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.The BW_UPDATE bit (register 0x0514[0] must be set to cause the normal and fast bandwidth parameters to be active.

Register 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	7:0	R/W	FAST_BW0_PLLB	48-bit integer number
0x050F	15:8	R/W	FAST_BW1_PLLB	
0x0510	23:16	R/W	FAST_BW2_PLLB	
0x0511	31:24	R/W	FAST_BW3_PLLB	
0x0512	39:32	R/W	FAST_BW4_PLLB	
0x0513	47:40	R/W	FAST_BW5_PLLB	
0x0514	0	S	BW_UPDATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLB to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	5:0	R/W	M_FRAC_EN_PLLB	DSPLL B M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEPW_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEPW_PLLB	
0x0525	23:16	R/W	M_FSTEPW_PLLB	
0x0526	31:24	R/W	M_FSTEPW_PLLB	
0x0527	39:32	R/W	M_FSTEPW_PLLB	
0x0528	47:40	R/W	M_FSTEPW_PLLB	
0x0529	55:48	R/W	M_FSTEPW_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0515–0x051F.

Register 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTO_EN_PLLB	Applies when FAST-LOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Register 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL_PLLB	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5-bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x052F DSPLLB Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R/W	HOLD_HIST_DELAY_PLLB	5-bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Register 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	IN_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.
IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]
IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]
IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]
IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Register 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x053F DSPLL B Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R	HOLD_HIST_VALID_PLLB	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x053F	2	R	FASTLOCK_STATUS_PLLB	0: Not in Fastlock 1: Fastlock active

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Register 0x0607

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL C is currently using.

Register 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	7:0	R/W	BW0_PLLC	48-bit integer number
0x0609	15:8	R/W	BW1_PLLC	
0x060A	23:16	R/W	BW2_PLLC	
0x060B	31:24	R/W	BW3_PLLC	
0x060C	39:32	R/W	BW4_PLLC	
0x060D	47:40	R/W	BW5_PLLC	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	7:0	R/W	FAST_BW0_PLLC	48-bit integer number
0x060F	15:8	R/W	FAST_BW1_PLLC	
0x0610	23:16	R/W	FAST_BW2_PLLC	
0x0611	31:24	R/W	FAST_BW3_PLLC	
0x0612	39:32	R/W	FAST_BW4_PLLC	
0x0613	47:40	R/W	FAST_BW5_PLLC	
0x0614	0	S	BW_UPDATE_PLLC	0: No effect. 1: Update both the Normal and Fastback BWs for PLL C.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLC to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	56-bit number
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	32-bit number
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UPDATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0621 DSPLL C M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	5:0	R/W	M_FRAC_EN_PLLC	DSPLL C M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.

Register 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	56-bit number
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F.

Register 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLC is out of lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Register 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	Must be set to 1 for normal operation.
0x062C	4	R/W	HOLD_EXIT_BW_SEL_PLLC	0: to use the fastlock loop BW when exiting from holdover 1: to use the normal loop BW when exiting from holdover

Register 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Register 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Register 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN2 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

IN3 Input 3 applies to LOS alarm 0x0637[3], OOF alarm 0x0637[7]

Register 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0639	6:4	R/W	IN3_PRIORITY_PLLC	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid

14.3.8. Page 7 Registers Si5347C/D

Note that register addresses for Page 7 DSPLL D Registers 0x0709–0x074D are incremented relative to similar DSPLL A/B/C addresses on Pages 4, 5, and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0508/0x0608.

Register 0x0708

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	1:0	R	IN_PLLD_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL D is currently using.

Register 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	7:0	R/W	BW0_PLLD	48 bit integer number
0x070A	15:8	R/W	BW1_PLLD	
0x070B	23:16	R/W	BW2_PLLD	
0x070C	31:24	R/W	BW3_PLLD	
0x070D	39:32	R/W	BW4_PLLD	
0x070E	47:40	R/W	BW5_PLLD	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	7:0	R/W	FAST_BW0_PLLD	48-bit integer number
0x0710	15:8	R/W	FAST_BW_1PLLD	
0x0711	23:16	R/W	FAST_BW2_PLLD	
0x0712	31:24	R/W	FAST_BW3_PLLD	
0x0713	39:32	R/W	FAST_BW_4PLLD	
0x0714	47:40	R/W	FAST_BW5_PLLD	
0x0715	0	S	BW_UPDATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers.

Register 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	56- bit number
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	32-bit number
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0722 DSPLL D M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	5:0	R/W	M_FRAC_EN_PLLD	DSPLL D M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_PLLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	56-bit number
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716–0x0720.

Register 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLD is out of lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Register 0x072 DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	Must be set to 1 for normal operation.
0x072D	4	R/W	HOLD_EXIT_BW_SEL_PLLD	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover

Register 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase build-out turned on)

Register 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applies to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

IN3 Input 3 applies to LOS alarm 0x0738[3], OOF alarm 0x0738[7]

Register 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x073A	6:4	R/W	IN3_PRIORITY_PLLD	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x0740	2	R	FASTLOCK_STATUS_PLLD	0: Not in Fastlock 1: Fastlock active

14.3.9. Page 9 Registers Si5347C/D

Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit optimizes the Vil, Vih, Vol, and Voh thresholds to match the VDDS voltage. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5347/46 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit high. This will ensure that both the host and the serial interfaces are operating at the optimum voltage thresholds.

Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See "5.Clock Inputs" on page 19 for more information.

When a clock is disabled, it is powered down.

- Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]
- Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]
- Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]
- Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

14.3.10. Page A Registers Si5347C/D

Register 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	3:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	3:0	R/W	N_PIBYP	Bypass the fractional part of the internal divider for PLLs (D C B A). Set to a 1 when the value is integer, as this may give slightly lower phase noise. May be set to 0 when the value is either fractional or integer.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	3:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.3.11. Page B Registers Si5347C/D

Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Register 0x0B44 Clock Control for Fractional Dividers

0x0B44	6	R/W	FRACN_CLK_DIS_PLLC	Clock disable for the fractional divide of the M divider in PLLC. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	7	R/W	FRACN_CLK_DIS_PLLD	Clock disable for the fractional divide of the M divider in PLLD. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Register 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (IN3 IN2 IN1 IN0). Must be set to 0 to enable the LOS function of the respective inputs.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B49 Calibration Bits

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	3:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (D C B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.4. Si5346 Register Map

14.4.1. Page 0 Registers Si5346

Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Register 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Register” is located at address 0x01 on every page. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Register 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x46	Four-digit “base” part number, one nibble per digit Example: Si5346A-A-GM. The base part number (OPN) is 5346, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/ synthesis mode 0 = A 1 = B 2 = C 3 = D

Refer to the device data sheet Ordering Guide section for more information about device grades.

Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5346C-**A**12345-GM, the device revision is “A” and stored as 0

Register 0x0006–0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0006	3:0	R	SPECIAL	ClockBuilder Pro version that was used to generate the NVM image Major.Minor.Revision.Special
0x0006	7:4	R	REVISION	
0x0007	7:0	R	MINOR	
0x0008	0	R	MINOR	
0x0008	4:1	R	MAJOR	
0x0008	7:5	R	TOOL	
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (–40 °C to 85 °C) ambient conditions
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5346C-A12345-GM.

Applies to a “base” or “blank” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5346C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5346 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Register 0x000B I2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	I2C_ADDR	7-bit I2C Address

Register 0x000C Internal Fault Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R	LOSREF	1 if no signal is detected on the XAXB pins.
0x000C	3	R	XAXB_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Bit 1 is the LOS status monitor for the XTAL or REFCLK at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude. Bit 5 indicates a timeout error when using SMBUS with the I^2C serial port.

Register 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input is currently LOS
0x000D	7:4	R	OOF	1 if the clock input is currently OOF

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Input 3 (IN3) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Register 0x000EHoldover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	1:0	R	LOL_PLL[B:A]	1 if the DSPLL is out of lock
0x000E	5:4	R	HOLD_PLL[B:A]	1 if the DSPLL is in holdover (or free run)

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Register 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	5:4	R	CAL_PLL[B:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4

DSPLL_B corresponds to bit 5

Register 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	2	R/W	LOSREF_FLG	Sticky version of LOSREF. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x000C	5	R/W	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000C.

Register 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	1 if the clock input is LOS
0x0012	7:4	R/W	OOF_FLG	1 if the clock input is OOF

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4]
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5]
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6]
- Input 3 (IN3) corresponds to LOS_FLG 0x0012 [3], OOF_FLG 0x0012[7]

Register 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	1:0	R/W	LOL_FLG_PLL[B:A]	1 if the DSPLL was unlocked
0x0013	5:4	R/W	HOLD_FLG_PLL[B:A]	1 if the DSPLL was in holdover (or freerun)

Sticky flag versions of address 0x000E.

DSPLL_A corresponds to bit 0,4

DSPLL_B corresponds to bit 1,5

Register 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	5:4	R/W	CAL_FLG_PLL[B:A]	1 if the DSPLL internal calibration was busy

These are sticky flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B corresponds to bit 5

Register 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	1	R/W	LOSXAXB_MSK	1 to mask out LOSXAXB.
0x0017	5	R/W	SMBUS_TIMEOUT_MSK	1 to mask out SMBUS_TIMEOUT.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1 to mask the clock input LOS flag
0x0018	7:4	R/W	OOF_INTR_MSK	1 to mask the clock input OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0], OOF_IN_INTR_MSK 0x0018 [4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1], OOF_IN_INTR_MSK 0x0018 [5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2], OOF_IN_INTR_MSK 0x0018 [6]
- Input 3 (IN3) corresponds to LOS_IN_INTR_MSK 0x0018 [3], OOF_IN_INTR_MSK 0x0018 [7]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	1:0	R/W	LOL_INTR_MSK_PLL[B:A]	1 to mask the clock input LOL flag
0x0019	5:4	R/W	HOLD_INTR_MSK_PLL[B:A]	1 to mask the holdover flag

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019 [0], HOLD_INTR_MSK_PLL 0x0019 [4]
- DSPLL B corresponds to LOL_INTR_MSK_PLL 0x0019 [1], HOLD_INTR_MSK_PLL 0x0019 [5]

These are the interrupt mask bits for the LOS and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	5:4	R/W	CAL_INTR_MSK_PLL[B:A]	1 to mask the DSPLL internal calibration busy flag

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect 1: initialize and calibrate the entire device. This will also align the outputs from both of the DSPLLs.
0x001C	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLa bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA and BW_UPDATE_PLLB at addresses 0x0414 and 0x514.

Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement

Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	S	HARD_RST	Perform Hard Reset with NVM read. 0: Normal Operation 1: Hard Reset the device
0x001E	2	S	SYNC	Logically equivalent to asserting the $\overline{\text{SYNC}}$ pin. Resets all R dividers to the same state.

Register 0x0022 Output Enable Group Controls

Reg Address	Bit Field	Type	Name	Description
0x0022	0	R/W	OE_REG_SEL	0: $\overline{\text{OE0}}$ and $\overline{\text{OE1}}$ pins disable 1: OE0 and OE1 register disable

Register 0x0022 Output Enable Group Controls

0x0022	1	R/W	OE0_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE0 selected outputs 1: Enable OE0 selected outputs
0x0022	2	R/W	OE1_REG_DIS	If OE_REG_SEL = 1: 0: Disable OE1 selected outputs 1: Enable OE1 selected outputs

By default ClockBuilder Pro sets OE0 controlling all outputs and OE1 unused. OUTALL_DISABLE_LOW 0x0102[0] must be high (enabled) to observe the effects of OE0 and OE1. Note that the OE0 and OE1 register bits (active high) have inverted logic sense from the pins (active low).

Register 0x0023-0x0024 OE0 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0023	3 4 7	R/W	OE0_OUT0_SEL OE0_OUT1_SEL OE0_OUT2_SEL	0: Output ignores OE0 1: Output disabled by OE0 See Table 26 for additional output disable information.
0x0024	0	R/W	OE0_OUT3_SEL	

Register 0x0025-0x0026 OE1 Output Disable Selection

Reg Address	Bit Field	Type	Name	Description
0x0025	3 4 7	R/W	OE1_OUT0_SEL OE1_OUT1_SEL OE1_OUT2_SEL	0: Output ignores OE1 1: Output disabled by OE1 See Table 26 for additional output disable information.
0x0026	0	R/W	OE1_OUT3_SEL	

Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	SPI_3WIRE	0: For 4-wire SPI 1: For 3-wire SPI

Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable 1: To enable LOS for a clock input

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Input 3 (IN3): LOS_EN[3]

Register 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec 1: For 100 msec 2: For 200 msec 3: For one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above
0x002D	7:6	R/W	LOS3_VAL_TIME	Clock Input 3,same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Register 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	16-bit Threshold Value
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 3, given a particular frequency plan.

Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	16-bit Threshold Value
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Register 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	16-bit Threshold Value
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Register 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	16-bit Threshold Value
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Register 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	16-bit Threshold Value
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 3, given a particular frequency plan.

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Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable 1: To enable
0x003F	7:4	R/W	FAST_OOF_EN	

bit 0,4 correspond to IN0

bit 1,5 correspond to IN1

bit 2,6 correspond to IN2

bit 3,7 correspond to IN3

Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	0: IN0 1: IN1 2: IN2 3: IN3 4: XAXB 5–7: Reserved

ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Register 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0048	7:0	R/W	OOF2_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0049	7:0	R/W	OOF3_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm set threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Register 0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004C	7:0	R/W	OOF2_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004D	7:0	R/W	OOF3_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm clear threshold for IN3, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	1:0	R/W	LOL_SLW_EN_PLL[B:A]	0: to disable fast LOL 1: To enable fast LOL

DSPLL A corresponds to bit 0

DSPLL B corresponds to bit 1

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Register 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values are in ppm.

The following are the thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm
- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm.

The following are the thresholds for the value that is placed in the four bits of the DSPLLs. ClockBuilder Pro sets these values.

- 0 = 0.2 ppm
- 1 = 0.6 ppm
- 2 = 2 ppm
- 3 = 6 ppm
- 4 = 20 ppm
- 5 = 60 ppm
- 6 = 200 ppm
- 7 = 600 ppm
- 8 = 2000 ppm

- 9 = 6000 ppm
- 10 = 20000 ppm

Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	1:0	R/W	LOL_TIMER_EN_PLL	0: To disable 1: To enable

LOL_TIMER extends the time after the LOL clear threshold has been met that LOL stays active.

DSPLL A bit 0

DSPLL B bit 1

Register 0x00A3-0x00A7 LOL Clear Delay DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x00A3	7:0	R/W	LOL_CLR_DELAY_PLLA	35-bit value
0x00A4	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A5	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A6	7:0	R/W	LOL_CLR_DELAY_PLLA	
0x00A7	2:0	R/W	LOL_CLR_DELAY_PLLA	

Register 0x00A8-0x00AC LOL Clear Delay DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x00A8	7:0	R/W	LOL_CLR_DELAY_PLLB	35-bit value
0x00A9	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AA	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AB	7:0	R/W	LOL_CLR_DELAY_PLLB	
0x00AC	2:0	R/W	LOL_CLR_DELAY_PLLB	

ClockBuilder Pro is used to set these values.

Register 0x00E2 Active NVM Bank

Reg Address	Bit Field	Type	Setting Name	Description
0x00E2	5:0	R	ACTIVE_NVM_BLANK	0x03 when no NVM has been burned 0x0F when 1 NVM bank has been burned 0x3F when 2 NVM banks have been burned When ACTIVE_NVM_BANK = 0x3F, the last bank has already been burned. See “4.1.1. Updating Registers during Device Operation” for a detailed description of how to program the NVM.

Register 0x00E3

Reg Address	Bit Field	Type	Setting Name	Description
0x00E3	7:0	R/W	NVM_WRITE	Write 0xC7 to initiate an NVM bank burn.

See "4.1.2.NVM Programming" on page 16.

Register 0x00E4

Reg Address	Bit Field	Type	Setting Name	Description
0x00E4	0	S	NVM_READ_BANK	1: To download NVM.

When set, this bit will read the NVM down into the volatile memory.

Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Setting Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus writes. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is most useful after powerup, after a hard reset 0x001E[1], or after an NVM write 0x00E3 to determine when the operation is complete. The “Device Ready” register is available on every page in the device at 0x##FE, where “##” represents the page address.

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Register 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers 1: Pass through the output enables

Register 0x0112, 0x0117, 0x0126, 0x012B Clock Output Driver and R-Divider Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0112 0x0117 0x0126 0x012B	0	R/W	OUT0_PDN OUT1_PDN OUT2_PDN OUT3_PDN	0: To power up the regulator, 1: To power down the regulator. When powered down, output pins will be high-impedance with a light pull-down effect.
0x0112 0x0117 0x0126 0x012B	1	R/W	OUT0_OE OUT1_OE OUT2_OE OUT3_OE	0: To disable the output 1: To enable the output
0x0112 0x0117 0x0126 0x012B	2	R/W	OUT0_RDIV_FORCE OUT1_RDIV_FORCE OUT2_RDIV_FORCE OUT3_RDIV_FORCE	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2.

The output drivers are all identical.

Register 0x0113, 0x0118, 0x0127, 0x012C Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x0113 0x0118 0x0127 0x012C	2:0	R/W	OUT0_FORMAT OUT1_FORMAT OUT2_FORMAT OUT3_FORMAT	0: Reserved 1: Differential Normal mode 2: Differential Low-Power mode 3: Reserved 4: LVCMOS single ended 5–7: Reserved
0x0113 0x0118 0x0127 0x012C	3	R/W	OUT0_SYNC_EN OUT1_SYNC_EN OUT2_SYNC_EN OUT3_SYNC_EN	0: Disable 1: Enable

Register 0x0113, 0x0118, 0x0127, 0x012C Output Format

0x0113 0x0118 0x0127 0x012C	5:4	R/W	OUT0_DIS_STATE OUT1_DIS_STATE OUT2_DIS_STATE OUT3_DIS_STATE	Determines the state of an output driver when disabled, selectable as 0: Disable low 1: Disable high
0x0113 0x0118 0x0127 0x012C	7:6	R/W	OUT0_CMOS_DRV OUT1_CMOS_DRV OUT2_CMOS_DRV OUT3_CMOS_DRV	LVCMOS output impedance drive strength see Table 22, “LVCMOS Output Impedance and Drive Strength Selections,” on page 37.

The output drivers are all identical.

Register 0x0114, 0x0119, 0x0128, 0x012D Output Amplitude

Reg Address	Bit Field	Type	Setting Name	Description
0x0114 0x0119 0x0128 0x012D	3:0	R/W	OUT0_CM OUT1_CM OUT2_CM OUT3_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.
0x0114 0x0119 0x0128 0x012D	6:4	R/W	OUT0_AMPL OUT1_AMPL OUT2_AMPL OUT3_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 21, “Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML,” on page 36.

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Register 0x0115, 0x011A, 0x00129, 0x012E R-Divider Mux Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0115 0x011A 0x0129 0x012E	1:0	R/W	OUT0_MUX_SEL OUT1_MUX_SEL OUT2_MUX_SEL OUT3_MUX_SEL	Output driver 0 input mux select.This selects the source of the multisynth. 0: DSPLL A 1: DSPLL B
0x0115 0x011A 0x0129 0x012E	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV	0: CLK and $\overline{\text{CLK}}$ not inverted 1: $\overline{\text{CLK}}$ inverted 2: CLK and $\overline{\text{CLK}}$ inverted 3: CLK inverted These bits have no effect on differential outputs.

Each output can be connected to either of the two DSPLLs using OUTx_MUX_SEL. The output drivers are all identical.

Register 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	6	R/W	OUT_DIS_MSK_LOSXAXB	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOSXAXB 1: All outputs remain enabled during LOSXAXB condition

Register 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	1:0	R/W	OUT_DIS_MASK_LOL_PLL[B:A]	0: LOL will disable all connected outputs 1: LOL does not disable any outputs

Bit 0 LOL_DSPLL_A mask

Bit 1 LOL_DSPLL_B mask

Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Setting Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0: No effect 1: All drivers powered down

14.4.3. Page 2 Registers Si5346

Register 0x0202-0x0205 X0 Adjust

Reg Address	Bit Field	Type	Setting Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The VCO locks to the XO that is formed by the crystal (or an XO) and the XAXB pins. XAXB_FREQ_OFFSET provides a static offset to the VCO frequency. It is programmed as a two's complement number. This register can be used to adjust the frequency of the VCO when it is locked to the XAXB frequency. ClockBuilder Pro calculates the correct values for these registers. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0206 XAXB Clock Input Reference Divide Value

Reg Address	Bit Field	Type	Setting Name	Description
0x0206	1:0	R/W	PXAXB	The divider value for the XAXB input

This can be used with external clock sources, not crystals.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 3 = pre-scale value 8

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	48-bit Integer Number
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers.

Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	32-bit Integer Number
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Table 46. Si5346 P1–P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211
0x0226-0x022B	P3_NUM	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value 1: Update P-divider value
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Note that these controls are not needed when following the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA and SOFT_RST_PLLB do not update the Px_NUM or Px_DEN values.

Register 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	44-bit Integer Number
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	32-bit Integer Number
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in "4.1.1.Updating Registers during Device Operation" on page 15 are followed.

Register 0x0250-0x0252 R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x0250	7:0	R/W	R0_REG	24-bit Integer divider divider value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x0251	15:8	R/W	R0_REG	
0x0252	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1–R9 dividers follow the same format as the R0 divider described above.

Table 47. Si5346-R1–R3 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0253-0x0255	R1_REG	24-bit Integer Number	0x0250-0x0252
0x025C-0x025E	R2_REG	24-bit Integer Number	0x0250-0x0252
0x025F-0x0261	R3_REG	24-bit Integer Number	0x0250-0x0252

Register 0x026B-0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, “ULT.1A” with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Register 0x0278- 0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5346C-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5346C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5346C-A-GM.

Applies to a “base” or “non-custom” OPN device. Base devices are factory preprogrammed to a specific base part type (e.g., Si5346 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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Register 0x030C DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x030C	0	S	N0_UPDATE_PLLA	Must write a 1 to this bit to cause DSPLL A internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0317 DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0317	0	S	N1_UPDATE_PLLB	Must write a 1 to this bit to cause DSPLL B internal divider changes to take effect.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Register 0x0407

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL A is currently using.

Register 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	7:0	R/W	BW0_PLLA	48 bit integer number
0x0409	15:8	R/W	BW1_PLLA	
0x040A	23:16	R/W	BW2_PLLA	
0x040B	31:24	R/W	BW3_PLLA	
0x040C	39:32	R/W	BW4_PLLA	
0x040D	47:40	R/W	BW5_PLLA	

The loop bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Register 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	7:0	R/W	FAST_BW0_PLLA	48-bit integer number
0x040F	15:8	R/W	FAST_BW1_PLLA	
0x0410	23:16	R/W	FAST_BW2_PLLA	
0x0411	31:24	R/W	FAST_BW3_PLLA	
0x0412	39:32	R/W	FAST_BW4_PLLA	
0x0413	47:40	R/W	FAST_BW5_PLLA	
0x0414	0	S	BW_UPDATE_PLLA	0: No effect. 1: Update both the Normal and Fast-lock BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	56- bit number
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x041C-0x041F M Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	32-bit number
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0421 DSPLL A M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	5:0	R/W	M_FRAC_EN_PLLA	DSPLL A M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0422 DSPLL A FINC/FDEC Masking

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0423-0x0429 DSPLLA M Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	56-bit number
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0415–0x041F.

Register 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FAST-LOCK_MAN_PLLA=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLA is out of lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Register 0x042C DSPLL A Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	Must be set to 1 for normal operation.
0x042C	4	R/W	HOLD_EXIT_BW_SEL_PLLA	0: to use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DELAY_PLLA	5- bit value

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation 1: To force holdover

Register 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Register 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]
IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]
IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]
IN3 Input 3 applies to LOS alarm 0x0437[3], OOF alarm 0x0437[7]

Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0439 DSPLL A Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0439	6:4	R/W	IN3_PRIORITY_PLLA	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x043F	2	R	FASTLOCK_STATUS_PLLA	0: Not in Fastlock 1: Fastlock active

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Register 0x0507

Reg Address	Bit Field	Type	Setting Name	Description
0x0507	7:6	R	IN_PLLB_ACTV	Currently selected DSPLL input clock. 0: IN0 1: IN1 2: IN2 3: IN3

These bits indicate which input clock DSPLL B is currently using.

Register 0x0508-0x050D DSPLL B Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	7:0	R/W	BW0_PLLB	Parameters that create the normal PLL bandwidth
0x0509	7:0	R/W	BW1_PLLB	
0x050A	7:0	R/W	BW2_PLLB	
0x050B	7:0	R/W	BW3_PLLB	
0x050C	7:0	R/W	BW4_PLLB	
0x050D	7:0	R/W	BW5_PLLB	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers. The BW_UPDATE bit (register 0x0514[0] must be set to cause the normal and fast bandwidth parameters to be active.

Register 0x050E-0x0514 DSPLL B Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	7:0	R/W	FAST_BW0_PLLB	Parameters that create the fast lock PLL bandwidth
0x050F	7:0	R/W	FAST_BW1_PLLB	
0x0510	7:0	R/W	FAST_BW2_PLLB	
0x0511	7:0	R/W	FAST_BW3_PLLB	
0x0512	7:0	R/W	FAST_BW4_PLLB	
0x0513	7:0	R/W	FAST_BW5_PLLB	
0x0514	0	S	BW_UPDATE_PLLB	0: No effect 1: Update both the Normal and Fast-lock BWs for PLL B.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLB to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Register 0x0515-0x051B MB Divider Numerator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB[	56- bit number
0x0516	15:8	R/W	M_NUM_PLLB[	
0x0517	23:16	R/W	M_NUM_PLLB[	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The M divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x051C-0x051F MB Divider Denominator for DSPLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	32-bit number
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Register 0x0520 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Register 0x0521 DSPLL B M Divider Fractional Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	5:0	R/W	M_FRAC_EN_PLLB	DSPLL B M divider fractional enable. 0x20: Integer-only division 0x31: Fractional (or Integer) division Required for DCO operation.

Register 0x0522 DSPLL B FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0522	0	R/W	M_FSTEP_MSK_PLLB	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates

Register 0x0523-0x0529 DSPLLB MB Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0523	7:0	R/W	M_FSTEP_PLLB	56-bit number
0x0524	15:8	R/W	M_FSTEP_PLLB	
0x0525	23:16	R/W	M_FSTEP_PLLB	
0x0526	31:24	R/W	M_FSTEP_PLLB	
0x0527	39:32	R/W	M_FSTEP_PLLB	
0x0528	47:40	R/W	M_FSTEP_PLLB	
0x0529	55:48	R/W	M_FSTEP_PLLB	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL B is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0515–0x051F.

Register 0x052A DSPLL B Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x052A	3:1	R/W	IN_SEL_PLLB	0: For IN0 1: For IN1 2: For IN2 3: For IN3 4–7: Reserved

This is the input clock selection for manual register based clock selection.

Register 0x052B DSPLL B Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052B	0	R/W	FASTLOCK_AUTOEN_PLLB	Applies when FAST-LOCK_MAN_PLLB=0. 0: Disable Auto Fastlock 1: Enable Auto Fastlock when PLLB is out of lock
0x052B	1	R/W	FASTLOCK_MAN_PLLB	0: For normal operation 1: For force fast lock

Register 0x052C DSPLL B Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x052C	3	R/W	HOLD_RAMP_BYP_PLLB	Must be set to 1 for normal operation.
0x052C	4	R/W	HOLD_EXIT_BW_SEL_PLLB	0: To use the fastlock loop BW when exiting from holdover 1: To use the normal loop BW when exiting from holdover

Register 0x052E DSPLL B Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x052E	4:0	R/W	HOLD_HIST_LEN_PLLB	5- bit value

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See "4.5.Holdover Mode" on page 17 to calculate the window length from the register value.

Register 0x052F DSPLLB Holdover History Delay and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x052F	4:0	R	HOLD_HIST_DELAY_PLLB	5- bit value
0x053F	2	R	FASTLOCK_STATUS_PLLB	0: Not in Fastlock 1: Fastlock active

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See "4.5.Holdover Mode" on page 17 to calculate the ignore delay time from the register value.

Register 0x0535 DSPLL B Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0535	0	R/W	FORCE_HOLD_PLLB	0: For normal operation 1: To force holdover

Register 0x0536 DSPLLB Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0536	1:0	R/W	CLK_SWITCH_MODE_PLLB	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0536	2	R/W	HSW_EN_PLLB	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Register 0x0537 DSPLLB Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0537	3:0	R/W	IN_LOS_MSK_PLLB	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic
0x0537	7:4	R/W	IN_OOF_MSK_PLLB	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0537[0], OOF alarm 0x0537[4]

IN1 Input 1 applies to LOS alarm 0x0537[1], OOF alarm 0x0537[5]

IN2 Input 2 applies to LOS alarm 0x0537[2], OOF alarm 0x0537[6]

IN3 Input 3 applies to LOS alarm 0x0537[3], OOF alarm 0x0537[7]

Register 0x0538 DSPLL B Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0538	2:0	R/W	IN0_PRIORITY_PLLB	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0538	6:4	R/W	IN1_PRIORITY_PLLB	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x0539 DSPLL B Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0539	2:0	R/W	IN2_PRIORITY_PLLB	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved
0x0539	6:4	R/W	IN3_PRIORITY_PLLB	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5–7: Reserved

Register 0x053F DSPLL B Hold Valid History

Reg Address	Bit Field	Type	Setting Name	Description
0x053F	1	R/W	HOLD_HIST_VALID_PLLB	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid

14.4.7. Page 9 Registers Si5346

Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	Selects between the XTAL or external reference clock on the XA/XB pins. Default is 0, XTAL. Set to 1 to use an external reference oscillator.

Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

The IO_VDD_SEL configuration bit optimizes the Vil, Vih, Vol, Voh thresholds to match the VDDS voltage. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I^2C or SPI host is operating at 3.3 V and the Si5347/46 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit high. This will ensure that both the host and the serial interfaces are operating at the optimum voltage thresholds.

Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for IN3–IN0
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN3–IN0. See "5.Clock Inputs" on page 19 for more information.

When a clock is disabled, it is powered down.

- Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]
- Input 1 corresponds to IN_EN 0x0949 [1], IN_PULSED_CMOS_EN 0x0949 [5]
- Input 2 corresponds to IN_EN 0x0949 [2], IN_PULSED_CMOS_EN 0x0949 [6]
- Input 3 corresponds to IN_EN 0x0949 [3], IN_PULSED_CMOS_EN 0x0949 [7]

14.4.8. Page A Register Si5346

Register 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Name	Description
0x0A03	1:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Name	Description
0x0A04	1:0	R/W	N_PIBYP	Bypass the fractional part of the internal divider for PLLs (B A). Set to a 1 when the value is integer, as this may give slightly lower phase noise. May be set to 0 when the value is either fractional or integer.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Name	Description
0x0A05	1:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0]

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

14.4.9. Page B Register Si5346

Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See "4.1.1.Updating Registers during Device Operation" on page 15 for more information.

Register 0x0B44 Clock Control for Fractional Dividers

Reg Address	Bit Field	Type	Name	Description
0x0B44	3:0	R/W	PDIV_FRACN_CLK_DIS	Clock Disable for the fractional divide of the input P dividers. [P3, P2, P1, P0]. Must be set to a 0 if the P divider has a fractional value. 0: Enable the clock to the fractional divide part of the P divider. 1: Disable the clock to the fractional divide part of the P divider.
0x0B44	4	R/W	FRACN_CLK_DIS_PLLA	Clock disable for the fractional divide of the M divider in PLLA. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.
0x0B44	5	R/W	FRACN_CLK_DIS_PLLB	Clock disable for the fractional divide of the M divider in PLLB. Must be set to a 0 if this M divider has a fractional value. 0: Enable the clock to the fractional divide part of the M divider. 1: Disable the clock to the fractional divide part of the M divider.

Register 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Controls the clock to the digital LOS circuitry. Must be set to 0 to enable the LOS function of the respective Inputs (IN3 IN2 IN1 IN0).

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B49 Calibration Bits

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	1:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs (B A). Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

APPENDIX A—CUSTOM DIFFERENTIAL AMPLITUDE CONTROLS

In some customer applications, it may be desirable to have larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings generated by Clockbuilder Pro. For example, “CML” format is sometimes desired for an application, but CML is not a defined standard, and, hence, the input amplitude of CML signals may differ between receivers. In these cases, the following information describes how to implement non-standard differential amplitudes.

The differential output driver has two basic modes of operation as well as variable output amplitude capability. The Normal mode has an internal impedance of ~100 Ω differential, while the Low Power mode has an internal impedance of >500 Ω differential. In both cases, when properly terminated with 100 Ω differential externally, the amplitudes listed in Table 48 result.

Table 48. Differential Output Amplitude Typical Values

OUTx_AMPL	Normal Mode OUTx_FORMAT = 1 (Vpp-SE mV - Typical)	Low Power Mode OUTx_FORMAT = 2 (Vpp SE mV - Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Notes:
1. In low power mode with VDDOx = 1.8 V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon 100 Ω differential termination

For applications using a custom differential output amplitude the common mode voltage should be selected as shown in Table 49. These settings, along with the settings given in Table 21, have been verified to give good signal integrity. Some extreme combinations of amplitude and common mode may have impaired signal integrity.

Also, in cases where the receiver is dc-biased either internally or through an external network, the outputs of this device must be ac-coupled. Output driver performance is not guaranteed when dc-coupled to a biased-input receiver.

Table 49. Differential Output Common Mode Voltage Settings

VDDOx (V)	Differential Format	OUTx_FORMAT (dec)	Common Mode Voltage (V)	OUTx_CM (dec)
3.3	Normal	1	2.05	11
3.3	Low Power	2	1.65	7
2.5	Normal	1	1.35	12
2.5	Low Power	2	1.15	10
1.8	Normal	1	0.80	13
1.8	Low Power	2	0.80	13

See also "6.3.Differential Outputs" on page 35 for additional information on the OUTx_FORMAT, OUTx_AMPL, and OUTx_CM controls.

Document Change List

Revision 0.1 to Revision 0.2

- Corrected Figure 23, “7-bit I2C Slave Address Bit-Configuration,” on page 50.

Revision 0.2 to Revision 0.3

- Updated “10.2. Recommended Crystals”.
  - Updated Table 33.

Revision 0.3 to Revision 0.95

- Added Appendix A with variable output amplitudes, including CML.
- Added recommended settings for compatibility with LVPECL, LVDS, HCSL, and CML.
- Added new section with recommended Stratum-3/3E Oscillators.
- Added register descriptions for some previously undescribed registers.
- Added pre- and post-amble control write sequence requirements.
- Added ground/thermal vias to the example PCB layout figures.
- Updated figures for: Modes of Operation, Termination for Input Signals, Output Terminations, XAXB Connections, Interrupt Generation and Masking.
- Updated typical LVCMOS output impedance values.
- Clarified clock alignment power supply sequencing.
- Clarified the section on Blank and Factory Programmed devices.
- Clarified the difference between Standard inputs and low duty-cycle Pulsed CMOS inputs.
- Incremented device revision from 0 to 1 for Rev. B in register 0x0005, “DEVICE_REV”.
- Removed “Stop Mid” differential output disable state option for new designs.
- See also the ClockBuilder Pro release notes for more information: http://www.silabs.com/Support%20Documents/Software/ClockBuilder-Pro-README.pdf

Revision 0.95 to Revision 1.0

- Added 4-output Si5347 C and D grade registers.
- Updated "7.Digitally Controlled Oscillator (DCO) Mode" on page 43.
  - Added direct write DCO mode usage instructions.
- Added settings descriptions of OUTx_RDIV_FORCE 0x0108/etc. and M_FRAC_EN_PLLx 0x0421[5:0] / 0x0521[5:0] / 0x0621[5:0] / 0x0722[5:0] for all devices.
- Corrected definition of device GRADE 0x0004[7:0] bits.

Revision 1.0 to Revision 1.1

- Added register 0x0020.
- Corrected description to FASTLOCK_AUTO_EN_PLLx, x = A, B, C, D.
- Added register 0x0B44.

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