APPLICATION MANUAL

RV-2123

Ultra-Low-Power Real Time Clock / Calendar Module

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CONTENTS

RV-2123-C2

Ultra Low Power Real Time Clock / Calendar Module with Serial Peripheral Interface (SPI-Bus)

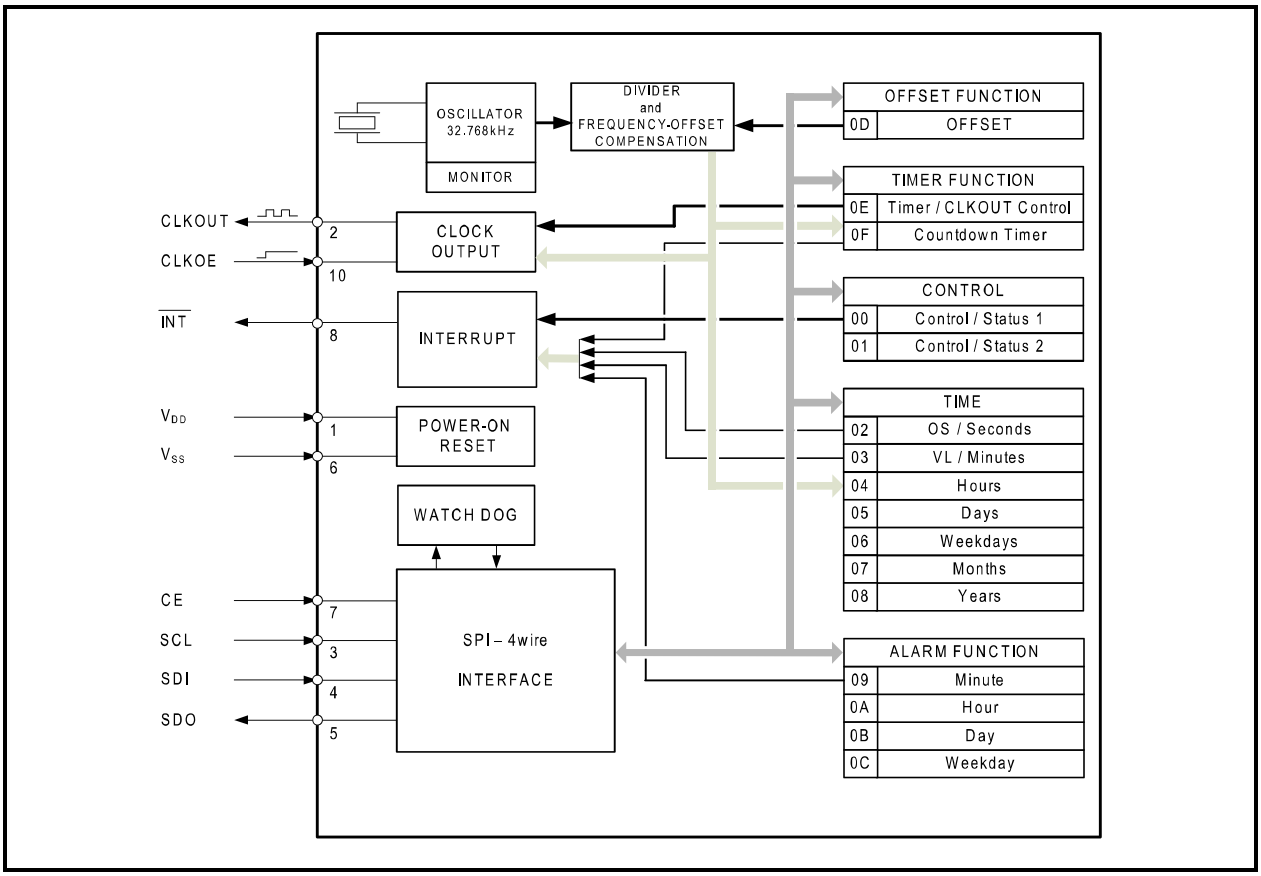
1.0 OVERVIEW

- RTC module with built-in "Tuning Fork" crystal oscillating at 32.768 kHz
- Ultra low power consumption: 130nA typ @ V_{DD} = 3.0V / T_{amb} = 25°C
- Wide clock operating voltage: 1.1 – 5.5V
- Wide Interface operating voltage: 1.6 – 5.5V
- User programmable Frequency Offset Compensation Register for improved time accuracy
- 4-wire SPI-Interface with a maximum data rate of 6.25 Mbits/s.
- Provides year, month, day, weekday, hours, minutes, seconds
- Alarm and Timer functions, internal low-voltage detector, power-on reset and watchdog function.
- Open-drain Interrupt and programmable CLKOUT pins for peripheral devices (32.768kHz down to 1Hz)
- Small and compact package-size of 5.0 x 3.2 x 1.2mm, RoHS-compliant and 100% lead-free.

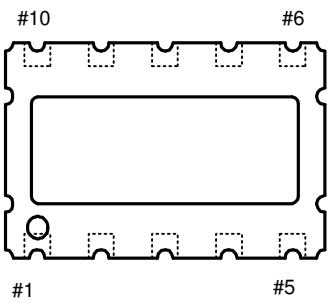
1.1 GENERAL DESCRIPTION

The RV-2123-C2 is a CMOS real-time clock/calendar module optimized for ultra low power consumption. Data is transferred serially via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.25Mbits/s, the built-in word address register is incremented automatically after each written or read data byte.
Beyond standard RTC-functions like year, month, day, weekday, hours, minutes, seconds information, the RV-2123-C2 offers Alarm and Timer-Interrupt function, programmable Clock-Output and Voltage-Low-Detector. A programmable Offset-Register allows fine tuning of the clock to improve time-accuracy @ 25°C, for ageing adjustment or to compensate the frequency-drift over the temperature of the 32.768 kHz "Tuning-Fork" crystals.

2.0 BLOCK DIAGRAM



2.1 PINOUT



# 1	V_{DD}	# 10	CLKOE
# 2	CLKOUT	# 9	N.C.
# 3	SCL	# 8	$\overline{INT}$
# 4	SDI	# 7	CE
# 5	SDO	# 6	V_{SS}

2.2 PIN DESCRIPTION

Symbol	Pin #	Description
V_{DD}	1	Positive supply voltage; positive or negative steps in supply voltage may affect oscillator performance, recommend 10 nF decoupling capacitor close to device
CLKOUT	2	Clock Output pin; open-drain
SCL	3	Serial Clock Input pin; may float when CE inactive
SDI	4	Serial Data Input pin; may float when CE inactive
SDO	5	Serial Data Output pin; push-pull; high-impedance when not driving; can be connected to SDI for single-wire data line
V_{SS}	6	Ground
CE	7	Chip Enable input; active HIGH; with internal pull-down
$\overline{INT}$	8	Interrupt output pin; open-drain; active LOW
NC	9	Not Connected
CLKOE	10	CLKOUT enable/disable pin; enable is active HIGH

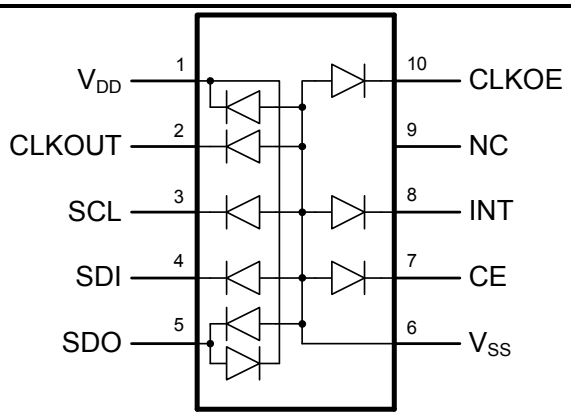
2.3 FUNCTIONAL DESCRIPTION

The RV-2123-C2 is a CMOS real-time clock/calendar module optimized for ultra low power consumption. The CMOS IC contains sixteen 8-bit registers with an auto-incrementing address counter, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and a 6.25 Mbits/s SPI-bus. An offset register allows fine tuning of the clock to compensate the frequency-deviation.

All sixteen registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

- The first two registers (memory address 00h and 01h) are used as control registers
- The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years). The Seconds, Minutes, Hours, Days, Weekdays, Months and Years registers are all coded in Binary-Coded-Decimal (BCD) format. When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented
- Addresses 09h through 0Ch define the alarm condition
- Address 0Dh defines the offset calibration
- Address 0Eh defines the clock out and timer mode
- Address registers 0Eh and 0Fh are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 µs to 4 h 15 min. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h)

2.4 DEVICE PROTECTION DIAGRAM



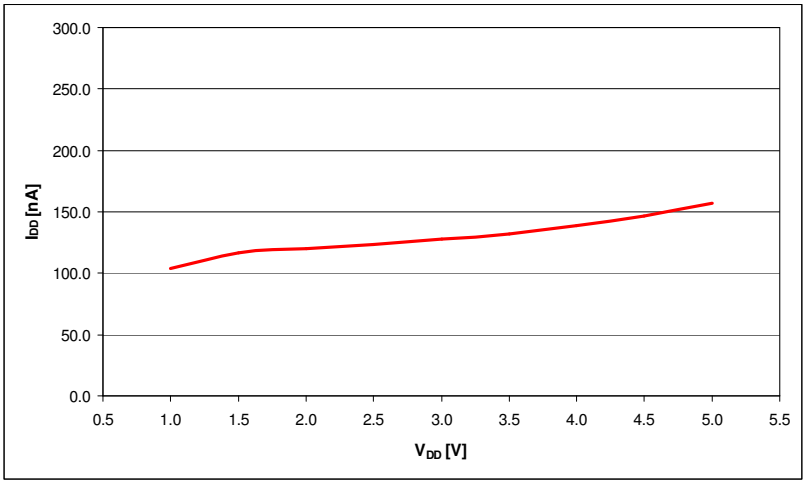
2.5 LOW POWER OPERATION

Minimum power operation will be achieved by reducing the number and frequency of switching signals inside the RTC-IC (low frequency timer clocks) and disabling not required functions such as CLKOUT.

Current consumption vs Supply Voltage

Configuration: "Time keeping mode"

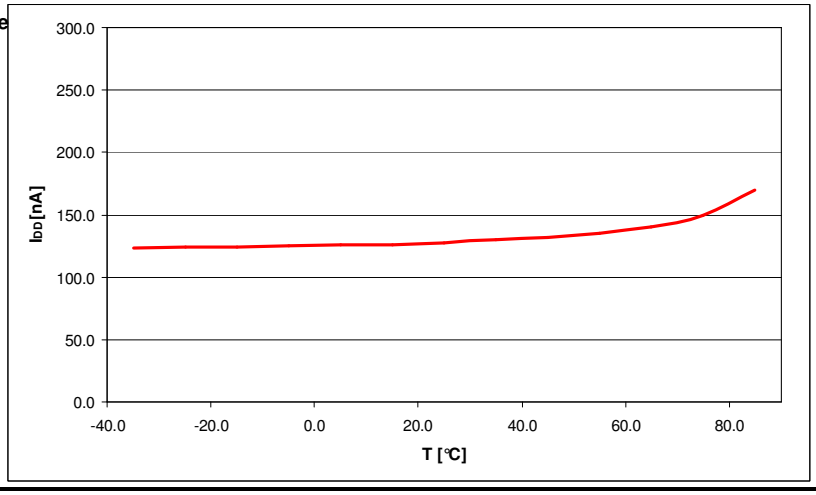
T_{amb}	= 25°C
CLKOUT	disabled
Timer clock	= 1/60 Hz
SPI bus	inactive
INT	inactive



Current consumption vs Temperature range

Configuration: "Time keeping mode"

V_{DD}	3.0 V
CLKOUT	disabled
Timer clock	= 1/60 Hz
SPI bus	inactive
INT	inactive



3.0 REGISTER ORGANIZATION

16 registers (00h – 0Fh) are available.

The time registers are encoded in the Binary Coded Decimal format (BCD) to simplify application use.
Other registers are either bit-wise or standard binary format.
When one of the time registers is read (registers 02h trough 08h), the content of all counters and registers are frozen to prevent faulty reading of the clock/calendar registers during carry condition.

Register overview

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control_1	TEST	SR	STOP	SR	SR	12_24	CIE	0
01h	Control_2	MI	SI	MSF	TI / TP	AF	TF	AIE	TIE
02h	Seconds	OS	40	20	10	8	4	2	1
03h	Minutes	X	40	20	10	8	4	2	1
04h	Hours	X	X	AMPM	10	8	4	2	1
05h	Days	X	X	20	10	8	4	2	1
06h	Weekdays	X	X	X	X	X	4	2	1
07h	Months / Century	X	X	X	10	8	4	2	1
08h	Years	80	40	20	10	8	4	2	1
09h	Minute Alarm	AEN_M	40	20	10	8	4	2	1
0Ah	Hour Alarm	AEN_H	X	20	10	8	4	2	1
0Bh	Day Alarm	AEN_D	X	20	10	8	4	2	1
0Ch	Weekday Alarm	AEN_W	X	X	X	X	4	2	1
0Dh	Offset Register	MODE	OFF6	OFF5	OFF4	OFF3	OFF2	OFF1	OFF0
0Eh	Timer CLKOUT	X	COF2	COF1	COF0	TE	X	CTD1	CTD0
0Fh	Countdown Timer	128	64	32	16	8	4	2	1

Bit positions labelled as "**X**" are not implemented and will return a "**0**" when read.
Bit positions labelled with "**0**" should always be written with logic "**0**".

3.1 STATUS REGISTER FUNCTION

3.1.1 CONTROL_1 (address 00h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control_1	TEST	0	STOP	SR	0	12_24	CIE	0

Bit	Symbol	Value	Description	Reference
7	TEST	0	normal mode	
		1	external clock test mode	do not use
6	SR	0	no software reset	see section 3.1.4
		1	used to initiate software reset (bit 6; 4; 3)	
5	STOP	0	RTC source clock runs	see section 3.8
		1	RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock I stopped. (CLKOUT at 32.768kHz / 16.384 kHz / 8.192 kHz still available)	
4	SR	0	no software reset	see section 3.1.4
		1	used to initiate software reset (bit 6; 4; 3)	
3	SR	0	no software reset	see section 3.1.4
		1	used to initiate software reset (bit 6; 4; 3)	
2	12_24	0	24 hour mode is selected	see section 3.2.1
		1	12 hour mode is selected	
1	CIE	0	No correction interrupt generated	see section 3.7
		1	correction interrupt pulses will be generated at every correction cycle	
0	0	0	unused	

3.1.2 CONTROL_2 (address 01h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control_2	MI	SI	MSF	TI / TP	AF	TF	AIE	TIE

Bit	Symbol	Value	Description	Reference
7	MI	0	minute interrupt is disabled	see section 3.5.1
		1	minute interrupt is enabled	
6	SI	0	second interrupt is disabled	see section 3.5.1
		1	second interrupt is enabled	
5	MSF	0	no minute or second interrupt generated	see section 3.4.1
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
4	TI_TP	0	interrupt pin follows Timer flags	see section 3.4.3
		1	interrupt pin generates a pulse	
3	AF	0	no alarm-interrupt generated	see section 3.3.2
		1	flag set when alarm interrupt generated; flag must be cleared to clear interrupt	
2	TF	0	no countdown timer-interrupt generated	see section 3.4.3
		1	flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt when TI_TP = 0.	
1	AIE	0	no interrupt generated from the alarm flag	see section 3.5.3
		1	interrupt generated when alarm flag is set	
0	TIE	0	no interrupt generated from the countdown timer	see section 3.5.2
		1	interrupt generated by the countdown timer	

3.1.3 OS FLAG (Oscillator Stop Flag; address 01h…bit 7)

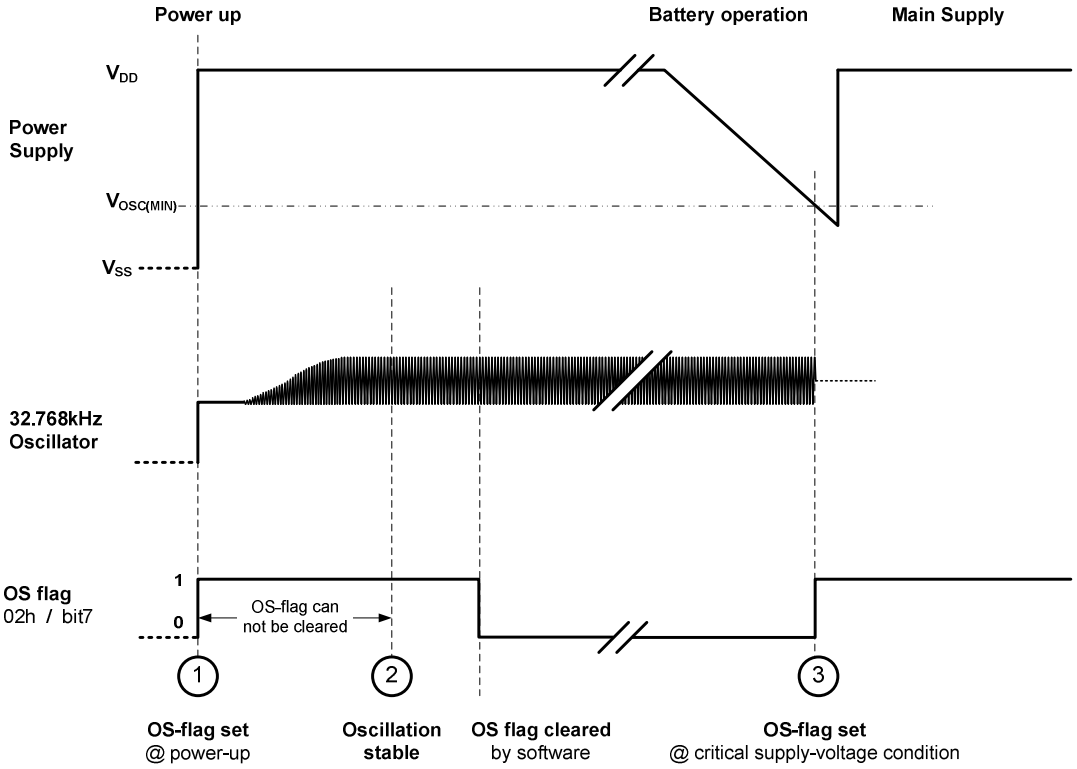
Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Seconds	**OS**	40	20	10	8	4	2	1

The RV-2123-C2 includes a flag (bit OS) which is set whenever the oscillator is stopped, see figure below. The flag will remain set until cleared by software. If the flag can not be cleared, then the RV-2123-C2 oscillator is not running.

This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to a critical level where oscillation might fail and the time-information might be corrupted. The oscillator is also considered to be stopped during the time between power-up and stable crystal oscillation; this time may be in the range of 500ms to 1s depending on the temperature and supply voltage.

At power-up the OS flag is always set.

OS flag set at power-up and critical V_{DD}



(1) OS-flag is automatically set at power-up.

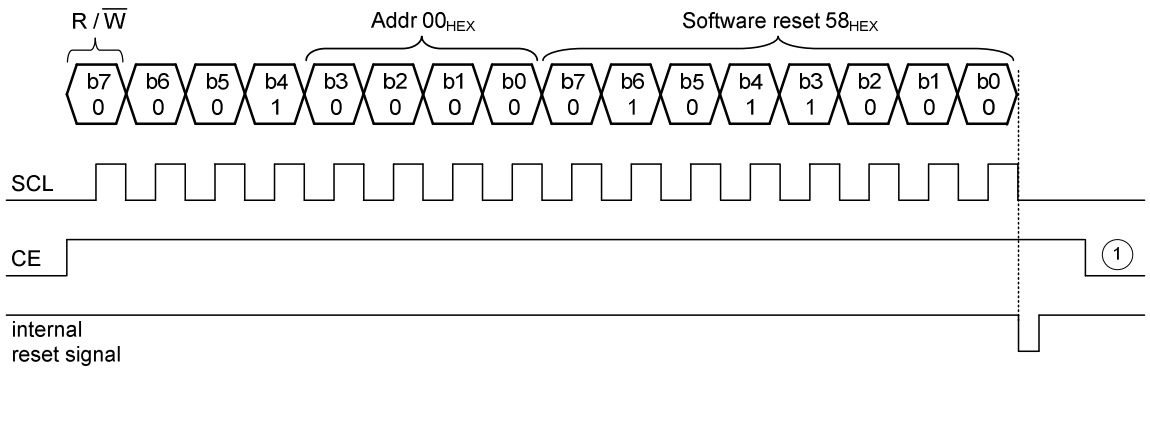
(2) OS-flag can not be cleared until a stable 32.768kHz oscillation is detected, typically it takes 500 to 1000msafter power-up.

(3) The OS-flag is set when the power-supply voltage drops below $V_{OSC(MIN)}$ where the oscillation may fail and the time-information might be corrupted.

3.1.4 RESET; POWER-UP AND SOFTWARE RESET

A reset is automatically generated at power on. A reset can also be initiated with the software reset command. It is generally recommended to make a software reset after power-up. A software reset can be initiated by setting the bits 6, 4 and 3 in register Control_1 to logic 1 and all other bits to logic 0 by sending the bit sequence 01011000b (58h), see below:

Software Reset command



(1) When CE becomes inactive, the Interface is reset.

If this bit sequence is not correct, the software reset instruction will be ignored to protect the device from accidently being reset. When sending the software instruction, the other bits are not written.
The SPI-bus is initialized whenever the chip enable pin CE is inactive

3.1.5 REGISTER RESET VALUES

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Control_1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
01h	Control_2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
02h	Seconds	**1**	X	X	X	X	X	X	X
03h	Minutes	**1**	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X
07h	Months / Century	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute Alarm	**1**	X	X	X	X	X	X	X
0Ah	Hour Alarm	**1**	-	X	X	X	X	X	X
0Bh	Day Alarm	**1**	-	-	-	-	X	X	X
0Ch	Weekday Alarm	**1**	-	-	-	-	X	X	X
0Dh	Offset Register	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
0Eh	Timer CLKOUT	-	**0**	**0**	**0**	**0**	-	**1**	**1**
0Fh	Countdown Timer	X	X	X	X	X	X	X	X

– bits labelled as – are not implemented
X bits labelled as X are undefined at power-up and unchanged by subsequent resets.

After reset, the following mode is entered:

- CLKOUT is activated, the frequency 32.768kHz is selected
- 24 hour mode is selected
- Offset register is set to 0
- No alarm is set
- Timer disabled
- No interrupts enabled

3.2 TIME AND DATE FUNCTION

The majority of the registers are coded in the Binary Coded Decimal (BCD) format; BCD format is used to simplify application use.

3.2.1 SECONDS, MINUTES, HOURS, DAYS, WEEKDAYS, MONTHS, YEARS REGISTER

Seconds (address 02h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Seconds	OS	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	OS	0	clock integrity is guaranteed
		1	clock integrity is not guaranteed, oscillator may have been interrupted or stopped
6 to 0	Seconds	00 to 59	This register holds the current seconds coded in BCD format

Minutes (address 03h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Minutes	X	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	X	-	unused
6 to 0	Minutes	00 to 59	This register holds the current minutes coded in BCD format

Hours (address 04h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Hours	X	X	AMPM	10	8	4	2	1

Bit	Symbol	Value	Description
7 and 6	X	-	unused
12 hour mode			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	Hours	01 to 12 [1]	These registers hold the current hours coded in BCD format for 12 hour mode
24 hour mode [2]			
5 to 0	Hours	00 to 23	These registers hold the current hours coded in BCD format for 24 hour mode

[1] User is requested to pay attention setting valid data only.
[2] Hour mode is set by the 12_24 bit in register Control_1

Days (address 05h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Days	X	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 and 6	X	-	unused
5 to 0	Days	01 to 31	This register holds the current days coded in BCD format [1]

[1] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4; including the year 00.

Weekdays (address 06h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Days	X	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7 to 3	X	-	unused
2 to 0	Days	0 to 6	This register holds the current days coded in BCD format

Day [1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	X	0	0	0
Monday	X	X	X	X	X	0	0	1
Tuesday	X	X	X	X	X	0	1	0
Wednesday	X	X	X	X	X	0	1	1
Thursday	X	X	X	X	X	1	0	0
Friday	X	X	X	X	X	1	0	1
Saturday	X	X	X	X	X	1	1	0

[1)] These bits may be re-assigned by the user.

Months (address 07h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Months	X	X	X	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 5	X	-	unused
4 to 0	Months	01 to 12	This register holds the current months coded in BCD format

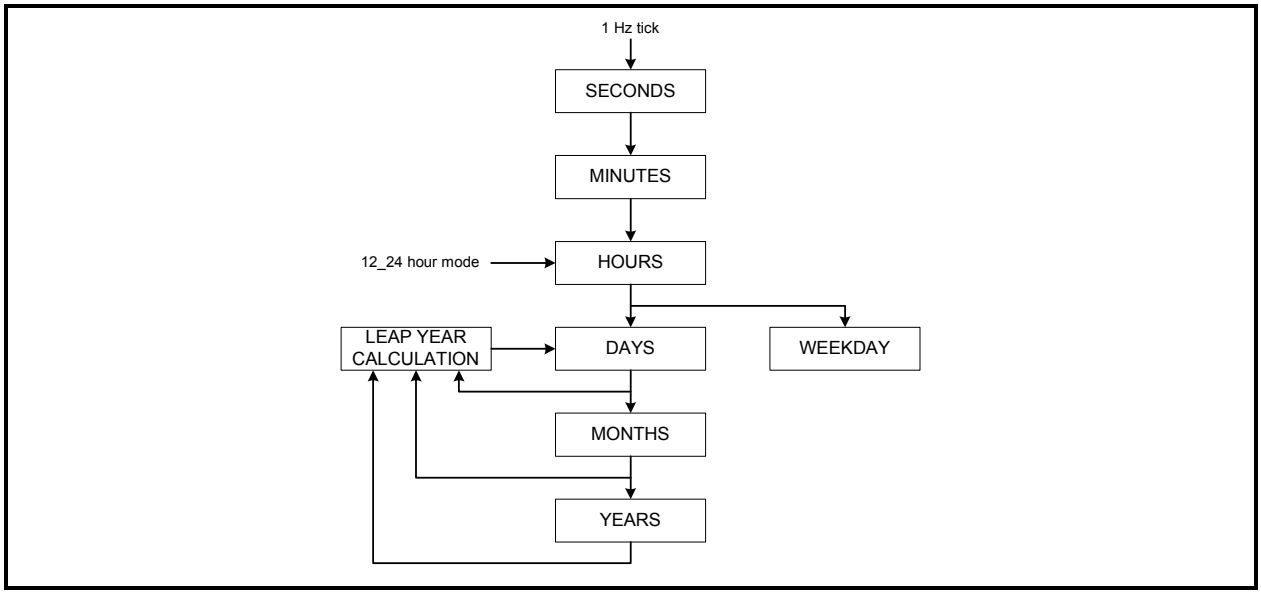
Day	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	X	0	0	0	0	1
February	X	X	X	0	0	0	1	0
March	X	X	X	0	0	0	1	1
April	X	X	X	0	0	1	0	0
May	X	X	X	0	0	1	0	1
June	X	X	X	0	0	1	1	0
July	X	X	X	0	0	1	1	1
August	X	X	X	0	1	0	0	0
September	X	X	X	0	1	0	0	1
October	X	X	X	1	0	0	0	0
November	X	X	X	1	0	0	0	1
December	X	X	X	1	0	0	1	0

Years (address 08h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h	Years	80	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7 to 0	Years	00 to 99	this register holds the current year coded in BCD format

3.2.2 DATA FLOW OF TIME AND DATE FUNCTION



3.3 ALARM FUNCTION

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding alarm enable bit (AENx) is logic 0, then that information will be compared with the current minute, hour, day and weekday information.

Alarm-Minute (address 09h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h	Minute Alarm	AEN_M	40	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AEN_M	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	Minute_Alarm	00 to 59	This register holds the minute alarm information coded in BCD format

Alarm-Hour (address 0Ah…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah	Hour Alarm	AEN_H	X	20	10	8	4	2	1

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1	hour alarm is disabled
6	X	-	unused
12 hour mode			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	Hour_Alarm	01 to 12	These registers hold the hour alarm information coded in BCD format when in 12 hour mode
24 hour mode			
5 to 0	Hour_Alarm	00 to 23	These registers hold the hour alarm information coded in BCD format when in 24 hour mode

Alarm-Day (address 0Bh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh	Day Alarm	AEN_D	X	20	10	8	4	2	1

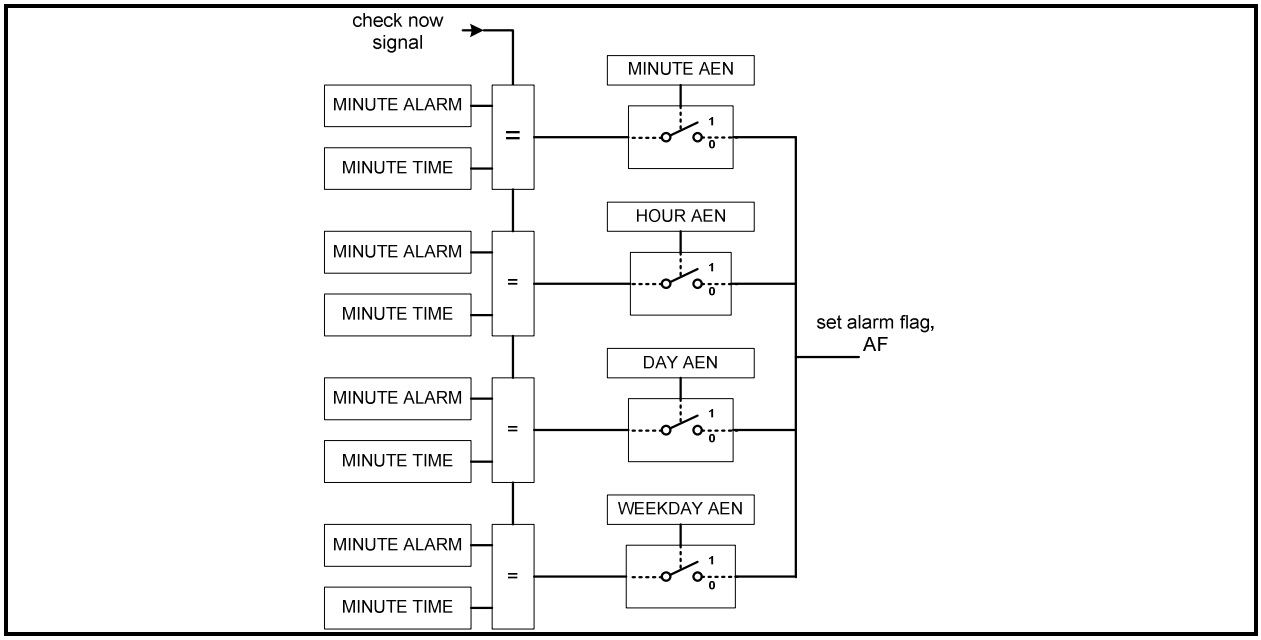
Bit	Symbol	Value	Description
7	AEN_D	0	day alarm is enabled
		1	day alarm is disabled
6	X	-	unused
5 to 0	Day_Alarm	01 to 31	This register holds the day alarm information coded in BCD format

Alarm-Weekday (address 0Ch…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch	Weekday Alarm	AEN_W	X	X	X	X	4	2	1

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
6 to 3	X	-	unused
2 to 0	Weekday_Alarm	0 to 6	This register holds the weekday alarm information coded in BCD format

3.3.1 ALARM FUNCTION BLOCK DIAGRAM

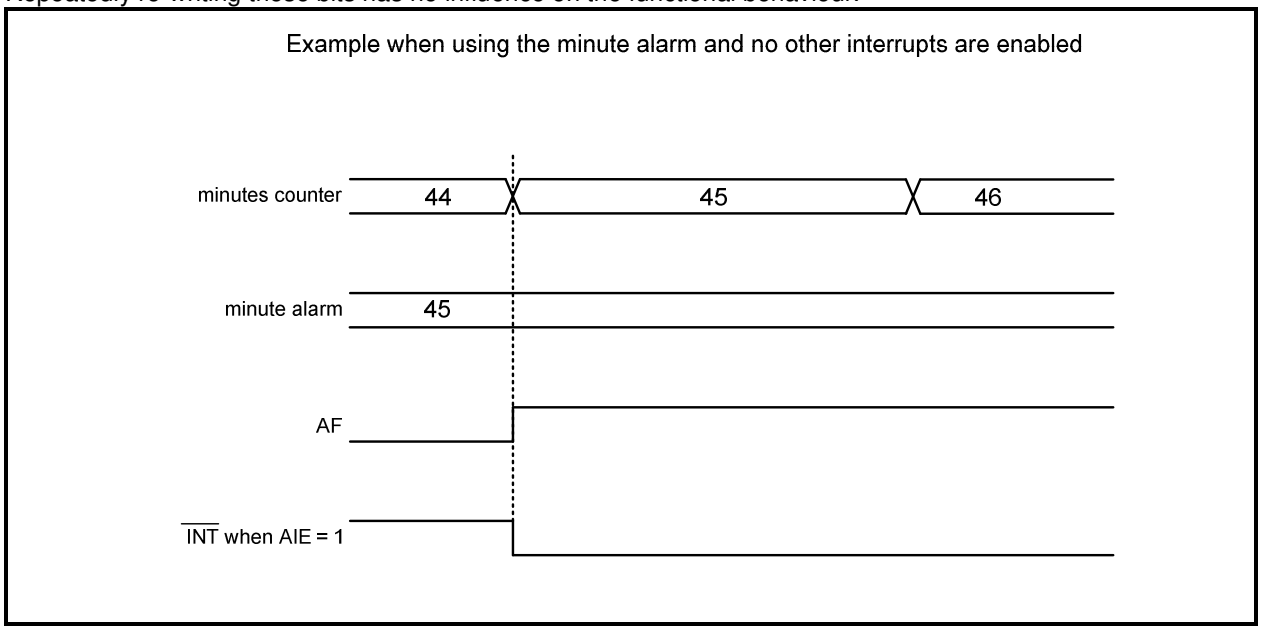


3.3.2 ALARM FLAG

When all enabled comparisons first match, the alarm flag bit AF is set. Bit AF will remain set until cleared by software. Once bit AF has been cleared it will only be set again when the time increments to match the alarm condition once more.

Alarm registers which have their bit AENx at logic 1 are ignored.

The tables below show an example for clearing AF-bit but leaving MSF and TF-bit unaffected. Clearing the flags is made by a write command; therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behaviour.



To prevent the timer flags being overwritten while clearing AF, a logical AND is performed during a write access. Writing a logic 1 will cause the flag to maintain its value, whilst writing a logic 0 will cause the flag to be reset.

The following tables show what instruction must be sent to clear bit AF. In this example, MSF and TF-bit are unaffected

Flag location in register Control_2 (address 01h…bits description)

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control_2	-	-	**MSF**	-	**AF**	**TF**	-	-

Example clearing only AF and leaving MSF and TF-bit unaffected

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control_2	-	-	**1**	-	**0**	**1**	-	-

3.4 TIMER FUNCTIONS

The RV-2123-C2 offers different Alarm and Timer functions which allow to simply generating highly versatile timing-functions:

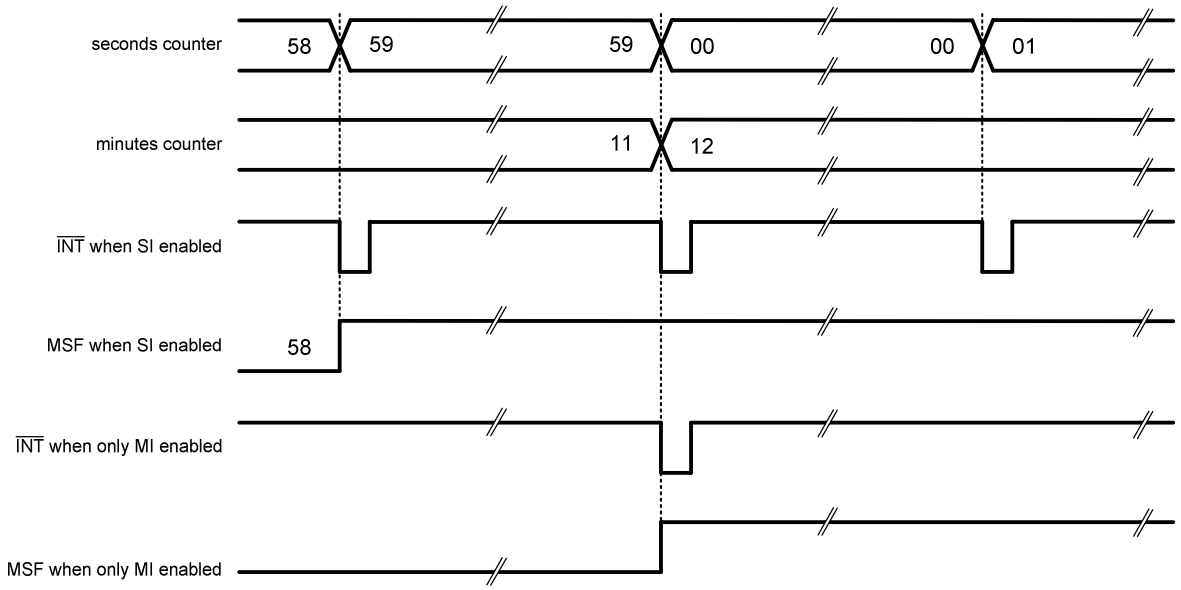
- Second and Minute Timer Interrupt (SI /MI in register Control_2; address 01h…..bits 7 and 6)
- Countdown Timer (register Coundown Timer; address 0fh…..bits 7-0) clocked by four selectable source clocks (4.096 kHz, 64 Hz, 1 Hz, or $^1/_{60}$Hz) controlled by the register Timer_CLKOUT at address 0Eh.
- The Interrupt can be configured to either generate a pulse or to follow the status of the interrupt flags generating a periodic Interrupt by the bit TI_TP (TI_TP in register Control_2; address 01h…..bit 4)

3.4.1 SECOND AND MINUTE TIMER INTERRUPT

The minute and second interrupts (bits SI and MI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from each other, however a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time.

$\overline{\text{INT}}$ example for SI and MI

In this example it is assumed that the timer flag is cleared before the next countdown period expires and that the pin $\overline{\text{INT}}$ is set to periodic mode.



The bit MSF (Minute and Second Flag) is set to logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{\text{INT}}$ pulse generation, even when the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{\text{INT}}$ pulse will still be generated.
The purpose of the flag is to allow the controlling system to interrogate the RV-2123-C2 and identify the source of the interrupt i.e. minute/second, countdown timer or alarm.

Effects of bits MI and SI on MSF and $\overline{INT}$ generation

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control_2	**MI**	**SI**	**MSF**	TI / TP	AF	TF	AIE	TIE

Bit	Bit 7	Bit 6	Result	Bit 5
	MI	**SI**		**MSF**
7 to 5	0	0	no interrupt generated	MSF never set
	0	1	an interrupt once per minute	MSF sets when minute-counter increments
	1	0	an interrupt once per second	MSF sets when second-counter increments
	1	1	an interrupt once per second	MSF sets when second-counter increments

The duration of both minute- and second-timers will be affected by the frequency-offset compensation in the register Offset_Register (address 0Dh…bits 7:0; see section 3.7. Only when the Offset_Register has the value 00h there won't be any correction pulses and the minute and second timer periods will be consistent.

3.4.2 COUNTDOWN TIMER FUNCTION

The 8-bit countdown timer at address 0Fh has four selectable source clocks (4.096kHz,64Hz,1Hz, or $^1/_{60}$Hz) controlled by the register Timer_CLKOUT at address 0Eh. The combination of the selectable source-clocks and the countdown timer value n allows for countdown periods in the range from 244 µs to 4h 15min.

Registers 01h, 0Eh and 0Fh are used to control the Countdown Timer function and Interrupt output.

Bit TE enables / disables the Countdown Timer.
Bits CTD0 and CTD1 select the timer-frequency and countdown-timer duration.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Timer CLKOUT	X	COF2	COF1	COF0	**TE**	X	**CTD1**	**CTD0**

Bit	Symbol		Value	Description		
3	TE	0	Countdown timer is disabled			
		1	Countdown timer is enabled			
1 to 0	**Bit 1**	**Bit 0**	**Timer Source Clock frequency** [1]	**Timer duration**		
	CTD1	CTD0		**Minimum n=1**	**Maximum n=255**	
	0	0	4.096 kHz	244 µs	62.256 ms	
	0	1	64 Hz	15.625 ms	3.984 s	
	1	0	1 Hz [2]	1 s	255 s	
	1	1	$^1/_{60}$ Hz [2]	60 s	4 h 15 min	

[1] When not in use, CTD must be set to $^1/_{60}$ Hz for power saving
[2] Time periods can be affected by correction pulses

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

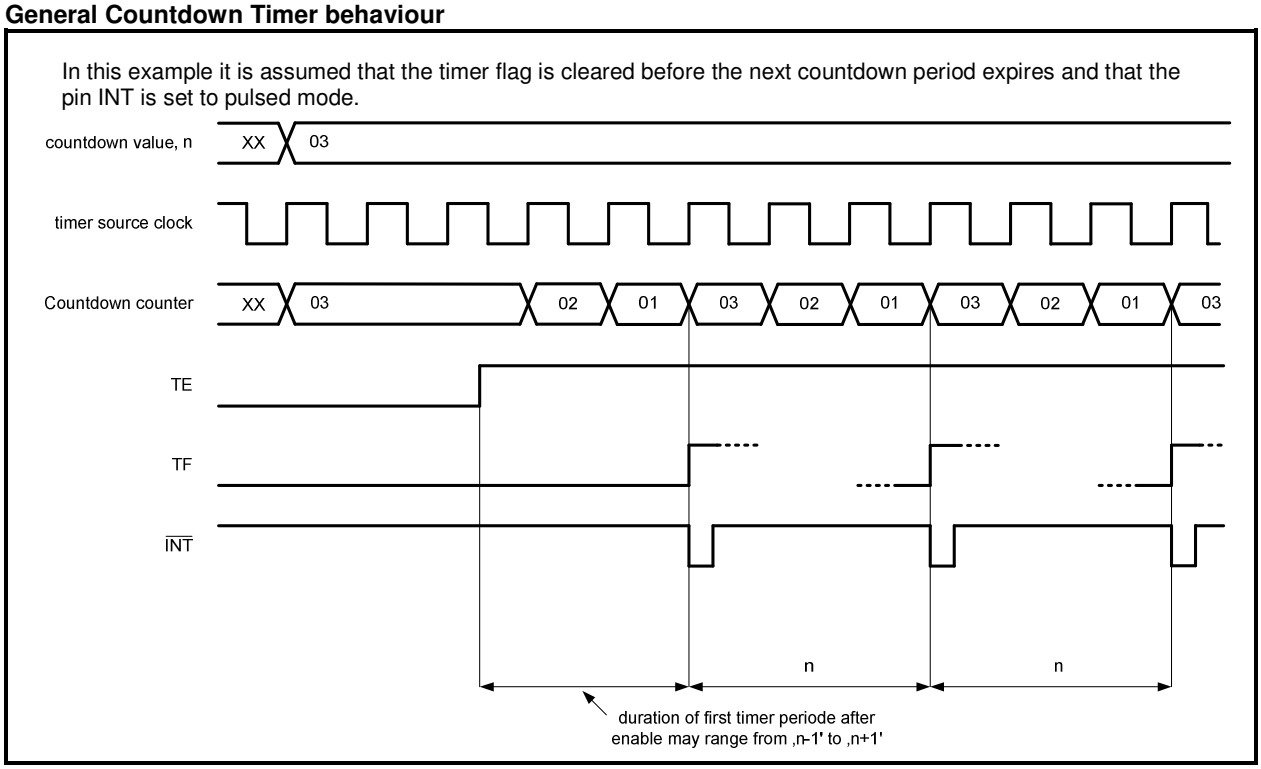
Register Countdown Timer (address 0Fh…bits description)
Registers 0Fh is loaded with the countdown timer value n.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh	Countdown Timer	128	64	32	16	8	4	2	1

Bit	Symbol	Value	Description	Reference
7 to 0	Countdown Timer	00 to FF	Countdown value = n Countdown period $= \frac{n}{SourceClockFrequency}$	

The timer counts down from a software-loaded 8-bit binary value, n.
Values from 1 to 255 are valid; loading the counter with 0 effectively stops the timer. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next Timer Period. Reading the timer will return the current value of the countdown counter, see figure below.

General Countdown Timer behaviour



If a new value of n is written before the end of the current timer period, then this value will take immediate effect. Micro Crystal does not recommend to changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous to the timer clock, therefore changing it without setting bit TE = 0 may result in a corrupted value loaded into the countdown counter which results an undetermined countdown period for the first period. The countdown value n will however be correctly stored and correctly loaded on subsequent timer periods.
When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See section 3.5 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see table below.

First period delay for Countdown Timer Counter value n

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Timer CLKOUT	X	COF2	COF1	COF0	TE	X	**CTD1**	**CTD0**

Bit	Symbol		Value	Description		
1 to 0	**Bit 1**	**Bit 0**	**Timer Source Clock frequency**		**First period delay for countdown timer**	
	CTD1	CTD0			**Minimum**	**Maximum**
	0	0	4.096 kHz		n	n+1
	0	1	64 Hz		n	n+1
	1	0	1 Hz		(n-1) +$^{1}/_{64}$ Hz	n +$^{1}/_{64}$ Hz
	1	1	$^{1}/_{60}$ Hz		(n-1) +$^{1}/_{64}$ Hz	n +$^{1}/_{64}$ Hz

3.4.2 COUNTDOWN TIMER FUNCTION (continue)

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF may only be cleared by software. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see section 3.5.2.

When reading the timer, the current countdown value is returned and not the initial value n. For accurate read back of the countdown value, the SPI-bus clock (SCL) must operate at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1Hz and $^1/_{60}$Hz will be affected by the Offset_Register. The duration of a program period will vary according to when the offset is initiated. For example, if a 100s timer is set using the 1Hz clock as source, then some 100s periods will contain correction pulses and there for be longer or shorter depending on the setting of the Offset_Register. See section 3.7 to understand the operation of the Offset_Register.

3.4.3 TIMER FLAGS

When a minute or second interrupt occurs, bit MSF is set to logic1. Similarly, at the end of a timer countdown or alarm event, bit TF or AF are set to logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logical AND is performed during a write access. Writing a logic1 will cause the flag to maintain it's value, whilst writing a logic0 will cause the flag to be reset. Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behaviour.

Flag location in register Control_2 (address 01h…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Control_2	MI	SI	**MSF**	TI / TP	**AF**	**TF**	AIE	TIE
Example to clear only Timer Flag TF (bit 2) in register Control_2									
01h	Control_2	-	-	**1**	-	**1**	**0**	-	-
Example to clear only Minute-Second Flag MSF (bit 5) in register Control_2									
01h	Control_2	-	-	**0**	-	**1**	**1**	-	-
Example to clear both Timer Flag TF (bit 2) and Minute-Second Flag MSF (bit 5) in register Control_2									
01h	Control_2	-	-	**0**	-	**1**	**0**	-	-

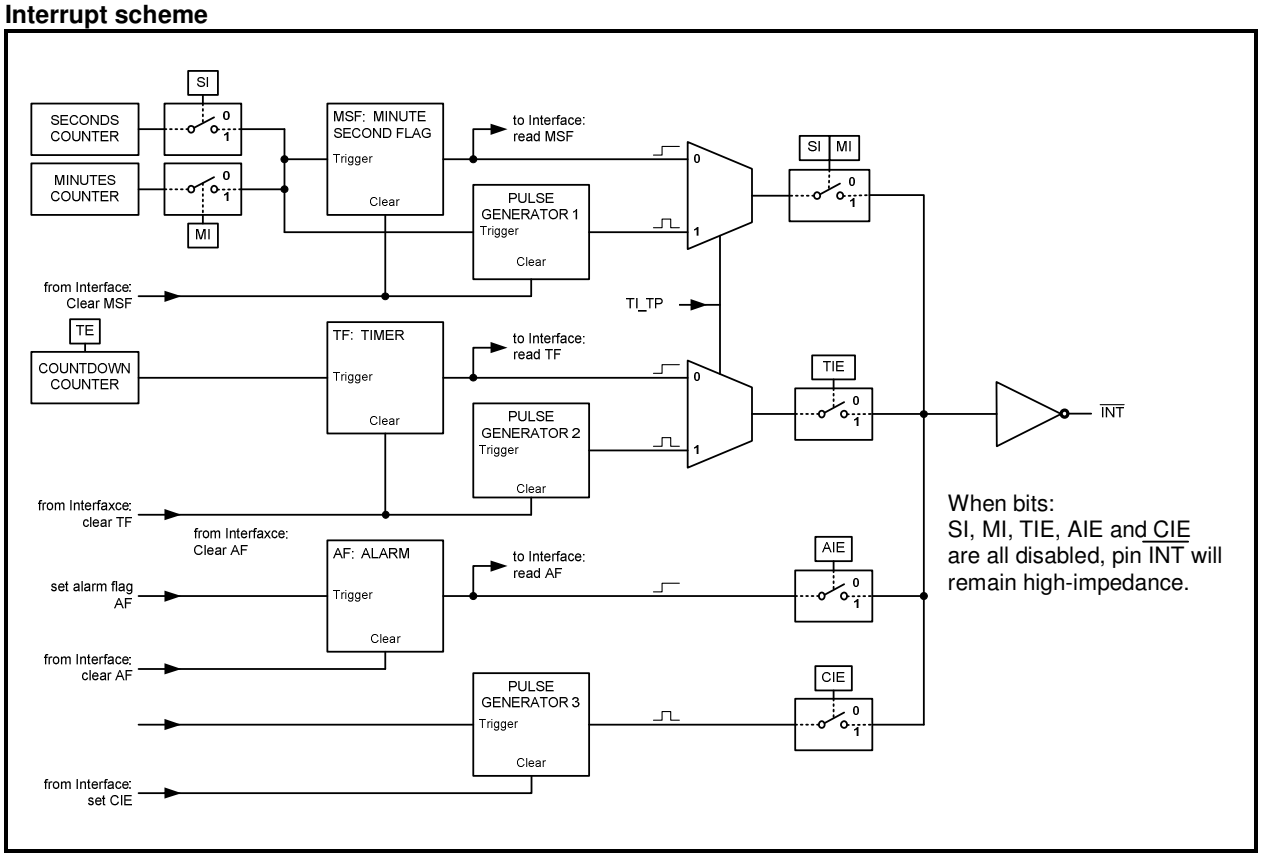
Clearing the alarm flag (bit AF) operates in exactly the same way.

3.5 INTERRUPT OUTPUT

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts may be sourced from four places: Second / Minute Timer, Countdown Timer, Alarm Function or Offset Function.

With bit TI_TP, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags (bits TF and MSF). Correction interrupt pulses are always $^{1}/_{128}$ seconds long.
Alarm interrupts always follow the condition of AF.

Interrupt scheme



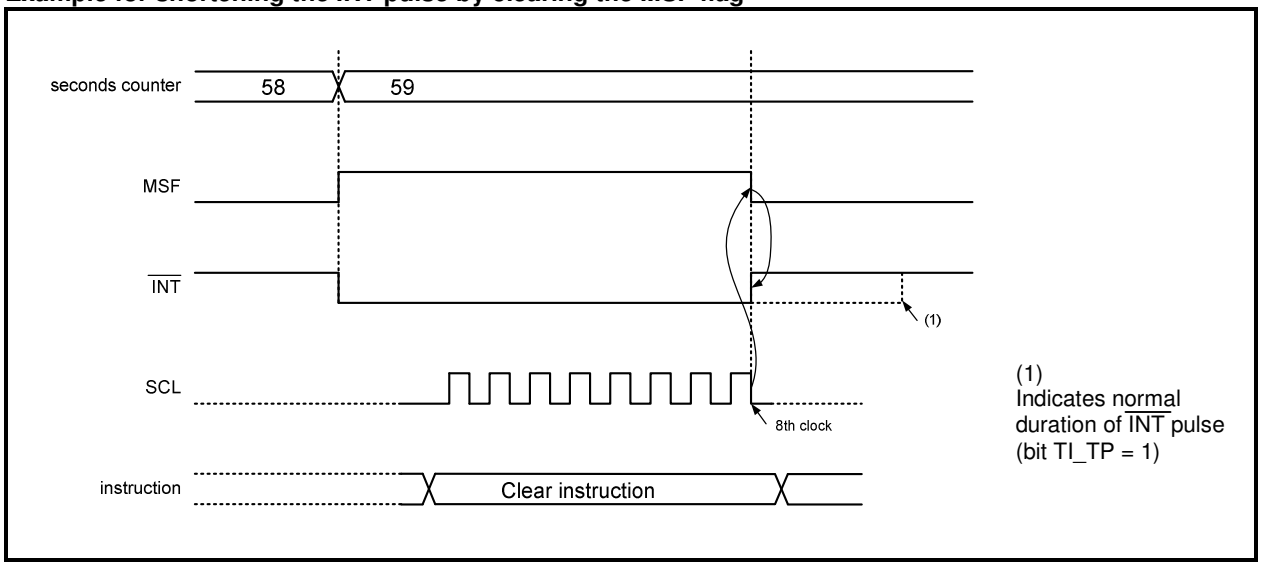
Note: The Interrupts from the three groups are wired-OR, meaning they will mask one another.

3.5.1 MINUTE / SECOND INTERRUPTS

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^1/_{64}$ seconds in duration.

If the MSF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e. the system does not have to wait for the completion of the pulse before continuing; see below Figure.

Example for shortening the $\overline{INT}$ pulse by clearing the MSF flag



The timing shown for clearing bit MSF in figure above is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, where $\overline{INT}$ may be shortened by setting both MI and SI or MSF to logic 0.

3.5.2 COUNTDOWN TIMER INTERRUPTS

Generation of interrupts from the countdown timer is controlled via the bit TIE, see section 3.1.2.

The pulse generator for the countdown timer interrupt is also based on the internal clock, but the timing is dependent on the selected source clock for the Countdown Timer and on the Countdown Value n. As a consequence, the width of the interrupt pulse varies, see table below.

$\overline{INT}$ operation (bit TI_TP = 1)

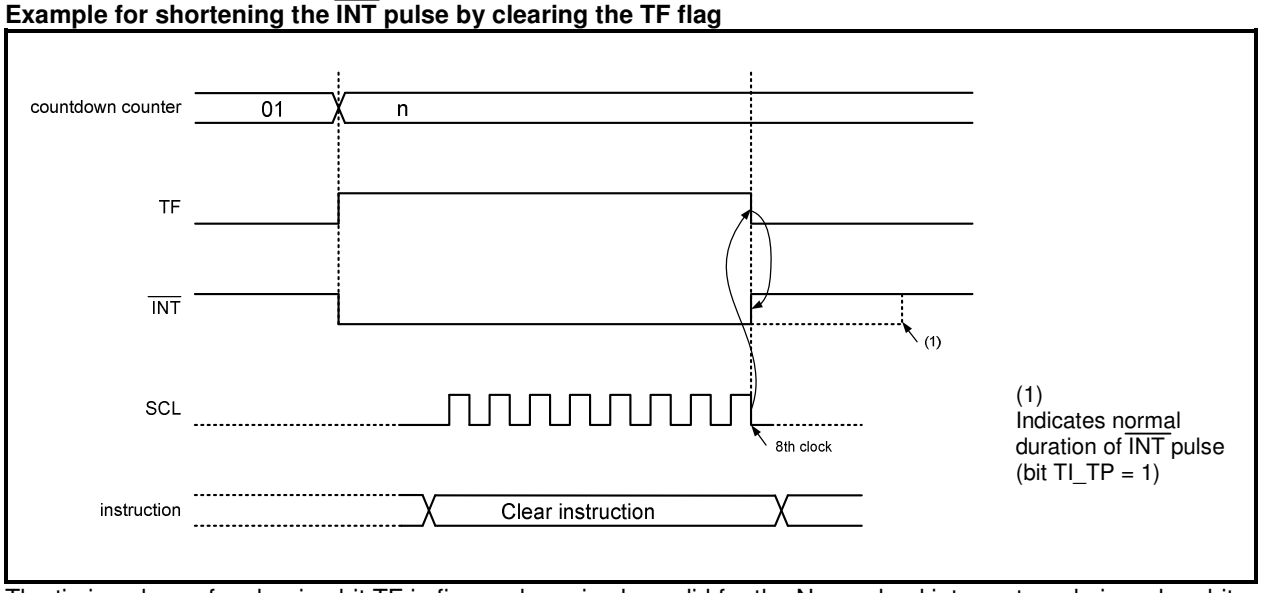
Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Timer CLKOUT	X	COF2	COF1	COF0	TE	X	**CTD1**	**CTD0**

Bit	Symbol				
	Bit 1	Bit 0	Timer Source Clock frequency	INT period [s]	
	CTD1	CTD0		n = 1 [1]	n > 1 [1]
1 to 0	0	0	4.096 kHz	$^1/_{8192}$	$^1/_{4096}$
	0	1	64 Hz	$^1/_{128}$	$^1/_{64}$
	1	0	1 Hz	$^1/_{64}$	$^1/_{64}$
	1	1	$^1/_{60}$ Hz	$^1/_{64}$	$^1/_{64}$

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing, see below Figure.
Instructions for clearing MSF can be found in section 3.4.3

Example for shortening the $\overline{INT}$ pulse by clearing the TF flag

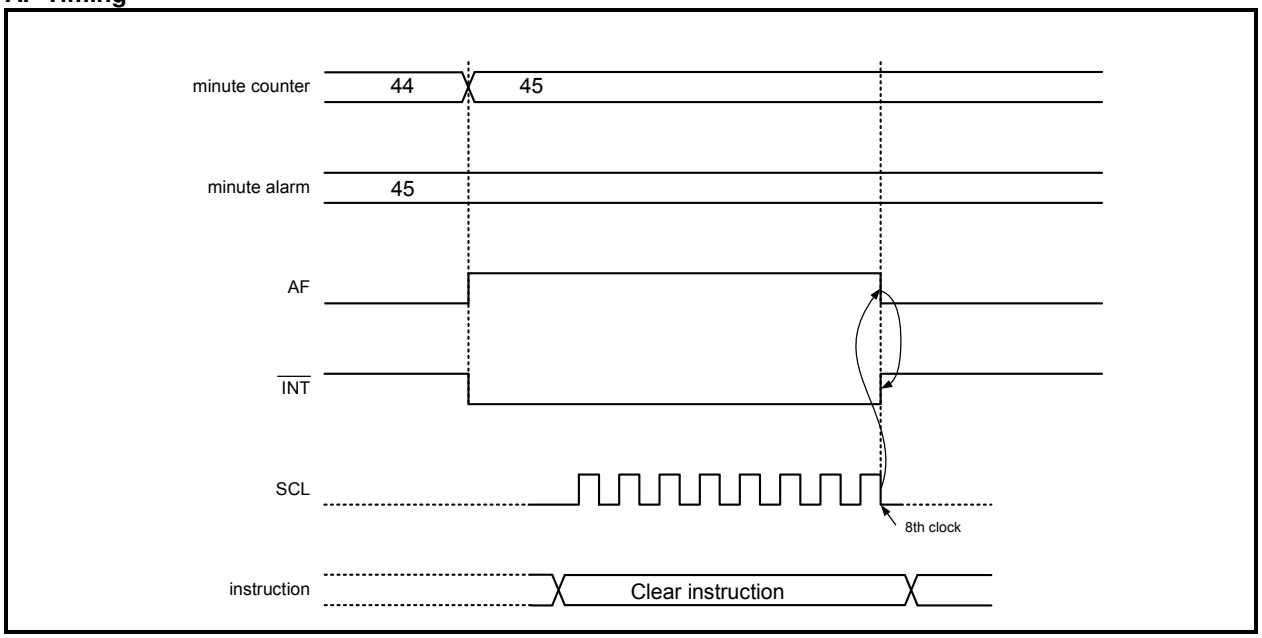


The timing shown for clearing bit TF in figure above is also valid for the Non-pulsed interrupt mode i.e. when bit TI_TP = 0, where $\overline{INT}$ may be shortened by setting bit TIE to logic0.

3.5.3 ALARM INTERRUPTS

Generation of interrupts from the Alarm function is controlled via bit AIE, see section 3.2.1. If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. Clearing bit AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts, see figure below.

AF Timing



Example where only the minute alarm is used and no other interrupts are enabled

3.5.4 CORRECTION PULSE INTERRUPTS

Interrupt pulses generated by correction events can be shortened by writing a logic 1 to bit CIE in register Control_1.

3.6 CLOCK OUTPUT CLKOUT

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF bits in the register Timer_CLKOUT. Frequencies of 32.768 kHz (default) down to 1Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is high-impedance.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation all, except the 32.768 kHz frequencies will be 50:50.

The 'STOP' function can also affect the CLKOUT signal, depending on the selected frequency. When 'STOP' is active, the CLKOUT pin will generate a continuous LOW for those frequencies that can be stopped. For more details see section 3.8.

Register Timer CLKOUT / CLKOUT Frequency Selection (address 0Eh…bits description)

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh	Timer CLKOUT	X	**COF2**	**COF1**	**COF0**	TE	X	CTD1	CTD0

Bit	Bit 6	Bit 5	Bit 4	CLKOUT frequency	typ. duty-cycle [1]	Effect of 'Stop'
	COF2	COF1	COF0	[Hz]	[%]	
6 to 4	0	0	0	32768	40:60 to 60:40	no effect
	0	0	1	16384	50:50	no effect
	0	1	0	8192	50:50	no effect
	0	1	1	4096	50:50	CLKOUT = LOW
	1	0	0	2048	50:50	CLKOUT = LOW
	1	0	1	1024	50:50	CLKOUT = LOW
	1	1	0	1 [2]	50:50	CLKOUT = LOW
	1	1	1	CLKOUT = high-Z		

[1] Duty cycle definition: % HIGH-level time : % LOW-level time
[2] 1 Hz clock pulses will be affected by offset correction pulses

3.6.1 CLOCK OUTPUT ENABLE PIN CLKOE

The CLKOE pin can be used to block the CLKOUT function and force the CLKOUT pin to a High-Impedance state. The effect is the same as setting COF[2:0]=111.

3.7 FREQUENCY OFFSET COMPENSATION REGISTER

The RV2123-C2 incorporates an offset register (address 0Dh) which can be used to implement several functions, like:

- Accuracy tuning
- Ageing adjustment
- Temperature compensation

The offset is made once every two hours in the normal mode, or once every hour in the coarse mode. Each LSB will introduce an offset of 2.17ppm for normal mode and 4.34ppm for coarse mode.
The values of 2.17ppm and 4.34ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63LSB to –64 LSB.

Frequency Offset Compensation

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh	Offset Register	MODE	OFF6	OFF5	OFF4	OFF3	OFF2	OFF1	OFF0

Bit	Symbol	Value	Description
7	Mode	0	Normal mode…correction is triggered once per 2 hours…1 LSB = 2.17 ppm
		1	Coarse mode…correction is triggered once per hour… 1 LSB = 4.34 ppm
6	OFF6	0	Frequency Offset correction faster
		1	Frequency Offset correction slower
5 to 0	Offset	00 to 63	These registers hold the frequency offset correction value in Binary format

Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Offset Correction Value in Decimal	Offset value in ppm	
								Normal Mode Bit 7 = 0	Course Mode Bit 7 = 1
0	1	1	1	1	1	1	+63	+136.71	+273.42
0	1	1	1	1	1	0	+62	+134.54	+269.08
			:				:	:	
0	0	0	0	0	1	0	+2	+4.34	+8.68
0	0	0	0	0	0	1	+1	+2.17	+4.34
0	**0**	**0**	**0**	**0**	**0**	**0**	**0** [1)]	**0**	**0**
1	1	1	1	1	1	1	-1	-2.17	-4.34
1	1	1	1	1	1	0	-2	-4.34	-8.68
			:				:	:	:
1	0	0	0	0	0	1	-63	-136.71	-273.42
1	0	0	0	0	0	0	-64	-138.88	-277.76

[1)] Default mode

The correction is made by adding or subtracting 64Hz clock correction pulses, thereby changing the period of a single second.

In normal mode, the correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values has been implemented.

In coarse mode, the correction is triggered once per hour and then correction pulses are applied once per minute up to a maximum of 60 minutes. When correction values of greater than 60 are used, additional correction pulses are made in the 59th minute see table on the next page:

3.7 FREQUENCY OFFSET COMPENSATION REGISTER (continue)

Correction pulses for coarse mode

Offset Correction Value	Hour : Minute	Correction pulses on INT per minute
+1 or -1	02 : 00	1
	02 : 01 to 02 : 59	0
+2 or -2	02 : 00	1
	02 : 01	1
	02 : 02 to 02 : 59	0
+3 or -3	02 : 00	1
	02 : 01	1
	02 : 02	1
	02 : 03 to 02 : 59	0
:	:	:
+59 or -59	02 : 00 to 02 : 58	1
	02 : 59	0
+60 or -60	02 : 00 to 02 : 59	1
+61 or -61	02 : 00 to 02 : 58	1
	02 : 59	2
+62 or -62	02 : 00 to 02 : 58	1
	02 : 59	3
+63 or -63	02 : 00 to 02 : 58	1
	02 : 59	4
-64	02 : 00 to 02 : 58	1
	02 : 59	5

[1] Example is given in a time range from 02:00 to 02:59
[2] Correction INT pulses are 1/128 seconds wide; for multiple pulses they are repeated at $^1/_{64}$ s interval.

It is possible to monitor when correction pulses are applied. The correction interrupt enable mode (CIE) will generate a $^1/_{128}$ second pulse on $\overline{INT}$ for every correction applied. In the case where multiple correction pulses area applied, a $^1/_{128}$ second interrupt pulse will be generated and repeated every $^1/_{64}$ seconds.

Correction is applied to the 1Hz clock. Any Timer or Clock-Output using a frequency of 1Hz or slower will also be affected by the Offset Correction pulses.

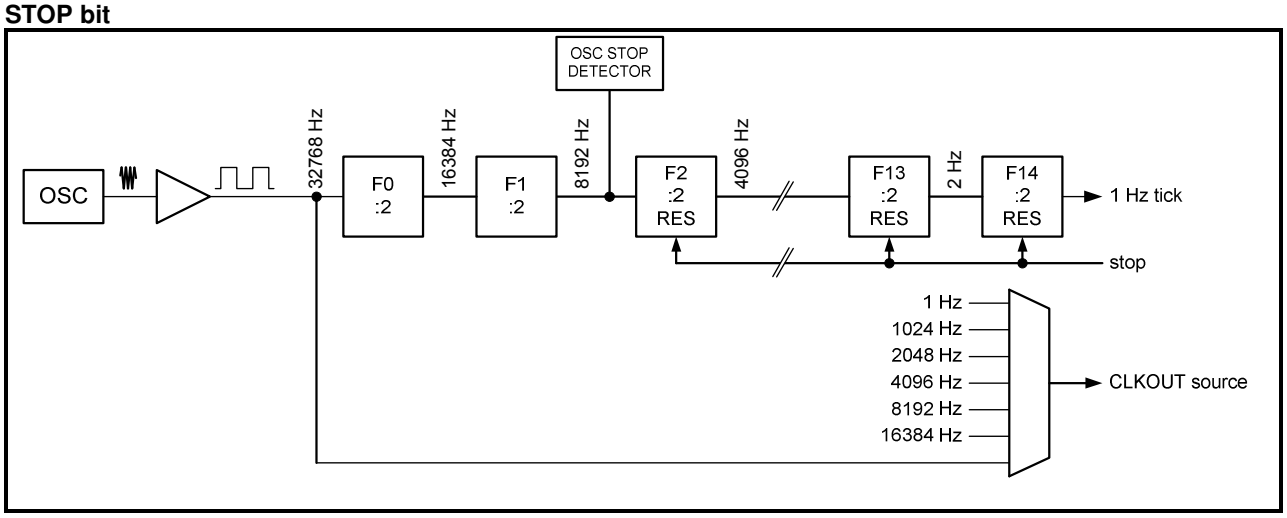
Effect of Offset Correction Pulses

CLKOUT Frequency [Hz]	Effect of Offset Correction	Timer source clock frequency [Hz]	Effect of Offset Correction
32768	no effect	4096	no effect
16384	no effect	64	no effect
8192	no effect	1	effected
4096	no effect	1/60	effected
2048	no effect		
1024	no effect		
1	effected		

3.8 STOP BIT FUNCTION

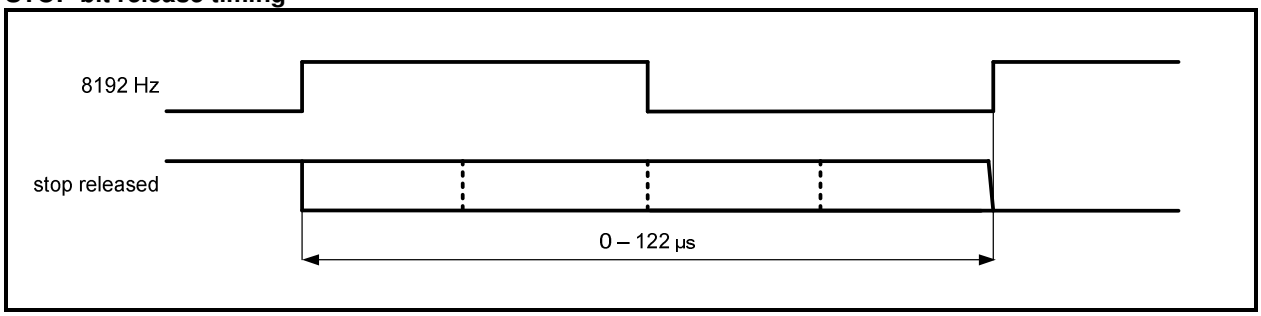
The function of the STOP bit is to allow for accurate starting of the time circuits. The stop function will cause the upper part of the prescaler (F2 to F14) to be held in reset and thus no 1Hz ticks will be generated. The time circuits can then be set and will not increment until the stop is released, see figure below.
Stop will not affect the output of 32.768 kHz, 16.384 kHz or 8.192 kHz, see section 3.6.

STOP bit



The lower two stages of the prescaler (F0 and F1) are not reset and because the SPI interface is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and $^{1}/_{8192}$ Hz cycle, see figure below.

STOP bit release timing



The first increment of the time circuits is between 0.499888 s and 0.500000 s after stop is released.
The uncertainty is caused by the prescaler bits F0 and F1 not being reset, see figure on top of the page.

4.0 3-LINE SERIAL INTERFACE (SPI)

Data transfer to and from the device is made via a 3-wire SPI-bus.

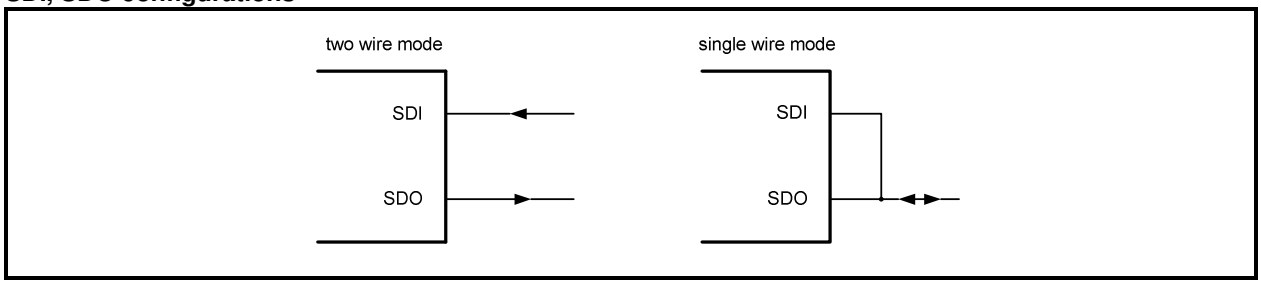
The data-lines for input and output are split into two separate-lines, however, the Data-Input and Data-Output lines can be connected together to facilitate a bidirectional data bus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first

Serial Interface SPI

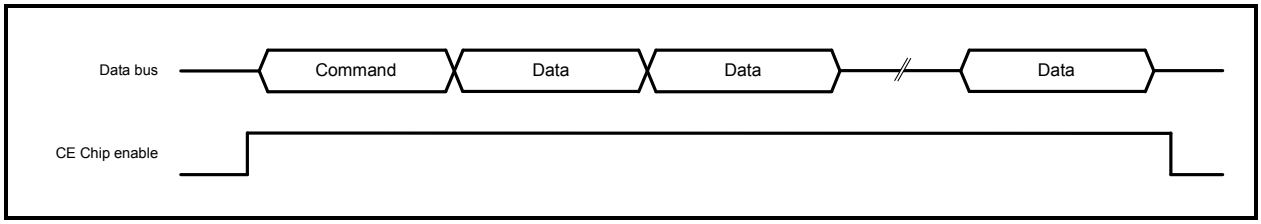
Symbol	Function	Pin #	Description
SCL	Serial Clock Input	3	Serial Clock Input pin; this Input may float when CE is LOW (inactive), may be higher than V_{DD}
SDI	Serial Data Input	4	Serial Data Input pin; this Input may float when CE is LOW (inactive), may be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	Serial Data Output	5	Serial Data Output pin; push-pull drives from V_{SS} to V_{DD}; high-impedance when not driving; can be connected to SDI for single-wire data line, output data is changed on the falling edge of SCL.
CE	Chip Enable input	7	Chip Enable input active HIGH but may not be wired permanently HIGH, with internal pull-down, when LOW the interface is reset; may be higher than $V_{DD,}$

The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Data is sampled on the rising edge of the clock and transferred internally on the falling edge.

SDI, SDO configurations



Data transfer overview



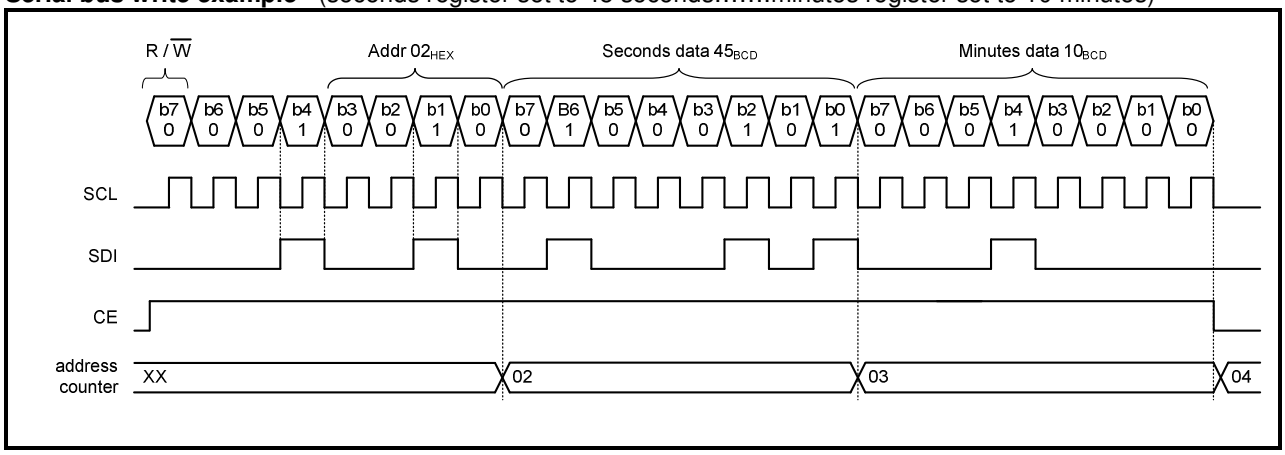
The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will rollover to zero after the last register is accessed. The read/$\overline{\text{write}}$ bit (R/$\overline{\text{W}}$) defines if the following bytes will be read or write information.

Command Byte definition

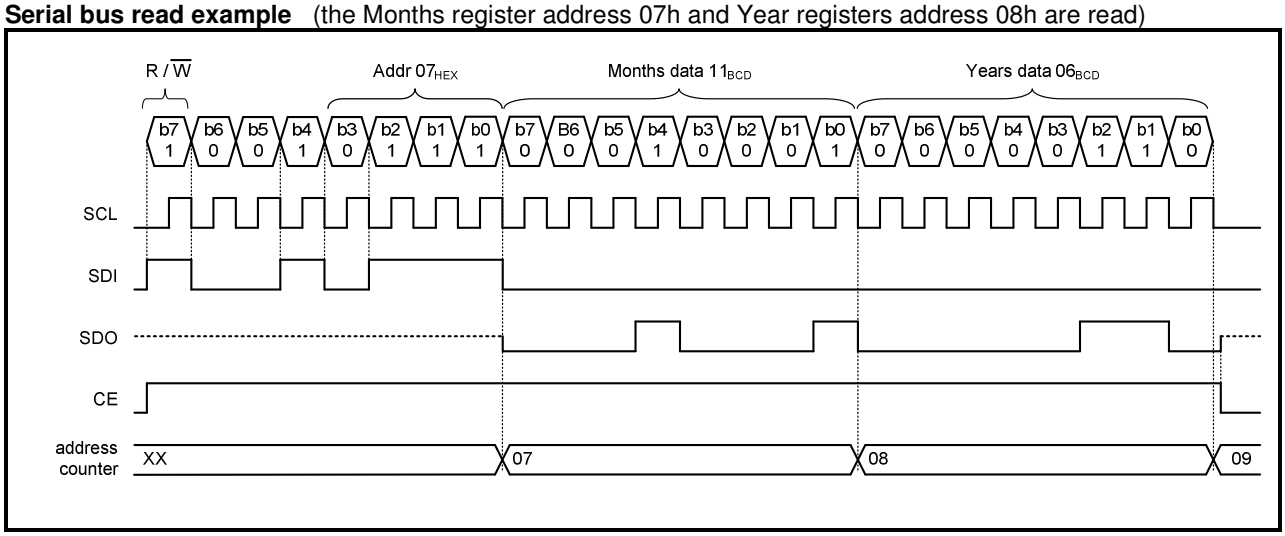
Bit	Symbol	Value	Description
7	R/W	**data read or write selection**	
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes will cause the device to ignore data transfer
3 to 0	RA	0h - Fh	register address range

4.1 SERIAL BUS READ / WRITE EXAMPLES

Serial bus write example (seconds register set to 45 seconds…….minutes register set to 10 minutes)



Serial bus read example (the Months register address 07h and Year registers address 08h are read)



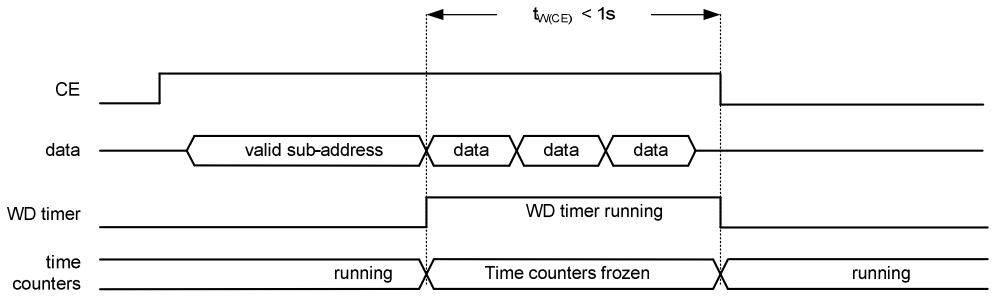
In this example the Months and Years registers are read, pins SDI and SDO are not connected together.
In this configuration it is important, that SDI pin is never left floating, it always must be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result. Short transission periods in the order of 200ns will not cause any problems.

4.2 INTERFACE WATCHDOG TIMER

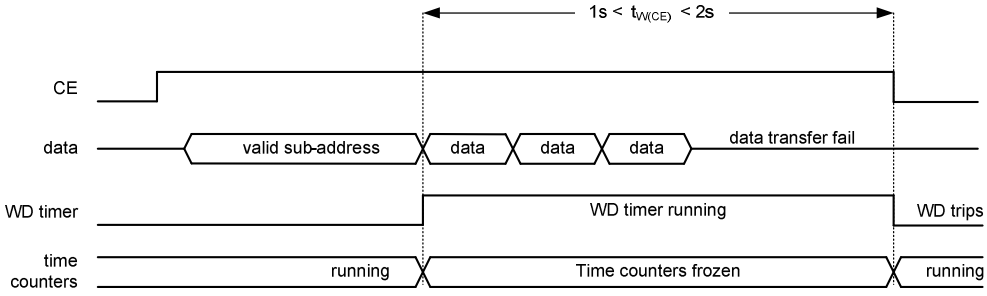
During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the RV-2123-C2 has a built in Watchdog Timer function.
Should the interface be active for more than 1 s from the time a valid sub-address is transmitted, then the RV-2123-C2 will automatically clear the Interface and allow the time counting circuits to continue counting.
CE must return LOW once more before a new data transfer can be executed.

Interface Watchdog Timer

Correct data transfer; read or write



Incorrect data transfer exceeding watchdog period; read or write:



The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 second will be lost from the time counters. The watchdog will triggered between 1 s and 2 s from receiving a valid sub-address and then will automatically clear the interface and allow the time counting circuits continue counting.

5.0 ELECTRICAL CHRACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System IEC 60134

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply voltage	V_{DD}	> GND / < V_{DD}	GND -0.5	+6.5	V
Supply current	I_{DD} ; I_{SS}	V_{DD} Pin	-50	+50	mA
Input voltage	V_I	Input Pin	GND -0.5	V_{DD} +0.5	V
Output voltage	V_O	$\overline{INT}$ / CLKOUT	GND -0.5	V_{DD} +0.5	V
DC Input current	I_I		-10	+10	mA
DC Output current	I_O		-10	+10	mA
Total power dissipation	P_{TOT}			300	mW
Operating ambient temperature range	T_{OPR}		-40	+85	°C
Storage temperature range	T_{STO}	stored as bare product	-55	+125	°C
Electro Static Discharge voltage	V_{ESD}	HBM [1)] MM [2)]		±3000 ±300	V V
Latch-up current	I_{LU}	[3)]		200	mA

1) HBM: Human Body Model, according to JESD22-A114.
2) MM: Machine Model, according to JESD22-A115.
3) Latch-up testing, according to JESD78.

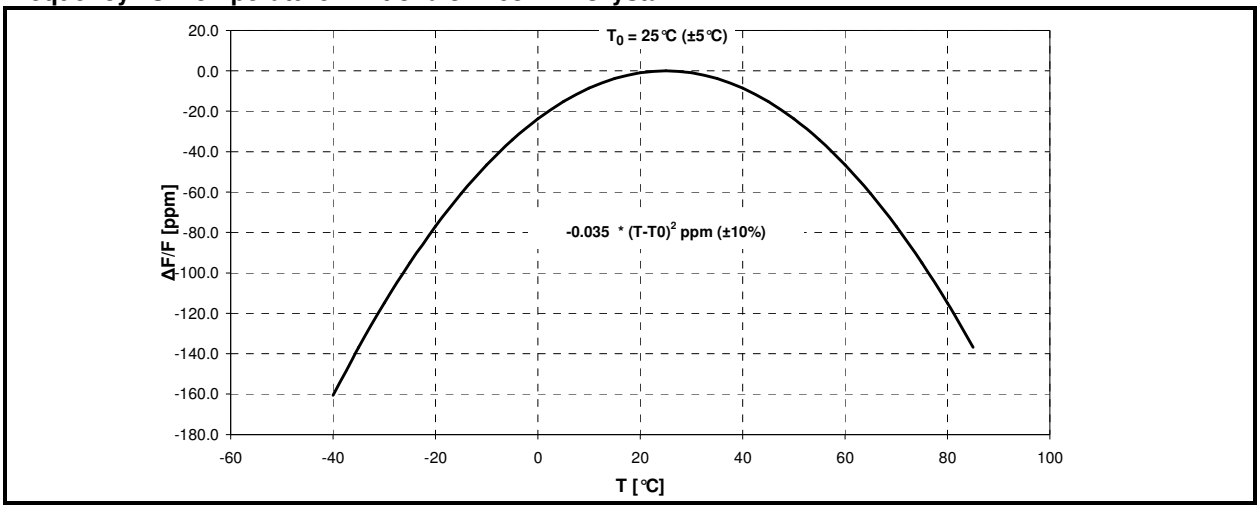
5.2 FREQUENCY AND TIME CHARACTERISTICS

V_{DD}= 3.0 V; V_{SS}= 0 V; T_{amb}= +25°C; f_{OSC}= 32.768 kHz

PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Frequency accuracy	ΔF / F	T_{AMB} = +25°C V_{DD} = 3.0 V	+/- 10	+/- 20	ppm
Frequency vs. voltage characteristics	ΔF / V	T_{AMB} = +25°C V_{DD} = 1.8 V to 5.5 V	+/- 0.8	+/- 1.0	ppm / V
Frequency vs. temperature characteristics	ΔF / F_{OPR}	$T_{reference}$ = +25°C V_{DD} = 3.0 V	$-0.035^{ppm}/_{°C^2}(T_{OPR}-T_O)^2$ +/-10%		ppm
Turnover temperature	T_O		+25	+/-5	°C
Aging first year max.	ΔF / F	T_{AMB} = +25°C		+/- 3	ppm
Oscillation start-up time	T_{START}	V_{DD} = 3.0 V	500	1000	ms
CLKOUT duty cycle		T_{AMB} = +25°C	50	40 / 60	%
Achievable Time accuracy with correct frequency-offset compensation	ΔT / T	$T_{Reference}$ = +25°C V_{DD} = 3.0 V	+/- 3 [1)]	+/- 5 [2)]	ppm

1) Based on customer set correct Frequency Offset compensation in “normal” mode
2) Based on customer set correct Frequency Offset compensation in “course” mode

Frequency vs. Temperature Drift of a 32.768 kHz Crystal



5.3 STATIC CHARACTERISTICS

V_{DD}= 1.1 V to 5.5 V; V_{SS}= 0 V; T_{amb}= -40 °C to +85 °C; f_{OSC}= 32.768 kHz

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
Supply voltage	V_{DD}	time-keeping mode [1] SPI bus inactive	1.1		5.5	V
		SPI bus active	1.6		5.5	V
Minimum supply voltage detection	$V_{OSC(min)}$	T_{amb} = 25°C		0.9		V
Supply current SPI bus inactive CLKOUT disabled T_{amb} = 25°C	I_{DD}	V_{DD} = 2.0 V [2]		120		nA
		V_{DD} = 3.0 V [2]		130		nA
		V_{DD} = 5.0 V [2]		140		nA
Supply current SPI bus inactive CLKOUT disabled T_{amb} = -40°C to +85°C	I_{DD}	V_{DD} = 2.0 V [2]			350	nA
		V_{DD} = 3.0 V [2]			370	nA
		V_{DD} = 5.0 V [2]			400	nA
Supply current SPI bus inactive CLKOUT enabled CLKOUT = 32.768 kHz T_{amb} = 25°C	I_{DD}	V_{DD} = 2.0 V		280		nA
		V_{DD} = 3.0 V		360		nA
		V_{DD} = 5.0 V		540		nA
Supply current SPI bus inactive CLKOUT enabled CLKOUT = 32.768 kHz T_{amb} = -40°C to +85°C	I_{DD}	V_{DD} = 2.0 V			470	nA
		V_{DD} = 3.0 V			570	nA
		V_{DD} = 5.0 V			770	nA
Supply current SPI bus active CLKOUT enabled T_{amb} = 25°C	I_{DD}	f_{SCL} = 4.5 MHz V_{DD} = 5.0 V		250	400	µA
		f_{SCL} = 1.0 MHz V_{DD} = 3.0 V		30	80	µA
Current consumption CLKOUT = 32.768kHz, C_{LOAD} = 7.5pF	I_{DD32K}	f_{SCL} = 0 Hz, V_{DD} = 5.0V		2.5	3.4	µA
		f_{SCL} = 0 Hz, V_{DD} = 3.0V		1.5	2.2	µA
		f_{SCL} = 0 Hz, V_{DD} = 2.0V		1.1	1.6	µA
Inputs						
LOW level input voltage	V_{IL}				30% V_{DD}	V
HIGH level input voltage	V_{IH}		70% V_{DD}			V
Input voltage	V_I	Pins: CE, SCL, SDI, CLKOE	-0.5		5.5	V
Input leakage current	I_L	V_I = V_{DD} or V_{SS} SCL, SDI, CLKOE, CLKOUT	-1	0	+1	µA
		V_I = V_{SS} on pin CE	-1	0		µA
Pull-down resistance	R_{PD}	on pin CE		240	550	kΩ
Input capacitance	C_I	[3]			7	pF
Outputs						
Output voltage	V_O	pins: CLKOUT; INT [4]	-0.5		5.5	V
		pin : SDO	-0.5		V_{DD} +0.5	
HIGH level output voltage	V_{OH}	pins: SDO	80% V_{DD}		V_{DD}	V
LOW level output voltage	V_{OL}	pins: CLKOUT; INT V_{DD} = 5V / I_{OL} = 1.5 mA	V_{SS}		0.4	V
		pin : SDO	V_{SS}		20% V_{DD}	
HIGH level output current	I_{OH}	pin : SDO V_{OH} = 4.6 V / V_{DD} = 5 V			1.5	mA
LOW level output current	I_{OL}	pin :SDO, INT, CLKOUT V_{OL} = 0.4 V / V_{DD} = 5 V	-1.5			mA
Output leakage current	I_{LO}	V_O = V_{DD} or V_{SS}	-1	0	+1	µA
Operating Temperature Range						
Operating temperature range	T_{OPR}		-40		+85	°C

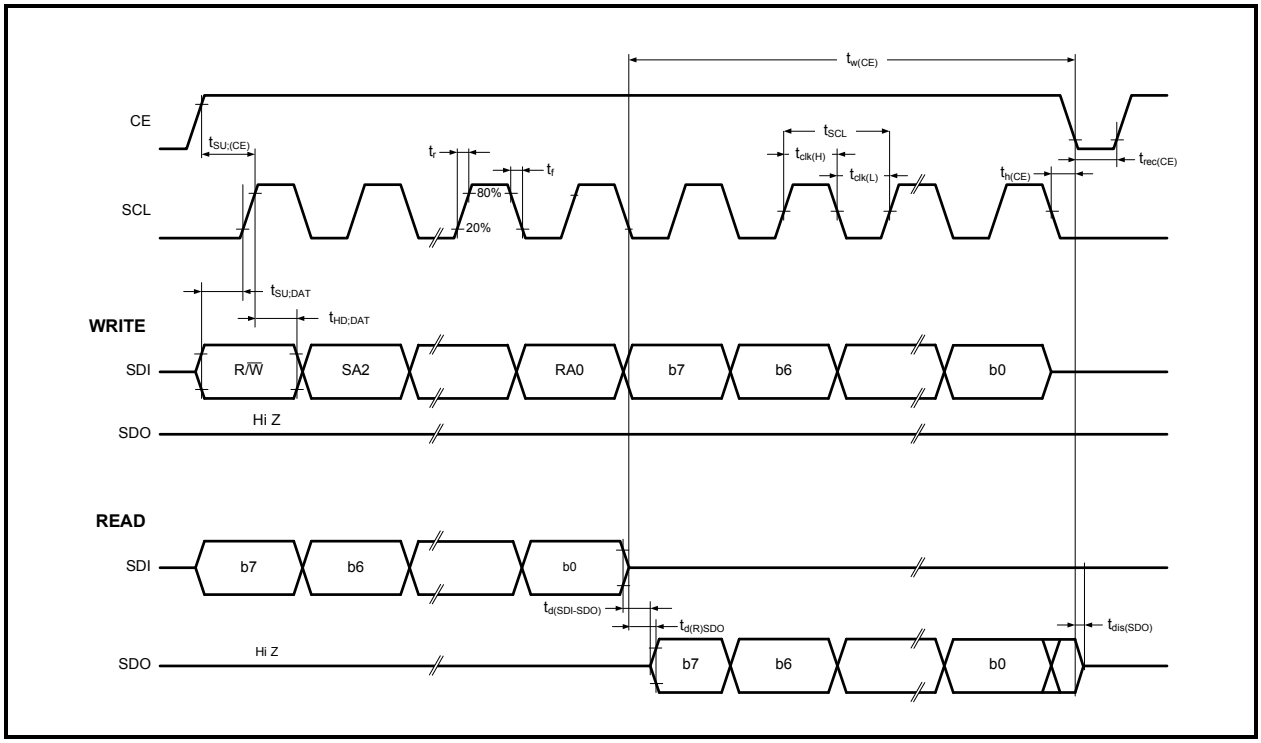
[1] For reliable oscillator start-up at power-up: V_{DD} = $V_{DD(min)}$ +0.3 V.
[2] Timer source clock = $^1/_{60}$ Hz, level of pins CE, SDI and SCL either V_{DD} or V_{SS}.
[3] Implicit by design.
[4] Refers to external pull-up voltage.

5.4 DYNAMIC CHARACTERISTICS SPI-BUS

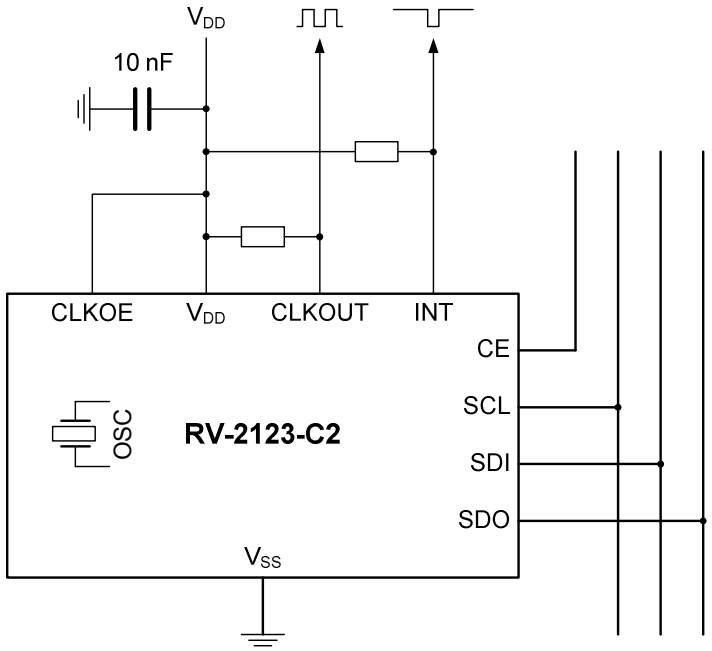
V_{SS}= 0 V; T_{amb}= -40°C to +85°C; All timing values are valid within the operating supply voltage range and references to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

PARAMETER	SYMBOL	CONDITIONS	V_{DD} = 1.6V		V_{DD} = 2.4V		V_{DD} = 3.3V		V_{DD} = 5.0V		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
SCL clock frequency	$f_{clk(SCL)}$			2.9		4.54		5.71		8.0	MHz
SCL time	t_{SCL}		345		220		175		125		ns
Clock HIGH time	$t_{clk(H)}$		90		50		45		40		ns
Clock LOW time	$t_{clk(L)}$		200		120		95		70		ns
Rise time	t_r	for SCL signal		100		100		50		50	ns
Fall time	t_f	for SCL signal		100		100		50		50	ns
CE setup time	$t_{su(CE)}$		40		35		30		25		ns
CE hold time	$t_{h(CE)}$		40		30		25		15		ns
CE recovery time	$t_{rec(CE)}$		30		25		20		15		ns
CE pulse width	$t_{w(CE)}$	Measured after valid subaddress is received		0.99		0.99		0.99		0.99	s
Setup time	t_{su}	Setup time for SDI data	10		5		3		2		ns
Hold time	t_h	Hold time for SDI data	25		10		8		5		ns
SDO read delay time	$t_{d(R)SDO}$	Bus load = 50pF		190		108		85		60	ns
SDO disable time	$t_{dis(SDO)}$	No load value; bus will be held up by bus-capacitance; use RC time constant with application values		70		45		40		27	ns
Transition time SDI to SDO	$t_{t(SDI-SDO)}$	To avoid bus conflict	0		0		0		0		ns

5.5 SPI INTERFACE TIMING

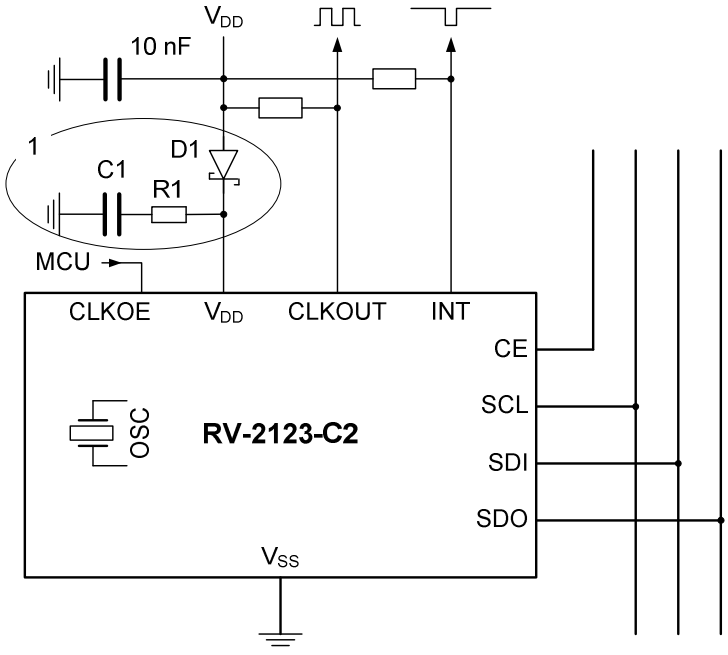


6.0 APPLICATION INFORMATION



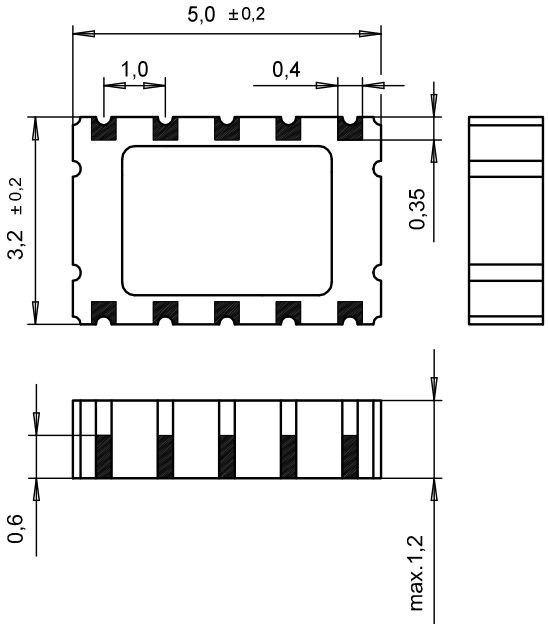
Backup Supply Operation

1 A backup cuper capacitor C1 of 1 farad combined with a low V_F diode D1 (for example: Schottky) can be used as a standby/back-up supply. The resistor R1 is used to limit the charge current of the C1 super capacitor.
With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for weeks.

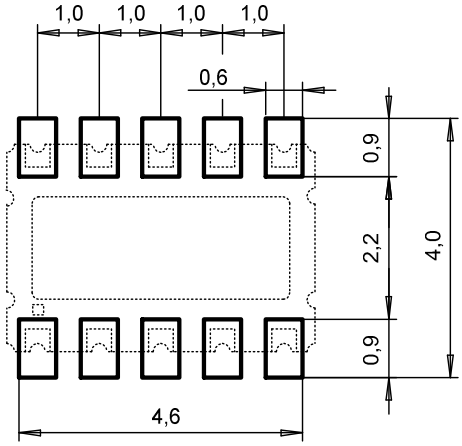


7.0 PACKAGE DIMENSIONS AND SOLDERPAD LAYOUT

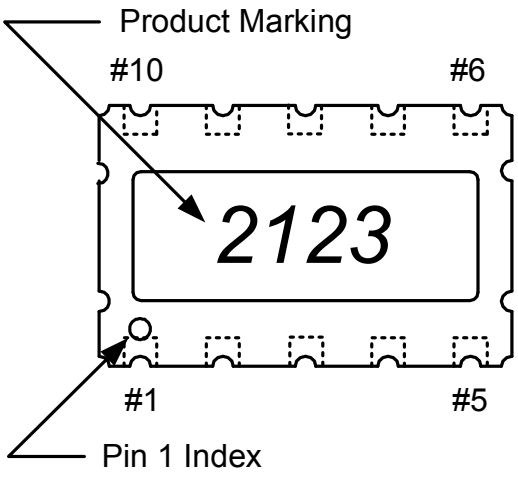
Package Dimensions; bottom view



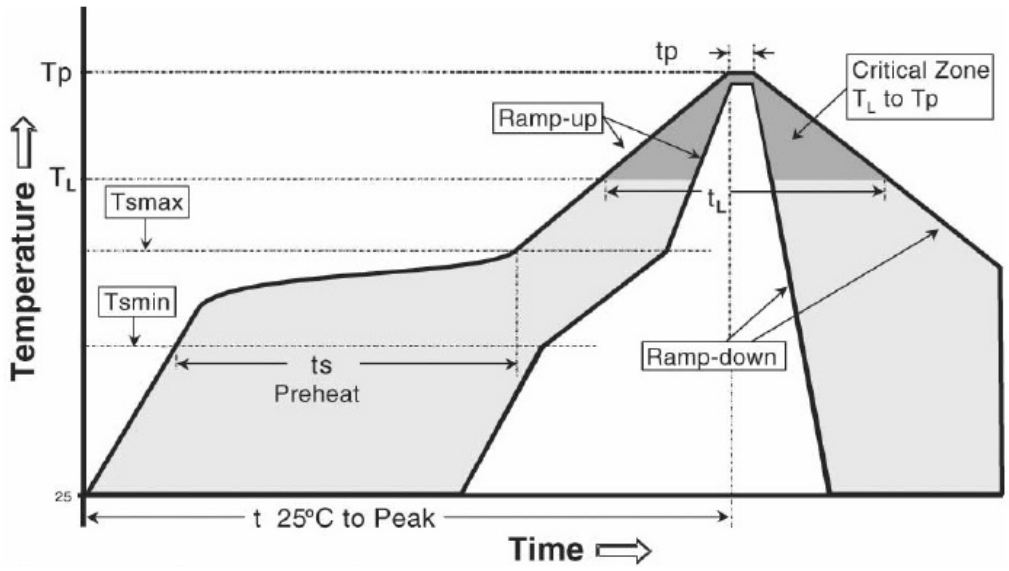
Recommended Solderpad Layout



7.1 PACKAGE MARKING AND PIN 1 INDEX



8.0 MAXIMUM REFLOW CONDITIONS (in accordance with IPC/JEDEC J-STD-020C "Pb-free")



Reflow Temperatures in accordance with IPC/JEDEC J-STD-020C "Pb-free soldering"

TEMPERATURES	SYMBOL	CONDITIONS	UNIT
Average ramp-up rate	Ts_{max} to Tp	3℃ / second max	℃ / s
Ramp down Rate	T_{cool}	6℃ / second max	℃ / s
Time 25℃ to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	m
PREHEAT			
Temperature min	Ts_{min}	150	℃
Temperature max	Ts_{max}	200	℃
Time Ts_{min} to Ts_{max}	ts	60 - 180	sec
TIME ABOVE LIQUIDUS			
Temperature liquidus	T_L	217	℃
Time above liquidus	t_L	60 – 150	sec
PEAK TEMPERATURE			
Peak Temperature	Tp	260	℃
Time within 5℃ of peak temperature	tp	20 - 40	sec

9.0 HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration

Keep the crystal from being exposed to **excessive mechanical shock and vibration**. Micro Crystal guarantees that the crystal will bear a mechanical shock of 5000g / 0.3 ms.
The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic Cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

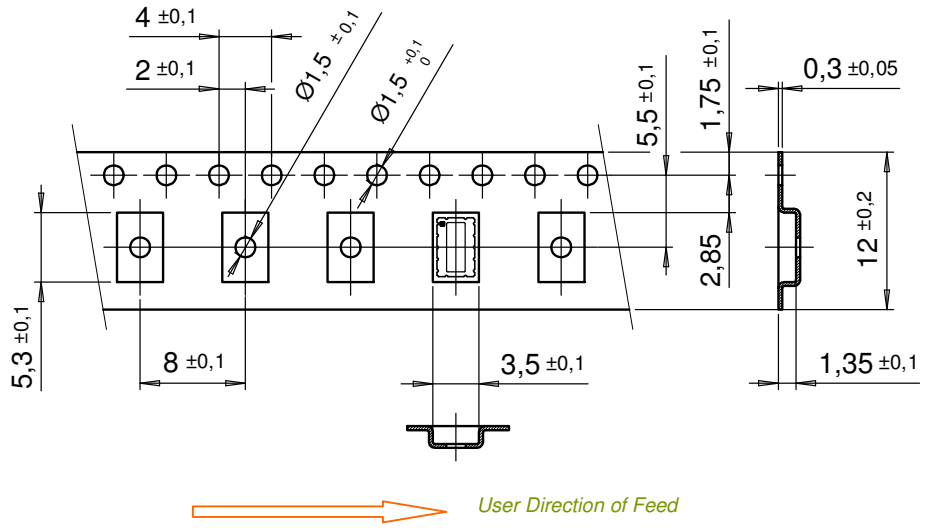
Overheating, rework high-temperature-exposure

Avoid overheating the package. The package is sealed with a sealring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the sealring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.
Use the following methods for re-work:

- Use a hot-air- gun set at 270°C
- Use 2 temperature-controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

10.0 PACKING INFO CARRIER TAPE

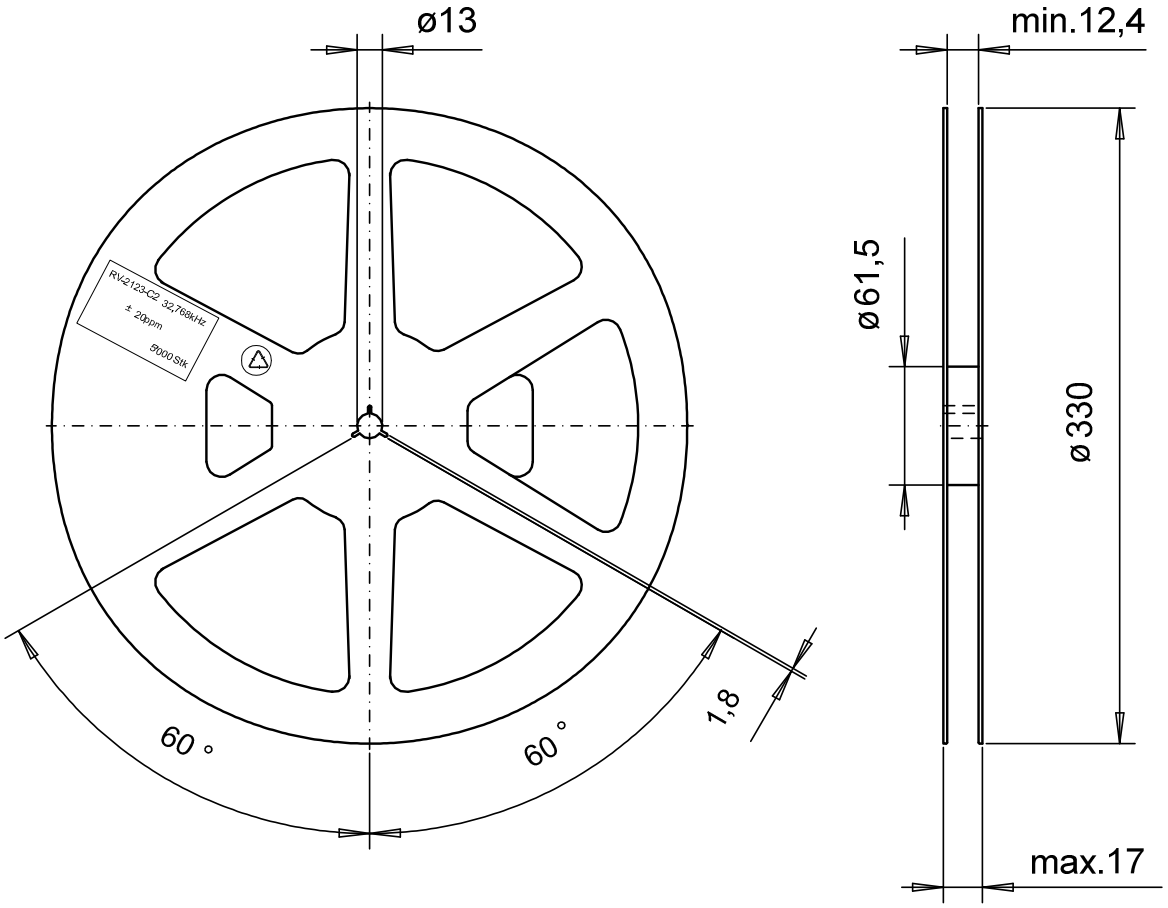
12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive	
Cover Tape:	Base Material:	Polyester, conductive	0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer	



Tape Leader and Trailer: 300 mm minimum All dimensions are in mm

REELS:	DIAMETER	MATERIAL.	RTC's per REEL.
	7"	Plastic, Polystyrene	1000
	10"	Plastic, Polystyrene	2500
	13"	Plastic, Polystyrol	5000

10.1 REEL 13 INCH FOR 12 mm TAPE



Reel:

Diameter	***Material***
13”	*Plastic, Polystyrol*

11.0 DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
March 2009	1.0	First release
January 2013	1.1	Writing corrections