Product Change Notification - SYST-27MPLJ170

Date:

29 Nov 2018

Product Category:

Ethernet Switches

Affected CPNs:

Notification subject:

Data Sheet - KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa Data Sheet Document Revision

Notification text:

SYST-27MPLJ170

Microchip has released a new DeviceDoc for the KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa of devices. If you are using one of these devices please read the document located at KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa.

Notification Status: Final

Description of Change: Below are the changes

Section/Figure/Entry	Correction
Section 8.1, "Package Mark- ing Information," on page 234	Updated top marking information.
Section 8.2, "Package Draw- ings," on page 235	Updated package drawings.
Table 4-2, "Enabling and Disabling Quiet-WIRE"	Updated MMD Quiet-WIRE Configuration 3 Register “Disable Quiet-WIRE” entry.
Table 4-17, "Matching Rule Options"	Table updated.
Section 4.4.9, "Tail Tagging Mode," on page 38	Section updated. Added PTP specific content.
Section 4.1.8, "LinkMD®+ Enhanced Diagnostics: Receive Signal Quality Indicator," on page 23	Updated LinkMD+ text.
Cover, Section 4.0, "Func- tional Description," on page 19, Section 5.0, "Device Registers," on page 69	Removed LinkMD references.
Section 4.1.6, "Quiet-WIRE Filtering," on page 22, Sec- tion 5.4, "MDIO Manageable Device (MMD) Registers (Indirect)," on page 202	Updated functional description and added Quiet-Wire register descriptions.
Section 4.4.15, "Low Latency Cut-Through Mode," on page 42	Minor text clarification.
Section 4.4.2.4, "Learning," on page 29	Text correction.
Section 4.4.2.6, "Aging," on page 30	Corrected “time stamp” to “age count” in multiple locations.
Section 4.2.2, "Tri-Color Dual-LED Mode," on page 25	Removed errant 1000Mbps references.
Section 5.2.2.5, "PHY Auto-Negotiation Advertisement Register," on page 146	Changed default value of Pause (Flow Control) Capability bit to a note referencing the LED1_1 configuration strap.
Section 5.2.8.4, "Port Authentication	Corrected bits 1:0 description.

Control Register," on page 173	
Section 5.1.6.11, "Global PTP Message Config 1 Reg- ister," on page 118	Corrected 802.3AS to 802.1AS and added descriptions.
Section 5.1.1.4, "Global Chip ID 3 Register," on page 72	Corrected bit 0 description.
Section 5.4, "MDIO Manage- able Device (MMD) Regis- ters (Indirect)," on page 202	Added definitions for MMD Signal Quality Register (ACh) and MMD Quiet-WIRE Configuration Registers (25h-34h).
Section 5.4, "MDIO Manage- able Device (MMD) Regis- ters (Indirect)," on page 202	Corrected the MMD register read example.
Section 5.4.5, "MMD Quiet- WIRE Configuration 1 Reg- ister," on page 204, Section 5.4.6, "MMD Quiet-WIRE Configuration 2 Register," on page 204, Section 5.4.7, "MMD Quiet-WIRE Configuration 3 Register," on page 205	Updated default value fields.
Table 6-2, “RGMII Timing Values,” on page 219	Revised minimum RGMII TSKEW parameter.
Table 3-3, “Configuration Strap Descriptions,” on page 17	Corrected swapping of LED2_0 and LED4_0, added notes in strapping. Corrected RXD6_0 and RXD7_0 in strapping table.
Table 1-3, “Register Nomenclature,” on page 7	Added additional W0C “Write zero to clear” bit type.
Section 5.5.1, "SGMII Con- trol Register," on page 208	Corrected defaults and bit types. Added details and updated bit names.
Section 5.5.2, "SGMII Status Register," on page 209	Corrected defaults and bit types. Updated Link Sta- tus description.
Section 5.5.5, "SGMII Auto- Negotiation Advertisement Register," on page 210	Added additional description.
Section 5.5.6, "SGMII Auto- Negotiation Link Partner Base Ability Register," on page 211, Section 5.5.7, "SGMII Auto-Negotiation Expansion Register," on page 212	Added new register definitions.
Section 5.5.8, "SGMII Digital Control Register," on page 212, Section 5.5.9, "SGMII Auto-Negotiation Control Register," on page 213, Section 5.5.10, "SGMII Auto-Negotiation Status Register," on page 214	Added additional description.
Section 5.1.3.1, "Power Down Control 0 Register," on page 82	Added SGMII-specific information to bits 4:3 description.
Section 5.2.1.5, "Port Inter- rupt Status Register," on page 139, Section 5.2.1.6, "Port Interrupt Mask Regis- ter," on page 140	Updated bit 3.
Section 2.1, "General Description," on page 8, Section 4.13.4, "Serial Giga- bit Media Independent Inter- face (SGMII) (Port 7)," on page 67	Updated SGMII description.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 29 Nov 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

KSZ8567S 7-Port 10/100 Ethernet AVB Switch with SGMII and RGMII/MII/RMII Interfa

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.
If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

KSZ8567STXI
KSZ8567STXI-TR
KSZ8567STXV-TRVAO
KSZ8567STXV-VAO