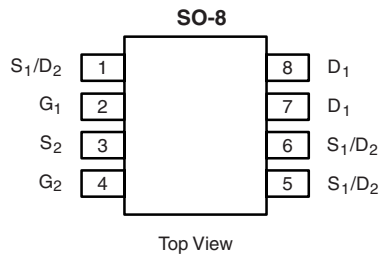


## Dual N-Channel 25-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a, e</sup>	Q <sub>g</sub> (Typ.)
Channel-1	25	0.023 at V <sub>GS</sub> = 10 V	8.0	5.5
		0.028 at V <sub>GS</sub> = 4.5 V	8.0	
Channel-2	25	0.023 at V <sub>GS</sub> = 10 V	8.0	5.5
		0.028 at V <sub>GS</sub> = 4.5 V	8.0	

SCHOTTKY PRODUCT SUMMARY		
V <sub>DS</sub> (V)	V <sub>SD</sub> (V) Diode Forward Voltage	I <sub>F</sub> (A) <sup>a</sup>
25	0.43 V at 1.0 A	2.3



Ordering Information: Si4670DY-T1-E3 (Lead (Pb)-free)  
 Si4670DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

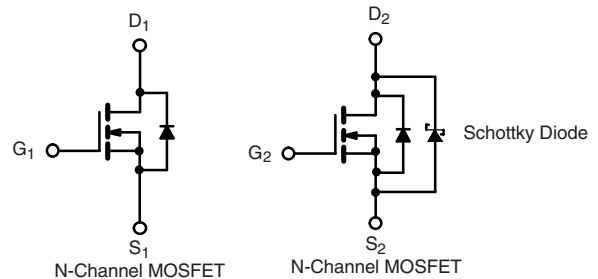
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Synchronous Buck Converter
- Game Machine
- Notebook



ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V <sub>DS</sub>	25	25	V
Gate-Source Voltage	V <sub>GS</sub>	± 16	± 16	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	8.0 <sup>e</sup>	8.0 <sup>e</sup>
		T <sub>C</sub> = 70 °C	7	7
		T <sub>A</sub> = 25 °C	7 <sup>b, c</sup>	7 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	5.6 <sup>b, c</sup>	5.6 <sup>b, c</sup>
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	30	30	
Source-Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	2.3	2.3
		T <sub>A</sub> = 25 °C	1.5 <sup>b, c</sup>	1.5 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	2.8	2.8
		T <sub>C</sub> = 70 °C	1.8	1.8
		T <sub>A</sub> = 25 °C	1.8 <sup>b, c</sup>	1.8 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.1 <sup>b, c</sup>	1.1 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	57	70	57	70	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	36	44	36	44	

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W (Channel-1 and Channel-2).
- Package limited.

SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Ch-1	25		V	
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Ch-2	25			
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\ \mu\text{A}$	Ch-1		25	mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\ \mu\text{A}$	Ch-1		- 4.7		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	Ch-1	1		2.2	
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	Ch-2	1		2.2	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch-1			100	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch-2			100	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			0.001	
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$	Ch-2		0.07	0.5	
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 100^\circ\text{C}$	Ch-1				0.025
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 100^\circ\text{C}$	Ch-2		5	20	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20		A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20			
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$	Ch-1		0.019	0.023	
		$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$	Ch-2		0.019	0.023	
		$V_{GS} = 4.5\text{ V}, I_D = 6.3\text{ A}$	Ch-1		0.023	0.028	
		$V_{GS} = 4.5\text{ V}, I_D = 6.3\text{ A}$	Ch-2		0.023	0.028	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 7\text{ A}$	Ch-1		23	S	
		$V_{DS} = 10\text{ V}, I_D = 7\text{ A}$	Ch-2		23		
<b>Dynamic<sup>a</sup></b>							
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		680	pF	
			Ch-2		680		
Output Capacitance	$C_{oss}$		Channel-2 $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1			120
				Ch-2			180
Reverse Transfer Capacitance	$C_{rss}$	Ch-1			55		
		Ch-2			70		
Total Gate Charge	$Q_g$	$V_{DS} = 13\text{ V}, V_{GS} = 10\text{ V}, I_D = 7\text{ A}$	Ch-1		12	18	
			Ch-2		12	18	
		Channel-1 $V_{DS} = 13\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-1		5.5	8.5	
			Ch-2		5.5	8.5	
Gate-Source Charge	$Q_{gs}$	Channel-2 $V_{DS} = 13\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-1		2	nC	
Ch-2			2				
Gate-Drain Charge	$Q_{gd}$	Channel-1 $V_{DS} = 13\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-1		1.5		
			Ch-2		1.5		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	Ch-1		2.5	$\Omega$	
			Ch-2		3.2		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .



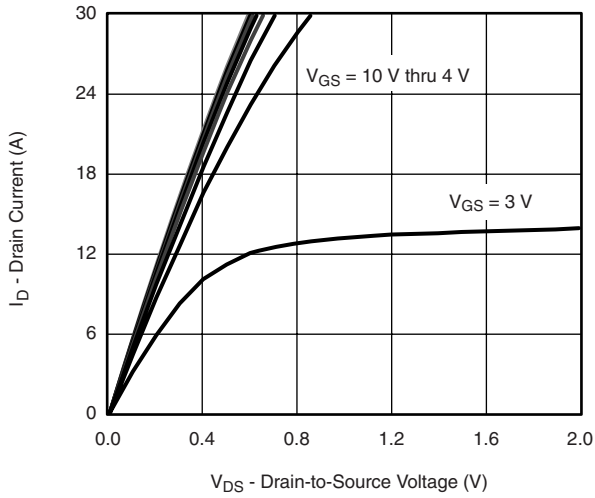
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 13\text{ V}$ , $R_L = 2.3\ \Omega$ $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		15	25	ns
			Ch-2		15	25	
Rise Time	$t_r$		Ch-1		50	75	
			Ch-2		50	75	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 13\text{ V}$ , $R_L = 2.3\ \Omega$ $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		20	30	
			Ch-2		20	30	
Fall Time	$t_f$		Ch-1		10	15	
			Ch-2		10	15	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 13\text{ V}$ , $R_L = 2.3\ \Omega$ $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	15	
			Ch-2		10	15	
Rise Time	$t_r$		Ch-1		12	20	
			Ch-2		12	20	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 13\text{ V}$ , $R_L = 2.3\ \Omega$ $I_D \cong 5.6\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		15	25	
			Ch-2		15	25	
Fall Time	$t_f$		Ch-1		10	15	
			Ch-2		10	15	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			2.3	A
			Ch-2			2.3	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			30	
			Ch-2			30	
Body Diode Voltage	$V_{SD}$	$I_S = 5.6\text{ A}$	Ch-1		0.8	1.2	V
		$I_S = 1\text{ A}$	Ch-2		0.37	0.43	
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 5.6\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	30	ns
			Ch-2		15	30	
Body Diode Reverse Recovery Charge	$Q_{rr}$	Channel-2 $I_F = 5.6\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		8	16	nC
			Ch-2		8	16	
Reverse Recovery Fall Time	$t_a$		Ch-1		8.5		ns
			Ch-2		8.5		
Reverse Recovery Rise Time	$t_b$		Ch-1		6.5		
			Ch-2		6.5		

Notes:

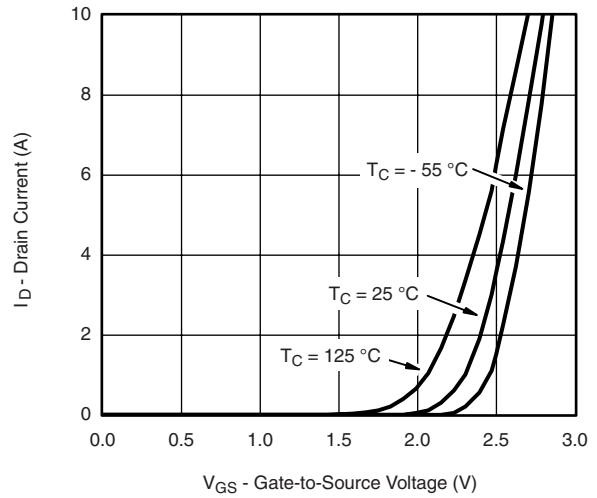
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

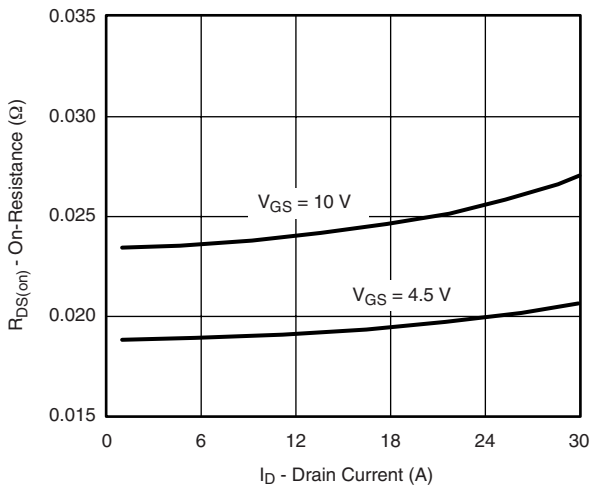
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



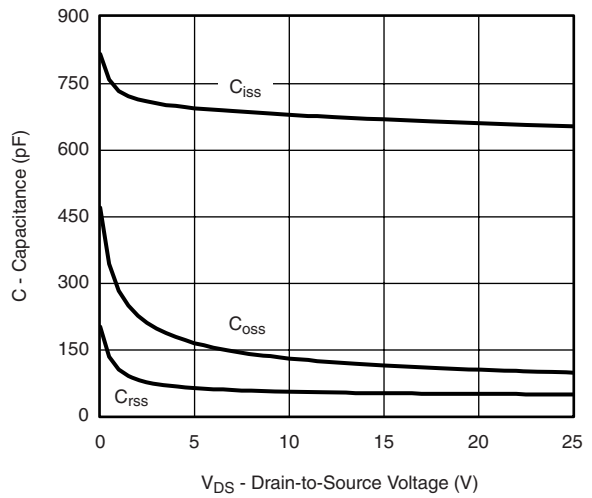
**Output Characteristics**



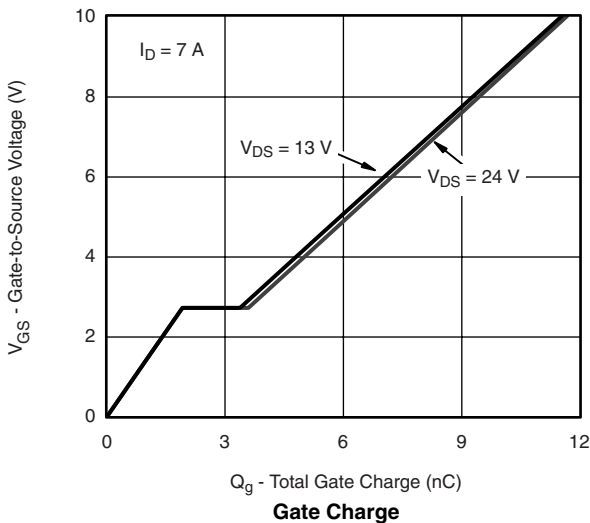
**Transfer Characteristics**



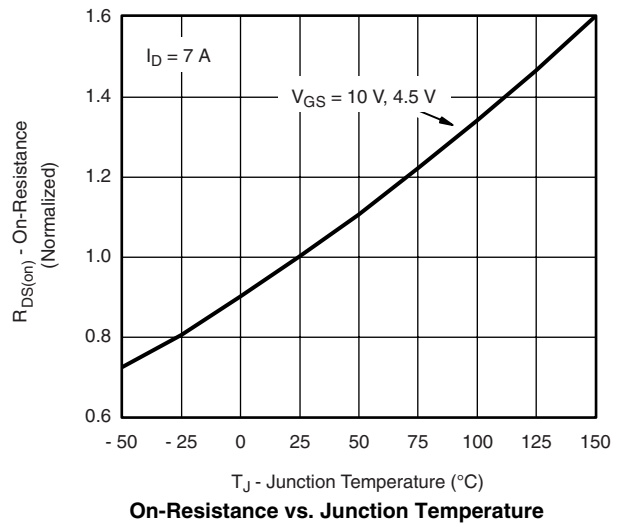
**On-Resistance vs. Drain Current**



**Capacitance**

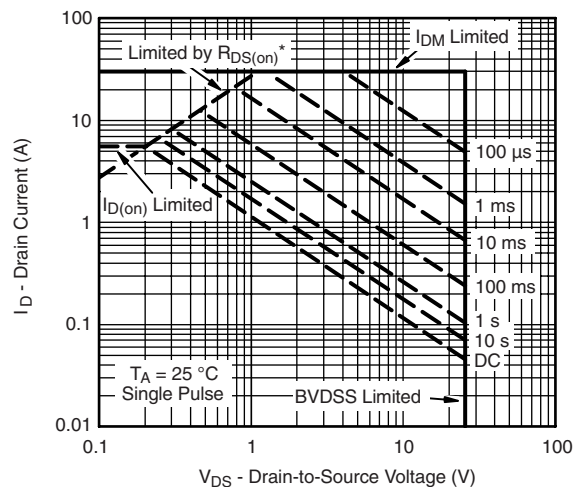
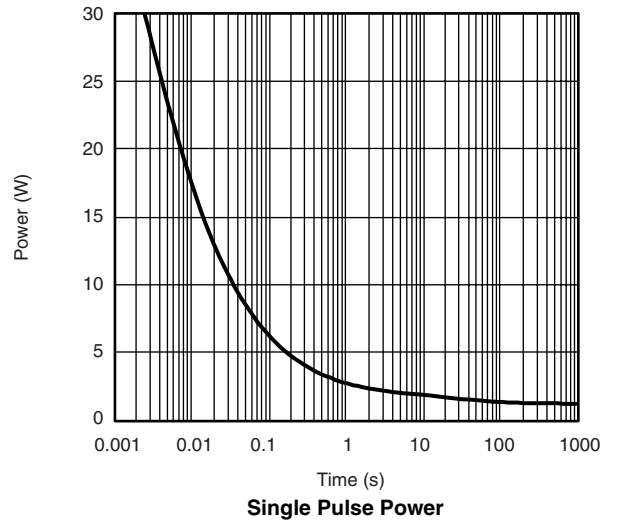
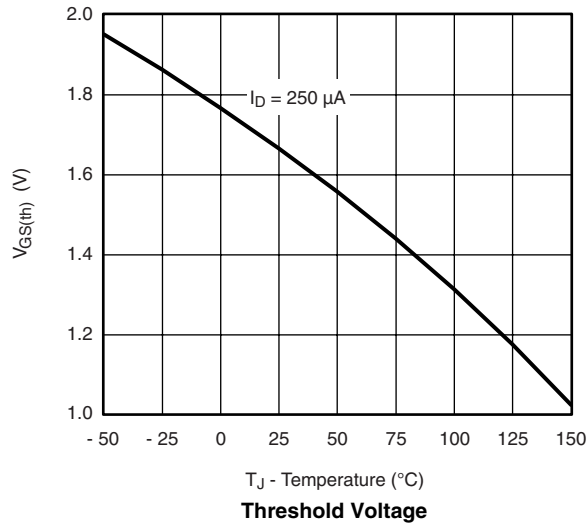
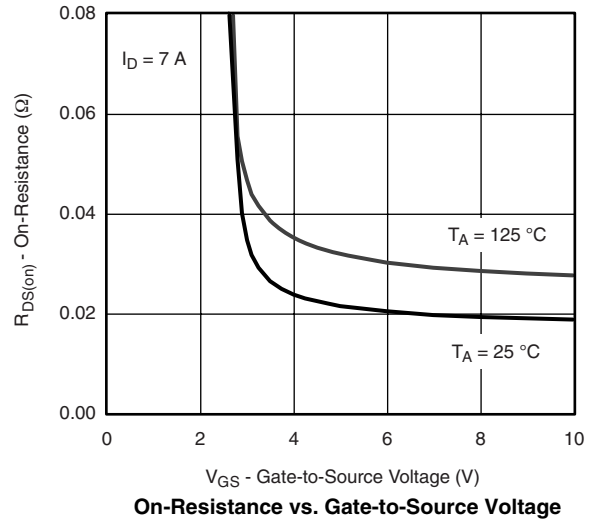
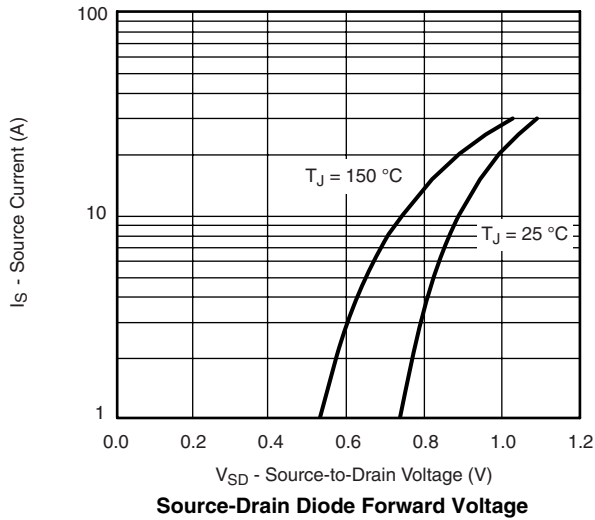


**Gate Charge**



**On-Resistance vs. Junction Temperature**

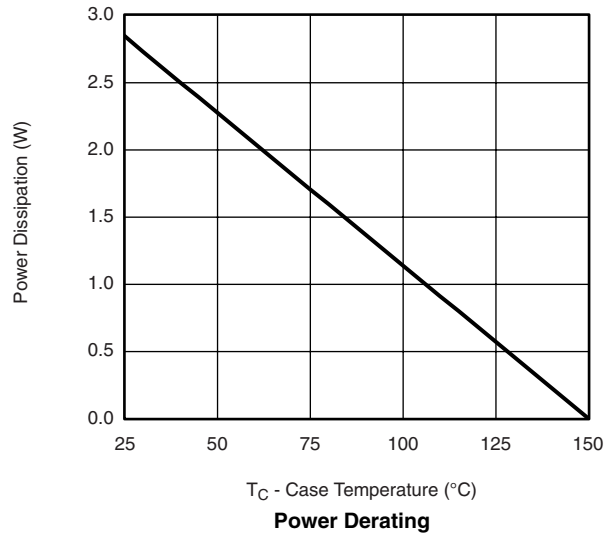
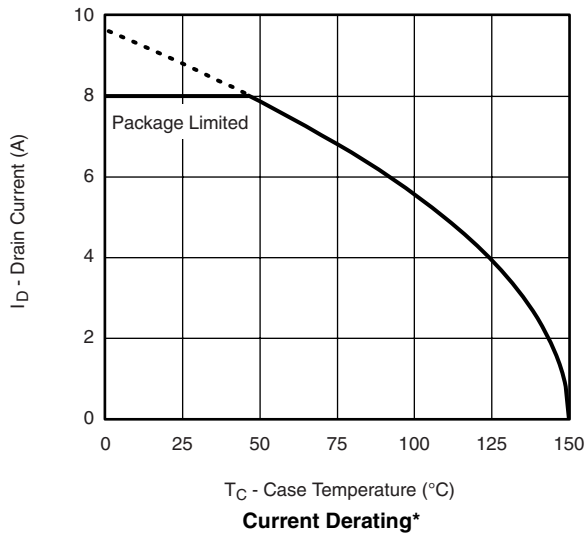
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

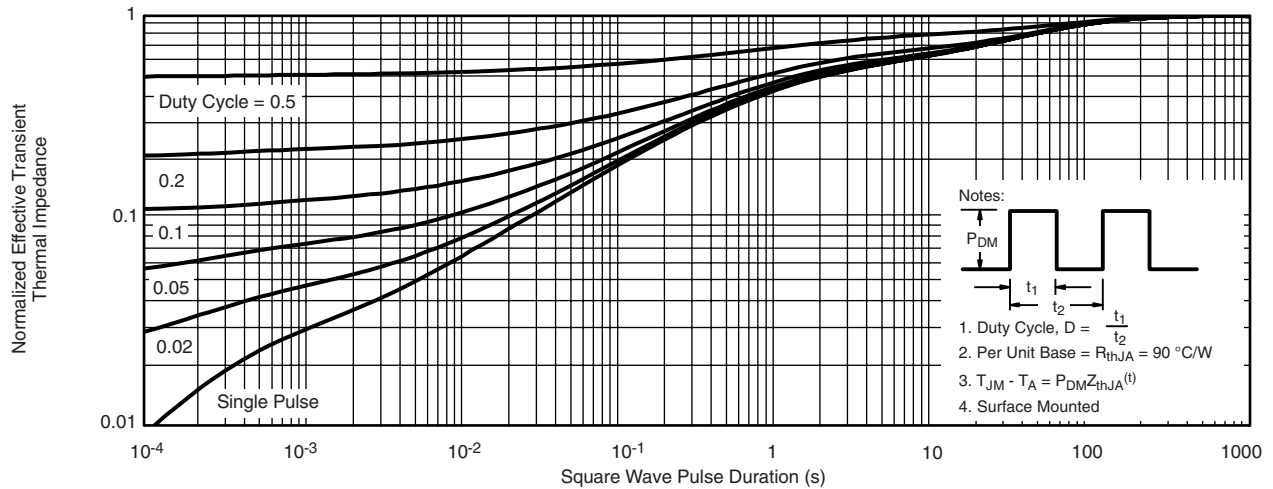
### Safe Operating Area, Junction-to-Ambient

## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

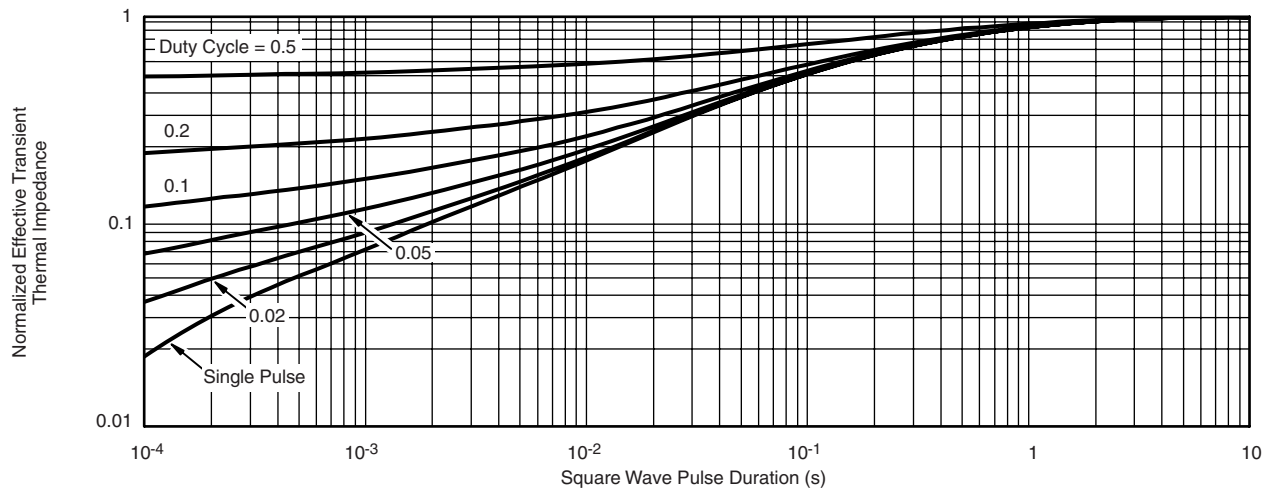


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

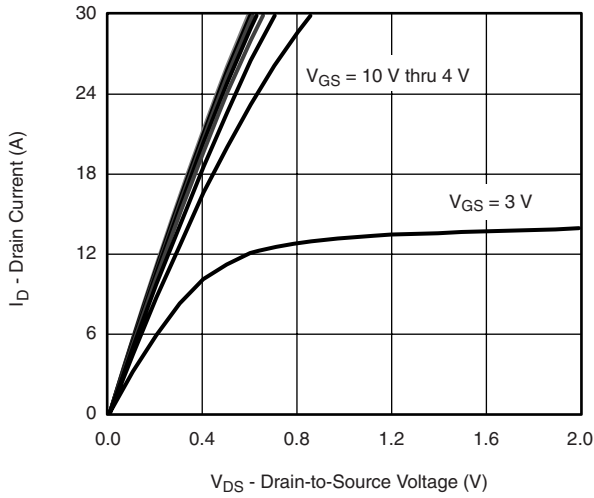


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

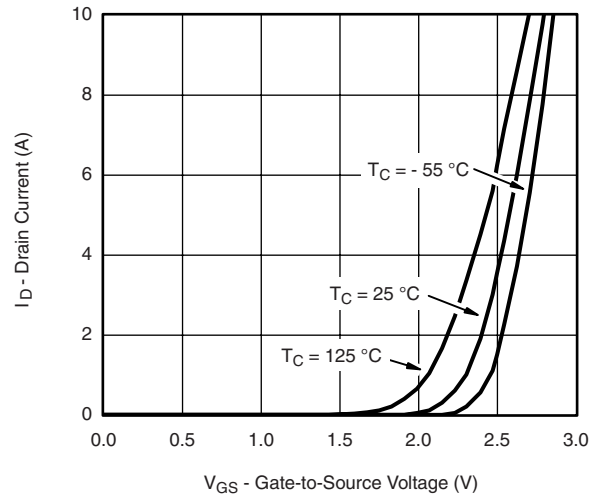


**Normalized Thermal Transient Impedance, Junction-to-Foot**

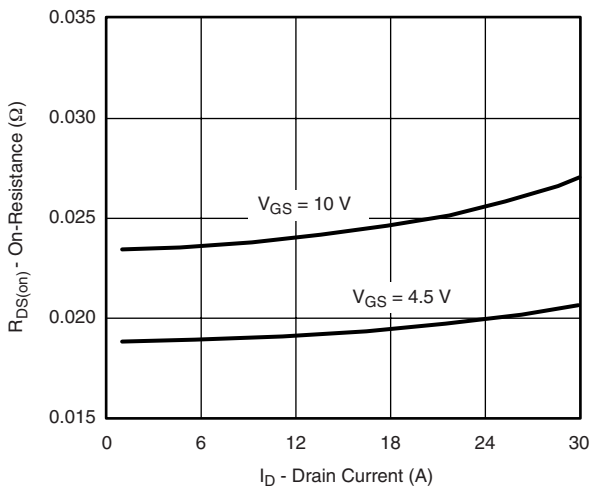
## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



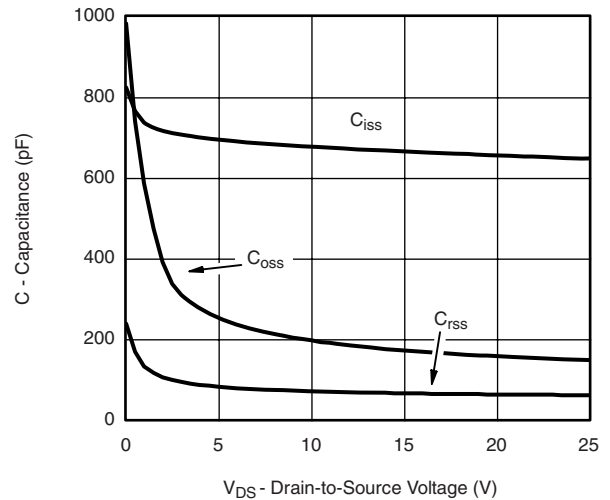
**Output Characteristics**



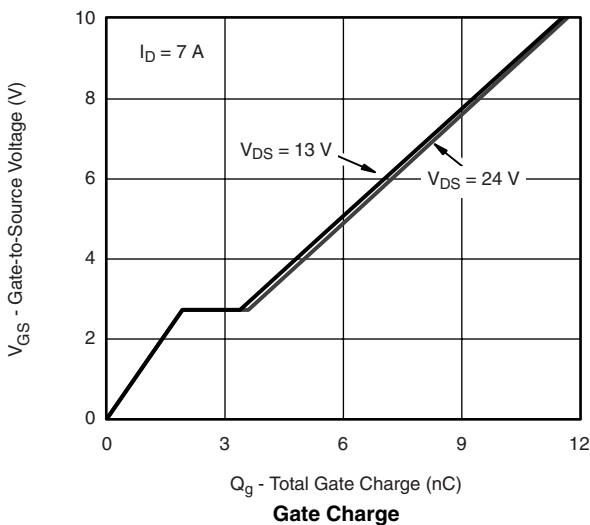
**Transfer Characteristics**



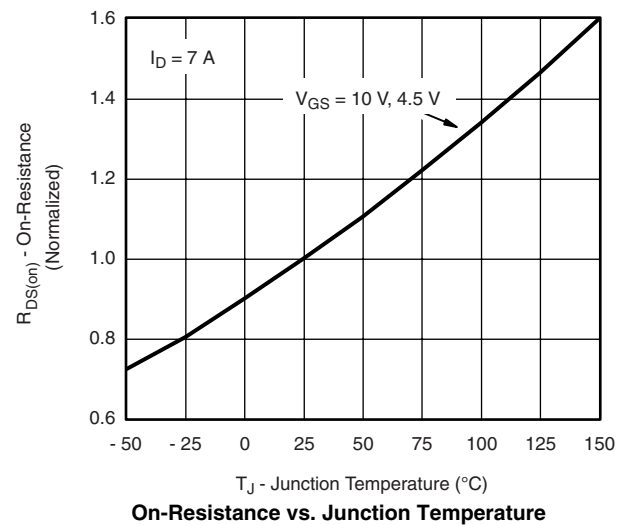
**On-Resistance vs. Drain Current**



**Capacitance**



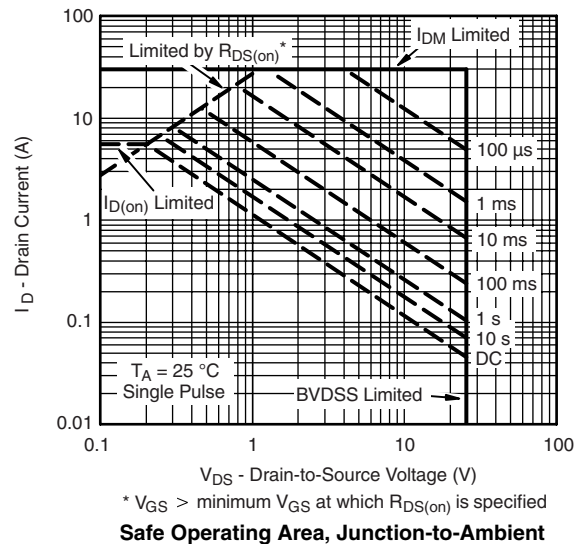
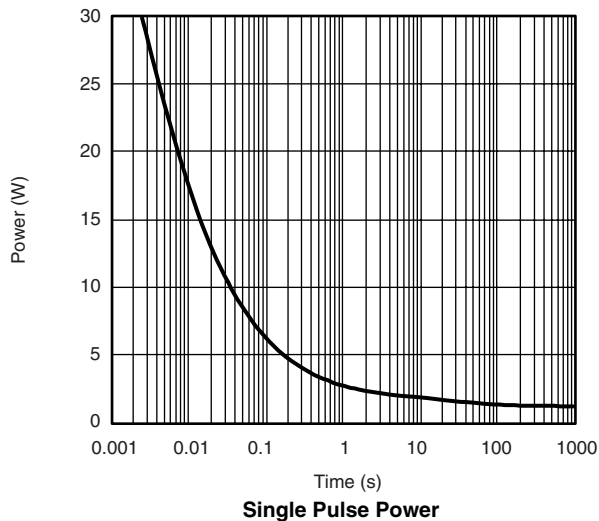
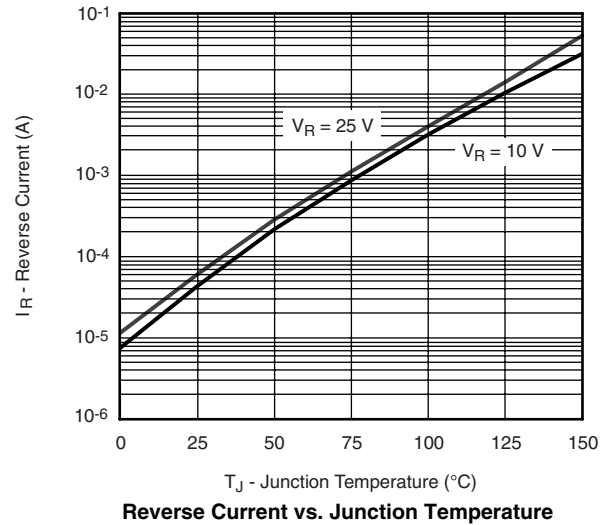
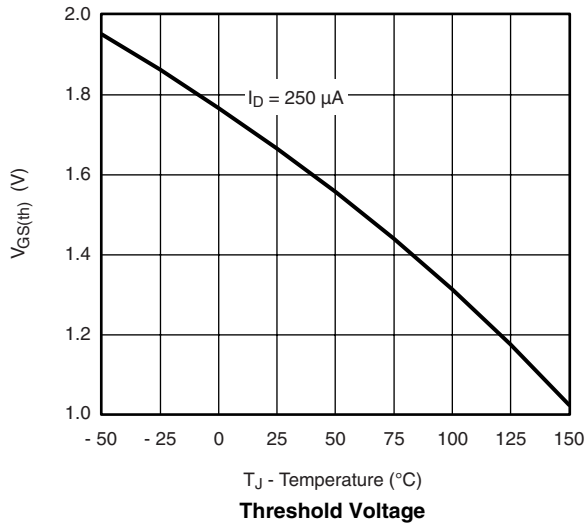
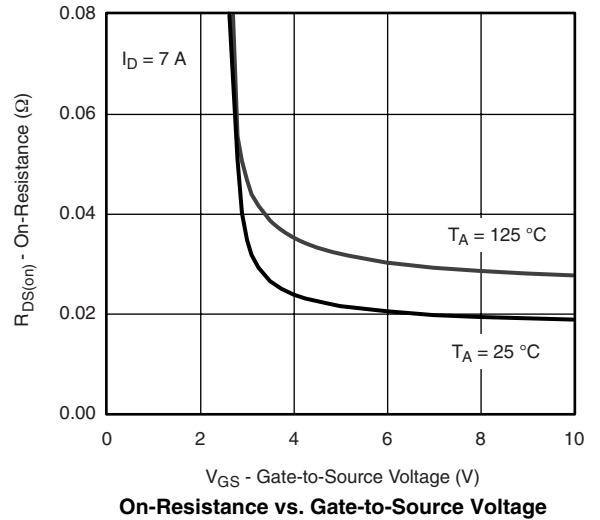
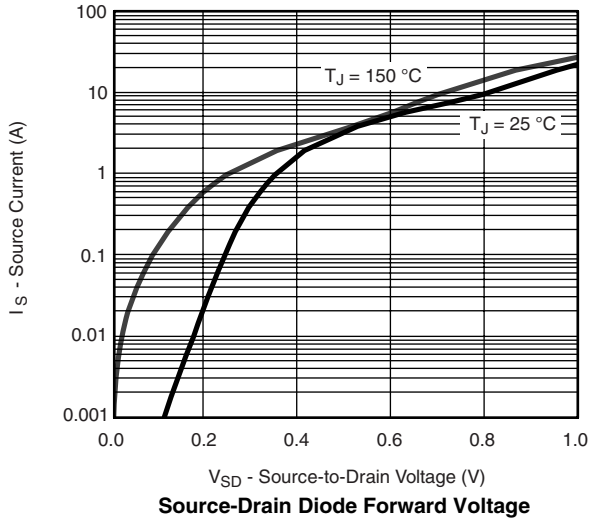
**Gate Charge**



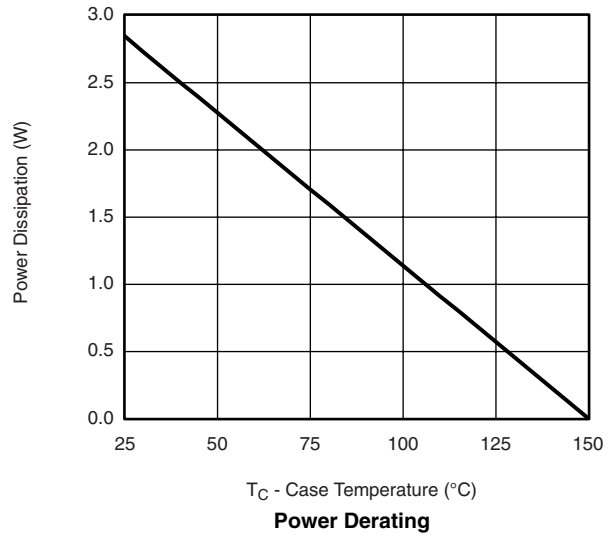
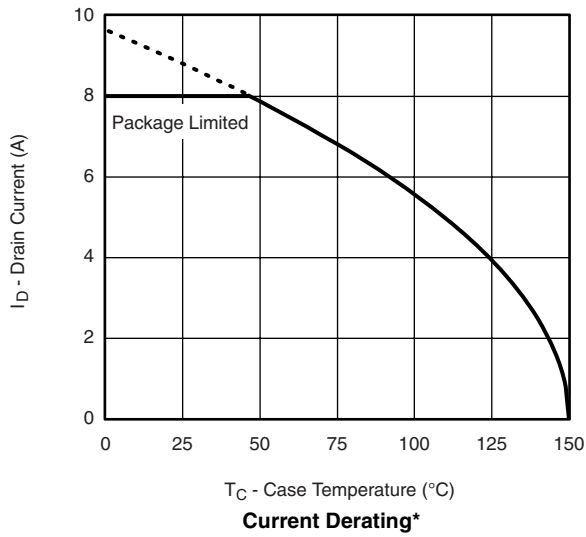
**On-Resistance vs. Junction Temperature**



## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

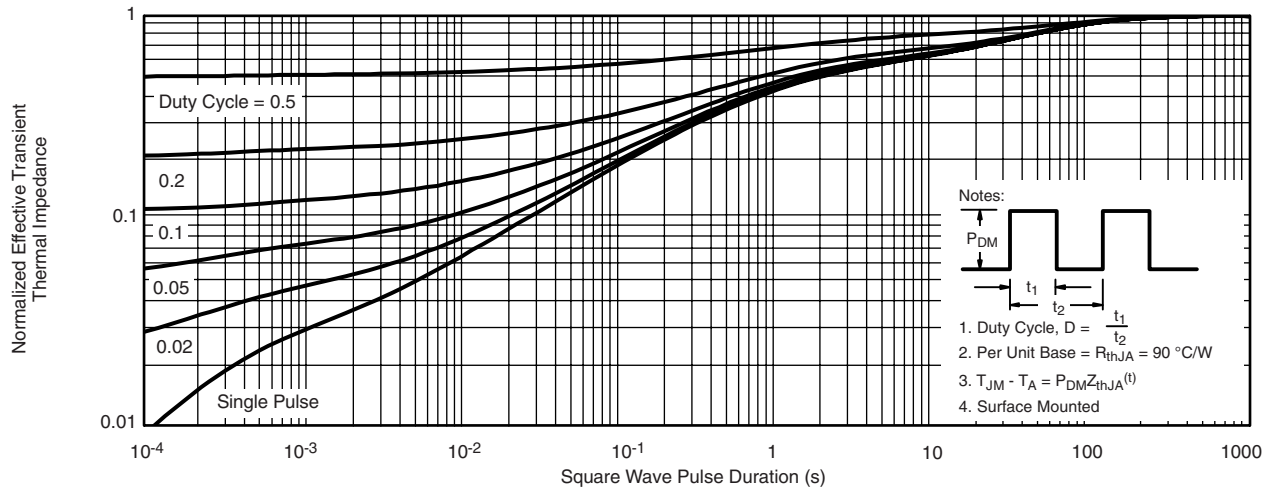


**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

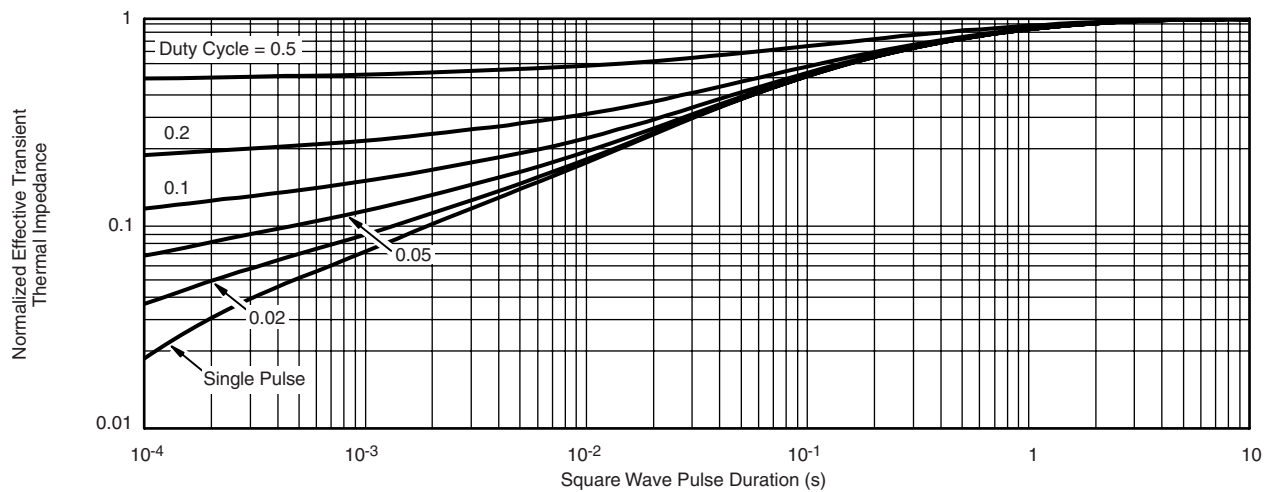


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



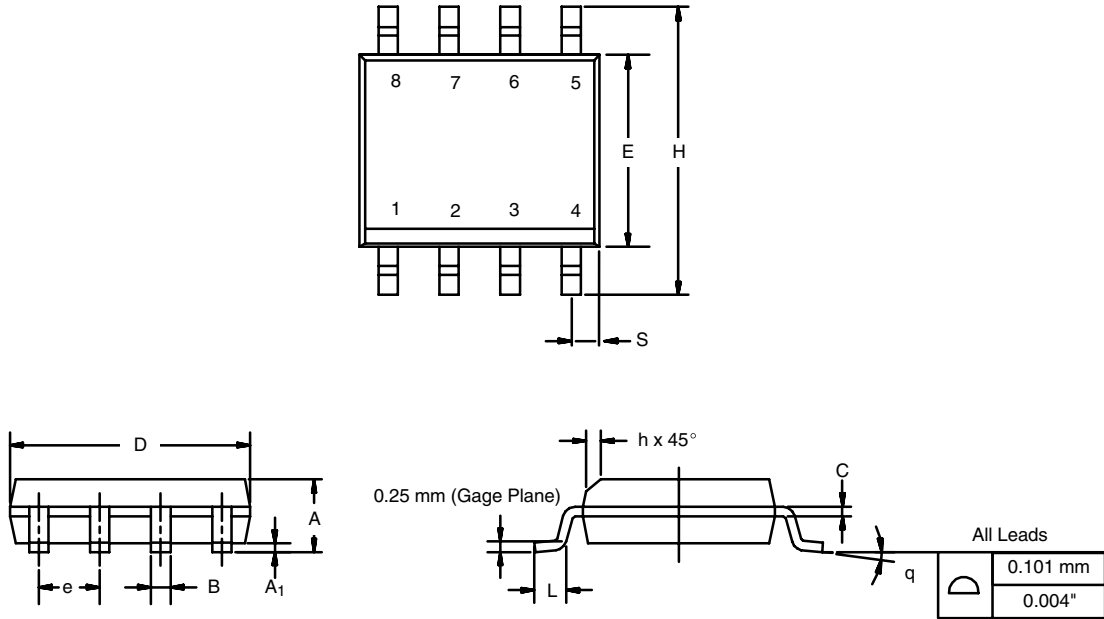
**Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?69595](http://www.vishay.com/ppg?69595).



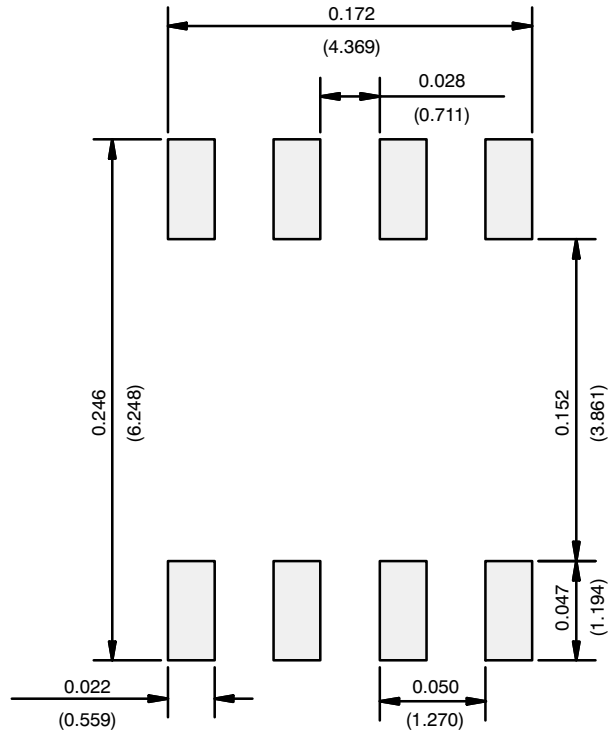
**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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