Click **here** to ask an associate for production status of specific part numbers.

MAX86174A/MAX86174B

Best-in-Class Optical Pulse Oximeter and Heart-Rate Sensor AFE for Wearable Health

General Description

The MAX86174A/MAX86174B are ultra-low-power optical data acquisition systems with both transmit and receive channels. On the transmitter side, the MAX86174A/MAX86174B have four LED driver output pins. Each pin is programmable from two, high-current, 8-bit LED drivers. On the receiver side, the MAX86174A consists of two optical readout channels that can operate simultaneously while the MAX86174B has a single optical readout channel. The devices have low-noise, charge-integrating analog front-end, 20-bit ADC, and best-in-class ambient-light cancellation (ALC) circuits.

Due to the low power consumption, compact size, ease and flexibility of use, the MAX86174A/MAX86174B are ideal for a wide variety of optical sensing applications such as pulse oximetry and heart-rate detection.

The MAX86174A/MAX86174B operate on a 1.8V main supply voltage and a 2.7V to 5.5V LED driver supply voltage. The devices support both I^2C- and SPI-compatible interfaces in a fully autonomous way. The devices have a large 256-word built-in FIFO. The MAX86174A/MAX86174B are available in a compact 16-WLP package.

Applications

- Wearable Devices for Fitness, Wellness and Medical Applications
- Clinical Accuracy
- Suitable for Wrist, Finger, Ear, and Other Locations
- Optimized Performance to Detect
  - Optical Heart Rate
  - Heart-Rate Variability
  - Oxygen Saturation (SpO_2)
  - Body Hydration
  - Muscle and Tissue Oxygen Saturation (SmO_2 and StO_2)
  - Maximum Oxygen Consumption (VO2 Max)

Benefits and Features

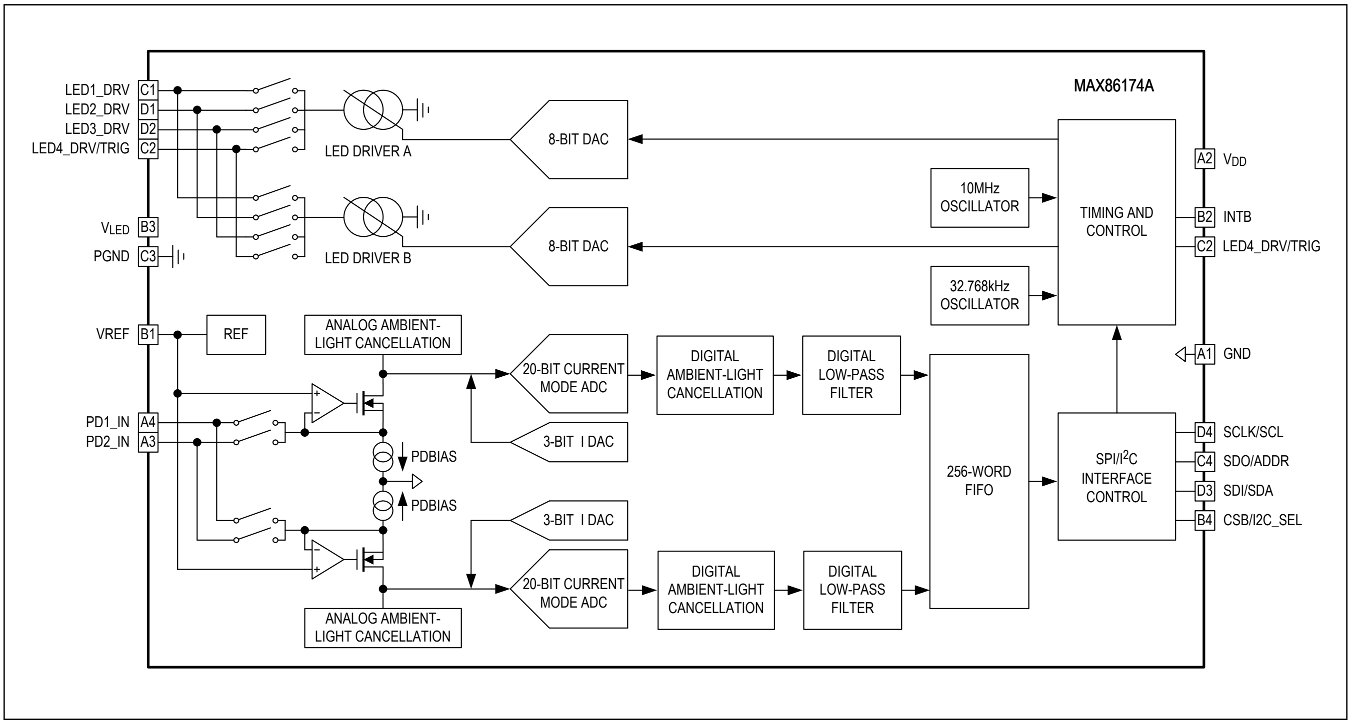
- Complete Optical Data Acquisition System
- Ultra-Low-Power Operation for Body Wearable Devices
  - Low-Power-Operation, Optical Readout Channel < 11µA (typ) at 25fps
  - Exposure Integration Period Ranging from 14.6µs to 117.1µs
  - Low Shutdown Current < 1µA (typ)
- Excellent Top-End Dynamic Range > 93dB in White Card Loop-Back Test (Nyquist Sample-to-Sample Variance)
- Extended Dynamic Range up to 111dB (Averaging and Off-Chip Filtering) to Enable SpO_2 on Wrist/Chest for Low Perfusion Cases
- Support Frame Rates from 1fps to 2048fps
- High-Resolution 20-Bit Charge-Integrating ADCs
- Support Both Burst Averaging and Decimation Averaging Modes
- On-Chip 12Hz Low-Pass Filter for Improved SNR and Reduced Power for Continuous Heart-Rate Measurement
- Supports Two PD Inputs for Multi-Parameter Measurements
- Supports Four LED Driver Output Pins Generated from Two 8-Bit LED Current Drivers
- Low Dark-Current Noise of < $50pA_{RMS}$ (Sample-to-Sample Variance in 117.1µs Integration Time)
- Excellent Ambient Range and Rejection Capability
  - 200µA Ambient Photodiode Current
  - > 70dB Ambient Rejection at 120Hz (Burst Average > 2)
- Miniature 1.67mm x 1.78mm, 0.4mm Ball Pitch, 4 x 4 WLP Package
- -40°C to +85°C Operating Temperature Range

Ordering Information appears at end of datasheet.

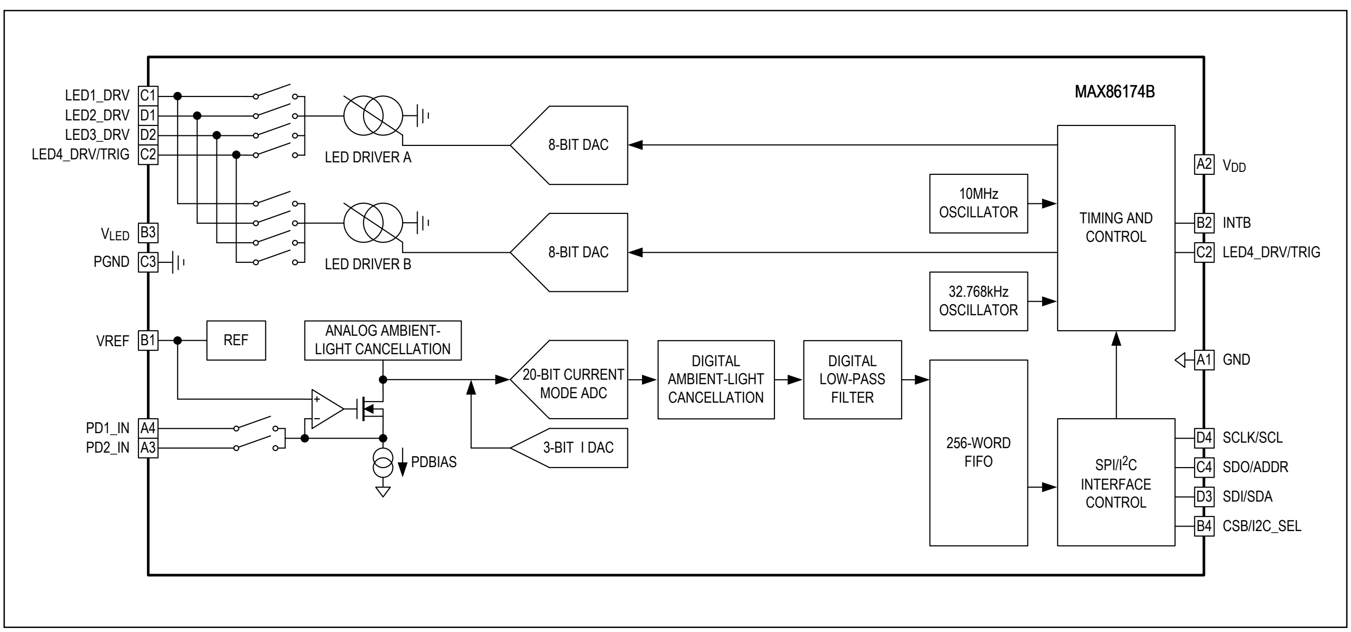
19-100999; Rev 1; 2/22

Simplified Block Diagram

MAX86174A



MAX86174B



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Absolute Maximum Ratings

V_{DD} to GND .... -0.3V to +2.2V
V_{LED} to PGND .... -0.3V to +6.0V
PGND to GND .... -0.3V to +0.3V
VREF to GND .... -0.3V to +2.2V
LEDn_DRV (n = 1 to 4), TRIG to PGND .. -0.3V to (V_{LED} + 0.3V)
PDm_IN to GND (m = 1, 2) .... -0.3V to +2.2V
SDO/ADDR to GND .... -0.3V to (V_{DD} + 0.3V)
SDI/SDA, SCLK/SCL, CSB/I2C_SEL, INTB to GND .... -0.3V to +6V
Output Short-Circuit Duration .... Continuous
Continuous Input Current into Any Pin (except LEDn_DRV Pins, n = 1 to 4) .... ±50mA
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -40°C to +150°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 WLP

Package Code	N161B1+1
Outline Number	21-100454
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	57.93°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Voltage	V_{DD}	Verified during PSRR Test	1.7	1.8	2.0	V
LED-Supply Voltage	V_{LED}	Verified during PSRR Test	2.7		5.5	V

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16μA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6μs, MEASx_LED_SETLNG = 6μs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Average V_{DD} Supply Current	I_{DD}	Single channel, one Measure/ Frame (Note 5a)	FR = 512fps		95	150	μA
			FR = 64fps		17		
			FR = 8fps		3.5		
		Single channel, four Measures/ Frame (Note 5a)	FR = 512fps		300	420	
			FR = 64fps		40		
			FR = 8fps		6.5		μA
		Dual channel, one Measure/Frame (Note 5b)	FR = 512fps		150	210	μA
			FR = 64fps		24		
			FR = 8fps		4.5		
		Dual channel, four Measures/Frame (Note 5b)	FR = 512fps		480	650	
			FR = 64fps		60		
			FR = 8fps		9.5		
Average V_{LED} Supply Current	I_{LED}	Single Channel, one LED/Frame, MEASx_LED_SETLNG = 1 (Note 5a)	FR = 512fps		870		μA
			FR = 64fps		98		
			FR = 8fps		12.5		
V_{DD} Current in Shutdown	I_{DD_SHDN}	T_A = +25°C			1.0	3	μA
V_{LED} Current in Shutdown	I_{LED_SHDN}	T_A = +25°C				0.5	μA
LED DRIVER							
LED Current Resolution					8		bits
Driver DNL	DNL_{TX}	MEASx_LED_RGE = 0x3		-1		+1	LSB
Driver INL	INL_{TX}	MEASx_LED_RGE = 0x3			1		LSB
Full-Scale LED Current	I_{LED}	MEASx_DRVy_PA = 0xFF	MEASx_LED_RGE = 0x0		32		mA
			MEASx_LED_RGE = 0x1		64		
			MEASx_LED_RGE = 0x2		96		
			MEASx_LED_RGE = 0x3	120	128	136	
LED Driver Rise Time		MEASx_DRVy_PA = 0xFF, 10% to 90%, all LED range settings				3	μs
LED Driver Fall Time		MEASx_DRVy_PA = 0xFF, 10% to 90%, all LED range settings				3	μs

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Output Voltage	V_{OL}	MEASx_DRVy_PA = 0xFF, < 1% change in LED current	MEASx_LED_RGE = 0x0		135		mV
			MEASx_LED_RGE = 0x1		260		
			MEASx_LED_RGE = 0x2		380		
			MEASx_LED_RGE = 0x3		500	800	
LED Driver DC V_{LED} PSR		MEASx_DRVy_PA = 0xFF, V_{DD} = 1.8V, V_{LEDn_DRV} = 1.2V, V_{LED} = 3.1V to 5.5V	MEASx_LED_RGE = 0x0		±5		µA/V
			MEASx_LED_RGE = 0x1		±5		µA/V
			MEASx_LED_RGE = 0x2		±5		
			MEASx_LED_RGE = 0x3	-150		+150	
LED Driver Compliance Interrupt Threshold		MEASx_LED_RGE = 0x0		120	148	180	mV
		MEASx_LED_RGE = 0x1		260	287	320	
		MEASx_LED_RGE = 0x2		395	425	460	
		MEASx_LED_RGE = 0x3		530	560	600	
READOUT CHANNEL							
ADC Resolution					20		bits
INL	INL_{RX}	MEASx_TINT = 117.1µs			±10		LSB
		MEASx_TINT = 14.6µs			±40		
DNL	DNL_{RX}	MEASx_TINT = 117.1µs			±3		LSB
		MEASx_TINT = 14.6µs			±10		
ADC Full-Scale Input Current	I_{FS}	MEASx_PPGy_ADC_RGE = 0x0			4.0		µA
		MEASx_PPGy_ADC_RGE = 0x1			8.0		
		MEASx_PPGy_ADC_RGE = 0x2			16.0		
		MEASx_PPGy_ADC_RGE = 0x3			32.0		
ADC Integration Time	t_{INT}	MEASx_TINT = 0x0			14.6		µs
		MEASx_TINT = 0x1			29.2		
		MEASx_TINT = 0x2			58.6		
		MEASx_TINT = 0x3			117.1		
Minimum Free-Running Frame Rate					1		fps
Maximum Free-Running Frame Rate					2048		fps
Internal Frame-Rate Clock	f_{FRAME_CLK}			-2% of typ	32768	+2% of typ	Hz

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRIG External Frame-Clock Frequency	$f_{TRIG\_EXT\_CLK}$			31000		34000	Hz
TRIG Pulse Width	t_{TRIG}			1			µs
Internal Power-Up Time					200		µs
ADC Clock Frequency	CLK			9.75	10.0	10.25	MHz
Maximum DC-Ambient-Light Rejection	ALR	ALC_OVF = 1			200		µA
Dynamic Ambient-Light Rejection		$I_{EXPOSURE}$ = 1µA, $I_{AMBIENT}$ = 1µA DC with ±0.4µA$_{P-P}$ 120Hz sine wave			80		dB
DC Ambient-Light Rejection		$I_{EXPOSURE}$ = 1µA, $I_{AMBIENT}$ = 1µA and 30µA			0.5		nA
Dark-Current Offset	DC_O	PDm_BIAS = 0x1, t_{INT} = 117.1µs			±1		Counts
Dark-Current Input-Referred Noise		MEASx_TINT = 14.6µs			212		pA_{RMS}
		MEASx_TINT = 29.2µs			150		
		MEASx_TINT = 58.6µs			106		
		MEASx_TINT = 117.1µs			75		pA_{RMS}
V_{DD} DC PSR		$I_{EXPOSURE}$ = 1µA, V_{DD} = 1.7V to 2.0V	t_{INT} = 14.6µs		1100		LSB/V
			t_{INT} = 29.2µs		750		
			t_{INT} = 58.6µs		530		
			t_{INT} = 117.1µs		410	800	
DIGITAL I/O CHARACTERISTICS							
Input-Voltage Low	V_{IL}	SDI/SDA, SCLK/SCL, TRIG, CSB/I2C_SEL				0.4	V
Input-Voltage High	V_{IH}	SDI/SDA, SCLK/SCL, TRIG, CSB/I2C_SEL		1.4			V
Input Hysteresis	V_{HYS}	SDI/SDA, SCLK/SCL, TRIG, CSB/I2C_SEL			430		mV
Input Capacitance	C_{IN}	SDI/SDA, SCLK/SCL, TRIG, CSB/I2C_SEL			10		pF
Input-Leakage Current	I_{IN}	SDI/SDA, SCLK/SCL, TRIG, CSB/I2C_SEL. T_A = +25°C, V_{IN} = 0V or 1.8V		-1	0.01	+1	µA
Output-Low Voltage	V_{OL}	SDO, INTB, SDI/SDA (in I^2C mode), I_{SINK} = 4mA				0.4	V
Output-High Voltage	V_{OH}	SDO, INTB, I_{SOURCE} = 4mA		V_{DD} - 0.4			V
Open-Drain Output-Low Voltage	V_{OL_OD}	INTB_OCFG = 0x0, I_{SINK} = 4mA				0.4	V
SPI TIMING CHARACTERISTICS (Note 4)							
SCLK Frequency	f_{SCLK}					24	MHz
SCLK Period	t_{CP}			41.7			ns
SCLK Pulse-Width High	t_{CH}			18			ns

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16μA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6μs, MEASx_LED_SETLNG = 6μs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse-Width Low	t_{CL}		18			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	Applies to 1st SCLK rising edge after CSB goes low	20			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding 1st rising edge	5			ns
Last SCLK Rise to CSB Rise	t_{CSH1}	Applies to last SCLK rising edge in a transaction	20			ns
Last SCLK Rise to next CSB Fall	t_{CSF}	Applies to last SCLK rising edge to next CSB falling edge (new transaction)	60			ns
CSB Pulse-Width High	t_{CSPW}		40			ns
SDI to SCLK Rise Setup Time	t_{DS}		5			ns
SDI to SCLK Rise Hold Time	t_{DH}		5			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 30pF			15	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF	20			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable Time			5	ns
I^2C TIMING CHARACTERISTICS (Note 4)						
I^2C Write Address		ADDR = 0		D4		Hex
		ADDR = 1		D6		
I^2C Read Address		ADDR = 0		D5		Hex
		ADDR = 1		D7		
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus-Free Time Between STOP and START Conditions	t_{BUF}		1.3			μs
Hold Time START and Repeat START Condition	$t_{HD,STA}$		0.6			μs
SCL Pulse-Width Low	t_{LOW}		1.3			μs
SCL Pulse-Width High	t_{HIGH}		0.6			μs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			μs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs
Pulse-Width of Suppressed Spike	t_{SP}		0		50	ns

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, MEASx_PPGy_ADC_RGE = 16µA, FR_CLK_DIV = 32 (f_{FRAME} = 1024fps), MEASx_TINT = 14.6µs, MEASx_LED_SETLNG = 6µs, MEASx_LED_RGE = 128mA, C_{PD} = 65pF, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + $0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + $0.1C_B$		300	ns
SDA Transmitting Fall Time	t_{TF}		20 + $0.1C_B$		300	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 2: All other register settings are assumed to be POR defaults, unless otherwise noted.

Note 3: Definitions of terms:
- Frame = All measurements made during a particular wake-up interval.
- Sample = Ambient-light-corrected exposure measurement where both LED exposure and ambient-light ADC conversions are taken.

Register nomenclature:
- ADC_RGE = Measurement of full-scale range as defined in the MEASx_PPGy_ADC_RGE registers (x = 1 to 6, y = 1, 2).
- TINT = ADC integration time as defined in the MEASx_TINT registers (x = 1 to 6).
- PDm_BIAS = Photodiode bias setting register (m = 1 to 2).
- LED_RGE = Measurement of full-scale range of the LED driver in the MEASx_LED_RGE register (x = 1 to 6).
- DRVy_PA = Measurement of the LED driver DAC code in the MEASx_DRVy_PA register (x = 1 to 6, y = A, B, C).
- LED_SETLNG = Measurement of the LED settling time in the MEASx_LED_SETLNG registers (x = 1 to 6).

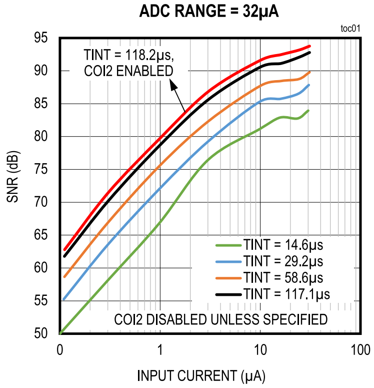
Note 4: For design guidance only. Not production tested.

Note 5: FR = PPG Frame Rate
- MEASx_TINT = 14.6µs, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, PPG1_PWRDN = 0, PPG2_PWRDN = 1
- MEASx_TINT = 14.6µs, MEASx_LED_RGE = 128mA, MEASx_DRVy_PA = 0x7F, PPG1_PWRDN = 0, PPG2_PWRDN = 0

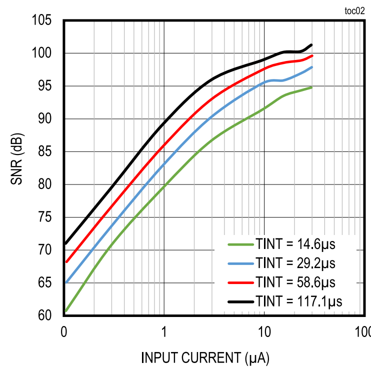
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, COI2 filter disabled, unless otherwise noted.)

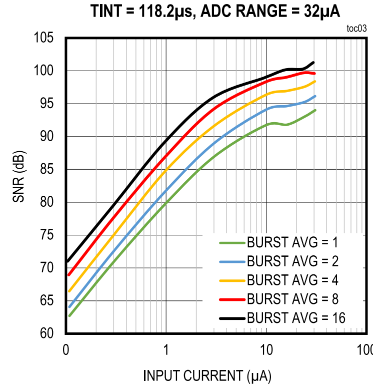
SNR vs. INPUT CURRENT
ADC RANGE = 32µA



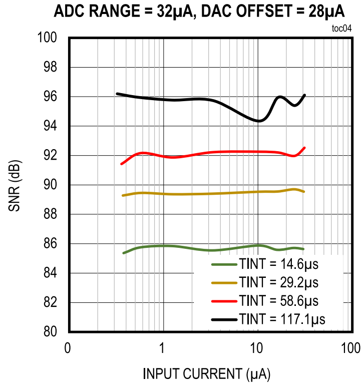
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
BURST AVERAGING = 16



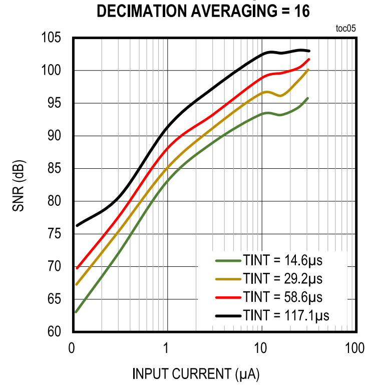
SNR vs. INPUT CURRENT
TINT = 118.2µs, ADC RANGE = 32µA



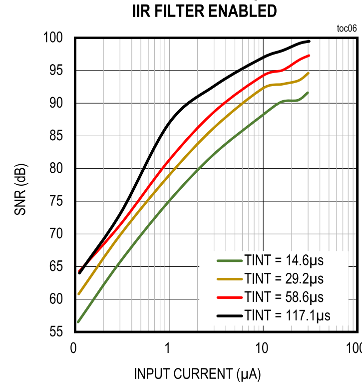
SNR vs. INPUT CURRENT
ADC RANGE = 32µA, DAC OFFSET = 28µA



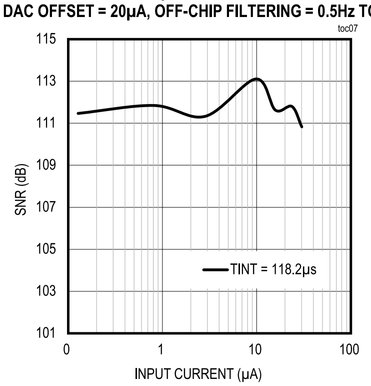
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
DECIMATION AVERAGING = 16



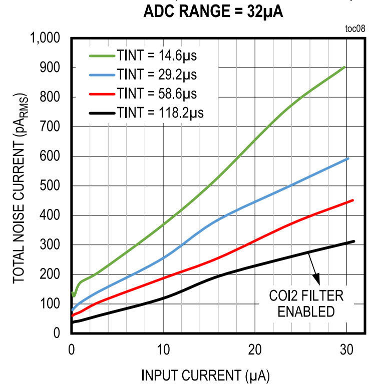
SNR vs. INPUT CURRENT
ADC RANGE = 32µA
IIR FILTER ENABLED



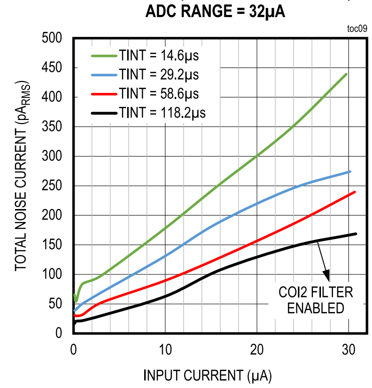
SNR vs. INPUT CURRENT
ADC RANGE = 32µA, BURST AVERAGING = 8x,
DAC OFFSET = 20µA, OFF-CHIP FILTERING = 0.5Hz TO 4Hz



TOTAL NOISE (0.5Hz–20Hz BANDWIDTH)
ADC RANGE = 32µA



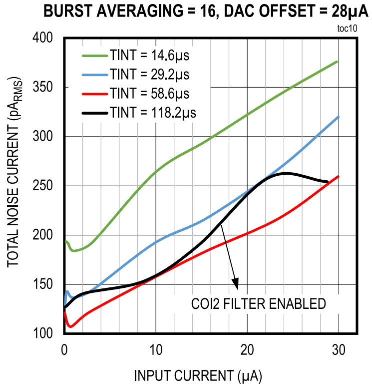
TOTAL NOISE (0.5Hz–5Hz BANDWIDTH)
ADC RANGE = 32µA



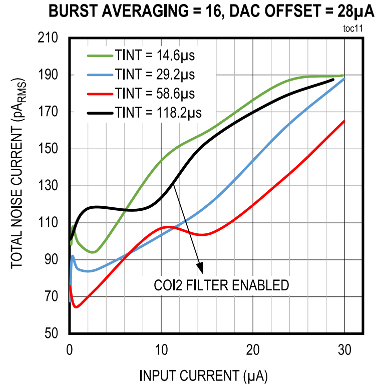
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, COI2 filter disabled, unless otherwise noted.)

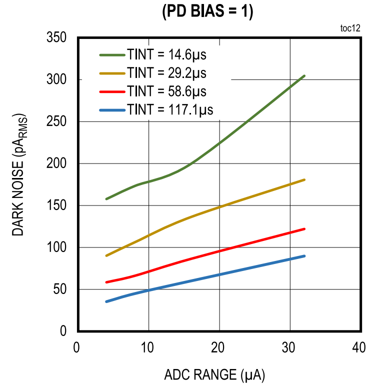
TOTAL NOISE (0.5Hz–20Hz BANDWIDTH)
ADC RANGE = 32µA,
BURST AVERAGING = 16, DAC OFFSET = 28µA



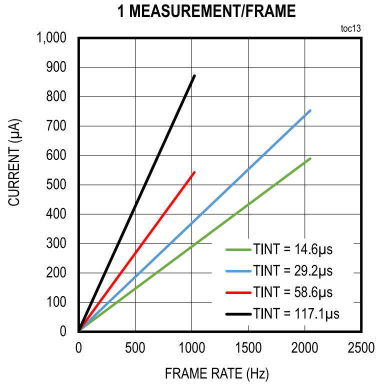
TOTAL NOISE (0.5Hz–5Hz BANDWIDTH)
ADC RANGE = 32µA,
BURST AVERAGING = 16, DAC OFFSET = 28µA



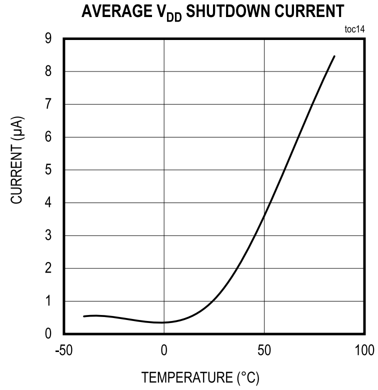
DARK NOISE vs. ADC RANGE
(PD BIAS = 1)



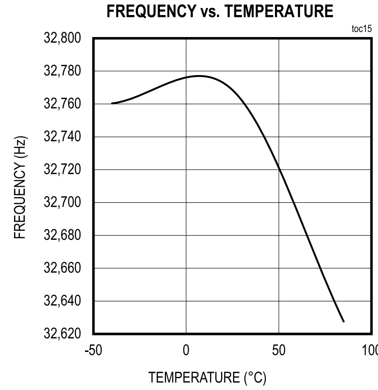
AFE POWER vs. FRAME RATE
1 MEASUREMENT/FRAME



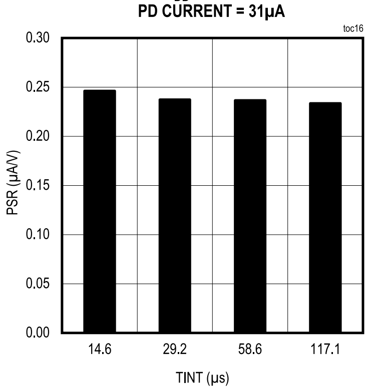
AVERAGE V_{DD} SHUTDOWN CURRENT



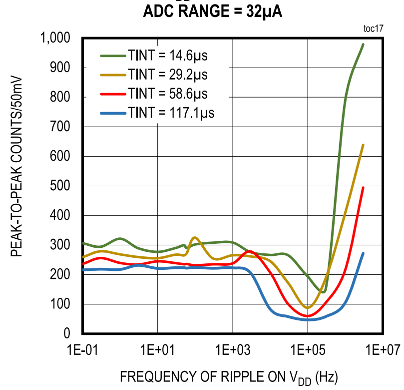
SLOW OSCILLATOR
FREQUENCY vs. TEMPERATURE



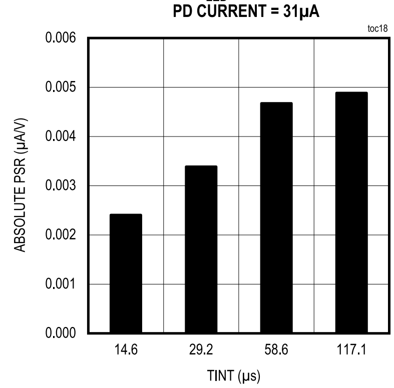
V_{DD} DC PSRR
PD CURRENT = 31µA



V_{DD} AC PSRR
ADC RANGE = 32µA

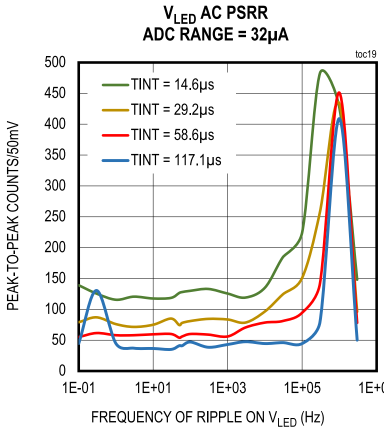


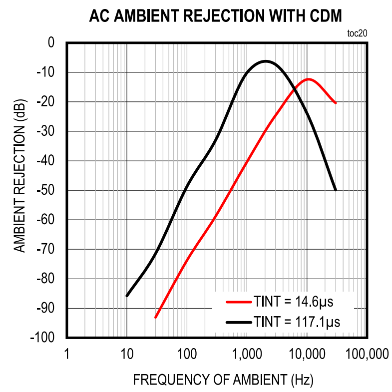
V_{LED} DC PSRR
PD CURRENT = 31µA

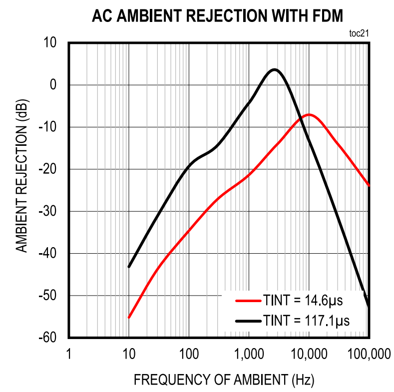


Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, COI2 filter disabled, unless otherwise noted.)

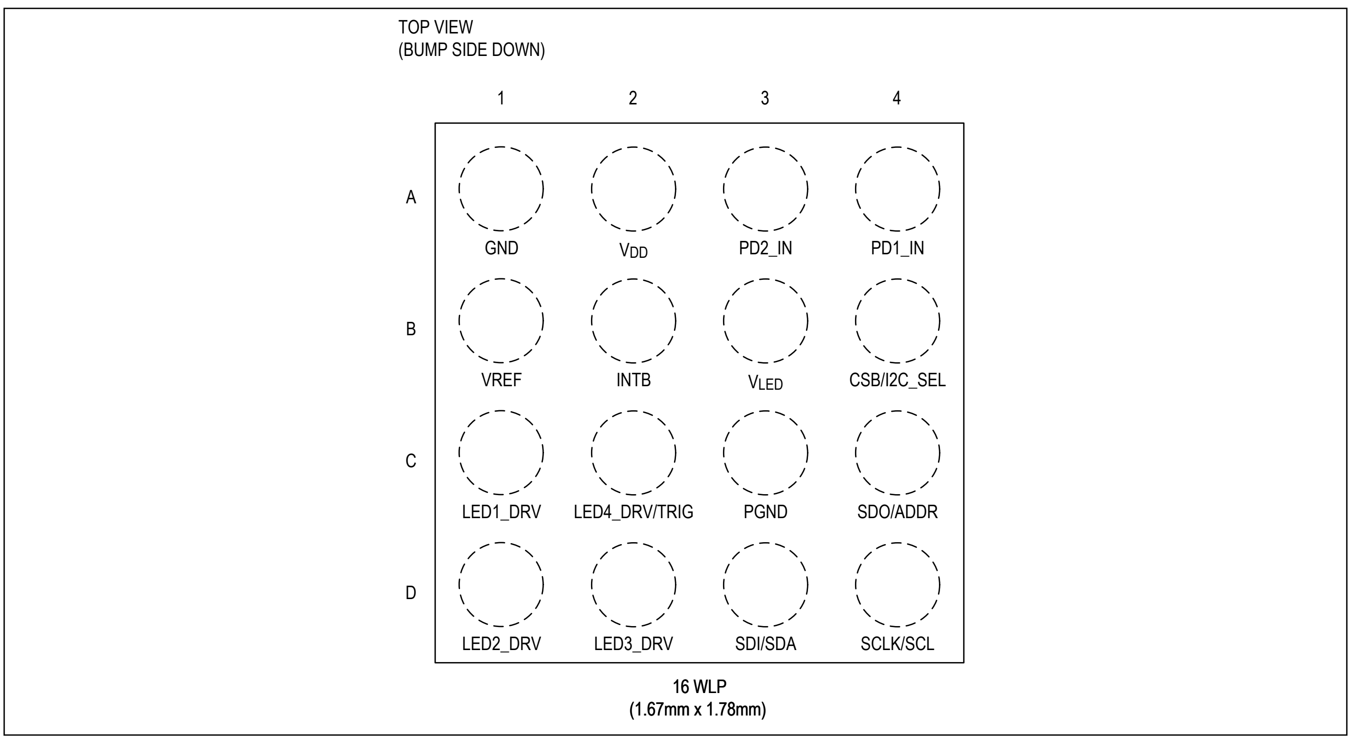






Pin Configuration

MAX86174A/MAX86174B



Pin Description

PIN	NAME	FUNCTION
POWER		
A2	V_{DD}	Power Supply. Connect to an externally regulated supply. Bypass with a 0.1μF capacitor as close as possible to the bump and a 10μF capacitor to GND.
A1	GND	Main Power Supply Return. Connect to PCB Ground. Refer to the *Layout Guidelines* section for more information.
B3	V_{LED}	LED Power Supply Input. In a configuration with more than one LED supply, connect V_{LED} to the highest LED supply voltage. Bypass with a 10μF capacitor to PGND.
C3	PGND	LED Power Return. Connect to PCB Ground. Refer to the *Layout Guidelines* section for more information.
CONTROL INTERFACE		
D4	SCLK/SCL	SPI Clock/I^2C Clock
C4	SDO/ADDR	SPI Data Output. In I^2C mode, this pin selects the I^2C device address.
D3	SDI/SDA	SPI Data Input/I^2C Data
B4	CSB/ I2C_SEL	SPI Chip Select Input. The state of this pin sets the serial interface to typical levels. Low = SPI and High = I^2C.
C2	TRIG	External Clock or Start of Conversion Trigger Input. Do not leave unconnected. Tie to GND or V_{DD} when it is not used.
B2	INTB	Interrupt Output. When INTB is not used, it can be left unconnected.
OPTICAL PINS		
A4	PD1_IN	Photodiode Cathode Input 1. Tie to GND when this pin is not used.
A3	PD2_IN	Photodiode Cathode Input 2. Tie to GND when this pin is not used.
C1	LED1_DRV	LED Output 1. Driven when MEASx_DRVy = 0 (x = 1 to 6, y = A, B). Connect the LED cathode to LED1_DRV and its anode to the V_{LED} supply. This pin can be left unconnected when not used.
D1	LED2_DRV	LED Output 2. Driven when MEASx_DRVy = 1 (x = 1 to 6, y = A, B). Connect the LED cathode to LED2_DRV and its anode to the V_{LED} supply. This pin can be left unconnected when not used.
D2	LED3_DRV	LED Output 3. Driven when MEASx_DRVy = 2 (x = 1 to 6, y = A, B). Connect the LED cathode to LED3_DRV and its anode to the V_{LED} supply. This pin can be left unconnected when not used.
C2	LED4_DRV	LED Output 4. Driven when MEASx_DRVy = 3 (x = 1 to 6, y = A, B). Connect the LED cathode to LED4_DRV and its anode to the V_{LED} supply. Do not leave unconnected when this pin is not used. When not used, tie to GND or V_{DD}.
REFERENCE		
B1	VREF	ADC Reference Buffer Output. Bypass to GND with a 1μF X5R ceramic capacitor.

Detailed Description

The MAX86174A/MAX86174B are complete integrated optical data acquisition systems, ideal for various applications including optical pulse-oximetry and heart-rate detection applications. The devices are designed for the demanding requirements of wearable devices and require minimal external hardware components for integration into a wearable device.

The MAX86174A includes dual optical-readout channels operating simultaneously and the MAX86174B has a single optical-readout channel. Both devices incorporate robust ambient light cancellation and two high-current LED drivers to form a complete optical-readout signal chain. The two LED drivers support up to 4 LED drive output pins through two on-chip 4x1 multiplexers and control logic. Both devices support 2 PD input pins.

The MAX86174A/MAX86174B are fully adjustable through software registers and the digital output data is stored in a 256-word FIFO. The FIFO allows the MAX86174A/MAX86174B to be connected to a microcontroller or processor on a shared bus, I^2C or SPI depending on the hardware selection on I2C_SEL pin, on which the data is not being read continuously from the MAX86174A/MAX86174B registers. Both operate in fully autonomous mode for low-power battery applications.

The MAX86174A/MAX86174B operate on a 1.8V main supply voltage, with a separate 2.7V to 5.5V LED driver-supply voltage (supplied at V_{LED}). Both devices have flexible exposure, timing and shutdown configurations as well as control of individual blocks to optimize measurements with minimum power consumption and a high level of accuracy. The MAX86174A/MAX86174B operate in a dynamic power-down mode, always powering down between frames; thus, minimizing power consumption. For more details on the power consumption at various frame rates, refer to the *Electrical Characteristics* table.

Keeping the ripple on the V_{LED} line as low as possible ensures the highest SNR is achieved. If a regulated supply is not available, the switching frequency on V_{LED} should be kept between 100kHz and 3MHz. By ensuring the switching frequency stays within the recommended range, along with a good load transient response, high SNR can be maintained at the heaviest loads (high LED drive-current applications).

The *MAX20345* or the smaller *MAX20343* are recommended solutions for a buck-boost supplying V_{LED}. Both offer highly efficient buck-boost regulators with a very small load ripple, fast load transient responses, and have load pulse consistencies that provide more than 93dB SNR in a white card DC SNR test.

The various blocks and features in the PPG system are discussed in detail in the following sections.

Optical Transmitter Overview

The MAX86174A/MAX86174B have two independent precision LED current drivers that are connected to four LED-driver pins through two 4x1 muxes. Two LED current DACs modulate LED pulses for a variety of optical measurements. The two LED current DACs have 8-bit dynamic range with four programmable full-scale range settings of 32mA, 64mA, 96mA, and 128mA (typ). The configuration of the LED drivers can be uniquely set for each measurement. The PPG MEASx Setup (x = 1 to 6) register blocks (0x20 to 0x4E) define how each LED driver is connected for that particular measurement. Each measurement can drive one or both LED drivers.

Table 1. LED Driver and LED Mux Configuration

MEASx_DRVy (x = 1 to 6, y = A, B)	LEDn_DRV PIN CONNECTED TO LED DRIVER (n = 1 to 4)
0x0	LED1_DRV
0x1	LED2_DRV
0x2	LED3_DRV
0x3	LED4_DRV

This configuration of LED drivers and LED muxes is highly flexible, not only allowing any of the four LED driver pins to be used at any one time, but also allowing for any pin to sink up to 256mA by combining both drivers to generate a higher output current. In this compact design, LED4_DRV shares the same pin package with the TRIG input. If LED4_DRV is in use, TRIGLED4_SEL[0](0x17) is configured to be 1. Figure 1 shows how the two LED drivers are connected to the four LED-driver pins.

Both LED drivers are low dropout-current sources allowing for low-noise, power-supply independent LED currents to be sourced with minimal voltage overhead; thereby, minimizing LED power consumption. Four full-scale range settings are provided to allow for the optimization of LED driver noise, and dropout voltage on the LEDn_DRV (n = 1 to 4) pins. Table 2 illustrates this trade-off.

Table 2. LED Driver Full-Scale Range Trade-Off

FULL-SCALE RANGE (mA)	RECOMMENDED MINIMUM VLEDn_DRV (mV)	PEAK REFLECTOR CARD SNR (dB) WITH COI2 FILTER ENABLED
32	300	87
64	500	91
96	700	92
128	900	93

The LED on-time is the sum of the receiver integration time selected in MEASx_TINT, and the LED settling time selected in MEASx_LED_SETLNG. The duty cycle is set by the ratio of the LED on-time and the frame period. The average LED supply current is calculated as the product of the programmed LED current and the duty cycle.

Note: MEASx_TINT[4:3] (x = 1–6) is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49 and MEASx_LED_SETLNG[4:3] (x = 1–6) is in registers 0x23, 0x2B, 0x33, 0x3B, 0x43, 0x4B.

The voltage on V_{LED} depends on the forward voltage (V_F) of the LEDs driven by the MAX86174A/MAX86174B. The AFE requires a minimum of 2.7V applied to the V_{LED} pin (see the *Electrical Characteristics* table). Additionally, the minimum required V_{LED} voltage in a system is determined by the sum of forward voltage (V_F) of each LED at maximum LED current and the minimum V_{LEDn_DRV} voltage in Table 2. Also note that Table 2 is based on the Maxim internal test board and it is recommended to test and verify the SNR with the best V_{LEDn_DRV} on the different PCBs.

The V_{LED} voltage must be above this minimum to avoid compression, and allow for enough headroom to supply the LED drive current as needed; otherwise, the I_{LED} can be reduced and more sensitive to V_{LED} supply changes. The voltage on the LEDn_DRV pins can be measured during an exposure to ensure the minimum headroom voltage is maintained during each LED exposure (LED on time). The minimum V_{LED} can be simply calculated by using the formulas below:

$V_{LED} \geq 2.7V$ and $V_{LED} \geq V_F + V_{LEDn\_DRV}$

where, V_F is a function of maximum LED current for the system.

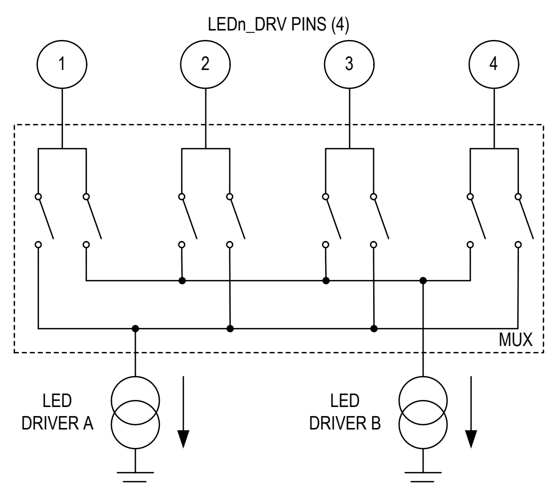


Figure 1. LED Drivers

Optical Receiver Overview

The optical path in MAX86174A/MAX86174B is composed of a front-end photodiode biasing circuit with an analog ambient-light cancellation (ALC) sample and hold circuit that nulls the ambient-light photodiode current at the input of the ADC. This front-end photodiode biasing circuit is followed by a current integrating, continuous-time sigma-delta ADC with a proprietary discrete time filter. This discrete time filter uses multiple dark and exposure samples to generate an accurate 20-bit effective exposure output signal with excellent low- and high-frequency ambient-light rejection.

The MAX86174A incorporates dual optical-signal paths and the MAX86174B incorporates a single optical-signal path. Both have four photodiode input pins which are configured by MEASx_PDSEL (x = 1 to 6) in each measurement. The on-chip Mux connects the two photodiode inputs to the optical signal path, as shown in Figure 2.

Note: MEASx_PDSEL[7:6] (x = 1–6) is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

For scenarios with MAX86174A requiring only one optical-signal path to be active (for example, lower power consumption), either one of the two channels can be powered down by setting PPG1_PWRDN[2](0x11) or PPG2_PWRDN[3](0x11) to 1. In this way, the MAX86174A is used in a single-channel configuration. By default, the MAX86174A PPG has dual channels enabled.

Each optical signal path supports four full-scale range settings of 4μA, 8μA, 16μA, and 32μA set in the MEASx_PPGy_ADC_RGE (x = 1 to 6, y = 1, 2 for MAX86174A, y = 1 for MAX86174B) field in each of the measurement configurations block. Also supported are four options for integration time, which effectively modulate the optical channel bandwidth, allowing for a trade-off between LED power consumption and PPG signal quality.

Note: MEASx_PPG1_ADC_RGE[1:0] (x = 1–6) and MEASx_PPG2_ADC_RGE[3:2] (x = 1–6) are in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A.

Each optical signal path also incorporates a 3-bit offset DAC for extending the optical dynamic range by sourcing some of the exposure current to the offset DAC. The current offset is selected in the MEASx_PPGy_DACOFF register bit field. This feature is especially useful under certain conditions that occur when attempting to limit the exposure ADC counts, for example, when avoiding saturation while increasing the exposure signal perfusion index.

Note: MEASx_PPG1_DACOFF[2:0] (x = 1–6) and MEASx_PPG2_DACOFF[6:4] (x = 1–6) are in registers 0x24, 0x2C, 0x34, 0x3C, 0x44, 0x4C.

Also, higher SNR is achieved by enabling the DAC offset in addition to utilizing the burst averaging and off-chip low-pass or band-pass filtering, allowing for 111dB SNR to be achieved. The optical channels also support multiple photodiode and LED settling time settings in order to support flexible multiparameter measurements for different types of photodiode/ LED wavelength combinations.

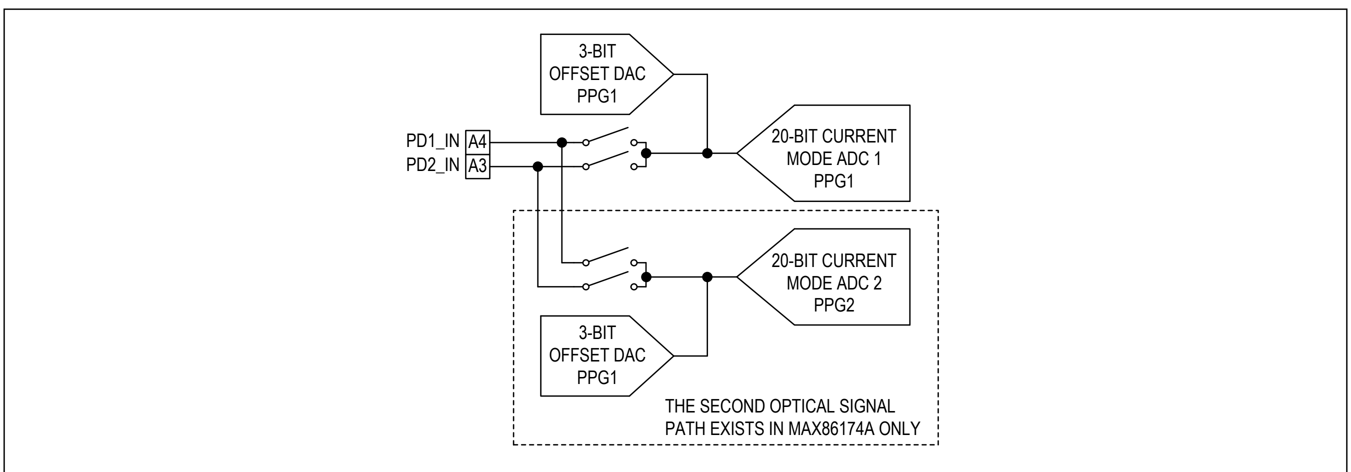


Figure 2. On-Chip Mux for the PD1_IN and PD2_IN pins

Most significantly, each signal path supports up to six unique combinations of the above configurations as needed. This allows a single optical AFE to support multiple optical measurements in a compact, energy-efficient design.

Photodiode Biasing

The MAX86174A/MAX86174B provide three photodiode biasing options to support a large range of photodiode capacitance. Each photodiode input can have a separate bias setting; thereby, allowing for different photodiodes to be used. The PDm_BIAS (m = 1, 2, register 0x15) settings adjust the PDm_IN bias point impedance to ensure that each photodiode settles rapidly enough to support the sample timing.

The PDm_BIAS impacts the dark current noise of the MAX86174A/MAX86174B. Because of the increased noise with a higher PDm_BIAS setting, the lowest recommended PDm_BIAS value should be used for any given photodiode capacitance.

Measurement Configuration and Timing

A measurement is essentially one combination of LED (or LEDs) and PD (or PDs) that results in an optical measurement. The MAX86174A/MAX86174B support six individual measurements, each of which can be configured independently. Each measurement can be configured by the group of registers named PPG MEASx Setup (x = 1 to 6). These registers set up a number of parameters as listed below.

- Connection of each of the two LED drivers to one of the four LED driver pins
- Connection of ADC channel(s) to one of two possible photodiodes
- Ambient measurement
- LED driver range and drive currents
- LED settling time
- PD settling time
- Number of burst averages of each measurement
- Ambient rejection scheme (CDM or FDM)
- On-chip decimation filter selection (COI or SINC3)
- ADC integration time
- ADC range for each channel
- DAC offset for each channel

A measurement can be configured to pulse one or two LED drivers sequentially at multiple wavelengths as is done in pulse oximetry measurements or simultaneously to drive multiple LEDs such as is done with heart-rate measurements on the wrist. A measurement is also configurable to measure direct ambient level. If direct ambient is enabled in a measurement through MEASx_AMB, it must be the last measurement in the sequence of enabled measurements.

Note: MEASx_AMB[6] (x = 1–6) is in registers 0x20, 0x28, 0x30, 0x38, 0x40, 0x48.

Figure 3 represents one measurement with only one of the LEDs active. No averaging is used. As seen in Figure 3 only LED1_DRV is pulsing during the exposure time. In this mode, each driver pulse results in a single optical sampled value for each PD input to be stored in the FIFO. For example, in a single-channel configuration, only one sample is stored in the FIFO for each driver pulse but for a dual-channel configuration, two samples are stored in the FIFO for each driver pulse.

This timing mode in Figure 3 is used when heart rate is being measured with a single LED.

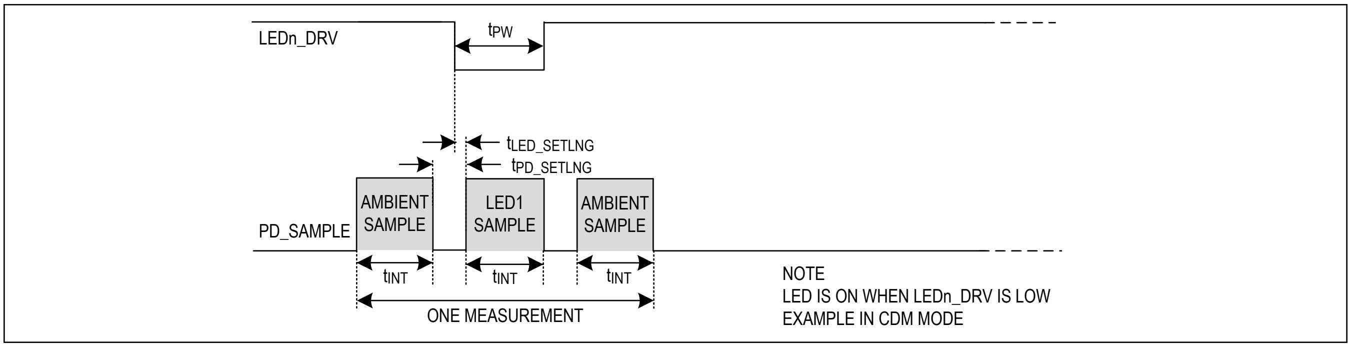


Figure 3. Measurement with One LED On

Ambient-Light Cancellation

The MAX86174A/MAX86174B implement ambient-light cancellation (ALC) in two steps, a coarse cancellation and a fine cancellation. Each PPG channel has its own dedicated ambient-light cancellation circuits. Also, each MEASx has its own ambient-light cancellation configuration. The coarse cancellation is in the analog domain. It is enabled by default and can be disabled by setting the ALC_DISABLE[4](0x13) to 1. The fine cancellation is a digital cancellation scheme and is configured with either a central difference method (CDM) or forward difference method (FDM) through the MEASx_FILT_SEL (x = 1 to 6) bit.

Note: MEASx_FILT_SEL[6] (x = 1–6) is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A.

ALC coarse cancellation can cancel up to 200µA of DC photodiode current. Any drift or residual from coarse cancellation is canceled by CDM/FDM cancellation.

One CDM sample is comprised of 3 ADC conversions, with 2 ambient and 1 exposure conversion where ambient-light estimation is made from dark measurements before and after the exposure measurement. One FDM sample is comprised of 2 ADC conversions with 1 ambient only and 1 exposure conversion where the ambient light is estimated by a dark measurement before the exposure measurement. The ambient and exposure samples are used for digital cancellation of any residual error (from ALC) or drift (in ambient signal). The final computed value is the effective exposure signal that is stored in the FIFO.

See Figure 4 for the timing diagram of CDM and Figure 5 for the timing diagram of FDM.

Ambient-light cancellation in low frequency ambient light improves when using burst average by setting MEASx_AVER ≥ 0x2. In addition, the MAX86174A/MAX86174B have a SINC3 decimation filter for the delta-sigma PPG ADC, which is enabled for each measurement individually by setting MEASx_SINC3_SEL. This filter provides improved high-frequency roll-off that improves the high-frequency ambient-light rejection. MAX86174A/MAX86174B by default uses a third order COI3 decimation filter that provides excellent quantization, but the roll-off at high frequencies is only 20dB/dec. The SINC3 filter provides a 60dB/dec roll-off for out-of-band frequencies; thus, improving ambient-light rejection at high frequencies. This filter is only available for MEASx_TINT = 0x3 (117.1µs). See Figure 11 for different decimation filters.

Note: MEASx_AVER[2:0] (x = 1–6) and MEASx_TINT[4:3] (x = 1–6) are in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49. MEASx_SINC3_SEL[7] (x = 1–6) is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A.

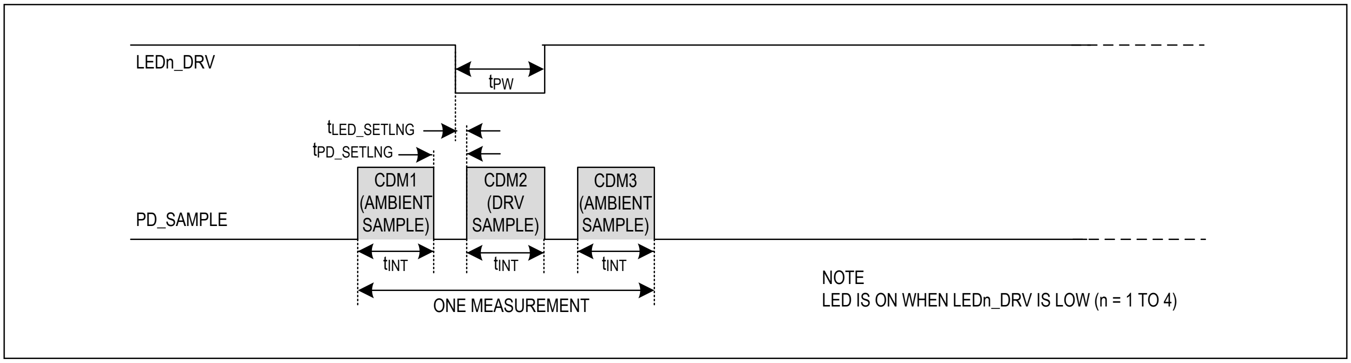


Figure 4. Central Difference Method (CDM)

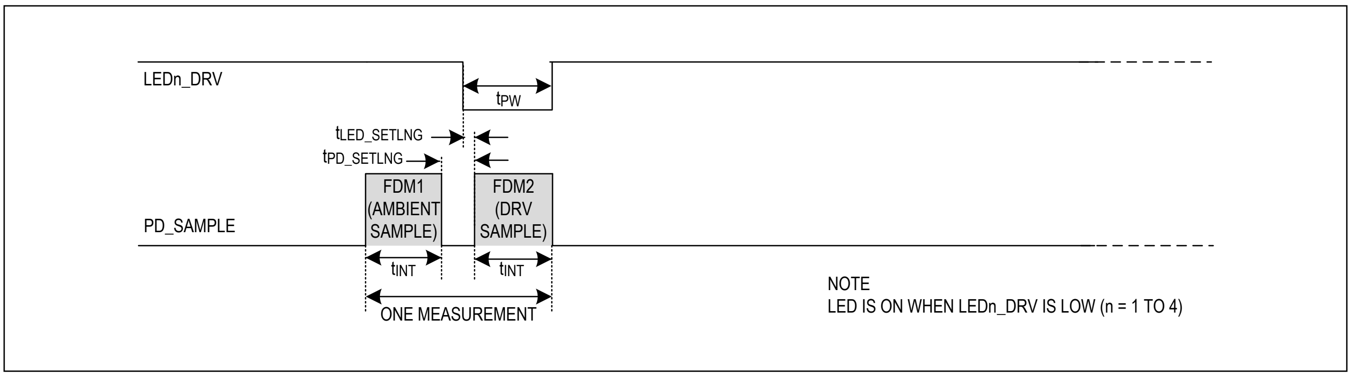


Figure 5. Forward Difference Method (FDM)

Frame and Frame Rate

A frame is a combination of one (min) to six (max) measurements configured in MEASx_EN (x = 1 to 6) (register 0x12). The frame rate defines how frequently a frame is repeated and is expressed in units of frames per second (fps). Frame rate is defined by two methods:

- Frame Rate = 32768/FR_CLK_DIV, where FR_CLK_DIV = 16 to 32766 are directly programmable (see *Register* 0x1B and 0x1C) or
- Frame Rate = Active edge of the TRIG input with SYNC_MODE[5:4](0x11) = 1.

Any combination of measurements can be enabled, but measurements are done in a numerical order inside a frame. For example, it is valid to enable MEAS1, MEAS2, and MEAS5 while MEAS3 and MEAS4 are skipped. But if a measurement of direct ambient is configured, then this measurement must be configured as the last measurement in the frame.

Figure 6 represents the timing diagram for one measurement with CDM enabled in each frame.

Figure 7 illustrates timing for six measurements in each frame. Each measurement can be configured independently using the PPG MEASx Setup register blocks (0x20 to 0x4E). Alternatively, all measurements share the same configuration of MEAS1 by setting MEAS1_CONFIG_SEL[0](0x13) to 1.

Figure 8 illustrates timing for six measurements in each frame with MEAS3 configured to have a burst average of 2. The result of MEAS3 in each frame only has one FIFO data pushed into FIFO per ADC channel. This FIFO data is the average of the two PD samples labeled as F1M3.

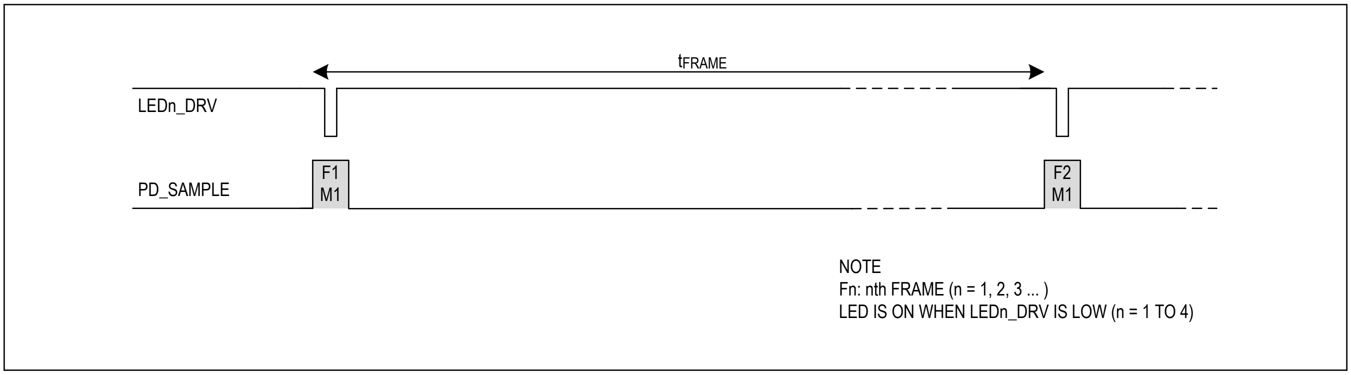


Figure 6. Frame with One Measurement

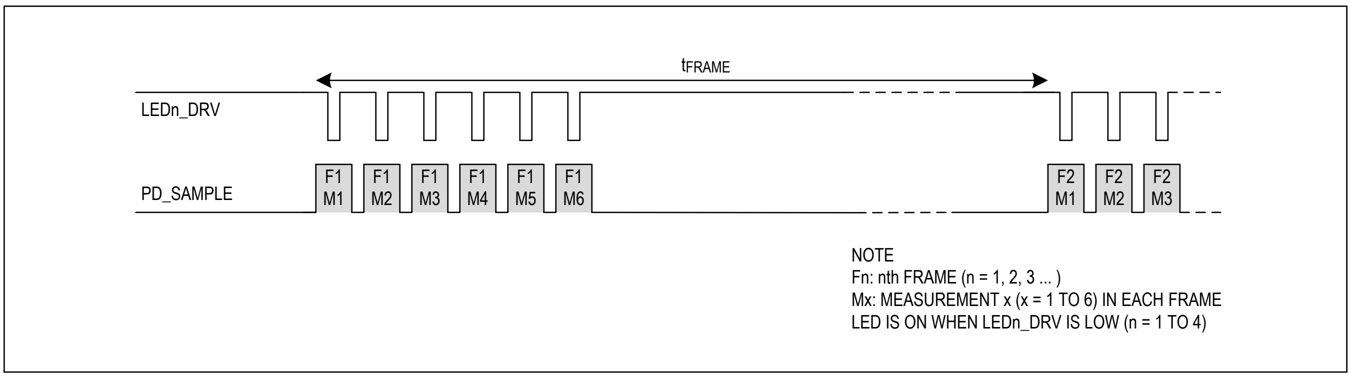


Figure 7. Frame with Six Measurements

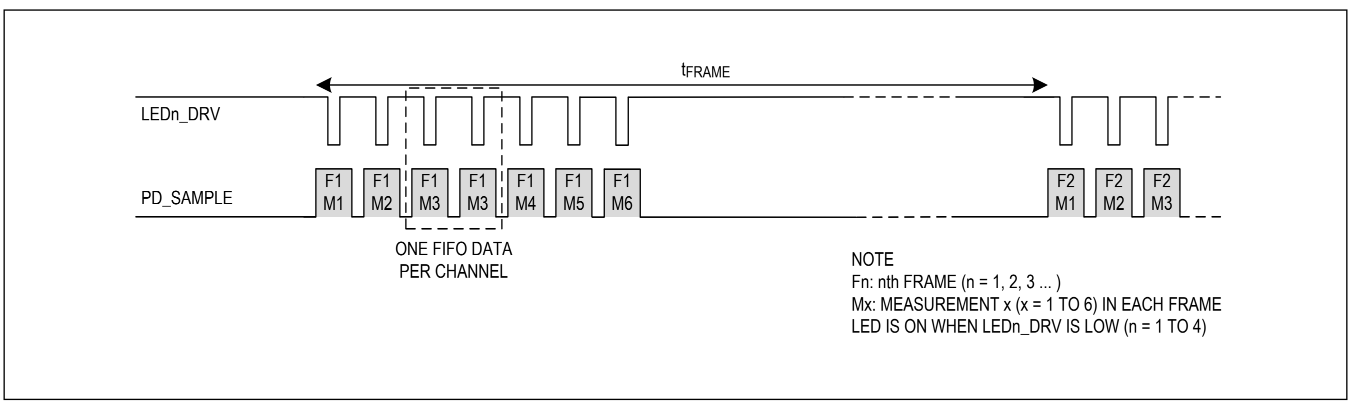


Figure 8. Frame with Measurement Burst Averaging

On-Chip Averaging

The MAX86174A/MAX86174B incorprote both burst average and decimation average on chip. Burst average applies to one measurement where a given number of LED bursts are fired. Decimation average is frame-based where a given number of measurements from successive frames are averaged, resulting in a lower FIFO data rate.

Burst Average

Burst average defines the number of LED exposures in one measurement and it is configured by the MEASx_AVER (x = 1 to 6) bit. Burst average works only with CDM, MEASx_FILT_SEL = 0. In each measurement, ($2^{(MEASx\_AVER +1)}$ + 1) ADC conversions of interleaved dark and exposure samples are made and the weighted computed average is fed to the digital low-pass filter. The example in Figure 9 has burst average of 2, MEASx_AVER = 0x1; hence, there are 5 conversions. When ambient-light cancellation is configured as FDM in a given measurement (MEASx_FILT_SEL = 1), only one dark ADC conversion and one exposure ADC conversion are done, regardless of the value of MEASx_AVER.

Note: MEASx_AVER[2:0] (x = 1–6) is in register 0x21, 0x29, 0x31, 0x39, 0x41, 0x49 and MEASx_FILT_SEL[6] (x = 1–6) is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A.

Burst averaging improves the exposure SNR. SNR benefits of the higher burst average ratio are shown in the *Typical Operating Characteristics* section. Besides, burst averaging can be used to improve ambient-light cancellation at the same LED power consumption level. For example, one application requires signal quality at MEASx_TINT = 117.1μs and burst average = 1x. Without increasing the LED illumination time, applying MEASx_TINT = 29.2μs but burst average = 4x can keep the exposure SNR the same and have better ambient cancellation at MEASx_TINT = 29.2μs.

Note: MEASx_TINT[4:3] (x = 1–6) is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

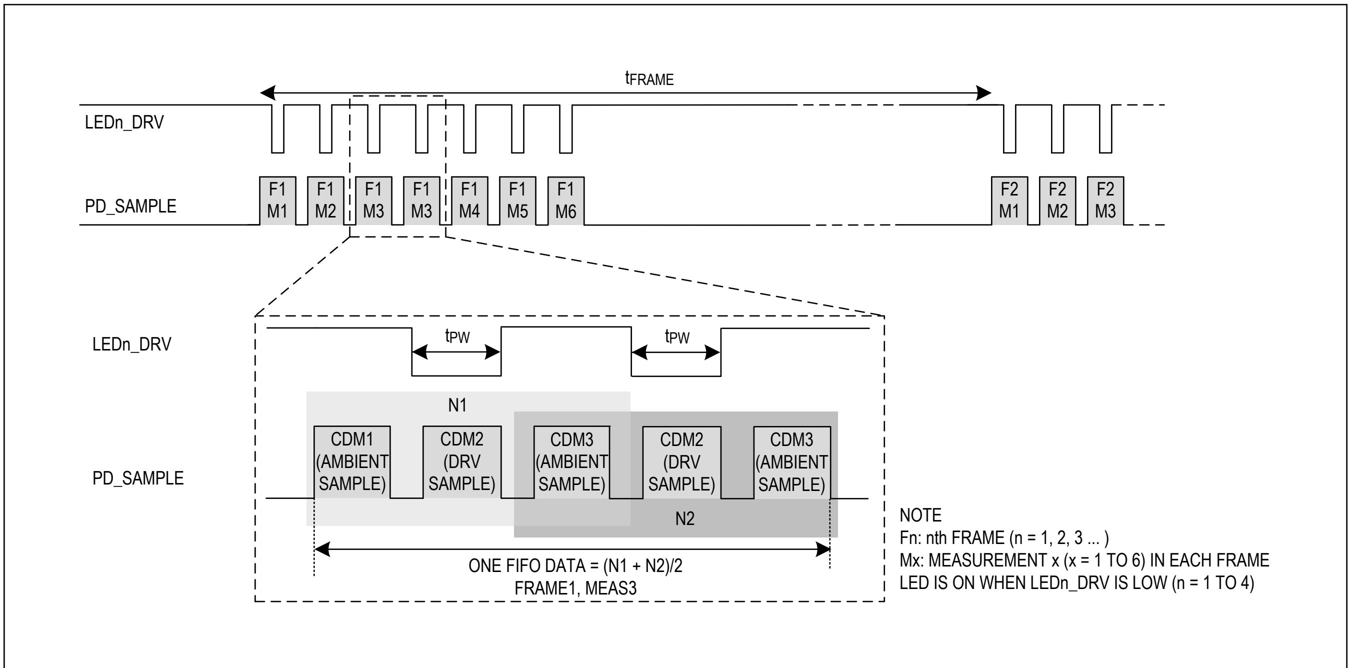


Figure 9. Illustration of Measurement with Burst Averaging

Decimation Average

Decimation averaging operates on multi-frames, which does not impact the LED exposure sequence nor front-end signal acquisition. It reduces the FIFO data rate. Figure 10 shows an example of a decimation average of 2.

Decimation averaging is integrated to reduce the data rate to FIFO in the digital low pass filter. See the *On-Chip Filtering* section for details.

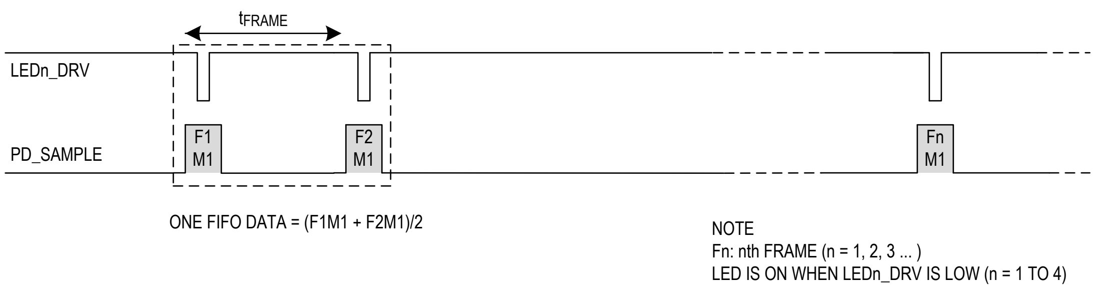


Figure 10. Frames with Decimation Average of 2

On-Chip Filtering

The MAX86174A/MAX86174B have two stages of on-chip filtering, decimation filtering at the ADC stage and digital low-pass filtering after the ADC stage.

ADC Decimation Filter

Users can select a second-order decimation filter (COI2), a third-order decimation filter (COI3), or SINC3 decimation filter. MAX86174A/MAX86174B by default use a third-order cascade of integrators (COI3) decimation filter. This filter provides excellent quantization, but only a 20dB/dec roll-off at higher frequencies. COI2 has a narrower bandwidth as compared to the COI3, which improves the PPG SNR by about 1dB to 2dB. The SINC3 filter has a better rollover (60dB/dec), and therefore, provides higher AC ambient-light cancellation at high frequencies and V_{LED} power-supply rejection. The SINC3 filter generates poor quantization performance and is, thus, only available on the longest integration time, MEASx_TINT = 0x3 (117.1µs). SINC3 is selected for each measurement individually by setting MEASx_SINC3_SEL to 1. To set the decimation filter to COI2 for all measurements, PPG_FILT2_SEL[7](0x14) is set to 1. Both SINC3 and COI2 can only be used with the longest integration time (MEASx_TINT = 0x3).

Note: MEASx_TINT[4:3] (x = 1–6) is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49 and MEASx_SINC3_SEL[7] (x = 1–6) is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A.

Table 3 shows the configuration for different ADC decimation filters. Combinations of the 3 parameters out of this table are not suggested.

Table 3. Configuration for ADC Decimation Filter

MEASx_SINC3_SEL	PPG_FILT2_SEL	MEASx_TINT	DECIMATION FILTER
0	0	All TINTs	COI3 (Default)
0	1	TINT = 0x3	COI2
1	0 or 1	TINT = 0x3	SINC3

See Figure 11 for the transfer function of different decimation filters.

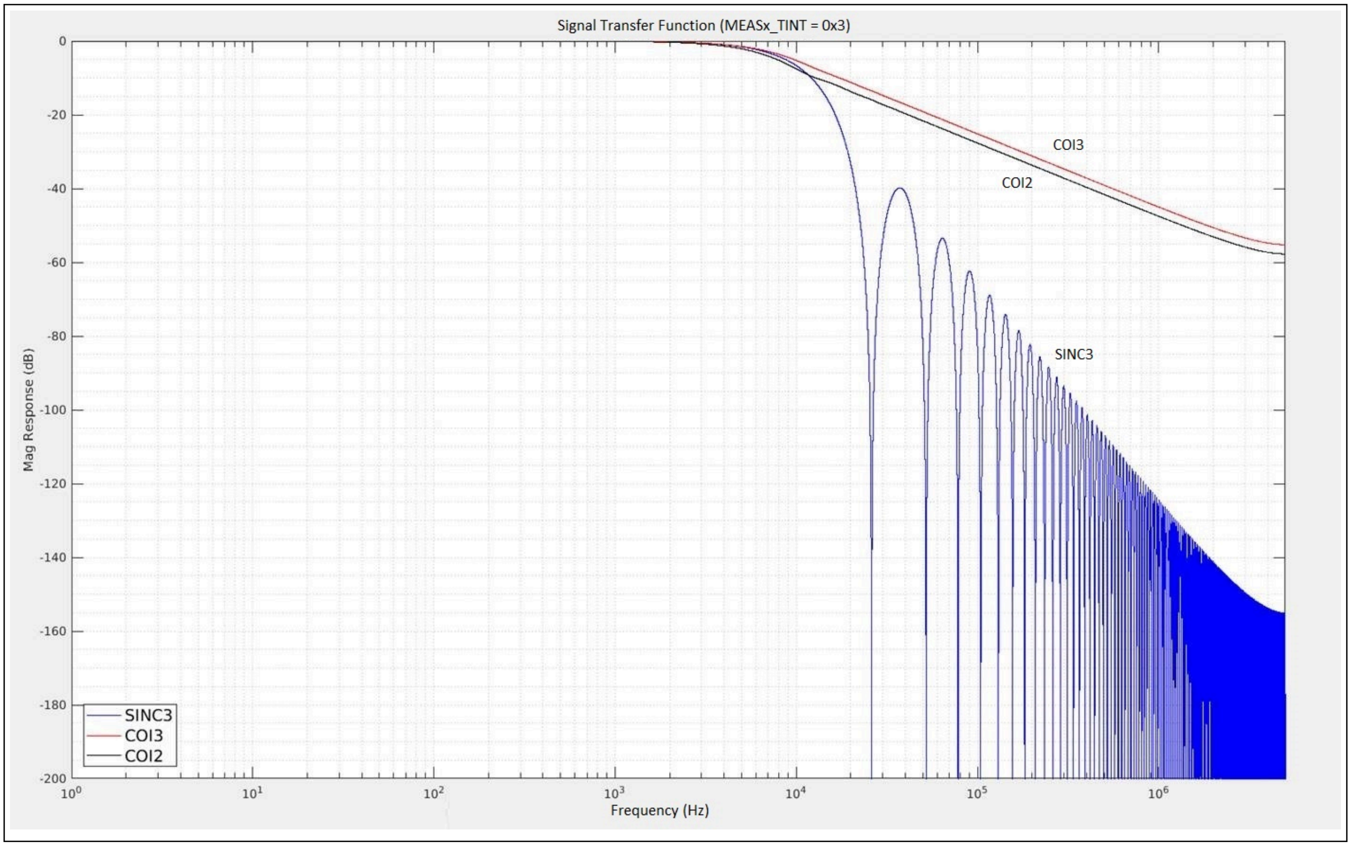


Figure 11. Signal Transfer Function of Decimation Filters

Digital Low-Pass Filter

The digital low-pass filter processes data before it gets saved in the FIFO. Users can either select an on-chip IIR filter or decimation averaging for low-pass filtering. The digital low-pass filter improves the SNR significantly. To enable digital low-pass filter, for all enabled measurements, DLPF_EN[5:4](0x14) is configured as needed. IIR filter configuration is programmed in IIR_CFG[3](0x14) and decimation averaging is set in DEC_AVE[2:0](0x14). The IIR cutoff frequency depends on the IIR_CFG bit. The decimation averaging option reduces the FIFO data rate by a factor of 2^{DEC_AVE}.

FIFO data rate = Frame rate x Number of enabled measurements x Number of enabled channels / 2^{DEC_AVE}.

AFE Exposure Control and SNR

MAX86174A/MAX86174B provide the options above to support extensive application scenarios that require different signal bandwidth and signal-to-noise (SNR) ratio. The Table 4 shows the SNR benefits when applying different parameters.

Table 4. Typical SNR Benefit Of Various Parameters

TINT (µs)	BURST AVERAGE	DAC OFFSET	COI2 FILTER	DIGITAL LPF	PEAK SNR (dB)	DIFFERENCE (dB)	BW (Hz)
14.6/117.1	1	0	OFF	OFF	83.9/91.6	+7.7	50
117.1	1/16	0	OFF	OFF	91.6/98.9	+7.3	50
117.1	1	0/28	OFF	OFF	91.6/94.1	+2.5	50
117.1	1	0	OFF/ON	OFF	91.6/92.7	+1.1	50

Table 4. Typical SNR Benefit Of Various Parameters (continued)

TINT (µs)	BURST AVERAGE	DAC OFFSET	COI2 FILTER	DIGITAL LPF	PEAK SNR (dB)	DIFFERENCE (dB)	BW (Hz)
117.1	1	0	OFF	OFF/ON	91.6/95.6	+4	11.5
117.1	1/16	0	ON	ON	96.5/101.6	+5.1	11.5
117.1	16	0/24	ON	ON	101.6/106.6	+5	11.5
117.1	16	24	ON	ON	106.6/111.8*	+5.2	0.5-4

* shows performance without/with an external band-pass filter (0.5-4Hz).

Threshold Detect Function

The MAX86174A/MAX86174B include a threshold detect function that enables users to detect ADC counts higher than a specified range or lower than a specified range.

The threshold detect function is used in proximity mode to reduce energy consumption and extend battery life when the sensor is not in contact with skin. There are two separate instances of the threshold detect function available in MAX86174A/MAX86174B, THRESHOLD1 and THRESHOLD2. Both are disabled by default.

The threshold detect function is enabled by selecting a measurement in THRESHx_MEAS_SEL(x = 1, 2) in register 0x50. For the dual channel MAX86174A, the threshold detect function is set up for either PPG1 or PPG2 by configuring THRESHx_PPG_SEL in register 0x51. In order to configure the threshold detect function, both an upper limit and a lower limit must be set. These can be configured in the PPG Threshold Interrupts registers (0x50 to 0x55).

In addition, two features are available to make the threshold detect function more adaptable for various system and application requirements. These are Time Hysteresis and Level Hysteresis, which are configurable through the TIME_HYST[4:3](0x51) and LEVEL_HYST[2:0] (0x51). Time hysteresis sets the number of consecutive samples that must be outside the limits defined by THRESHOLDx_UPPER and THRESHOLDx_LOWER in order to assert the threshold interrupt. Level hysteresis defines the sample variation around THRESHOLDx_UPPER and THRESHOLDx_LOWER. This value is in ADC counts and is applied at ±0.5 x LEVEL_HYST around THREHSOLDx_UPPER as well as ±0.5 x LEVEL_HYST around THRESHOLDx_LOWER. Specifically, in order for a threshold interrupt to be asserted, a sample must either transition above the THRESHOLDx_UPPER + 0.5 x LEVEL_HYST and stay above THRESHOLDx_UPPER - 0.5 x LEVEL_HYST for the number of samples defined in TIME_HYST or transition below THRESHOLDx_LOWER - 0.5 x LEVEL_HYST and stay below THRESHOLDx_LOWER + 0.5 x LEVEL_HYST for the number of samples defined in TIME_HYST as shown in Figure 12.

Note: THRESHOLD1_UPPER[7:0] is register 0x52, THRESHOLD2_UPPER is register 0x54, THRESHOLD1_LOWER is register 0x53, and THRESHOLD2_LOWER is register 0x55.

If a threshold detect function instance is enabled, the corresponding THRESHx_HILO interrupt bit (register 0x00) is asserted and threshold mode is activated when the ADC counts of the assigned measurement on the specified PPG channel drop below the lower limit, or exceed the upper limit (in consideration with LEVEL_HYST and TIME_HYST settings). The upper threshold check is disabled by setting THRESHx_UPPER (0x52, 0x54) to 0xFF. The PPG ADC reading, if negative, is clipped to 0x00000 before comparing with the threshold limits. Therefore, programming THRESHOLDx_LOWER to 0x00 effectively disables the lower threshold check.

Threshold detect function enables low power consumption while in automatic proximity detect mode. See the *Automatic Proximity Detect Mode* section for details. Alternatively, the LED configuration during the threshold detect active mode is determined by the firmware settings as needed for each application. Lower settings of LED current, ADC integration time, and frame rate result in reducing power consumption during situations when there is no reflective returned signal.

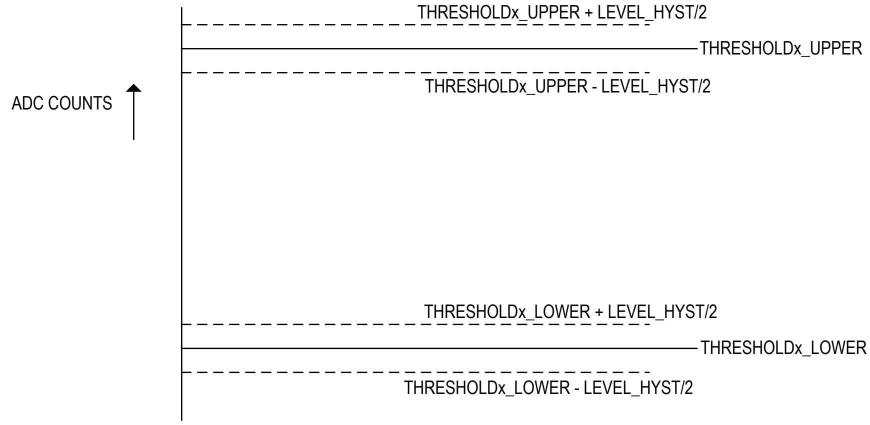


Figure 12. Threshold limits with LEVEL_HYST

Automatic Proximity Detect Mode

The MAX86174A/MAX86174B include a proximity detect function that switches the device automatically between proximity detect mode (PROX mode) and normal mode. Using the threshold detect function (see the *Threshold Detect Function* section), the proximity mode significantly reduces energy consumption; thereby, extending battery life when the device is in PROX mode.

When PROX_AUTO[2](0x13) is set to 1, PROX mode is enabled. In this mode, PPG measurement 6 (MEAS6) is reserved for proximity function and is automatically enabled even when MEAS6_EN[5](0x12) is programmed to 0. THRESHOLD1 is used for proximity detect, but THRESH1_MEAS_SEL[2:0](0x50) is ignored. Instead measurement 6 is considered for this threshold instance.

The device enters PROX mode when the measurement 6 ADC reading is is below the threshold determined by the THRESHOLD1_LOWER[7:0](0x53) register; otherwise, it is in normal mode. THRESHOLD1_UPPER[7:0](0x52) is not used. The device switches between PROX mode and normal mode automatically. While in PROX mode, the frame rate automatically changes to 8fps, and only measurement 6 is selected for ADC conversions. While in normal mode, measurement 6 and all the enabled measurements 1 to 5 are selected for ADC conversions, and the frame rate is as programmed in the FR_CLK_DIV[14:0](0x1B, 0x1C). In order to reduce power consumption while in PROX mode, MEAS6 LED drive current should be as low as possible. The LED current for MEAS6 is configured through MEAS6_DRVA_PA[7:0](0x4D) and MEAS6_DRVB_PA[7:0](0x4E).

If THRESH1_HILO interrupt is enabled using THRESH1_HILO_EN1[1](0x58), an interrupt is asserted on the INTB pin when the part switches from normal mode to PROX mode, and also for each ADC conversion while the part is in PROX mode. There is no interrupt when the part switches from PROX mode to normal mode.

In order to get an interrupt when switching from PROX mode to normal mode, a second threshold instance is enabled using the THRESH2_HILO_EN[2](0x58) interrupt enable bit. THRESHOLD2_UPPER[7:0](0x54) should be programmed to be equal to THRESHOLD1_LOWER, and THRESHOLD2_LOWER[7:0](0x55) should be zero. THRESH2_MEAS_SEL[6:4](0x50) should be programmed to select MEAS6. THRESH2_PPG_SEL[7](0x51) should be programmed the same as THRESH1_PPG_SEL[6](0x51). When configured this way, THRESHOLD2 generates an interrupt when switching from PROX mode to normal mode and does not generate an interrupt when the part switches from normal mode to PROX mode.

If it is desired to reduce the number of interrupts, the THRESH1_HILO interrupt should be enabled when the part is in normal mode, and THRESH2_HILO should be enabled when the part is in PROX mode. If interrupts are not needed for detecting switching between PROX and normal modes, Threshold 2 Interrupt registers do not need to be programmed.

False detection of PROX mode and normal mode can be avoided by enabling time hysteresis and level hysteresis through TIME_HYST[4:3](0x51) and LEVEL_HYST[2:0](0x51) in register 0x51 as needed. See the *Threshold Detect Function* section for more details on threshold interrupts.

Synchronization Modes

The MAX86174A/MAX86174B support three modes of frame-rate control. These modes can be selected through SYNC_MODE[5:4](0x11).

The three modes are an internally timed frame rate through an internal oscillator and divider, an externally timed frame rate through an external frame trigger input, and an externally timed frame rate through an external frame timing clock and the internal frame clock divider.

The three synchronization modes are explained in the following sections.

Table 5. Clock Sources in Each Synchronization Mode

SYNC_MODE	PPG ADC CLK	PPG FRAME RATE	PPG MEASUREMENT TIMING
0x0	Internal fast oscillator (10MHz)	Internal slow oscillator (32.768KHz)	Internal slow oscillator
0x1	Internal fast oscillator	External pulse on TRIG	Internal slow oscillator
0x2, 0x3	Internal fast oscillator	External pulse on TRIG	External pulse on TRIG

Internal Frame Oscillator and Divider Mode

SYNC_MODE = 0x0 or 0x3 is the free running mode of operation. In this mode, the MAX86174A/MAX86174B use the internal 32.768kHz oscillator, and the internal user programmable divider, FR_CLK_DIV[14:0](0x1B, 0x1C) to set the time between subsequent frames or the frame rate. ADC Sync signals are generated internally using the 10MHz ADC clock.

In this mode, TRIGLED4_SEL[0](0x17) must be set to 1 and TRIG_ICFG[0](0x16) is also ignored.

External Frame Trigger Input Mode

SYNC_MODE = 0x1 enables the TRIG input pin to be a start for a frame sync signal. A frame cycle begins upon receipt of an active edge on the TRIG input. This frame includes powering up and then executing each enabled measurement from MEAS1 to MEAS6. ADC Sync signals are generated internally using the10MHz ADC clock. The internal 32.768KHz frame clock is disabled.

External Frame Clock Input Mode

SYNC_MODE = 0x2 enables the TRIG input to be an external frame clock input. This input clock effectively replaces the MAX86174A/MAX86174B internal 32.768kHz oscillator. The MAX86174A/MAX86174B use the FR_CLK_DIV register value to divide this external clock input 32.0kHz/32.768kHz to generate the effective frame rate. ADC clock signals are generated internally using the 10MHz clock. However, in this case the stability of the frame rate is driven entirely by the external frame clock input.

Start of sampling process can be controlled by an SPI software Sync command, which zeros out the frame rate divider and restarts the frame counting process.The device then advances with the external TRIG input clock. Subsequent software sync commands abort the current frame and restart a new frame.

This mode is useful when the microcontroller can output the crystal based RTC clock on a GPIO pin; thereby, enabling the user to synchronize multiple sensors through the same oscillator.

FIFO Description

The FIFO holds a maximum of 256 samples and supports various data types. Each sample in the FIFO is 3 bytes wide and includes a tag and data. FIFO_DATA[23:20] contain the tag that identifies the source of each sample data. Data in FIFO_DATA[23:0] is right justified for all data types. FIFO_DATA[19:0] contain the data in two's complement form. The MSB of the PPG data FIFO_DATA[19:0] is the sign bit. Table 6 shows each data type in the FIFO along with the associated tag for MAX86174A/MAX86174B.

The sequencing of exposures is controlled by MEAS1_EN through MEAS6_EN bits in the System Configuration 2 register. The ADC conversion sequence cycles through the enabled measurements starting from MEAS1.

When COLLECT_RAW_DATA[1](0x13) is set to 0, the computed data is saved as a single MEASx sample in the FIFO. When COLLECT_RAW_DATA is set to 1, the exposure sample and the dark (ambient) sample(s) are saved as separate samples in the FIFO (see the *Ambient Rejection* section). The raw exposure sample is tagged with its corresponding

MEASx (x = 1 to 6) and PPGy (y = 1, 2 for MAX86174A and y = 1 for MAX86174B) tag, but all dark samples are tagged with the same DARK tag which is common to all measurements.

Table 6. FIFO Tags

TAG[3:0]	DATA TYPE	DATA[19:0]
0x0	MEAS 1 PPG1	Measurement 1 ADC1 data
0x1	MEAS 2 PPG1	Measurement 2 ADC1 data
0x2	MEAS 3 PPG1	Measurement 3 ADC1 data
0x3	MEAS 4 PPG1	Measurement 4 ADC1 data
0x4	MEAS 5 PPG1	Measurement 5 ADC1 data
0x5	MEAS 6 PPG1	Measurement 6 ADC1 data
0x6	MEAS 1 PPG2	Measurement 1 ADC2 data (MAX86174A only)
0x7	MEAS 2 PPG2	Measurement 2 ADC2 data (MAX86174A only)
0x8	MEAS 3 PPG2	Measurement 3 ADC2 data (MAX86174A only)
0x9	MEAS 4 PPG2	Measurement 4 ADC2 data (MAX86174A only)
0xA	MEAS 5 PPG2	Measurement 5 ADC2 data (MAX86174A only)
0xB	MEAS 6 PPG2	Measurement 6 ADC2 data (MAX86174A only)
0xC	PPG1/2 DARK	Dark data when COLLECT_RAW_DATA = 1
0xD	PPG1/2 ALC OVF	ALC overflow detected. Location of data indicates the measurement and the photodiode.
0xE	PPG1/2 EXP OVF	Exposure overflow detected. Location of data indicates the measurement and the photodiode.
	Marker	11111111111111111110 (0xFFFFE)
	Invalid data	11111111111111111111 (0xFFFFF)

When both ALC overflow and exposure overflow are detected on the same measurement, the sample is tagged with the ALC OVF tag. An attempt to read an empty FIFO returns the INVALID_DATA tag.

MAX86174A/MAX86174B provide a feature of saving a FIFO marker when needed in an application. For example, in order to distinguish data saved in FIFO before and after a configuration change, a marker can be saved in the FIFO just before the configuration change. The marker tag is 24 bits and it is 0xFFFFFE.

Setting FIFO_MARK[5](0x09) to 1 saves the marker tag in the FIFO.

For details on FIFO configuration, see the *Register Map* (register 0x03 to 0x09).

FIFO configuration is best explained by a few examples.

Example 1: Single channel optical measurement using MAX86174B.

Assume it is desired to perform an SpO_2 measurement and also monitor the ambient level on the photodiode to adjust the IR and red LED intensity using a single optical channel with photodiodes 1 and 2 selected for PPG1. To perform this measurement, configure the following registers.

```
//System Configuration
        MEAS1_EN = 0b1          //enable measurement 1, 2, and 3
        MEAS2_EN = 0b1
        MEAS3_EN = 0b1
//Measurement 1 Setup
        MEAS1_AMB = 0b0         //Ambient measurement off
        MEAS1_DRVA = 0b00       //LED Driver A driving IR LED on LED1_DRV
        MEAS1_AVER as desired   //Number of LED pulses in each frame
        MEAS1_PPG_TINT as desired  //ADC integration time control
        MEAS1_PDSEL = 0b00      //Photodiode 1 and 2 selected on PPG channel 1
        MEAS1_PPG1_ADC_RGE as desired//ADC range control for PPG1 ADC
```

```
        MEAS1_LED_SETLNG as desired  //LED settling time
        MEAS1_PD_SETLNG as desired   //Settling time for photodiode
        MEAS1_DRVA_PA as desired     //LED driver A current driving the IR LED on LED1_DRV
        MEAS1_DRVB_PA = 0x00         //LED driver B current should be set to 0
    //Measurement 2 Setup
        MEAS2_AMB = 0b0              //Ambient measurement off
        MEAS2_DRVB= 0b01             //LED Driver B driving red LED on LED2_DRV
        MEAS2_AVER as desired        //Number of LED pulses in each frame
        MEAS2_PPG_TINT as desired    //ADC integration time control
        MEAS2_PDSEL = 0b00           //Photodiode 1 and 2 selected on PPG channel 1
        MEAS2_PPG1_ADC_RGE as desired//ADC range control for PPG1 ADC
        MEAS2_LED_SETLNG as desired  //LED settling time
        MEAS2_PD_SETLNG as desired   //Settling time for photodiode
        MEAS2_DRVA_PA = 0x00         //LED driver A current should be set to 0
        MEAS2_DRVB_PA as desired     //LED driver B current driving the red LED on LED2_DRV
    //Measurement 3 Setup
        MEAS3_AMB = 0b1              //Ambient measurement selected
        MEAS3_PPG_TINT as desired    //ADC integration time control
        MEAS3_PDSEL = 0b00           //Photodiode 1 and 2 selected on PPG channel 1
        MEAS3_PPG1_ADC_RGE as desired//ADC range control for PPG1 ADC
        MEAS3_PD_SETLNG as desired   //Settling time for photodiode
```

With this configuration the sample sequence and the data format in the FIFO follows the following time/location sequence.

```
tag 0, Measurement 1 PPG1 (sample from IR LED)
tag 1, Measurement 2 PPG1 (sample from red LED)
tag 2, Measurement 3 PPG1 (ambient sample)
tag 0, Measurement 1 PPG1 (sample from IR LED)
tag 1, Measurement 2 PPG1 (sample from red LED)
tag 2, Measurement 3 PPG1 (ambient sample)
... tag 0, Measurement 1 PPG1 (sample from IR LED)
tag 1, Measurement 2 PPG1 (sample from red LED)
tag 2, Measurement 3 PPG1 (ambient sample)
```

For a second example, assume it is desired to pulse IR LED and RED LED simultaneously while also monitoring the ambient level.

```
    System Configuration
        MEAS1_EN = 1'b1        (IR LED and RED LED exposure)
        MEAS2_EN = 1'b0        (NONE)
        MEAS3_EN = 1'b0        (NONE)
        MEAS4_EN = 1'b1        (DIRECT AMBIENT exposure)
        MEAS5_EN = 1'b0        (NONE)
        MEAS6_EN = 1'b0        (NONE)
    Measurement 1 Setup (IR LED on LED DRVA on pin 1, RED LED on LED DRVB on pin 3)
        MEAS1_AMB = 1'b0        (Ambient measurement off)
```

MEAS1_DRVA= 2'b00 (LED Driver A on LED1_DRV and Current is non-zero)

MEAS1_DRVB= 2'b10 (LED Driver B on LED3_DRV and Current is non-zero)

MEAS1_PPG1_ADC_RGE[1:0] (PPG1 Gain Range Control)

MEAS1_PPG2_ADC_RGE[1:0] (PPG2 Gain Range Control)

MEAS1_PPG_TINT[1:0] (LED Pulse Width Control)

MEAS1_DRVA_PA[7:0] = 8'h0B (LED Driver A Current)

MEAS1_DRVB_PA[7:0] = 8'h0E (LED Driver B Current)

Measurement 4 Setup (Ambient measurement)

MEAS4_AMB = 1'b1 (Ambient measurement selectedf)

MEAS4_DRVA= 2'b00 (Don't Care because MEAS4_AMB = 1)

MEAS4_DRVB= 2'b00 (Don't Care because MEAS4_AMB = 1)

MEAS4_PPG1_ADC_RGE[1:0] (PPG1 Gain Range Control)

MEAS4_PPG2_ADC_RGE[1:0] (PPG2 Gain Range Control)

MEAS4_PPG_TINT[1:0] (LED Pulse Width Control)

In this case, the sequencing in the FIFO is,

tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG 1 Ambient data
tag 4, PPG 2 Ambient data
tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG1 Ambient data
tag 4, PPG2 Ambient data
... tag 1, PPG1 IR+RED data
tag 1, PPG2 IR+RED data
tag 4, PPG1 Ambient data
tag 4, PPG2 Ambient data

where:

PPGy IR_RED data = Ambient corrected exposure data from IR and RED for optical channel y

PPGy Ambient data = Direct ambient corrected sample for optical channel y

y is 1 for optical channel 1, and 2 for optical channel 2

The number of bytes of data for the two optical channels in one frame is given by: 2 x 3 x N where:

N = Number of measurements enabled in each frame

To calculate the number of data items available in the FIFO one can perform the following pseudo-code:

```
read the OVF_COUNTER register
read the FIFO_DATA_COUNT registers
if OVF_COUNTER == 0 //no overflow occurred
   NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
   NUM_AVAILABLE_SAMPLES = 256   // overflow occurred and data has been lost
endif
```

It is important to flush the FIFO after SW_FORCE_SYNC. When a frame is aborted, for example due to the

SW_FORCE_SYNC command, a new frame starts. But part of the frame before the SW_FORCE_SYNC command might have already been saved in the FIFO. Therefore, data alignment for the two optical channels might be lost.

Digital Interface

The MAX86174A/MAX86174B support both I^2C and SPI interfaces. The I2C_SEL pin selects between the two interfaces. When I2C_SEL is pulled high, the interface is in the I^2C mode and idles looking for a start condition on the SCL and SDA pins while the SPI interface is held in a reset state. When I2C_SEL is pulled low, the I^2C interface is disabled and the SPI interface is activated with the SDO pin going active. In the following sections both interface timings and protocols are described.

SPI/I^2C Selection for Serial Interface

MAX86174A/MAX86174B can be configured to use either I^2C or SPI for serial communication with an external host. When the CSB/I2C_SEL pin is high, the device is in I^2C mode. When the CSB/I2C_SEL pin is low, the device is in SPI mode. Immediately after power up, either I^2C or SPI can be used to do any read/write transaction if the host drives the CSB/I2C_SEL pin.

If the application uses I^2C for serial communication, the I2C_SEL (CSB) input pin is permanently tied to '1.' The SCL (SCLK) and SDA (SDI) pins are used for serial communication using I^2C for reading from and writing to registers. In I^2C mode, ADDR (SDO) is an input pin and is used for I^2C address select as shown in Table 7.

Table 7. Slave Addresses for I^2C Mode

ADDR	WRITE ADDRESS	READ ADDRESS
0	0xD4	0xD5
1	0xD6	0xD7

If the application uses SPI for serial communication, after power up the host should use the SPI interface to disable the I^2C interface by writing 1 to the DISABLE_I2C[7](0x11). The SCLK (SCL), SDI (SDA), SDO (ADDR), and CSB (I2C_SEL) pins are used for serial communication using SPI for reading from and writing to any other registers. In this mode, the SDO (ADDR) pin is an output pin and has a pullup. When idle or during SPI write transactions, this pin is in a high impedance state (Hi-Z). For SPI read, this pin is in a Hi-Z state during the address and command phases, and is driven high or low during the read phase.

SPI Interface

The SPI interface on the MAX86174A/MAX86174B is SPI-/QSPI-/Microwire-/DSP-compatible consisting of a serial data input (SDI), a serial data output (SDO), a serial clock line (SCLK), and a chip select (CSB). In SPI mode, the SDI/SDA pin operates as SDI and the SCLK/SCL pin operates as SCLK. The timing of the SPI interface is shown in Figure 13. Data is strobed on the SCLK rising edge while clocked out on the SCLK falling edge. All single-word SPI read and write operations are done in a 3-byte, 24-clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one-byte register address, A[7:0], followed by a one-byte command word, which defines the transaction as write or read, followed by a single-byte data word either written to or read from the register location provided in the first byte.

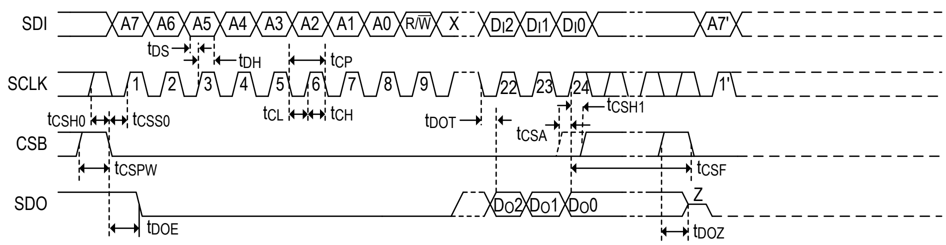


Figure 13. Detailed SPI Timing Diagram

Single Word SPI Register Read and Write Transactions

SPI Write mode operations are executed on the 24th SCLK rising edge using the first three bytes of data available. In write mode, any data supplied after the 24th SCLK rising edge is ignored as shown in Figure 14. Subsequent writes require CSB to deassert high and then assert low for the next write command. A rising CSB edge preceding the 24th rising edge of SCLK by t_{CSA} as shown in Figure 13, results in the transaction being aborted.

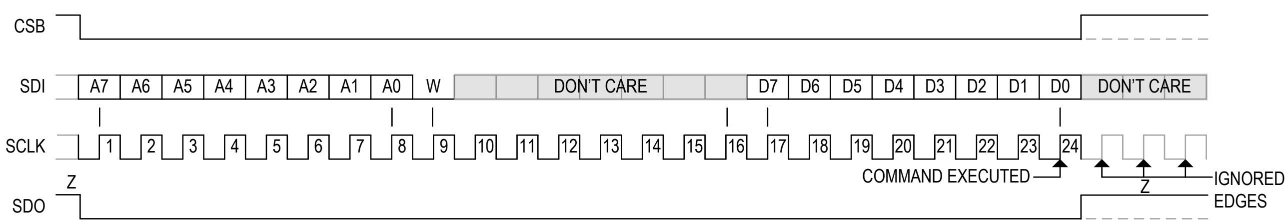


Figure 14. SPI Write Transaction

Read mode operations access the requested data on the 16th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the microcontroller to latch the data MSB on the 17th SCLK rising edge as shown in Figure 15. Configuration and status registers are available using normal-mode read-back sequences. FIFO reads must be done with a burst mode FIFO read (see the *SPI Burst Mode Read Transaction* section). In a normal read sequence, any SCLK rising edges after the 24th SCLK rising edge are ignored and if more than 24 SCLK rising edges are provided the device reads back zeros.

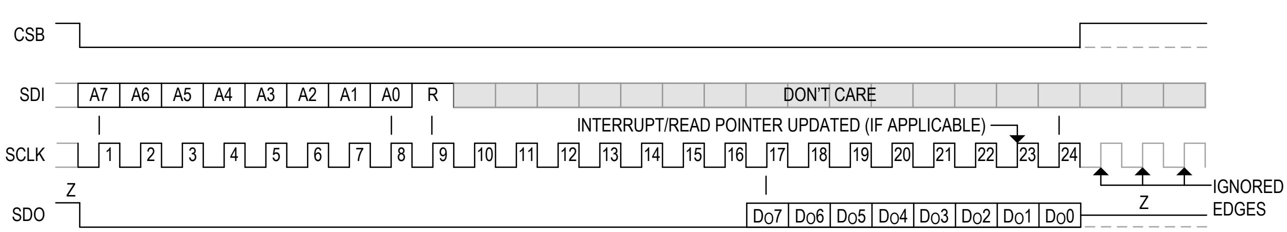


Figure 15. SPI Read Transaction

SPI Burst Mode Read Transaction

The MAX86174A/MAX86174B have a FIFO burst read mode to increase data transfer efficiency. The first 16 SCLK cycles operate exactly as described for normal read mode—the first byte being the register address, the second being a read command. The subsequent SCLKs consist of FIFO data, 24 SCLKs per word. All words in the FIFO should be read with a single-FIFO burst-read command.

Each FIFO sample consists of 3 bytes per sample, and thus, requires 24 SCLKs per sample to readout. The first byte (SCLK 17 to 24) consists of a tag indicating the data type of the subsequent bits as well as the MSBs of the data. The next two bytes (SCLK 24 to 40) consist of data. For example, Figure 16 shows a FIFO burst read consisting of three PPG samples in FIFO, labeled A through C, each with a 4-bit tag and 20-bit data. The number of words in the FIFO depends on the FIFO configuration. See the *FIFO Description* section for more details the FIFO configuration and readout.

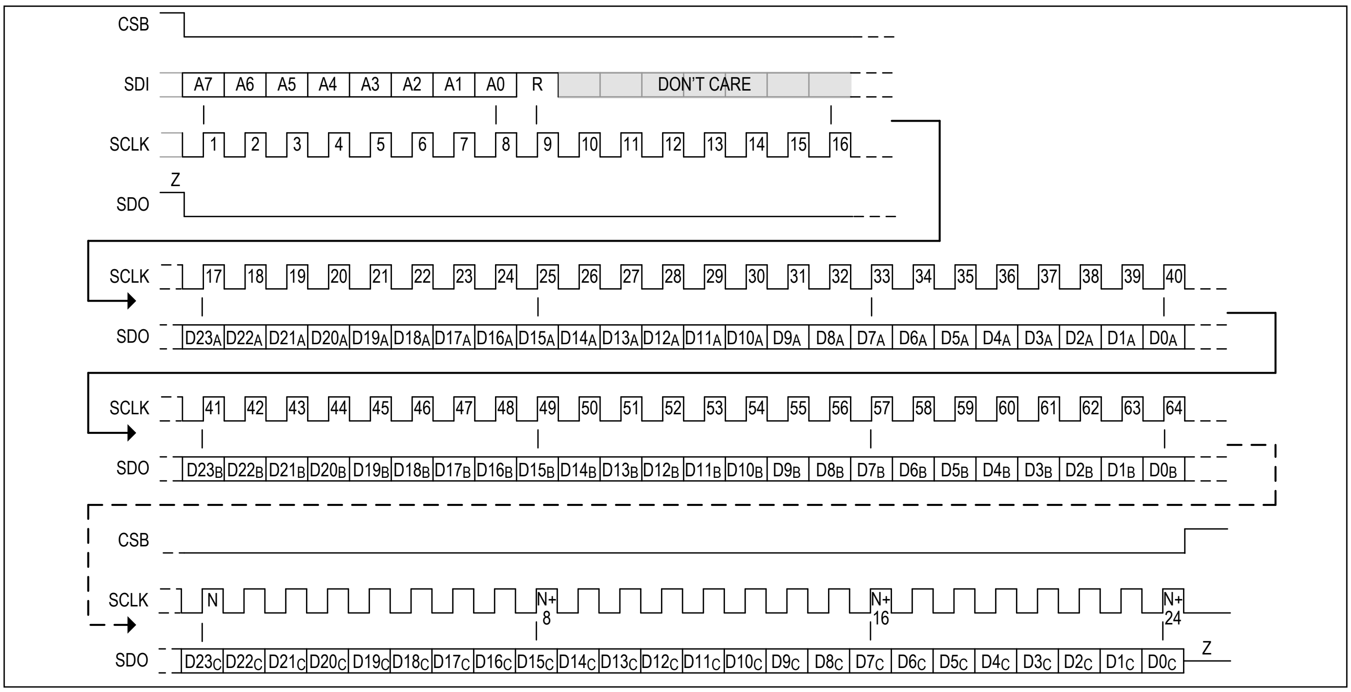


Figure 16. SPI FIFO Burst Mode Read Transaction

I2C-/SMBus-Compatible Serial Interface

The I2C interface on the MAX86174A/MAX86174B is an I2C-/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). In I2C mode, the SDI/SDA pin operates as SDA and the SCLK/SCL pin operates as SCL. These two pins are used for the communication between the MAX86174A/MAX86174B and the master at clock rates up to 400kHz. Figure 17 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX86174A/MAX86174B by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX86174A/MAX86174B is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX86174A/MAX86174B transmits the proper slave address followed by a series of nine SCL pulses. The MAX86174A/MAX86174B transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge (NACK), and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

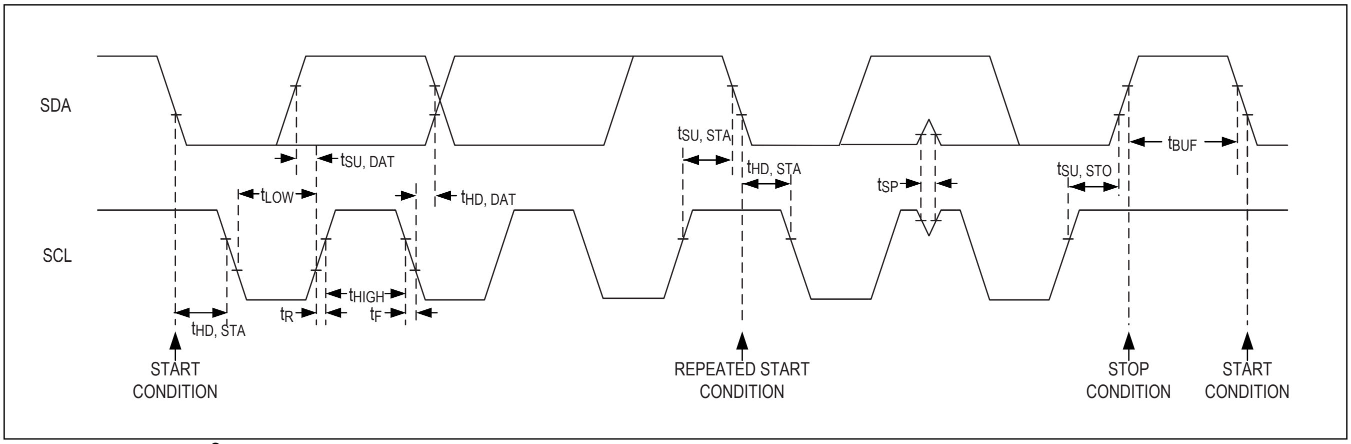


Figure 17. Detailed I^{2}C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition, which indicates the beginning of a transmission. A START condition is a high-to-low transition on SDA while SCL is high as shown in Figure 18. The master terminates transmission, and frees the bus, by issuing a STOP condition. A STOP condition is a low-to-high transition on SDA while SCL is high as shown in Figure 18. The bus remains active if a REPEATED START condition is generated instead of a STOP condition. A REPEATED START condition is the same as a START condition (high-to-low transition with SCL high), but it is sent after a START condition.

The MAX86174A/MAX86174B recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

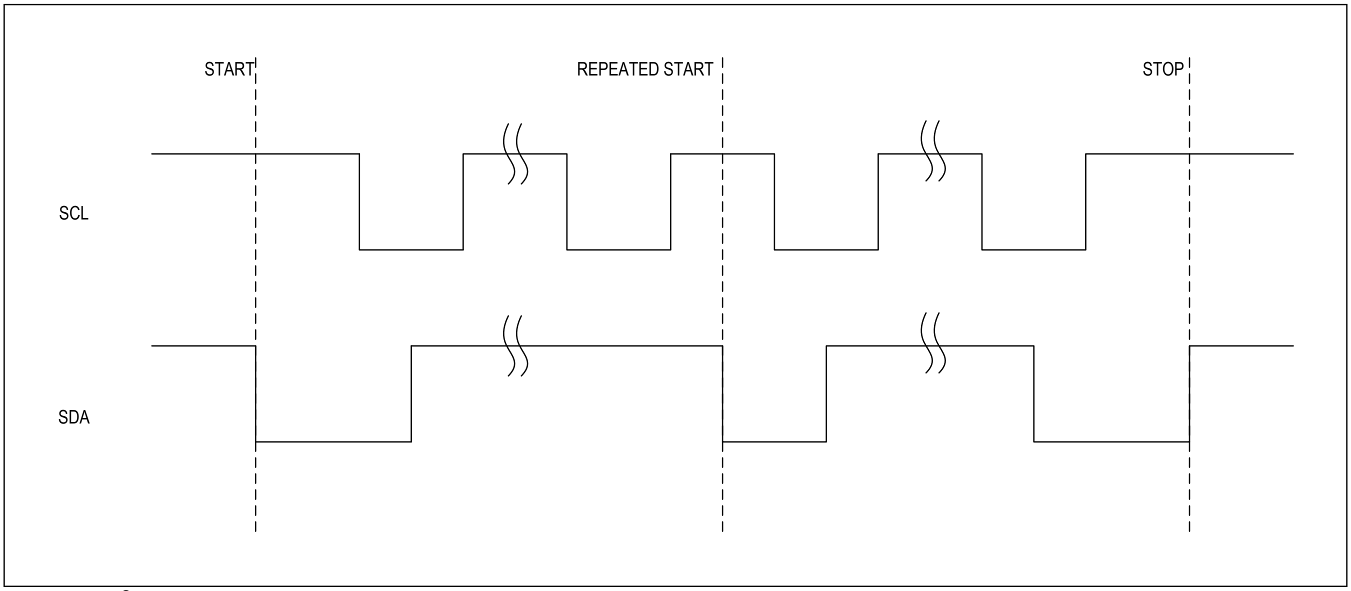


Figure 18. I²C START, STOP, and REPEATED START Conditions

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX86174A/MAX86174B use to handshake receive each byte of data when in write mode as shown in Figure 19. The MAX86174A/MAX86174B pulldown SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86174A/MAX86174B is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX86174A/MAX86174B, followed by a STOP condition.

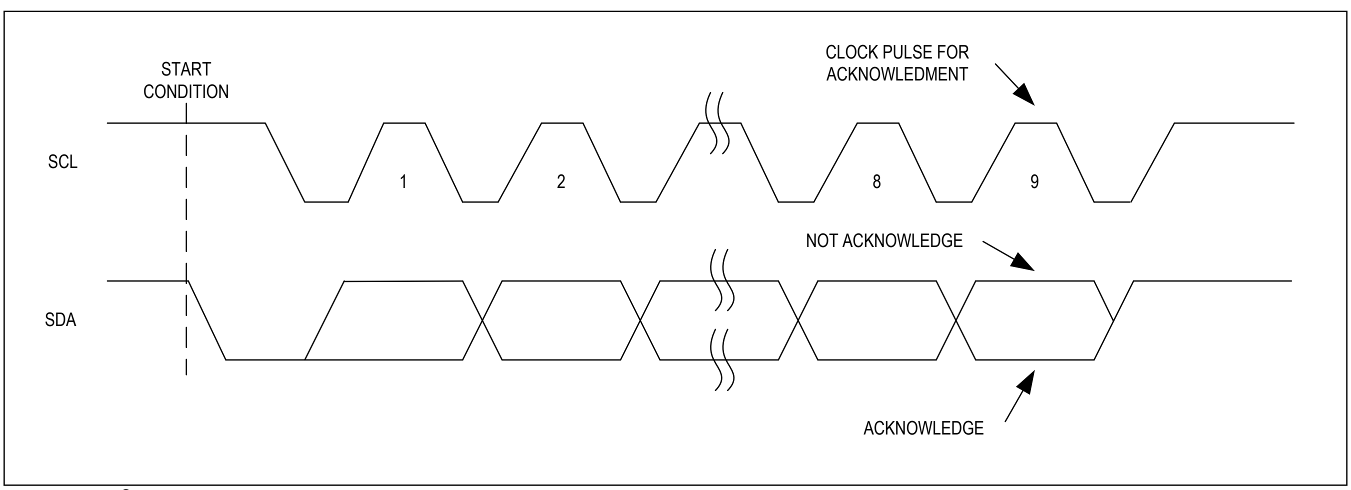


Figure 19. I²C Acknowledge Bit

I²C Write Data Format

A write to the MAX86174A/MAX86174B includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 20 illustrates the proper frame format for writing one byte of data. Figure 21 illustrates the frame format for writing multiple bytes of data.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX86174A/MAX86174B. The MAX86174A/MAX86174B acknowledge receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the internal register address pointer of the MAX86174A/MAX86174B. The pointer tells the MAX86174A/MAX86174B where to write the next byte of data. An acknowledge pulse is sent by the MAX86174A/MAX86174B upon receipt of the address pointer data.

The third byte sent to the MAX86174A/MAX86174B contains the data to be written to the pointed register. An acknowledge pulse from the MAX86174A/MAX86174B signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The auto-increment feature is disabled when there is an attempt to write to the FIFO Data register(0x0C).

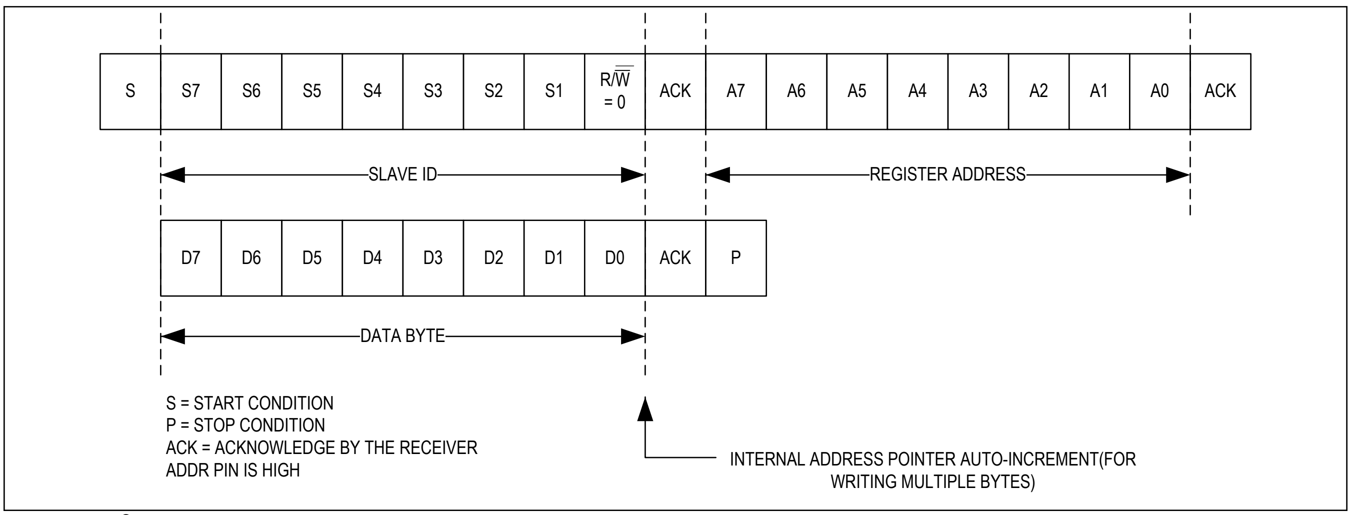


Figure 20. I²C Single Byte Write Transaction

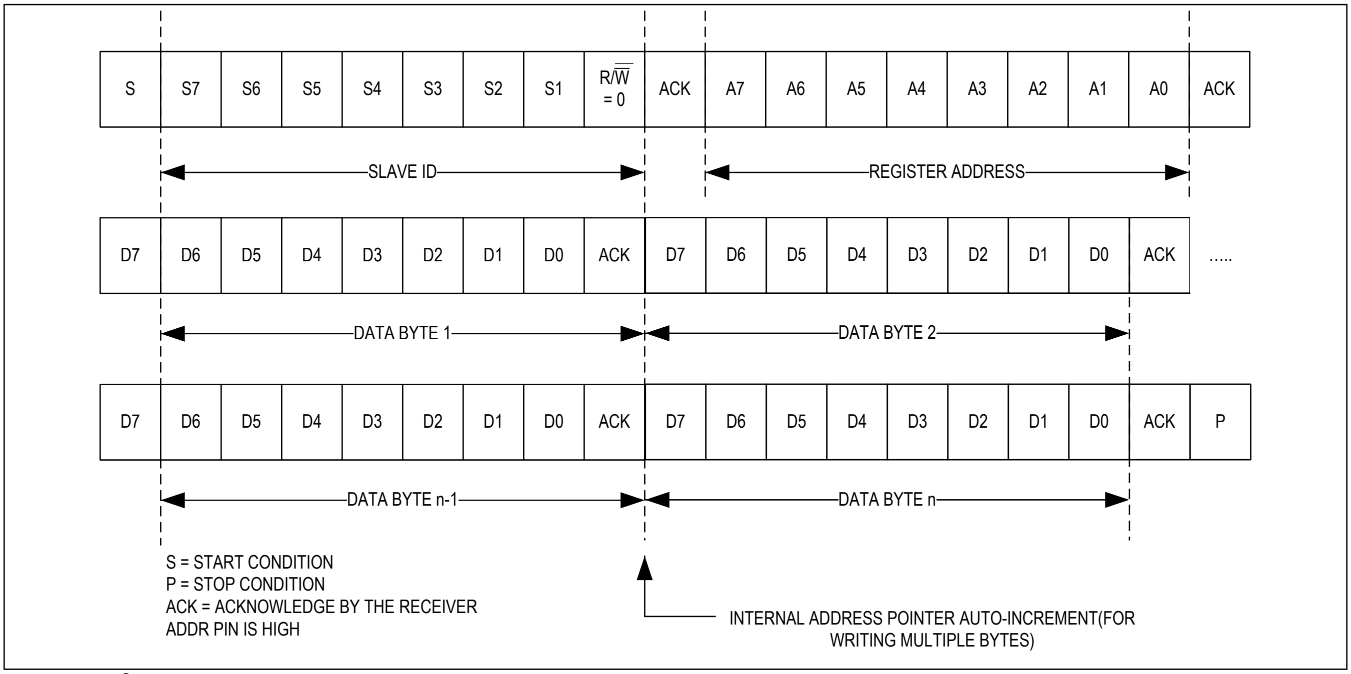


Figure 21. I²C Multi-Byte Write Transaction

I²C Read Data Format

A read from the MAX86174A/MAX86174B includes sending the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX86174A/MAX86174B acknowledges receipt of the slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX86174A/MAX86174B has the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto-increment feature is disabled when there is an attempt to read from the FIFO Data register (0x07). A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX86174A/MAX86174B slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX86174A/MAX86174B then transmit the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 22 illustrates the frame format for reading one byte from the MAX86174A/MAX86174B. Figure 23 illustrates the frame format for reading multiple bytes from the MAX86174A/MAX86174B.

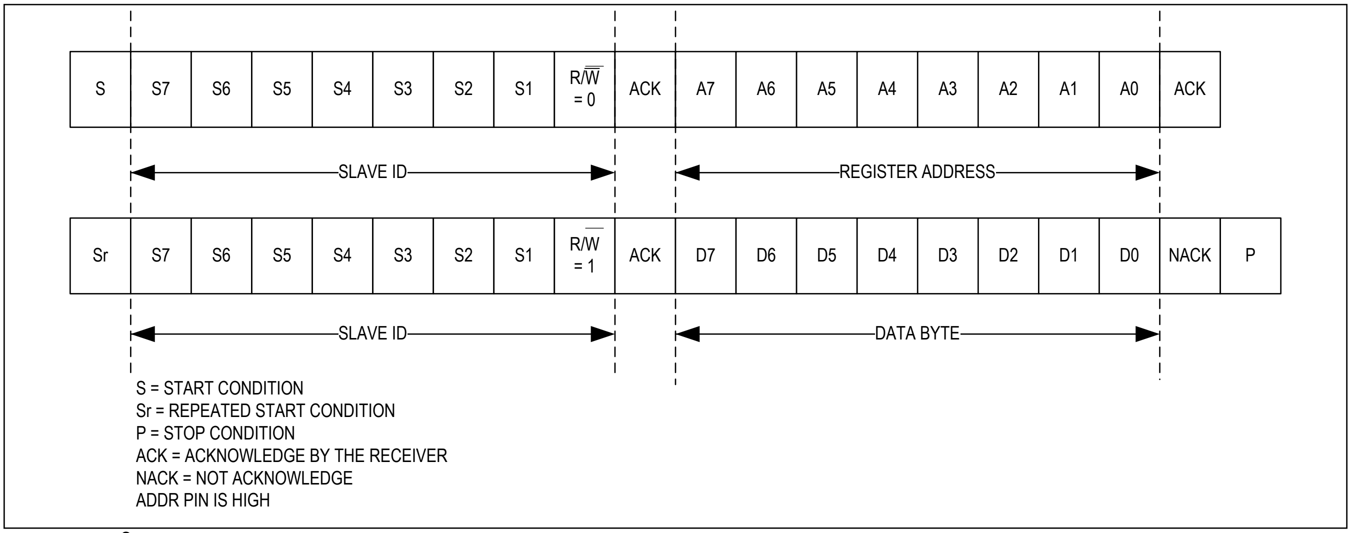


Figure 22. I²C Single Byte Read Transaction

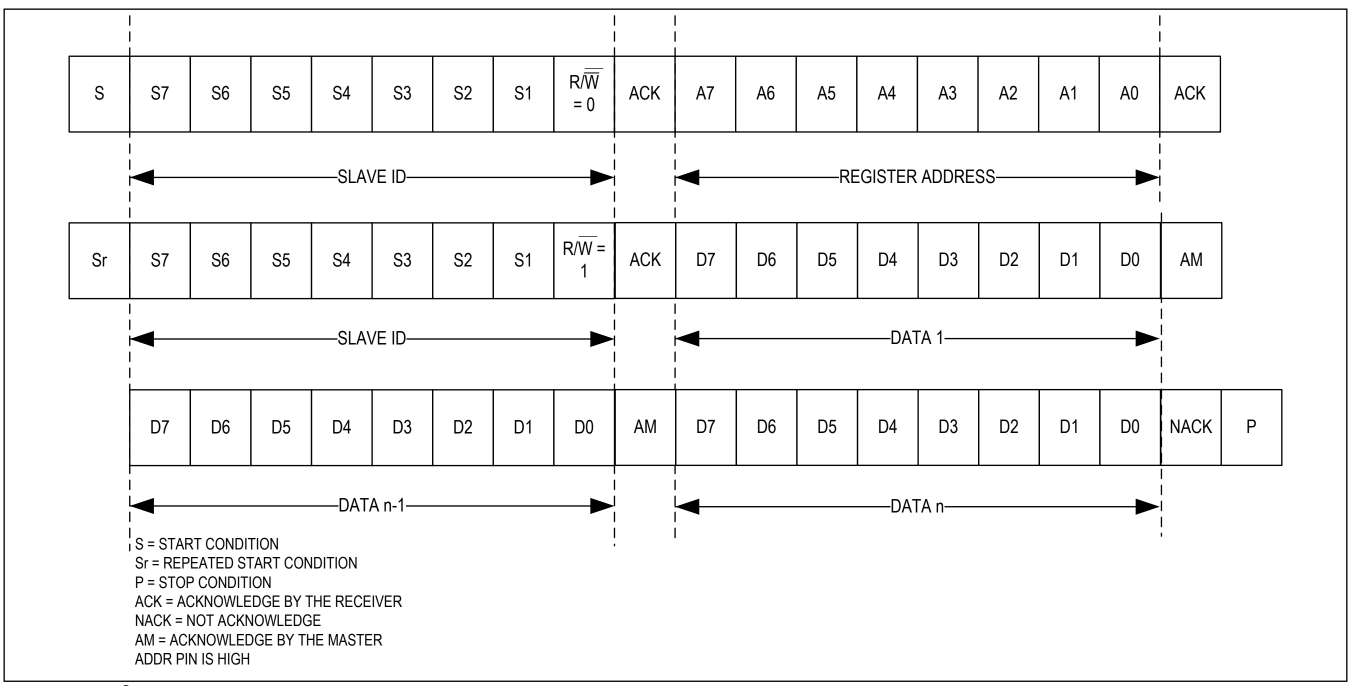


Figure 23. I²C Multi-Byte Read Transaction

I²C Broadcast

The MAX86174A/MAX86174B provide a feature of I²C broadcast write transactions to multiple devices simultaneously using the I²C serial interface. The host microcontroller uses the address programmed in I2C_BCAST_ADDR[7:1](0x18) to send a write command to multiple devices and the slave devices respond with an ACK. To use the broadcast feature, I2C_BCAST_EN[0[(0x18) must be set to 1.

This feature is especially useful for:

1. Synchronizing PPG ADC conversion on multiple devices using the SW_FORCE_SYNC bit.
2. Programming same configuration to multiple devices at the same time.

Read transactions in broadcast mode are not supported. If a host sends out a read command using the I^2C broadcast address, the device responds with a NACK.

Layout Guidelines

MAX86174A/MAX86174B is a high dynamic range analog front-end (AFE) and its performance can be adversely impacted by the physical printed circuit board (PCB) layout. It is recommended that all bypass recommendations in the *Pin Description* table be followed, and it is recommended that GND and PGND be shorted to a single PCB ground plane.

The V_{DD} pin should be decoupled with a 0.1μF or larger ceramic chip capacitor to the PCB Ground plane. In addition, the VREF pin should be decoupled to the PCB Ground plane with a 1.0μF ceramic capacitor. The voltage on the VREF pin is nominally 1.21V, so a 6.3V-rated ceramic capacitor should be adequate for this purpose. It is recommended that all decoupling capacitors use individual vias to the PCB Ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

The most critical aspect of the PCB layout of MAX86174A/MAX86174B is the handling of the PDm_IN (m = 1, 2) nodes. Parasitic capacitive coupling to the PDm_IN can result in additional noise being injected into the MAX86174A/MAX86174B front-end. To minimize external interference coupling to PD_IN, it is recommended the PD_IN node be fully shielded by the pseudo PD_GND node. An example of this recommendation is shown below. In the three layers shown, the PDm_IN node is shielded with a coplanar pseudo PD_GND trace on the top layer (Figure 24), the layer on which the MAX86174A/MAX86174B is mounted. On the bottom layer (Figure 26), the photodiode cathode is entirely shielded with the pseudo PD_GND shield, which is also the photodiode anode. Note also that the PD_GND shield also extends below the photodiode. This is done because in most photodiodes, the cathode is the bulk of the silicon. Thus, shielding beneath the photodiode terminates the capacitance to the bulk or cathode side to the reference node, PD_GND. On the layer just above the bottom, layer 5 in this case (Figure 25), the section of the GND plane has been opened up, connected to PD_GND to shield the PD_IN node below the photodiode cathode contact. Finally, the pseudo PD_GND should only be attached to the AFE GND pin in only one point.

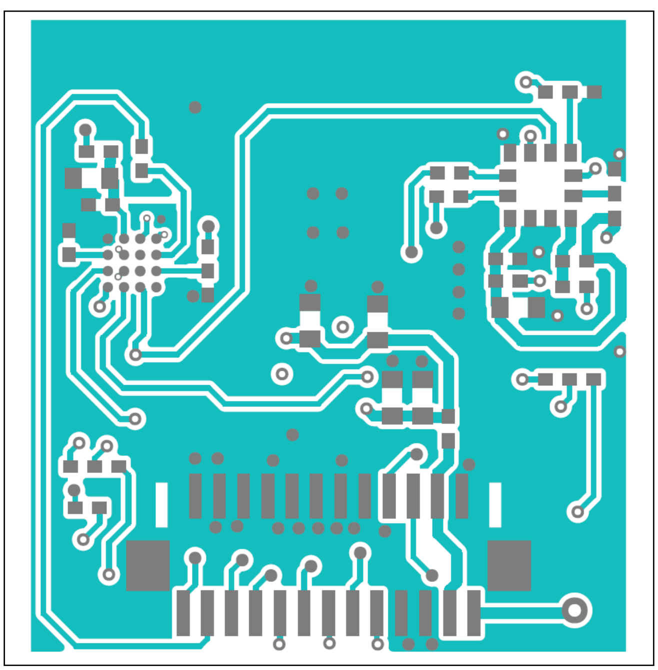


Figure 24. Top Layer—AFE Layer

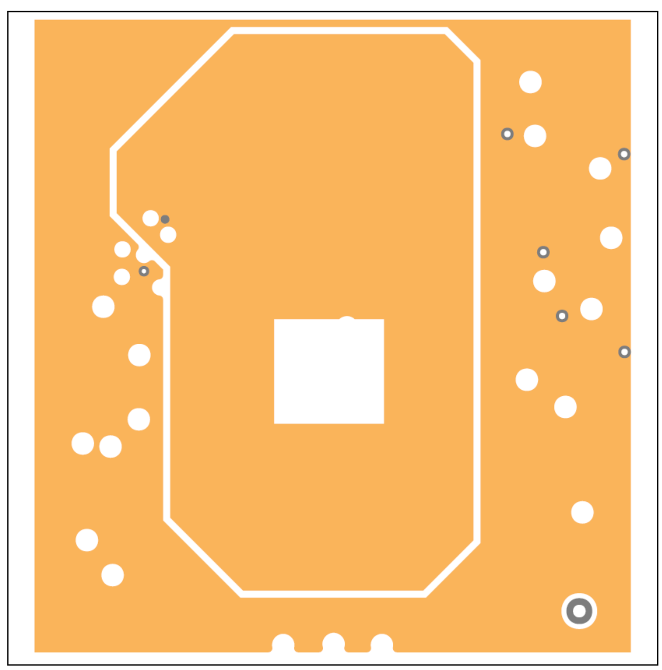


Figure 25. Layer 5—Pseudo PD_GND Shields PD_IN

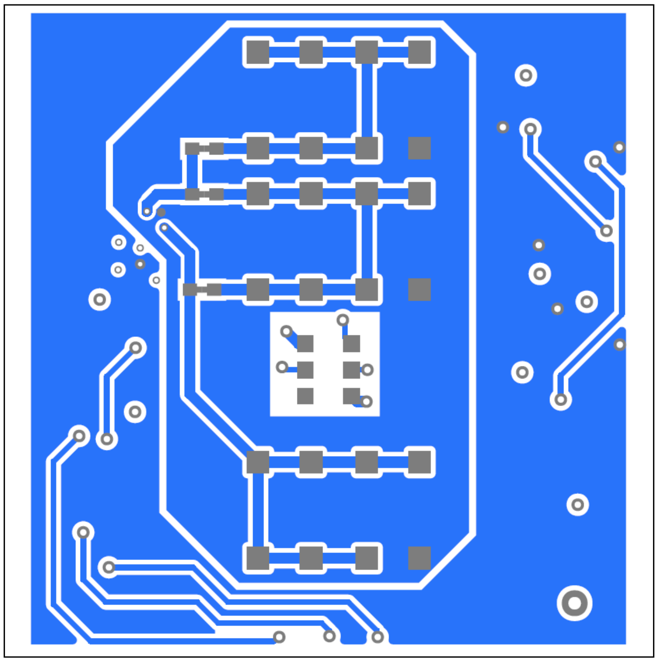


Figure 26. Bottom Layer—Optics Layer

Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	Status 1[7:0]	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
0x01	Status 2[7:0]	INVALID_CFG	–	–	–	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
FIFO									
0x03	FIFO Write Pointer[7:0]	FIFO_WR_PTR[7:0]							
0x04	FIFO Read Pointer[7:0]	FIFO_RD_PTR[7:0]							
0x05	FIFO Counter 1[7:0]	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
0x06	FIFO Counter 2[7:0]	FIFO_DATA_COUNT[7:0]							
0x07	FIFO Data Register[7:0]	FIFO_DATA[7:0]							
0x08	FIFO Configuration 1[7:0]	FIFO_A_FULL[7:0]							
0x09	FIFO Configuration 2[7:0]	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
System Control									
0x10	System Sync[7:0]	–	SW_FORCE_SYNC	–	–	–	–	–	–
0x11	System Configuration 1[7:0]	DISABLE_I2C	–	SYNC_MODE[1:0]		PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
0x12	System Configuration 2[7:0]	–	–	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
0x13	System Configuration 3[7:0]	–	–	–	ALC_DISABLE	PROX_DATA_EN	PROX_AUTO	COLLECT_RAW_DATA	MEAS1_CONFIG_SEL
0x14	PPG Filter Setup[7:0]	PPG_FILT2_SEL	–	DLPF_EN[1:0]		IIR_CFG	DEC_AVE[2:0]		
0x15	Photodiode Bias[7:0]	–	–	–	–	PD2_BIAS[1:0]		PD1_BIAS[1:0]	
0x16	Pin Functional Configuration[7:0]	–	–	–	–	–	INTB_FCFG[1:0]		TRIG_ICFG
0x17	Output Pin Configuration[7:0]	–	–	–	–	–	INTB_OCFG[1:0]		TRIGLED4_SEL
0x18	I2C Broadcast Address[7:0]	I2C_BCAST_ADDR[6:0]							I2C_BCAST_EN
PPG Frame Rate Clock									
0x1A	FR Clock Frequency Select[7:0]	–	–	–	FR_CLK_FINE_TUNE[4:0]				
0x1B	FR Clock Divider MSB[7:0]	–	FR_CLK_DIV[14:8]						

ADDRESS	NAME	MSB							LSB
0x1C	FR Clock Divider LSB[7:0]	FR_CLK_DIV[7:0]							
PPG MEAS1 Setup									
0x20	MEAS1 Selects[7:0]	–	MEAS1_AMB	–	–	MEAS1_DRVB[1:0]		MEAS1_DRVA[1:0]	
0x21	MEAS1 Configuration 1[7:0]	MEAS1_PDSEL[1:0]		–	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
0x22	MEAS1 Configuration 2[7:0]	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	MEAS1_LED_RGE[1:0]		MEAS1_PPG2_ADC_RGE[1:0]		MEAS1_PPG1_ADC_RGE[1:0]	
0x23	MEAS1 Configuration 3[7:0]	MEAS1_PD_SETLNG[2:0]			MEAS1_LED_SETLNG[1:0]		–	–	–
0x24	MEAS1 Configuration 4[7:0]	–	MEAS1_PPG2_DACOFF[2:0]			–	MEAS1_PPG1_DACOFF[2:0]		
0x25	MEAS1 LEDA Current[7:0]	MEAS1_DRVA_PA[7:0]							
0x26	MEAS1 LEDB Current[7:0]	MEAS1_DRVB_PA[7:0]							
PPG MEAS2 Setup									
0x28	MEAS2 Selects[7:0]	–	MEAS2_AMB	–	–	MEAS2_DRVB[1:0]		MEAS2_DRVA[1:0]	
0x29	MEAS2 Configuration 1[7:0]	MEAS2_PDSEL[1:0]		–	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
0x2A	MEAS2 Configuration 2[7:0]	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	MEAS2_LED_RGE[1:0]		MEAS2_PPG2_ADC_RGE[1:0]		MEAS2_PPG1_ADC_RGE[1:0]	
0x2B	MEAS2 Configuration 3[7:0]	MEAS2_PD_SETLNG[2:0]			MEAS2_LED_SETLNG[1:0]		–	–	–
0x2C	MEAS2 Configuration 4[7:0]	–	MEAS2_PPG2_DACOFF[2:0]			–	MEAS2_PPG1_DACOFF[2:0]		
0x2D	MEAS2 LEDA Current[7:0]	MEAS2_DRVA_PA[7:0]							
0x2E	MEAS2 LEDB Current[7:0]	MEAS2_DRVB_PA[7:0]							
PPG MEAS3 Setup									
0x30	MEAS3 Selects[7:0]	–	MEAS3_AMB	–	–	MEAS3_DRVB[1:0]		MEAS3_DRVA[1:0]	
0x31	MEAS3 Configuration 1[7:0]	MEAS3_PDSEL[1:0]		–	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
0x32	MEAS3 Configuration 2[7:0]	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	MEAS3_LED_RGE[1:0]		MEAS3_PPG2_ADC_RGE[1:0]		MEAS3_PPG1_ADC_RGE[1:0]	
0x33	MEAS3 Configuration 3[7:0]	MEAS3_PD_SETLNG[2:0]			MEAS3_LED_SETLNG[1:0]		–	–	–
0x34	MEAS3 Configuration 4[7:0]	–	MEAS3_PPG2_DACOFF[2:0]			–	MEAS3_PPG1_DACOFF[2:0]		
0x35	MEAS3 LEDA Current[7:0]	MEAS3_DRVA_PA[7:0]							
0x36	MEAS3 LEDB Current[7:0]	MEAS3_DRVB_PA[7:0]							

ADDRESS	NAME	MSB							LSB
PPG MEAS4 Setup									
0x38	MEAS4 Selects[7:0]	–	MEAS4_AMB	–	–	MEAS4_DRVB[1:0]		MEAS4_DRVA[1:0]	
0x39	MEAS4 Configuration 1[7:0]	MEAS4_PDSEL[1:0]		–	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
0x3A	MEAS4 Configuration 2[7:0]	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	MEAS4_LED_RGE[1:0]		MEAS4_PPG2_ADC_RGE[1:0]		MEAS4_PPG1_ADC_RGE[1:0]	
0x3B	MEAS4 Configuration 3[7:0]	MEAS4_PD_SETLNG[2:0]			MEAS4_LED_SETLNG[1:0]		–	–	–
0x3C	MEAS4 Configuration 4[7:0]	–	MEAS4_PPG2_DACOFF[2:0]			–	MEAS4_PPG1_DACOFF[2:0]		
0x3D	MEAS4 LEDA Current[7:0]	MEAS4_DRVA_PA[7:0]							
0x3E	MEAS4 LEDB Current[7:0]	MEAS4_DRVB_PA[7:0]							
PPG MEAS5 Setup									
0x40	MEAS5 Selects[7:0]	–	MEAS5_AMB	–	–	MEAS5_DRVB[1:0]		MEAS5_DRVA[1:0]	
0x41	MEAS5 Configuration 1[7:0]	MEAS5_PDSEL[1:0]		–	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
0x42	MEAS5 Configuration 2[7:0]	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	MEAS5_LED_RGE[1:0]		MEAS5_PPG2_ADC_RGE[1:0]		MEAS5_PPG1_ADC_RGE[1:0]	
0x43	MEAS5 Configuration 3[7:0]	MEAS5_PD_SETLNG[2:0]			MEAS5_LED_SETLNG[1:0]		–	–	–
0x44	MEAS5 Configuration 4[7:0]	–	MEAS5_PPG2_DACOFF[2:0]			–	MEAS5_PPG1_DACOFF[2:0]		
0x45	MEAS5 LEDA Current[7:0]	MEAS5_DRVA_PA[7:0]							
0x46	MEAS5 LEDB Current[7:0]	MEAS5_DRVB_PA[7:0]							
PPG MEAS6 Setup									
0x48	MEAS6 Selects[7:0]	–	MEAS6_AMB	–	–	MEAS6_DRVB[1:0]		MEAS6_DRVA[1:0]	
0x49	MEAS6 Configuration 1[7:0]	MEAS6_PDSEL[1:0]		–	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
0x4A	MEAS6 Configuration 2[7:0]	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	MEAS6_LED_RGE[1:0]		MEAS6_PPG2_ADC_RGE[1:0]		MEAS6_PPG1_ADC_RGE[1:0]	
0x4B	MEAS6 Configuration 3[7:0]	MEAS6_PD_SETLNG[2:0]			MEAS6_LED_SETLNG[1:0]		–	–	–
0x4C	MEAS6 Configuration 4[7:0]	–	MEAS6_PPG2_DACOFF[2:0]			–	MEAS6_PPG1_DACOFF[2:0]		
0x4D	MEAS6 LEDA Current[7:0]	MEAS6_DRVA_PA[7:0]							
0x4E	MEAS6 LEDB Current[7:0]	MEAS6_DRVB_PA[7:0]							

ADDRESS	NAME	MSB							LSB
PPG Threshold Interrupts									
0x50	THRESHOLD MEAS SEL[7:0]	–	THRESH2_MEAS_SEL[2:0]			–	THRESH1_MEAS_SEL[2:0]		
0x51	THRESHOLD HYST[7:0]	THRESH2_PPG_SEL	THRESH1_PPG_SEL	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
0x52	PPG HI THRESHOLD1[7:0]	THRESHOLD1_UPPER[7:0]							
0x53	PPG LO THRESHOLD1[7:0]	THRESHOLD1_LOWER[7:0]							
0x54	PPG HI THRESHOLD2[7:0]	THRESHOLD2_UPPER[7:0]							
0x55	PPG LO THRESHOLD2[7:0]	THRESHOLD2_LOWER[7:0]							
Interrupt Enables									
0x58	Interrupt Enable 1[7:0]	A_FULL_EN	FRAME_RDY_EN	FIFO_DATA_RDY_EN	ALC_OVF_EN	EXP_OVF_EN	THRESH2_HILO_EN	THRESH1_HILO_EN	–
0x59	Interrupt Enable 2[7:0]	INVALID_CFG_EN	–	–	–	LED4_COMPB_EN	LED3_COMPB_EN	LED2_COMPB_EN	LED1_COMPB_EN
Part ID									
0xFE	Revision ID[7:0]	–	–	–	–	–	–	–	–
0xFF	Part ID[7:0]	PART_ID[7:0]							

Register Details

Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	FRAME_RDY	FIFO_DATA_RDY	ALC_OVF	EXP_OVF	THRESH2_HILO	THRESH1_HILO	PWR_RDY
Reset	0	0	0	0	0	0	0	1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

A_FULL is set to 1 when the FIFO has reached the threshold programmed in the FIFO_A_FULL[7:0](0x08). This is a read-only bit and it is cleared when the Status 1 Register is read. It is also cleared when FIFO Data Register (0x07) is read, if FIFO_STAT_CLR[3](0x09) = 1.

A_FULL	DECODE
0	Normal operation
1	Indicates that the FIFO buffer has reached the threshold set by FIFO_A_FULL[7:0](0x08).

FRAME_RDY

FRAME_RDY is set to 1 when a full frame conversion has completed and it is ready in FIFO. A frame consists of FIFO data for all the PPG ADC conversions for the sequence programmed in the MEASx (x = 1 to 6) enable registers. This is a read-only bit and it is cleared by reading the Status 1 register. It is also cleared by reading the FIFO Data register (0x07) if FIFO_STAT_CLR[3](0x09) = 1.

FRAME_RDY	DECODE
0	Normal operation
1	A complete PPG frame is ready in the FIFO.

FIFO_DATA_RDY

FIFO_DATA_RDY is set to 1 when new data is available in the FIFO. This is a read-only bit and it is cleared by reading the Status 1 register (0x00). It is also cleared by reading the FIFO Data Register (0x07) if FIFO_STAT_CLR[3](0x09) = 1.

FIFO_DATA_RDY	DECODE
0	Normal operation
1	New data is available in the FIFO.

ALC_OVF

ALC_OVF is set to 1 when the ambient-light cancellation function of the photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC. This is a read-only bit and it is cleared by reading the Status 1 register (0x00).

ALC_OVF	DECODE
0	Normal operation
1	The ambient-light cancellation function of the photodiode has reached its maximum limit due to overflow.

EXP_OVF

EXP_OVF is set to 1 when an exposure measurement is either over range or under range for any of the enabled PPG measurements. A measurement is over range if it is higher than positive full scale (524287) minus roughly 16384, or under range if it is lower than negative full-scale / 4 (-131072) minus roughly 16384. This is a read-only bit, and it is cleared by reading the Status 1 register.

EXP_OVF	DECODE
0	Normal operation
1	The exposure data is over range or under range.

THRESH2_HILO

THRESH2_HILO is set to 1 when the THRESH2_MEAS_SEL[6:4](0x50) instance qualifies as above THRESHOLD2_UPPER[7:0](0x54) or below THRESHOLD2_LOWER[7:0](0x55). This is a read-only bit and it is cleared by reading the Status 1 register (0x00).

See the Threshold Detection Function section for a complete explanation of how the ADC is qualified as above or below threshold.

THRESH2_HILO	DECODE
0	ADC reading is within the threshold 2 range.
1	ADC reading is either above the THRESHOLD2_UPPER level or below the THRESHOLD2_LOWER level.

THRESH1_HILO

THRESH1_HILO is set to 1 when the THRESH1_MEAS[2:0](0x50) instance qualifies as above THRESHOLD1_UPPER[7:0](0x52) or below THRESHOLD1_LOWER[7:0](0x53). This is a read-only bit and it is cleared by reading the Status 1 register (0x00).

See the Threshold Detection Function section for a complete explanation of how the ADC is qualified as above or below threshold.

THRESH1_HILO	DECODE
0	ADC reading is within the threshold 1 range.
1	ADC reading is either above the THRESHOLD1_UPPER level or below the THRESHOLD1_LOWER level.

PWR_RDY

PWR_RDY is set to 1 when V_{DD} goes below the undervoltage lockout (UVLO) threshold, which is approximately 1.3V. If this condition occurs, all registers are reset to their POR state. This bit is not triggered by a soft-reset. This is a read-only bit and it is cleared when the Status 1 register is read, or by setting the SHDN[1](0x11) bit to 1.

PWR_RDY is a non-maskable interrupt, so it is asserted on the INTB pin.

PWR_RDY	DECODE
0	Normal operation
1	Indicates that V_{DD} goes below the UVLO threshold.

Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_CFG	–	–	–	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
Reset	0	–	–	–	0	0	0	0
Access Type	Read Only	–	–	–	Read Only	Read Only	Read Only	Read Only

INVALID_CFG

INVALID_CFG is set to 1 when the frame rate set by clock divider FR_CLK_DIV[14:0] (0x1B, 0x1C) is too fast to accommodate the programmed PPG measurements enabled in a frame. This is a read-only bit and it gets cleared when the Status 2 register (0x01) is read.

INVALID_CFG	DECODE
0	Normal operation
1	The PPG frame rate is too fast to accommodate the programmed PPG measurements enabled in a frame.

LED4_COMPB

LEDn_COMPB (n = 1 to 4) is set to 1 when the voltage at the LEDn_DRV pin is below the LED compliance voltage

. LEDn_COMPB is a read-only bit and is cleared when the

Status 2 register (0x01) is read.

LED4_COMPB	DECODE
0	The LEDn_DRV pin has sufficient voltage to support the programmed current.
1	The LEDn_DRV pin is below the voltage needed to support the programmed current. Power-supply rejection on LEDn is degraded and LEDn current is inaccurate.

LED3_COMPB

See LED4_COMPB for details.

LED2_COMPB

See LED4_COMPB for details.

LED1_COMPB

See LED4_COMPB for details.

FIFO Write Pointer (0x03)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR points to the FIFO location where the next sample is written. This pointer advances for each sample pushed on to the circular FIFO. The write pointer wraps around to count 0x00 as the next FIFO location after count 0xFF.

FIFO Read Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

FIFO_RD_PTR

FIFO_RD_PTR points to the FIFO location from which the next sample is to be read using the serial interface. This pointer advances each time a sample is read from the circular FIFO. The read pointer can be both read and written to. This allows rereading (or retrying) samples from the FIFO. However, writing to FIFO_RD_PTR can have adverse effects if it results in the FIFO being almost full. The read pointer wraps around to count 0x00 after count 0xFF.

FIFO Counter 1 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
Reset	0	0x00						
Access Type	Read Only	Read Only						

FIFO_DATA_COUNT

FIFO_DATA_COUNT[8](0x05) is a read-only bit that holds the most significant bit of the number of items available in the FIFO for the host to read. The lower 8 bits are in the FIFO_DATA_COUNT[7:0](0x06) register. FIFO_DATA_COUNT increments when a new item is pushed to the FIFO, and decrements when the host reads a item from the FIFO.

FIFO_DATA_COUNT is useful for debug.

OVF_COUNTER

The overflow counter OVF_COUNTER logs the number of samples lost if the FIFO is not read in a timely fashion. When FIFO is full any new samples results in either new or old samples getting lost depending on the FIFO_RO[1](0x09) setting.

This is a read-only register. When a complete sample is read from the FIFO and the read pointer advances, the OVF_COUNTER is reset to zero. It should be read immediately before reading the FIFO in order to check if an overflow condition has occured. This counter saturates at count value 0x7F.

FIFO Counter 2 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[7:0] is a read-only register that holds the lower 8 bits of the number of items available in the FIFO for the host to read.

See the FIFO_DATA_COUNT[8](0x05) description for details.

FIFO Data Register (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0xFF							
Access Type	Read Only							

FIFO_DATA

FIFO_DATA is used to get data from the FIFO using burst reads only. When burst reading from this register, the register address pointer does not auto-increment, and the FIFO_RD_PTR[7:0](0x04) advances to provide subsequent samples. Each sample is three bytes, so burst reading three bytes in the FIFO_DATA register through the serial interface advances the FIFO_RD_PTR by one count. The format and data type of the data stored in the FIFO is determined by the tag associated with the data. For details and examples of various data types in some use cases, see the FIFO Description section. This is a read-only register.

FIFO Configuration 1 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0x7F							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL sets the high watermark for the FIFO and determines when the status bit A_FULL[7](0x00) is asserted. The A_FULL bit is asserted when the FIFO holds (256 FIFO_A_FULL) samples. For example, if set to 0x0F, A_FULL gets asserted when there are 15 empty spaces left (241 samples in FIFO). If A_FULL_EN[7](0x58) is set to 1, then A_FULL being asserted results in an interrupt on the interrupt pin INTB. This condition should prompt the processor to read samples from FIFO before it fills and overflows

FIFO_A_FULL	FREE SPACES BEFORE INTERRUPT IS ASSERTED	NUMBER OF SAMPLES IN FIFO
0	0	256
1	1	255
2	2	254
3	3	253
...	...	...
254	254	2
255	255	1

FIFO Configuration 2 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	–	–	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	0	0	1	0	0	–
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

FIFO_MARK

When FIFO_MARK is set to 1, a marker tag is pushed to the FIFO. FIFO_MARK is a self-clearing bit. The marker tag is useful for differentiating the data in the FIFO before and after the tag.

See the FIFO Description section for the marker tag information.

FIFO_MARK	DECODE
0	Normal data saved in FIFO
1	Save a marker in FIFO

FLUSH_FIFO

When the FLUSH_FIFO bit is set to 1, the FIFO gets flushed, FIFO_WR_PTR[7:0](0x03), FIFO_RD_PTR[7:0](0x04), FIFO_DATA_COUNT[8:0](0x05, 0x06), and OVF_COUNTER[6:0](0x05) are reset to zero. The contents of the FIFO are lost. FLUSH_FIFO is a self-clearing bit.

FLUSH_FIFO	DECODE
0	Normal mode
1	FIFO is flushed

FIFO_STAT_CLR

FIFO_STAT_CLR determines if a FIFO_DATA[7:0](0x07) register read clears the status bits A_FULL[7](0x00), FRAME_RDY[6](0x00), and FIFO_DATA_RDY[5](0x00) and their corresponding interrupts.

FIFO_STAT_CLR	DECODE
0	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts do not get cleared by a FIFO_DATA[7:0](0x07) register read. They get cleared by a Status 1 register read.
1	A_FULL, FRAME_RDY and FIFO_DATA_RDY status and interrupts get cleared by a FIFO_DATA[7:0](0x07) register read or a Status 1 register read.

A_FULL_TYPE

A_FULL_TYPE defines the behavior of the status bit A_FULL[7](0x00) and its corresponding interrupt.

A_FULL_TYPE	DECODE
0	A_FULL interrupt is asserted when the almost full condition is detected. It is cleared by a Status 1 register read, but re-asserts for every sample if the almost full condition persists.
1	A_FULL interrupt is asserted when the almost full condition is detected. The interrupt gets cleared by a Status 1 register read, and does not re-assert until FIFO is read and then a new almost full condition is detected.

FIFO_RO

FIFO_RO bit controls the behavior of the FIFO when the FIFO becomes completely filled with data. Push to FIFO is enabled when FIFO is full if FIFO_RO is set to 1 and old samples are lost. Both FIFO Write Pointer (0x03) and FIFO Read Pointer (0x04) increment for each sample after the FIFO is full. If FIFO_RO is set to 0, new samples are lost and the FIFO is not updated. FIFO Write Pointer and FIFO Read Pointer do not increment until a sample is read from the FIFO.

FIFO_RO	DECODE
0	The FIFO stops on full.
1	The FIFO automatically rolls over on full.

System Sync (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	SW_FORCE_SYNC	–	–	–	–	–	–
Reset	–	0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

SW_FORCE_SYNC

Writing SW_FORCE_SYNC to 1 aborts the conversion of the current frame and starts a new frame. This is a self-clearing bit.

SW_FORCE_SYNC	DECODE
0	Normal mode
1	Manully start a new frame

System Configuration 1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	DISABLE_I2C	–	SYNC_MODE[1:0]		PPG2_PWRDN	PPG1_PWRDN	SHDN	RESET
Reset	0	–	0x0		0	0	0	0
Access Type	Write, Read	–	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

DISABLE_I2C

DISABLE_I2C disables the I^2C interface or not. For the SPI interface, the user must set DISABLE_I2C to 1 during initialization after powering up. See the Digital Interface section for details.

DISABLE_I2C	DECODE
0	The CSB/I2C_SEL pin selects interface.
1	I2C is disabled. The part uses the SPI interface only.

SYNC_MODE

SYNC_MODE selects the frame synchronization modes. See the Synchronization Modes section for details.

SYNC_MODE	TRIG INPUT	OPERATING MODES
0x0, 0x3	Not used	Internal frame oscillator and divider mode
0x1	Frame sync on TRIG input	External frame trigger input mode
0x2	External frame-rate clock on TRIG input	External frame-clock input mode

PPG2_PWRDN

PPG2_PWRDN enables or disables PPG channel 2. This bit is ignored in MAX86174B in which there is only a single PPG readout channel.

PPG2_PWRDN	DECODE
0	PPG channel 2 is enabled.
1	PPG channel 2 is powered down.

PPG1_PWRDN

PPG1_PWRDN enables or disables PPG channel 1. This bit is ignored in MAX86174B in which there is only a single PPG readout channel.

PPG1_PWRDN	DECODE
0	PPG channel 1 is enabled.
1	PPG channel 1 is powered down.

SHDN

Setting the SHDN bit to 1 puts the MAX86174A/MAX86174B into shutdown mode. While in shutdown mode, all configuration registers retain their values and the write/read operations function as normal. In this mode, the oscillator is shut down and the part draws minimum current. All interrupts are cleared. If this bit is asserted during an active conversion then the conversion is aborted. Set SHDN to 0 to put the part back in normal mode.

SHDN	DECODE
0	Normal mode
1	Shutdown mode

RESET

Setting RESET to 1 resets all registers to their power-on-reset state. This is a self-clearing bit and resets to 0 after the reset sequence is completed.

RESET	DECODE
0	Normal mode
1	All registers restored to power-on-reset state.

System Configuration 2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
Reset	–	–	0	0	0	0	0	0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

MEAS6_EN

See MEAS1_EN for details.

MEAS5_EN

See MEAS1_EN for details.

MEAS4_EN

See MEAS1_EN for details.

MEAS3_EN

See MEAS1_EN for details.

MEAS2_EN

See MEAS1_EN for details.

MEAS1_EN

MEASx_EN (x = 1 to 6) enables or disables PPG measurement programmed in the corresponding PPG MEASx Setup registers.

MEASx_EN (x = 1 to 6)	DECODE
0	Measurement x is disabled.
1	Measurement x is enabled.

System Configuration 3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALC_DISABLE	PROX_DATA_EN	PROX_AUTO	COLLECT_RAW_DATA	MEAS1_CONFIG_SEL
Reset	–	–	–	0	0	0	0	0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

ALC_DISABLE

ALC_DISABLE disables the front-end analog ambient-light cancellation circuit for PPG measurements. This bit does not alter the digital ambient-light cancellation.

ALC_DISABLE	DECODE
0	Normal operation
1	Front-end analog ambient-light cancellation is disabled.

PROX_DATA_EN

PROX_DATA_EN enables MEAS6 data to be saved in the FIFO when PROX_AUTO[2](0x13) is 1. If PROX_AUTO is set to 0, PROX_DATA_EN is ignored.

PROX_DATA_EN	DECODE
0	MEAS6 data is not saved in FIFO when PROX_AUTO is 1.
1	MEAS6 data is saved in FIFO when PROX_AUTO is 1.

PROX_AUTO

PROX_AUTO enables automatic proximity detect mode. For more details, see the Automatic Proximity Detect Mode section.

PROX_AUTO	DECODE
0	Normal mode
1	Automatic proximity detect mode

COLLECT_RAW_DATA

COLLECT_RAW_DATA pushes each ambient conversion and exposure conversion within a PPG measurement separately to the FIFO. Setting COLLECT_RAW_DATA to 1 inhibits the digital ambient cancellation. This allows a customized ambient rejection algorithm to be run in a host processor.

When COLLECT_RAW_DATA is set to 1, PROX_AUTO[2](0x13), THRESH1_MEAS_SEL[2:0](0x50), and THRESH2_MEAS_SEL[6:4](0x50) should be set to zero.

COLLECT_RAW_DATA	DECODE
0	Computed data for each measurement is saved in the FIFO.
1	Raw data for all ambient conversions and LED conversions in each measurement is saved in the FIFO.

MEAS1_CONFIG_SEL

MEAS1_CONFIG_SEL selects whether all enabled PPG measurements use the same configuration settings defined in MEAS1 setup registers (0x20 to 0x26). This allows for reduced setup configuration writes. The configuration settings used by all enabled measurements are as follows:

MEAS1_SINC3_SEL

MEAS1_FILT2_SEL

MEAS1_FILT_SEL

MEAS1_TINT

MEAS1_AVER

MEAS1_PPG1_ADC_RGE

MEAS1_PPG2_ADC_RGE

MEAS1_PD_SETLNG

MEAS1_LED_SETLNG

MEAS1_LED_RGE

MEAS1_PD1_SEL

MEAS1_PD2_SEL

MEAS1_CONFIG_SEL	DECODE
0	Use measurement-specific configurations defined in each measurement setup registers.
1	Use MEAS1 configuration for all enabled measurements.

PPG Filter Setup (0x14)

BIT	7	6	5	4	3	2	1	0
Field	PPG_FILT2_SEL	–	DLPF_EN[1:0]		IIR_CFG	DEC_AVE[2:0]		
Reset	0	–	0x0		0	0x0		
Access Type	Write, Read	–	Write, Read		Write, Read	Write, Read		

PPG_FILT2_SEL

PPG_FILT2_SEL enables either a second-order decimation filter or a third-order decimation filter. When PPG_FILT2_SEL is set to

1 (second-order decimation filter), MEASx_SINC3_SEL (x = 1 to 6) must be set to 0, and MEASx_TINT must be 0x3.

Note: MEASx_SINC3_SEL[7] is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A and MEASx_TINT[4:3] is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

PPG_FILT2_SEL	DECODE
0	3rd order decimation filter is used.
1	2nd order decimation filter is used if MEASx_SINC3_SEL = 0 and MEASx_TINT = 3.

DLPF_EN

DLPF_EN enables the digital low-pass filter as shown in the table below. When using the digital low-pass filter, COLLECT_RAW_DATA[1](0x13) must be set to 0. If COLLECT_RAW_DATA is 1, digital low-pass filter is disabled.

DLPF_EN	DECODE
0x0	Disable digital low-pass filter.
0x1	Enable digital low-pass filter using decimation averaging in DEC_AVE[2:0](0x14).
0x2, 0x3	Enable digital low-pass filter using IIR with the cut-off frequency set in IIR_CFG[3](0x14).

IIR_CFG

IIR_CFG selects the low-pass IIR filter configuration when DLPF_EN is 0x2 or 0x3. When using the IIR filter, the PPG frame rates supported are 100Hz and 200Hz.

IIR_CFG	DECODE
0	Cut-off frequency, f_{CO} = 11.5Hz
1	Cut-off frequency, f_{CO} = 12.07Hz

DEC_AVE

DEC_AVE sets the number of adjacent samples from each individual PPG channel that are averaged on-chip before being written to the FIFO if DLPF_EN[5:4](0x14) is 0x1. Number of samples averaged is 2^{DEC_AVE}. When DLPF_EN is 0x2 or 0x3, DEC_AVE defines the decimation ratio for the IIR low-pass filter output.

DEC_AVE	NUMBER OF SAMPLES AVERAGED, WHEN DLPF_EN = 0x1	DECIMATION RATIO WHEN DLPF = 0x2 or 0x3
0	1	1
0x1	2	2
0x2	4	4
0x3	8	8

DEC_AVE	NUMBER OF SAMPLES AVERAGED, WHEN DLPF_EN = 0x1	DECIMATION RATIO WHEN DLPF = 0x2 or 0x3
0x4	16	16
0x5, 0x6, 0x7	32	32

Photodiode Bias (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PD2_BIAS[1:0]		PD1_BIAS[1:0]	
Reset	–	–	–	–	0x1		0x1	
Access Type	–	–	–	–	Write, Read		Write, Read	

PD2_BIAS

PDm_BIAS (m = 1, 2) selects the bias for photodiode m depending on the photodiode capacitance.

Note when PD1 and PD2 are connected to the same PPG channel (MEASx_PDSEL = 0x0 or 0x3, x = 1 to 6), the greater of two PD_bias settings is used.

Note: MEASx_PDSEL[7:6] is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

See the Photodiode Biasing section for details.

PDm_BIAS (m = 1, 2)	PHOTODIODE CAPACITANCE (pF)
0x0	Do not use
0x1	0 to 125
0x2	125 to 250
0x3	250 to 500

PD1_BIAS

See PD2_BIAS[3:2](0x15) for details.

Pin Functional Configuration (0x16)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	INTB_FCFG[1:0]		TRIG_ICFG
Reset	–	–	–	–	–	0x1		0
Access Type	–	–	–	–	–	Write, Read		Write, Read

INTB_FCFG

INTB_FCFG controls the function of the INTB pin.

INTB_FCFG	DECODE
0x0	Disabled
0x1	INTB is enabled and is cleared upon reading of any status register or FIFO as applicable.
0x2	INTB is enabled and is self-clearing after 30.5μs (if fast clock is 10MHz), or reading the corresponding Status register or FIFO as applicable.
0x3	INTB is enabled and is self-clearing after 244μs (if fast clock is 10MHz), or reading the corresponding Status register or FIFO as applicable.

TRIG_ICFG

TRIG_ICFG bit sets the input active edge of the TRIG pin.

TRIG_ICFG	DECODE
0	TRIG active edge is falling (PORb default).
1	TRIG active edge is rising.

Output Pin Configuration (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	INTB_OCFG[1:0]		TRIGLED4_SEL
Reset	–	–	–	–	–	0x0		0
Access Type	–	–	–	–	–	Write, Read		Write, Read

INTB_OCFG

INTB_OCFG[1:0] selects the output drive type for the INTB pin, as shown in the table below.

INTB_OCFG	DECODE
0x0	Open-drain, active-low output
0x1	Active drive to V_{DD} and GND, the active level is a high output.
0x2	Active drive to V_{DD} and GND, the active level is a low output.
0x3	Do not use.

TRIGLED4_SEL

TRIGLED4_SEL selects the TRIG/LED4_DRV pin to be used as the LED4_DRV or TRIG input. It must only be set to 1 when SYNC_MODE[5:4](0x11) is 0x0. TRIG_ICFG[0](0x16) is also ignored when this bit is set.

TRIGLED4_SEL	DECODE
0	The LED4_DRV/TRIG pin is used as digital input TRIG.
1	The LED4_DRV/TRIG pin is used as LED4_DRV.

I2C Broadcast Address (0x18)

BIT	7	6	5	4	3	2	1	0
Field	I2C_BCAST_ADDR[6:0]							I2C_BCAST_EN
Reset	0x00							0
Access Type	Write, Read							Write, Read

I2C_BCAST_ADDR

I2C_BCAST_ADDR is used to define the upper 7 bits of the I^2C address in I^2C broadcast mode (I2C_BCAST_EN[0](0x18) = 1) when writing to multiple devices simultaneously using the I^2C serial interface. I2C_BCAST_ADDR is ignored in SPI mode.

See the I^2C Broadcast section for more details.

I2C_BCAST_EN

I2C_BCAST_EN enables write transactions to multiple devices using the broadcast address programmed in

I2C_BCAST_ADDR in I2C mode. I2C read transactions are not supported when I2C_BCAST_ADDR is used.

Note that for devices using SPI for serial interface, broadcast write transactions can be achieved by driving CSB pins low on multiple devices at the same time.

I2C_BCAST_EN	DECODE
0	Normal mode. I2C transactions are for one device only.
1	I2C broadcast mode. Write transactions to multiple devices are enabled.

FR Clock Frequency Select (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FR_CLK_FINE_TUNE[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

FR_CLK_FINE_TUNE

FR_CLK_FINE_TUNE is used to fine tune the internal 32.768kHz frame-rate clock. This register can be used to compensate the internal oscillator for thermal drift. This can be accomplished by measuring the time between interrupts using a microcontroller crystal-based real-time oscillator as a reference and computing the error in the time between interrupts. FR_CLK_FINE_TUNE is a two's complement code with a resolution of 0.2%/LSB. The total range is -3.2% to +3.0% around the factory trimmed value. See the table below for the shift in internal primary frame-rate clock vs. trim code.

FR_CLK_FINE_TUNE	SHIFT IN OSCILLATOR FREQUENCY (%)
0x10	-3.2
0x11	-3.0
0x12	-2.8
0x13	-2.6
0x14	-2.4
0x15	-2.2
0x16	-2.0
0x17	-1.8
0x18	-1.6
0x19	-1.4
0x1A	-1.2
0x1B	-1.0
0x1C	-0.8
0x1D	-0.6
0x1E	-0.4
0x1F	-0.2
0x00	0.0
0x01	0.2
0x02	0.4
0x03	0.6
0x04	0.8
0x05	1.0

FR_CLK_FINE_TUNE	SHIFT IN OSCILLATOR FREQUENCY (%)
0x06	1.2
0x07	1.4
0x08	1.6
0x09	1.8
0x0A	2.0
0x0B	2.2
0x0C	2.4
0x0D	2.6
0x0E	2.8
0x0F	3.0

FR Clock Divider MSB (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	–	FR_CLK_DIV[14:8]						
Reset	–	0x01						
Access Type	–	Write, Read						

FR_CLK_DIV

FR_CLK_DIV_H has the upper 7 bits of the 15-bit FR_CLK_DIV[14:0] clock divider, which defines the PPG frame rate.

The FR_CLK_DIV should be programmed such that all the conversions selected in the MEASx_EN (x = 1 to 6) bits in the System Configuration 2 (register 0x12) can be completed within the frame period. In the event that the number of enabled measurements as well as the integration time and number of burst average of each enabled measurement results in a frame measurement time that is longer than the primary frame clock period divided by FR_CLK_DIV, then a timing error occurs. This timing error produces the INVALID_CFG[7](0x01) to be set.

FR_CLK_DIV = 0x7FFF and FR_CLK_DIV < 0x0010 are reserved. FR_CLK_DIV should be at least 0x0010, which corresponds to the period for the smallest frame.

The time for each frame to complete is given by:

$t_{MEASUREMENT} = t_{INIT1} + t_{MEAS1} + t_{MEAS2} + t_{MEAS3} + ... + t_{MEAS6}$

Where:

if the MEASx_SINC3 = 1 or MEASx_FILT = 0 then:

t_{MEASx} = [t_{init} + MEASx_TINT * (2*MEASx_AVER+1) + 2*MEASx_AVER* MEASx_PD_SETLNG] * MEASx_EN

if MEASx_SINC3 = 0 and MEASx_FILT = 1 then:

t_{MEASx} = [t_{init} + 2*MEASx_TINT + MEASx_PD_SETLNG] * MEASx_EN

$t_{INIT1} = 7 \times t_{CLOCK}$

$t_{INIT} = 3 \times t_{CLOCK}$

MEASx_TINT = the integration time defined in measurement x = 1 to 6 and is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

MEASx_EN = 1 if the measurement is enabled and 0 if it is not, for measurement x = 1 to 6

MEASx_AVER = configuration of burst averages defined in measurement x = 1 to 6 and is in registers 0x21, 0x29, 0x31, 0x39, 0x41, 0x49.

MEASx_PD_SETLNG = photodiode settling time defined in measurement x = 1 to 6 and is in registers 0x23, 0x2B, 0x33, 0x3B, 0x43, 0x4B.

t_{CLOCK} = the frame-clock period, which is 1/(the slow oscillator) second. It is 1/32768s when SYNC_MODE = 0x0

t_{MEASx} is rounded up to an integer multiple of t_{CLOCK}.

In SYNC_MODE = 0x0 and 0x2 a valid measurement requires:

$t_{MEASUREMENT} < FR\_CLK\_DIV/f_{PRIMARY\_FRAME\_CLOCK}$

Where:

$f_{PRIMARY\_FRAME\_CLOCK}$ = either the internal primary frame clock (SYNC_MODE = 0) or the external frame clock input through the TRIG input (SYNC_MODE = 0x2)

In SYNC_MODE = 1 a valid measurement requires:

$t_{MEASUREMENT} < t_{TRIG\_PERIOD}$

Where:

t_{TRIG_PERIOD} = Period of the TRIG input signal

FR_CLK_DIV[14:0]	FRAME RATE (fps)
0x7FFF	Reserved
0x7FFE	1.000061
0x7FFD	1.000092
...	...
0x0100	128 (default)
...	...
0x0012	1820.44
0x0011	1927.53
0x0010	2048.00
0x000F to 0x0000	Reserved

FR Clock Divider LSB (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	FR_CLK_DIV[7:0]							
Reset	0x00							
Access Type	Write, Read							

FR_CLK_DIV

FR_CLK_DIV_L is the lower byte of the 15-bit FR_CLK_DIV[14:0] clock divider that defines the frame rate.

See FR_CLK_DIV_H for more details.

MEAS1 Selects (0x20)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_AMB	–	–	MEAS1_DRVB[1:0]		MEAS1_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS1_AMB

MEASx_AMB (x = 1 to 6) enables or disables direct ambient measurement. When MEASx_AMB is set to 1, MEASx_DRVA, and MEASx_DRVB are ignored.

Note: MEASx_DRVA is in registers 0x25, 0x2D, 0x35, 0x3D, 0x45, 0x4D and MEASx_DRVB is in registers 0x26, 0x2E, 0x36, 0x3E, 0x46, 0x4E.

The direct ambient measurement should always be the last enabled measurement in the frame.

MEASx_AMB (x = 1 to 6)	DECODE
0	Normal mode
1	Direct ambient-light measurement.

MEAS1_DRVB

MEASx_DRVB (x = 1 to 6) selects the LEDn_DRV pin (n = 1 to 4) driven by LED driver B.

MEASx_DRVB (x = 1 to 6)	PIN DRIVEN BY LED DRIVER B
0x0	LED1_DRV
0x1	LED2_DRV
0x2	LED3_DRV
0x3	LED4_DRV

MEAS1_DRVA

MEASx_DRVA (x = 1 to 6) selects the LEDn_DRV pin (n = 1 to 4) driven by LED driver A.

MEASx_DRVA (x = 1 to 6)	PIN DRIVEN BY LED DRIVER A
0x0	LED1_DRV
0x1	LED2_DRV
0x2	LED3_DRV
0x3	LED4_DRV

MEAS1 Configuration 1 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PDSEL[1:0]		–	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS1_PDSEL

MEASx_PDSEL (x = 1 to 6) selects which PDm_IN (m = 1, 2) pin is connected to optical channel 1 or 2.

MEASx_PDSEL (x = 1 to 6)	MAX86174A	MAX86174B
0x0	PD1 + PD2 combined and connected to PPG1	Reserved
0x1	PD2 connected to PPG1; PD1 connected to PPG2	PD2 connected to a single PPG channel
0x2	PD1 connected to PPG1; PD2 connected to PPG2	PD2 connected to a single PPG channel
0x3	PD1 + PD2 combined and connected to PPG2	Reserved

MEAS1_TINT

MEASx_TINT[1:0] (x = 1 to 6) bits set the integration time of PPG ADC as shown in the table below.

MEASx_TINT (x = 1 to 6)	INTEGRATION TIME (µs) (WITH 3rd ORDER DECIMATION FILTER)	INTEGRATION TIME (µs) (WITH 2nd ORDER DECIMATION FILTER)
0x0	14.6	-
0x1	29.2	-
0x2	58.6	-
0x3	117.1	118.2

MEAS1_AVER

MEASx_AVER (x = 1 to 6) sets the number of exposures per burst that are averaged in order to improve the exposure SNR and improve ambient light cancellation. MEASx_AVER works only with central ambient cancellation, MEASx_FILT_SEL = 0.

MEASx_AVER (x = 1 to 6)	NUMBER OF LED PULSES IN BURST
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

MEAS1 Configuration 2 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_SINC3_SEL	MEAS1_FILT_SEL	MEAS1_LED_RGE[1:0]		MEAS1_PPG2_ADC_RGE [1:0]		MEAS1_PPG1_ADC_RGE [1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS1_SINC3_SEL

MEASx_SINC3_SEL (x = 1 to 6) enables the SINC3 decimation filter for the PPG ADC. If MEASx_SINC3_SEL is set to 1, MEASx_TINT must be set to 3 and MEASx_FILT2_SEL must be set to 0. For more information on SINC3 decimation filter, see the ADC Decimation Filter section.

MEASx_SINC3_SEL (x = 1 to 6)	DECODE
0	SINC3 filter is not used.
1	SINC3 decimation filter is used only if MEASx_TINT = 0x3 (115.2µs).

MEAS1_FILT_SEL

MEASx_FILT_SEL (x = 1 to 6) selects the digital ambient light rejection method to be used. See the Ambient Rejection section for details and if burst average is applied with ALC, see the Burst Average section for ADC conversions.

MEASx_FILT_SEL (x = 1 to 6)	DECODE
0	Center difference method (CDM)
1	Forward difference method (FDM). MEASx_AVER is ignored.

MEAS1_LED_RGE

MEASx_LED_RGE (x = 1 to 6) selects the drive-current range for both LED current drivers, DRVA and DRVB, for measurement x.

MEASx_LED_RGE (x = 1 to 6)	LED FULL SCALE RANGE (mA)
0x0	32
0x1	64
0x2	96
0x3	128

MEAS1_PPG2_ADC_RGE

MEASx_PPGy_ADC_RGE (x = 1 to 6, y = 1, 2) selects the positive full-scale range of the PPG ADC on channel y for measurement x.

MEASx_PPGy_ADC_RGE (x = 1 to 6, y = 1, 2)	LSB (pA)	FULL SCALE (µA)
0x0	7.6	4.0
0x1	15.3	8.0
0x2	30.5	16.0
0x3	61.0	32.0

MEAS1_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS1 Configuration 3 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD_SETLNG[2:0]			MEAS1_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS1_PD_SETLNG

MEASx_PD_SETLNG (x = 1 to 6) selects the time between dark and exposure samples for measurement x. This accomodates photodiodes with longer settling time.

PD settling time should always be more than LED settling time selected in MEASx_LED_SETLNG. Note that for the same setting of both MEASx_PD_SETLNG and MEASx_LED_SETLNG, the photodiode settling time is 0.1µs higher than the LED settling time, and thus, satisfies the requirement of higher PD settling time.

MEASx_PD_SETLNG (x = 1 to 6)	TIME BETWEEN SAMPLES (µs)
0x0	8.1
0x1	12.1
0x2	16.1
0x3	24.1
0x4	32.1
0x5	48.1
0x6	64.1
0x7	80.1

MEAS1_LED_SETLNG

MEASx_LED_SETLNG (x = 1 to 6) selects the delay from the rising edge of LED to start of the exposure ADC integration. This allows for the LED current to settle before the start of ADC integration. LED settling time for a measurement must always be less than the photodiode settling time for the same measurement.

MEASx_LED_SETLNG (x = 1 to 6)	LED SETTLING TIME (µs)
0x0	8.0
0x1	12.0
0x2	16.0
0x3	24.0

MEAS1 Configuration 4 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS1_PPG2_DACOFF[2:0]			–	MEAS1_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS1_PPG2_DACOFF

MEASx_PPGy_DACOFF (x = 1 to 6, y = 1, 2) selects the offset DAC current added to the ADC on PPG channel y during the exposure interval. This allows for a larger convertible exposure range for ADCy by sourcing some of the photodiode DC exposure current from the offset DAC.

MEASx_PPGy_DACOFF (x = 1 to 6, y = 1, 2)	INJECTED OFFSET CURRENT TO ADCy (µA)
0x0	0
0x1	4
0x2	8
0x3	12
0x4	16
0x5	20
0x6	24
0x7	28

MEAS1_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS1 LEDA Current (0x25)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVA_PA

MEASx_DRVA_PA (x = 1 to 6) selects the LED drive current on LED driver A for measurement x. If MEASx_DRVA_PA is set to 0x00, LED Driver A is disabled for measurement x. The full-scale range selected by MEASx_LED_RGE determines the LED current for each LSB of the MEASx_DRVA_PA setting. For example, when MEASx_LED_RGE = 0, one LSB of MEASx_DRVA_PA is 0.125mA of the LED driver current on DRVA, but when MEASx_LED_RGE = 3, each LSB of MEASx_DRVA_PA setting is 0.5mA of the LED driver current on DRVA.

Note: MEASx_LED_RGE[5:4] is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A

MEASx_DRVA_PA (x = 1 to 6)	**LED CURRENT (mA)**	**LED CURRENT (mA)**	**LED CURRENT (mA)**	**LED CURRENT (mA)**
MEASx_LED_RGE (x = 1 to 6)	**0x0**	**0x1**	**0x2**	**0x3**
0x00	0.000	0.000	0.000	0.000
0x01	0.125	0.250	0.375	0.500
0x02	0.250	0.500	0.750	1.000
0x03	0.375	0.750	1.125	1.500
...				
0xFC	31.500	63.000	94.500	126.000
0xFD	31.625	63.250	94.875	126.500
0xFE	31.750	63.500	95.250	127.000
0xFF	31.875	63.750	95.625	127.500
LSB	0.125	0.250	0.375	0.500

MEAS1 LEDB Current (0x26)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	MEAS1_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVB_PA

MEASx_DRVB_PA (x = 1 to 6) selects the LED drive current on LED driver B for measurement x. If MEASx_DRVB_PA is set to 0x00, LED Driver B is disabled for measurement x. The full-scale range selected by MEASx_LED_RGE determines the LED current for each LSB of the MEASx_DRVB_PA setting. For example, when MEASx_LED_RGE = 0, one LSB of MEASx_DRVB_PA is 0.125mA of the LED driver current on DRVB, but when MEASx_LED_RGE = 3, each LSB of MEASx_DRVB_PA setting is 0.5mA of the LED driver current on DRVB.

Note: MEASx_LED_RGE[5:4] is in registers 0x22, 0x2A, 0x32, 0x3A, 0x42, 0x4A

MEASx_DRVB_PA (x = 1 to 6)	**LED CURRENT (mA)**	**LED CURRENT (mA)**	**LED CURRENT (mA)**	**LED CURRENT (mA)**
MEASx_LED_RGE (x = 1 to 6)	**0x0**	**0x1**	**0x2**	**0x3**
0x00	0.000	0.000	0.000	0.000
0x01	0.125	0.250	0.375	0.500
0x02	0.250	0.500	0.750	1.000
0x03	0.375	0.750	1.125	1.500
...				
0xFC	31.500	63.000	94.500	126.000
0xFD	31.625	63.250	94.875	126.500
0xFE	31.750	63.500	95.250	127.000
0xFF	31.875	63.750	95.625	127.500
LSB	0.125	0.250	0.375	0.500

MEAS2 Selects (0x28)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_AMB	–	–	MEAS2_DRVB[1:0]		MEAS2_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS2_AMB

See MEAS1_AMB[6](0x20) for details.

MEAS2_DRVB

See MEAS1_DRVB[3:2](0x20) for details.

MEAS2_DRVA

See MEAS1_DRVA[1:0](0x20) for details.

MEAS2 Configuration 1 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PDSEL[1:0]		–	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS2_PDSEL

See MEAS1_PDSEL[7:6](0x21) for details.

MEAS2_TINT

See MEAS1_TINT[4:3](0x21) or details.

MEAS2_AVER

See MEAS1_AVER[2:0](0x21) for details.

MEAS2 Configuration 2 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_SINC3_SEL	MEAS2_FILT_SEL	MEAS2_LED_RGE[1:0]		MEAS2_PPG2_ADC_RGE [1:0]		MEAS2_PPG1_ADC_RGE [1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS2_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x22) for details.

MEAS2_FILT_SEL

See MEAS1_FILT_SEL[6](0x22) for details.

MEAS2_LED_RGE

See MEAS1_LED_RGE[5:4](0x22) for details.

MEAS2_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS2_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS2 Configuration 3 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD_SETLNG[2:0]			MEAS2_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS2_PD_SETLNG

See MEAS1_PD_SETLNG[7:5](0x23) for details.

MEAS2_LED_SETLNG

See MEAS1_LED_SETLNG[4:3](0x23) for details.

MEAS2 Configuration 4 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_PPG2_DACOFF[2:0]			–	MEAS2_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS2_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS2_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS2 LEDA Current (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x25) for details.

MEAS2 LEDB Current (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS2_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x26) for details.

MEAS3 Selects (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_AMB	–	–	MEAS3_DRVB[1:0]		MEAS3_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS3_AMB

See MEAS1_AMB[6](0x20) for details.

MEAS3_DRVB

See MEAS1_DRVB[3:2](0x20) for details.

MEAS3_DRVA

See MEAS1_DRVA[1:0](0x20) for details.

MEAS3 Configuration 1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PDSEL[1:0]		–	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS3_PDSEL

See MEAS1_PDSEL[7:6](0x21) for details.

MEAS3_TINT

See MEAS1_TINT[4:3](0x21) for details.

MEAS3_AVER

See MEAS1_AVER[2:0](0x21) for details.

MEAS3 Configuration 2 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_SINC3_SEL	MEAS3_FILT_SEL	MEAS3_LED_RGE[1:0]		MEAS3_PPG2_ADC_RGE [1:0]		MEAS3_PPG1_ADC_RGE [1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS3_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x22) for details.

MEAS3_FILT_SEL

See MEAS1_FILT_SEL[6](0x22) for details.

MEAS3_LED_RGE

See MEAS1_LED_RGE[5:4](0x22) for details.

MEAS3_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS3_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS3 Configuration 3 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD_SETLNG[2:0]			MEAS3_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS3_PD_SETLNG

See MEAS1_PD_SETLNG[7:5](0x23) for details.

MEAS3_LED_SETLNG

See MEAS1_LED_SETLNG[4:3](0x23) for details.

MEAS3 Configuration 4 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_PPG2_DACOFF[2:0]			–	MEAS3_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS3_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS3_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS3 LEDA Current (0x35)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x25) for details.

MEAS3 LEDB Current (0x36)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS3_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x26) for details.

MEAS4 Selects (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_AMB	–	–	MEAS4_DRVB[1:0]		MEAS4_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS4_AMB

See MEAS1_AMB[6](0x20) for details.

MEAS4_DRVB

See MEAS1_DRVB[3:2](0x20) for details.

MEAS4_DRVA

See MEAS1_DRVA[1:0](0x20) for details.

MEAS4 Configuration 1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PDSEL[1:0]		–	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS4_PDSEL

See MEAS1_PDSEL[7:6](0x21) for details.

MEAS4_TINT

See MEAS1_TINT[4:3](0x21) for details.

MEAS4_AVER

See MEAS1_AVER[2:0](0x21) for details.

MEAS4 Configuration 2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_SINC3_SEL	MEAS4_FILT_SEL	MEAS4_LED_RGE[1:0]		MEAS4_PPG2_ADC_RGE [1:0]		MEAS4_PPG1_ADC_RGE [1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS4_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x22) for details.

MEAS4_FILT_SEL

See MEAS1_FILT_SEL[6](0x22) for details.

MEAS4_LED_RGE

See MEAS1_LED_RGE[5:4](0x22) for details.

MEAS4_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS4_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS4 Configuration 3 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD_SETLNG[2:0]			MEAS4_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS4_PD_SETLNG

See MEAS1_PD_SETLNG[7:5](0x23) for details.

MEAS4_LED_SETLNG

See MEAS1_LED_SETLNG[4:3](0x23) for details.

MEAS4 Configuration 4 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_PPG2_DACOFF[2:0]			–	MEAS4_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS4_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS4_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS4 LEDA Current (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x25) for details.

MEAS4 LEDB Current (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS4_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x26) for details.

MEAS5 Selects (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_AMB	–	–	MEAS5_DRVB[1:0]		MEAS5_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS5_AMB

See MEAS1_AMB[6](0x20) for details.

MEAS5_DRVB

See MEAS1_DRVB[3:2](0x20) for details.

MEAS5_DRVA

See MEAS1_DRVA[1:0](0x20) for details.

MEAS5 Configuration 1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PDSEL[1:0]		–	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS5_PDSEL

See MEAS1_PDSEL[7:6](0x21) for details.

MEAS5_TINT

See MEAS1_TINT[4:3](0x21) for details.

MEAS5_AVER

See MEAS1_AVER[2:0](0x21) for details.

MEAS5 Configuration 2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_SINC3_SEL	MEAS5_FILT_SEL	MEAS5_LED_RGE[1:0]		MEAS5_PPG2_ADC_RGE[1:0]		MEAS5_PPG1_ADC_RGE[1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS5_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x22) for details.

MEAS5_FILT_SEL

See MEAS1_FILT_SEL[6](0x22) for details.

MEAS5_LED_RGE

See MEAS1_LED_RGE[5:4](0x22) for details.

MEAS5_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS5_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS5 Configuration 3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD_SETLNG[2:0]			MEAS5_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS5_PD_SETLNG

See MEAS1_PD_SETLNG[7:5](0x23) for details.

MEAS5_LED_SETLNG

See MEAS1_LED_SETLNG[4:3](0x23) for details.

MEAS5 Configuration 4 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_PPG2_DACOFF[2:0]			–	MEAS5_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS5_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS5_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS5 LEDA Current (0x45)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x25) for details.

MEAS5 LEDB Current (0x46)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS5_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x26) for details.

MEAS6 Selects (0x48)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_AMB	–	–	MEAS6_DRVB[1:0]		MEAS6_DRVA[1:0]	
Reset	–	0	–	–	0x0		0x0	
Access Type	–	Write, Read	–	–	Write, Read		Write, Read	

MEAS6_AMB

See MEAS1_AMB[6](0x20) for details.

MEAS6_DRVB

See MEAS1_DRVB[3:2](0x20) for details.

MEAS6_DRVA

See MEAS1_DRVA[1:0](0x20) for details.

MEAS6 Configuration 1 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PDSEL[1:0]		–	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
Reset	0x0		–	0x3		0x0		
Access Type	Write, Read		–	Write, Read		Write, Read		

MEAS6_PDSEL

See MEAS1_PDSEL[7:6](0x21) for details.

MEAS6_TINT

See MEAS1_TINT[4:3](0x21) for details.

MEAS6_AVER

See MEAS1_AVER[2:0](0x21) for details.

MEAS6 Configuration 2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_SINC3_SEL	MEAS6_FILT_SEL	MEAS6_LED_RGE[1:0]		MEAS6_PPG2_ADC_RGE[1:0]		MEAS6_PPG1_ADC_RGE[1:0]	
Reset	0	0	0x3		0x2		0x2	
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	

MEAS6_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x22) for details.

MEAS6_FILT_SEL

See MEAS1_FILT_SEL[6](0x22) for details.

MEAS6_LED_RGE

See MEAS1_LED_RGE[5:4](0x22) for details.

MEAS6_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS6_PPG1_ADC_RGE

See MEAS1_PPG2_ADC_RGE[3:2](0x22) for details.

MEAS6 Configuration 3 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD_SETLNG[2:0]			MEAS6_LED_SETLNG[1:0]		–	–	–
Reset	0x1			0x1		–	–	–
Access Type	Write, Read			Write, Read		–	–	–

MEAS6_PD_SETLNG

See MEAS1_PD_SETLNG[7:5](0x23) for details.

MEAS6_LED_SETLNG

See MEAS1_LED_SETLNG[4:3](0x23) for details.

MEAS6 Configuration 4 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_PPG2_DACOFF[2:0]			–	MEAS6_PPG1_DACOFF[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

MEAS6_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS6_PPG1_DACOFF

See MEAS1_PPG2_DACOFF[6:4](0x24) for details.

MEAS6 LEDA Current (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x25) for details.

MEAS6 LEDB Current (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS6_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x26) for details.

THRESHOLD MEAS SEL (0x50)

BIT	7	6	5	4	3	2	1	0
Field	–	THRESH2_MEAS_SEL[2:0]			–	THRESH1_MEAS_SEL[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

THRESH2_MEAS_SEL

THRESH2_MEAS_SEL enables threshold detect function and selects the PPG measurement for the second instance of the threshold function. For details see the Threshold Detect Function section.

If threshold detect function is enabled, COLLECT_RAW_DATA[1](0x13) and SMP_AVE[2:0](0x14) must be set to zero.

THRESH2_MEAS_SEL	DECODE
0x0	THRESH2_HILO detect is disabled
0x1	MEAS1 selected
0x2	MEAS2 selected
0x3	MEAS3 selected
0x4	MEAS4 selected
0x5	MEAS5 selected
0x6	MEAS6 selected
0x7	RESERVED, THRESH2_HILO detect is disabled

THRESH1_MEAS_SEL

THRESH1_MEAS_SEL enables threshold detect function and selects the PPG measurement for the first instance of the threshold function. For details see the Threshold Detect Function section.

If the threshold detect function is enabled, COLLECT_RAW_DATA[1](0x13) and SMP_AVE[2:0](0x14) must be set to zero.

THRESH1_MEAS_SEL	DECODE
0x0	THRESH1_HILO detect is disabled
0x1	MEAS1 selected
0x2	MEAS2 selected
0x3	MEAS3 selected
0x4	MEAS4 selected
0x5	MEAS5 selected
0x6	MEAS6 selected
0x7	RESERVED, THRESH1_HILO detect is disabled

THRESHOLD HYST (0x51)

BIT	7	6	5	4	3	2	1	0
Field	THRESH2_PPG_SEL	THRESH1_PPG_SEL	–	TIME_HYST[1:0]		LEVEL_HYST[2:0]		
Reset	0	0	–	0x0		0x0		
Access Type	Write, Read	Write, Read	–	Write, Read		Write, Read		

THRESH2_PPG_SEL

THRESH1_PPG_SEL selects the optical channel for THRESHOLD 1.

THRESH2_PPG_SEL	CHANNEL THAT THRESHOLD2 IS APPLIED
0	Optical Channel 1
1	Optical Channel 2

THRESH1_PPG_SEL

THRESH1_PPG_SEL selects the optical channel for THRESHOLD 1.

THRESH1_PPG_SEL	CHANNEL THAT THRESHOLD1 IS APPLIED
0	Optical Channel 1
1	Optical Channel 2

TIME_HYST

Time hysteresis selects the number of consecutive samples outside the limits defined by THRESHOLDx_UPPER (x = 1, 2) and THRESHOLDx_LOWER in order to trigger the threshold interrupt THRESHx_HILO (in register 0x00). TIME_HYST applies to both instances of threshold interrupts. For details, see the Threshold Detect Funciton section.

TIME_HYST	NUMBER OF SAMPLES BEFORE INTERRUPT IS SET
0x0	Time hysteresis is disabled
0x1	2
0x2	4
0x3	8

LEVEL_HYST

LEVEL_HYST sets the variation in ADC counts permitted when the THRESHx_HILO (x = 1, 2) interrupt is triggered. This value is in ADC counts and is applied at ±0.5 x LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. LEVEL_HYST applies to both instances of threshold interrupts. For details, see the Threshold Detect Function section.

LEVEL_HYST	MAGNITUDE OF HYSTERESIS (LSBs)
0x0	Level hysteresis is disabled.
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

PPG HI THRESHOLD1 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD1_UPPER

THRESHOLDx_UPPER (x = 1, 2) defines the upper threshold limit for THRESHOLD x. Each LSB of THRESHOLDx_UPPER represents 2048 LSBs of the corresponding selected measurement (THRESHx_MEAS_SEL) ADC code.

THRESHOLDx_UPPER must be programmed to be greater than THRESHOLDx_LOWER; otherwise, the interrupt behavior is undefined.

THRESHOLDx_UPPER (x = 1, 2)	UPPER LIMIT FOR THRESHOLD x
0x00	0, upper threshold is disabled
0x01	2048
0x02	4096
0x03	6144
...	...
0xFD	518144
0xFE	520192
0xFF	522240

PPG LO THRESHOLD1 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD1_LOWER

THRESHOLDx_LOWER (x = 1, 2) defines the lower threshold limit for THRESHOLD x. Each LSB of THRESHOLDx_LOWER represents 2048 LSBs of the selected measurement (THRESHx_MEAS_SEL) ADC code.

THRESHOLDx_LOWER (x = 1, 2)	LOWER LIMIT FOR THRESHOLD x
0x00	0, lower threshold is disabled
0x01	2048
0x02	4096
0x03	6144
...	...
0xFD	518144
0xFE	520192
0xFF	522240

PPG HI THRESHOLD2 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD2_UPPER

See THRESHOLD1_UPPER[7:0](0x52) for details.

PPG LO THRESHOLD2 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD2_LOWER

See THRESHOLD1_LOWER[7:0](0x53) for details.

Interrupt Enable 1 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	FRAME_RDY_EN	FIFO_DATA_RDY_EN	ALC_OVF_EN	EXP_OVF_EN	THRESH2_HILO_EN	THRESH1_HILO_EN	–
Reset	0	0	0	0	0	0	0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–

A_FULL_EN

Enables the A_FULL[7](0x00) status bit to trigger the INTB output pin.

A_FULL_EN	DECODE
0	The A_FULL status bit does not impact the INTB output pin.
1	The INTB pin is triggered when A_FULL is set to 1.

FRAME_RDY_EN

Enables the FRAME_RDY[6](0x00) status bit to trigger the INTB output pin.

FRAME_RDY_EN	DECODE
0	The FRAME_RDY status bit does not impact the INTB output pin.
1	The INTB pin is triggered when FRAME_RDY is set to 1.

FIFO_DATA_RDY_EN

Enables the FIFO_DATA_RDY[5](0x00) status bit to trigger the INTB output pin.

FIFO_DATA_RDY_EN	DECODE
0	The FIFO_DATA_RDY status bit does not impact the INTB output pin.
1	The INTB pin is triggered when FIFO_DATA_RDY is set to 1.

ALC_OVF_EN

Enables the ALC_OVF[4](0x00) status bit to trigger the INTB output pin.

ALC_OVF_EN	DECODE
0	The ALC_OVF status bit does not impact the INTB output pin.
1	The INTB pin is triggered when ALC_OVF is set to 1.

EXP_OVF_EN

Enables the EXP_OVF[3](0x00) status bit to trigger the INTB output pin.

EXP_OVF_EN	DECODE
0	The EXP_OVF status bit does not impact the INTB output pin.
1	The INTB pin is triggered when EXP_OVF is set to 1.

THRESH2_HILO_EN

Enables the THRESH2_HILO[2](0x00) status bit to trigger the INTB output pin.

THRESH2_HILO_EN	DECODE
0	The THRESH2_HILO status bit does not impact the INTB output pin.
1	The INTB pin is triggered when THRESH2_HILO is set to 1.

THRESH1_HILO_EN

Enables the THRESH1_HILO[1](0x00) status bit to trigger the INTB output pin.

THRESH1_HILO_EN	DECODE
0	The THRESH1_HILO status bit does not impact the INTB output pin.
1	The INTB pin is triggered when THRESH1_HILO is set to 1.

Interrupt Enable 2 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_CFG_EN	–	–	–	LED4_COMPB_EN	LED3_COMPB_EN	LED2_COMPB_EN	LED1_COMPB_EN
Reset	0	–	–	–	0	0	0	0
Access Type	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

INVALID_CFG_EN

Enables the INVALID_CFG[7](0x01) status bit to trigger the INTB output pin.

INVALID_CFG_EN	DECODE
0	The INVALID_CFG status bit does not impact the INTB output pin.
1	The INTB pin is triggered when INVALID_CFG is set to 1.

LED4_COMPB_EN

Enables the LED4_COMPB[3](0x01) status bit to trigger the INTB output pin.

LED4_COMPB_EN	DECODE
0	The LED4_COMPB status bit does not impact the INTB output pin.
1	The INTB pin is triggered when LED4_COMPB is set to 1.

LED3_COMPB_EN

Enables the LED3_COMPB[2](0x01) status bit to trigger the INTB output pin.

LED3_COMPB_EN	DECODE
0	The LED3_COMPB status bit does not impact the INTB output pin.
1	The INTB pin is triggered when LED3_COMPB is set to 1.

LED2_COMPB_EN

Enables the LED2_COMPB[1](0x01) status bit to trigger the INTB output pin.

LED2_COMPB_EN	DECODE
0	The LED2_COMPB status bit does not impact the INTB output pin.
1	The INTB pin is triggered when LED2_COMPB is set to 1.

LED1_COMPB_EN

Enables the LED1_COMPB[0](0x01) status bit to trigger the INTB output pin.

LED1_COMPB_EN	DECODE
0	The LED1_COMPB status bit does not impact the INTB output pin.
1	The INTB pin is triggered when LED1_COMPB is set to 1.

Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x40							
Access Type	Read Only							

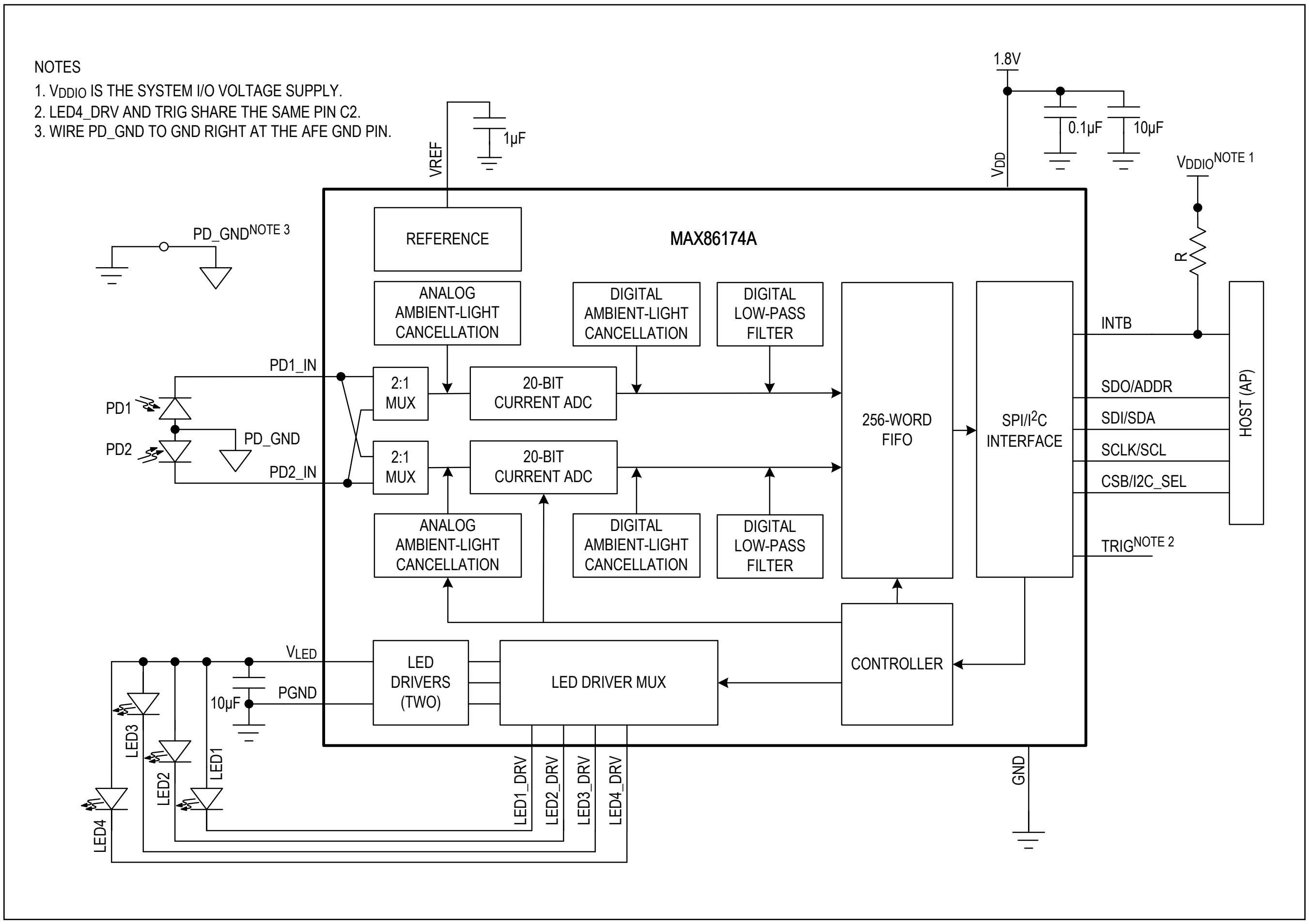
PART_ID

This register stores the Part Identifier for the chip.

PART_ID	PART NUMBER	DESCRIPTION
0x40	MAX86174A	Dual-PPG channel
0x41	MAX86174B	Single-PPG channel

Typical Application Circuits

MAX86174A/MAX86174B



Ordering Information

PART NUMBER	TEMPERATURE RANGE	BUMP
MAX86174AENE+	-40°C to +85°C	16
MAX86174AENE+T	-40°C to +85°C	16
MAX86174BENE+*	-40°C to +85°C	16
MAX86174BENE+T*	-40°C to +85°C	16

+ Denotes lead(Pb)-free/RoHS compliance.

T = Tape-and-reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Release for Market Intro	—
1	2/22	Updated *General Description*, *Benefits and Features*, *Absolute Maximum Ratings*, and *Electrical Characteristics* table	1, 7, 9, 38, 39, 40