Customer Information Notification | 202003033I

Issue Date: 17-Apr-2020
Effective Date: 18-Apr-2020

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QUALITY

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[ ] Wafer Fab Process

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[ ] Assembly Materials

[ ] Assembly Location

[ ] Product Marking

[ ] Mechanical Specification

[ ] Packing/Shipping/Labeling

[ ] Test Location

[ ]Test Process

[ ] Test Equipment

[ ] Design

[ ] Errata

[ ] Electrical spec./Test coverage

[X] Other - Datasheet update for clarification

MPC5775E/MPC5775B Data Sheet Updates To Rev.2

Description

NXP Semiconductors announces data sheet update for the MPC5775E/MPC5775B from revision 1 to revision 2. The revision history included in the updated document provides a details description of the changes.

Data sheet changes:
1. Page 79: In Figure 42, added optional feature field S.
2. Page 23: In Table 16, updated the footnote (no.13) from "TUE does not apply to differential conversions" to "TUE, Gain, and Offset specifications do not apply to differential conversions".
3. Page 11: In Table 4, added Max value 120uA for 40°C and 360uA for 85°C for ISTBY.
4. Page 30: In Table 17, changed the condition of dGROUP from "Within pass band: Tclk is fADCD_M / 2" to "Within pass band: Tclk is 2/fADCD_M".
5. Page 31: Updated the footnote (no.15) of tLATENCY, changed the Register Latency formula from "where fADCD_S is the after-decimation ADC output data rate, fADCD_M is the modulator sampling rate and fFM_PER_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)fFM_PER_CLK" to "where fADCD_S is the after-decimation ADC output data rate, fADCD_M/2 is the modulator sampling rate and fFM_PER_CLK is the frequency of the peripheral bridge clock feeds to the ADC S/D module. REGISTER LATENCY = tLATENCY + 0.5/fADCD_S + 2 (~+1)/fADCD_M + 2(~+1)/fFM_PER_CLK".

The MPC5775E/MPC5775B data sheet revision 2 is attached to this notice and can be found at:
https://www.nxp.com/products/processors-and-microcontrollers/power-architecture/mpc55xx-5xxx-mcus/ultra-reliable-mpc57xx-mcus/mpc5775b-and-mpc5775e-microcontrollers-for-battery-management-systems-bms-and-inverter-applications:MPC5775B-E?tab=Documentation_Tab

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02.
Reason
The data sheet has been updated to provide additional technical clarification.

Identification of Affected Products
Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

No impact on form, fit, function, reliability or quality.
Data Sheet Revision
A new datasheet will be issued

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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Affected Part Numbers

SPC5775BDK3MME2

SPC5775EDK3MME3