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NTE74HCT14 & NTE74HCT14T
Integrated Circuit
TTL – High Speed CMOS,
Hex Inverting Schmitt Trigger

Description:

The NTE74HCT14 (14–Lead DIP) and NTE74HCT14T (SOIC–14) are hex inverting Schmitt trigger devices that utilizes advanced silicon–gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS–TTL loads. Inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND.

Features:

- Propagation Delay: 13ns (typ)
- Wide Power Supply Range: 4.5V to 5.5V
- Low Quiescent Current: 10μA (max)
- Low Input Current: 1μA (max)
- Fanout of 10 LS–TTL Loads
- Typical Hysteresis Voltage: 0.6V at V_{CC} = 4.5V
- TTL, LS Pinout and Input Threshold Compatible

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C

DC Electrical Characteristics: (V_{CC} = 5.5V unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Positive–Going Threshold Voltage	V_{T+}	Minimum	V_{CC} = 4.5V	1.5	1.2	1.2	V
				1.7	1.4	1.4	V
		Maximum	V_{CC} = 4.5V	1.5	1.9	1.9	V
				1.7	2.1	2.1	V
Negative–Going Threshold Voltage	V_{T-}	Minimum	V_{CC} = 4.5V	0.9	0.5	0.5	V
				1.0	0.6	0.6	V
		Maximum	V_{CC} = 4.5V	0.9	1.2	1.2	V
				1.0	1.4	1.4	V
Hysteresis Voltage	V_H	Minimum	V_{CC} = 4.5V	0.6	0.4	0.4	V
				0.7	0.4	0.4	V
		Maximum	V_{CC} = 4.5V	0.6	1.4	1.4	V
				0.7	1.5	1.5	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\|$ = 20μA, V_{CC} = 4.5V	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	4.2	3.98	3.84	V
			$\|I_{OUT}\|$ = 4.8mA,	5.2	4.98	4.84	V
Minimum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\|$ = 20μA, V_{CC} = 4.5V	0	0.1	0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	0.2	0.26	0.33	V
			$\|I_{OUT}\|$ = 4.8mA	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		–	1.0	10	μA
		V_{IN} = 2.4V or 0.5V		–	2.4	2.4	mA

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

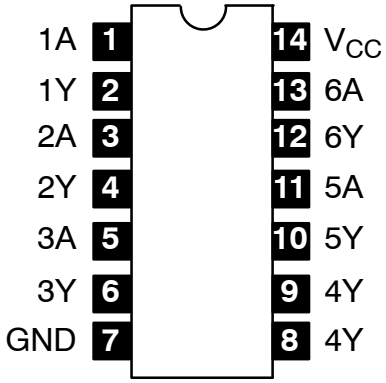
Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Propagation Delay	t_{PLH}, t_{PHL}		10	18	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, t_r = t_f = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C	T_A = –40° to +85°C		Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}, t_{PHL}		–	20	25	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		9	15	19	ns
Power Dissipation Capacitance	C_{PD}	Per Gate, Note 4	–	25	–	pF
Maximum Input Capacitance	C_{IN}		5	10	10	pF

Note 4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Pin Connection Diagram



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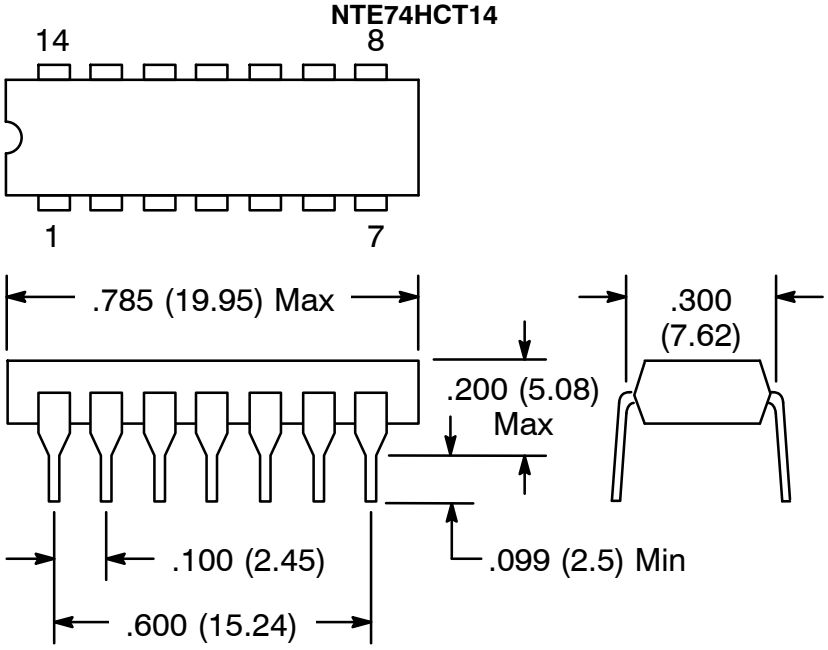

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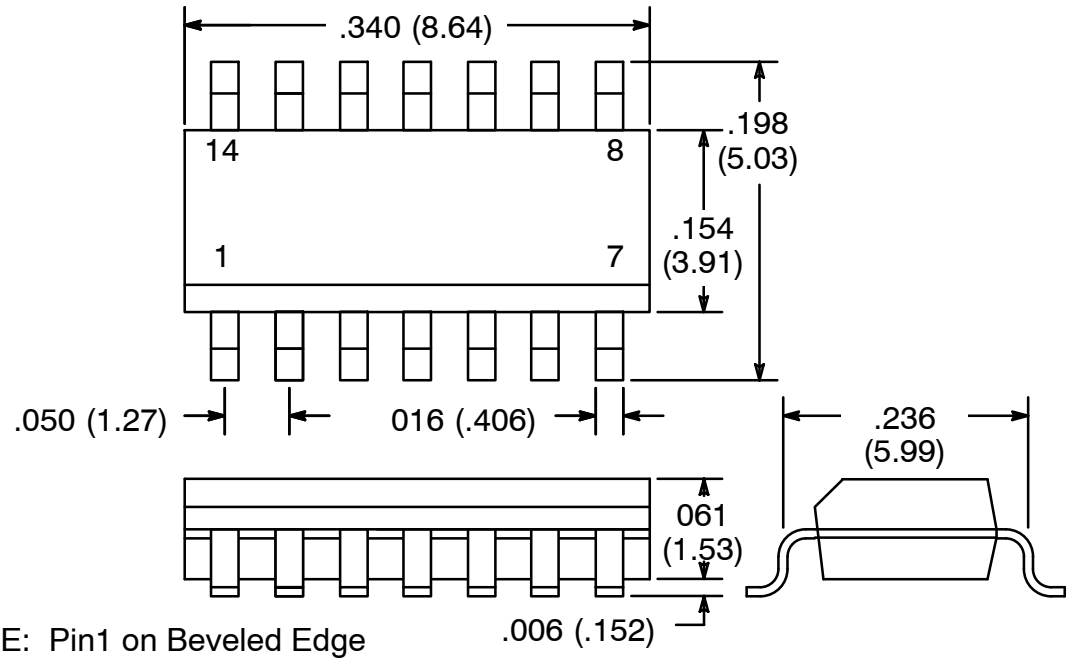

NOTE: Pin1 on Beveled Edge