LTC3331EUH
Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger

DESCRIPTION

Demonstration Circuit DC2151A is a nanopower buck-boost DC/DC with energy harvesting battery charger featuring the LTC®3331. The LTC3331 integrates a high voltage energy harvesting power supply plus a DC/DC converter powered by a rechargeable cell battery to create a single output supply for alternative energy applications. The energy harvesting power supply, consisting of an integrated low-loss full-wave bridge with a high voltage buck converter, harvests energy from piezoelectric, solar or magnetic sources. The rechargeable cell input powers a buck-boost converter capable of operating down to 1.8V at its input. Either DC/DC converter can deliver energy to a single output. The buck operates when harvested energy is available, reducing the quiescent current drawn on the battery to essentially zero. The buck-boost takes over when harvested energy goes away.

A 10mA shunt allows simple battery charging with harvest energy while a low battery disconnect function protects the battery from deep discharge. A supercapacitor balancer is also integrated, allowing for increased output storage.

Voltage and current settings for input and output as well as the battery float voltage are programmable via pin-strapped logic inputs.

The LTC3331EUH is available in a 5mm × 5mm 32-lead QFN surface mount package with exposed pad.

BOARD PHOTO

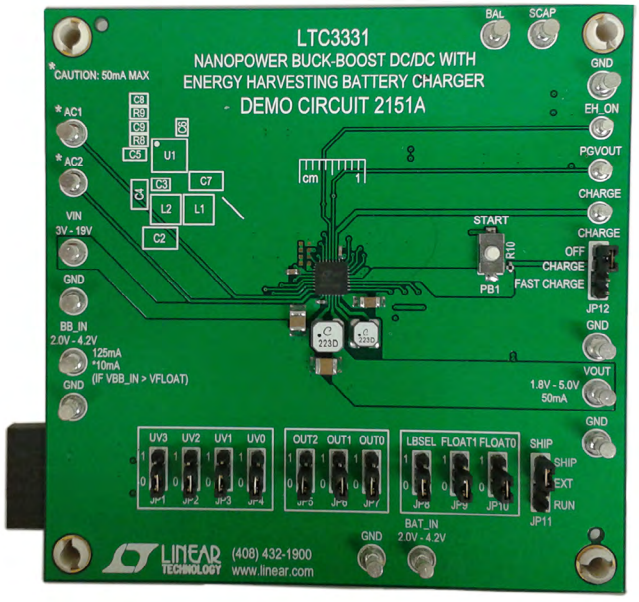

Figure 1. DC2151A Demoboard

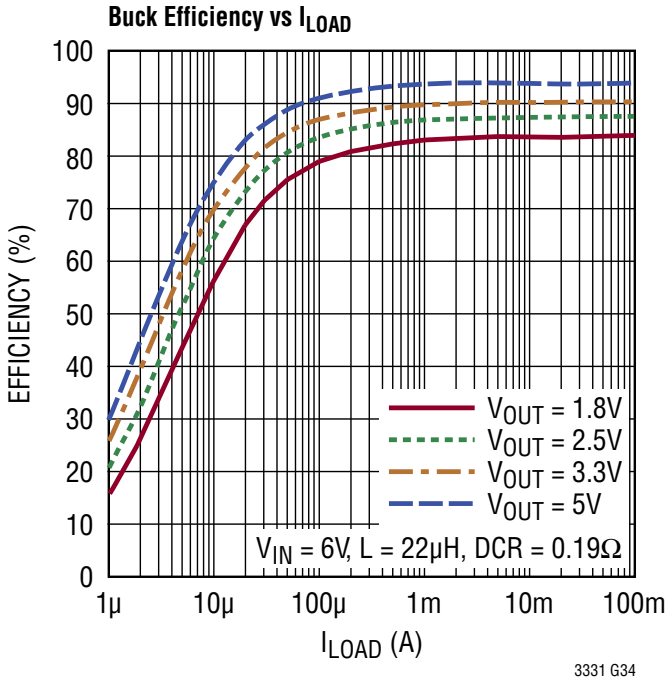

Figure 2. Typical Efficiency of DC2151A

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN		MAX	UNITS
V_{IN}	Input Voltage Range		3.0	to	18.0	V
V_{OUT} 1.8V	Output Voltage Range	OUT0=0, OUT1=0, OUT2=0	1.728	to	1.872	V
V_{OUT} 2.5V	Output Voltage Range	OUT0=1, OUT1=0, OUT2=0	2.425	to	2.575	V
V_{OUT} 2.8V	Output Voltage Range	OUT0=0, OUT1=1, OUT2=0	2.716	to	2.884	V
V_{OUT} 3.0V	Output Voltage Range	OUT0=1, OUT1=0, OUT2=0	2.910	to	3.090	V
V_{OUT} 3.3V	Output Voltage Range	OUT0=0, OUT1=0, OUT2=1	3.200	to	3.400	V
V_{OUT} 3.6V	Output Voltage Range	OUT0=1, OUT1=0, OUT2=1	3.492	to	3.708	V
V_{OUT} 4.5V	Output Voltage Range	OUT0=0, OUT1=1, OUT2=1	4.365	to	4.635	V
V_{OUT} 5.0V	Output Voltage Range	OUT0=1, OUT1=1, OUT2=1	4.850	to	5.150	V
V_{BAT} 3.45V	Float Voltage Range	FLOAT1=0, FLOAT=0	3.381	to	3.519	V
V_{BAT} 4.00V	Float Voltage Range	FLOAT1=0, FLOAT=1	3.920	to	4.080	V
V_{BAT} 4.1V	Float Voltage Range	FLOAT1=1, FLOAT=0	4.018	to	4.182	V
V_{BAT} 4.2V	Float Voltage Range	FLOAT1=1, FLOAT=1	4.116	to	4.284	V

OPERATING PRINCIPLE

Refer to the block diagram within the LTC3331 data sheet for its operating principle.

The LTC3331 combines a buck switching regulator and a buck-boost switching regulator to produce an energy harvesting solution with battery backup. The converters are controlled by a prioritizer that selects which converter to use based on the availability of a battery and/or harvestable energy. If harvested energy is available, the buck regulator is active and the buck-boost is off. With a battery charger and a supercapacitor balancer and an array of different configurations, the LTC3331 suits many applications.

The synchronous buck converter is an ultralow quiescent current power supply tailored to energy harvesting applications. It is designed to interface directly to a piezoelectric or alternative A/C energy source, rectify and store the harvested energy on an external capacitor while maintaining a regulated output voltage. It can also bleed off any excess input power via an internal protective shunt regulator.

An internal full-wave bridge rectifier, accessible via AC1 and AC2 inputs, rectifies AC sources such as those from a piezoelectric element. The rectified output is stored on a capacitor at the V_{IN} pin and can be used as an energy reservoir for the buck converter. The bridge rectifier has a total drop of about 800mV at typical piezo-generated currents, but is capable of carrying up to 50mA.

When the voltage on V_{IN} rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled.

These thresholds can be set according to Table 4 of the data sheet which offers UVLO rising thresholds from 4V to 18V with large or small hysteresis windows.

Two internal rails, CAP and V_{IN2}, are generated from V_{IN} and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the V_{IN2} rail serves as logic high for output voltage select bits UV [3:0]. The V_{IN2} rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below V_{IN}. These are not intended to be used as external rails. Bypass capacitors should be connected to the CAP and V_{IN2} pins to serve as energy reservoirs for driving the buck switches. When V_{IN} is below 4.8V, V_{IN2} is equal to V_{IN} and CAP is held at GND. V_{IN3} is an internal rail used by the buck and the buck-boost. When the LTC3331 runs the buck, V_{IN3} will be a Schottky diode drop below V_{IN2}. When it runs as a buck-boost V_{IN3} is equal to BAT.

OPERATING PRINCIPLE

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 250mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. When the buck brings the output voltage into regulation, the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode, load current is provided by the buck output capacitor. When the output voltage falls below the regulation point, the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 50mA average load current when it is switching. V_{OUT} can be set from 1.8V to 5.0V via the output voltage select bits OUT [2:0] according to Table 1 of the data sheet.

The buck-boost uses the same hysteretic algorithm as the buck to control the output, V_{OUT}, with the same sleep comparator. The buck-boost has three modes of operation: buck, buck-boost and boost. An internal mode comparator determines the mode of operation based on BAT and V_{OUT}. In each mode, the inductor current ramps up to I_{PEAK} which is programmable via I_{PK} [2:0]. See Table 3 of the data sheet.

An integrated battery charger operating from the V_{IN2} rail charges the battery through the BB_IN pin. Connecting BB_IN to the BAT_OUT pin, an internal MOSFET Switch will then connect the battery charger to BAT_IN. The battery charger is a shunt regulator which can sink up to 10mA. The battery float voltage is programmable with two bits and a third bit is used to program the battery connect and disconnect voltage levels. This disconnect feature protects the battery from permanent damage by deep discharge. Disconnecting the battery from the BAT_OUT=BB_IN node prevents the load as well as the LTC3331 quiescent current from further discharging the battery.

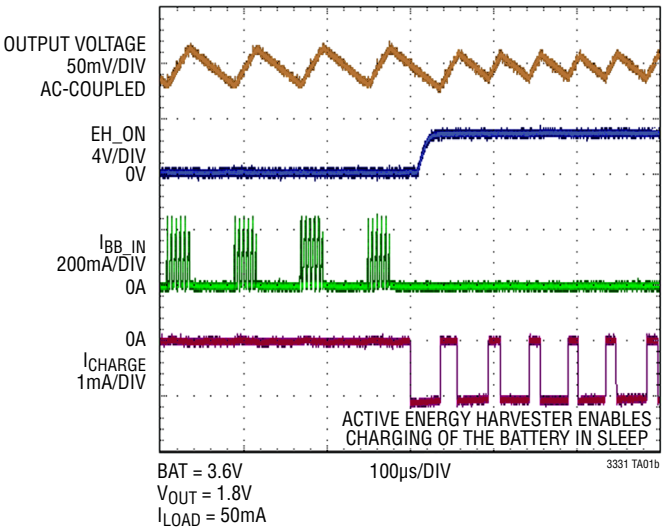

Figure 3. Charging Battery with Harvested Energy

A SHIP mode is provided which manually disconnects the battery. This may be helpful to prevent the battery from discharging when no harvestable energy is available for long periods of time, such as during shipping. Bring the SHIP pin high to engage the SHIP mode. To disengage the SHIP mode, bring the SHIP pin low. The BB_IN pin needs to be brought above the low battery connect (LBC) threshold to reconnect the battery.

Power good comparator, PGVOUT, produces a logic high referenced to the highest of V_{IN2}, BAT and V_{OUT} less a Schottky diode drop. PGVOUT will transition high the first time the respective converter reaches the programmed SLEEP threshold, signaling that the output is in regulation. The pin will remain high until the voltage falls to 92% of the desired regulated voltage.

An integrated supercapacitor balancer with 150nA of quiescent current is available to balance a stack of two supercapacitors. Typically the input, SCAP, will be tied to V_{OUT} to allow for increased energy storage at V_{OUT} with supercapacitors. The BAL pin is tied to the middle of the stack and can source or sink 10mA to regulate the BAL pin's voltage to half that of the SCAP voltage. To disable the balancer and its associated quiescent current, the SCAP and BAL pins can be tied to ground.

QUICK START PROCEDURE

Using short twisted pair leads for any power connections, with all loads and power supplies off, refer to Figure 4 for the proper measurement and equipment setup.

Follow the procedure below:

1. Before connecting PS1 to the DC2151A, PS1 must have its current limit set to 300mA and PS2 must have its current limit set to 100mA. For most power supplies with a current limit adjustment feature the procedure to set the current limit is as follows. Turn the voltage and current adjustment to minimum. Short the output terminals and turn the voltage adjustment to maximum. Adjust the current limit to 300mA for PS1 and 100mA for PS2. Turn the voltage adjustment to minimum and remove the short between the output terminals. The power supply is now current-limited to 300mA and 100mA respectively.
2. Initial Jumper, PS and LOAD settings:

   JP1 = 0 JP2 = 0 JP3 = 0 JP4 = 0

   JP5 = 0 JP6 = 0 JP7 = 0 JP8 = 0

   JP9 = 0 JP10 = 0

   JP11 = RUN JP12 = OFF

   PS1 = OFF PS2 = OFF LOAD1 = OFF

   Remove battery from battery holder
3. Connect PS1 to the V_{IN} Terminals, then turn on PS1 and slowly increase voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 5.0V.
4. Set LOAD1 to 50mA. Verify voltage on V_{OUT} is within the V_{OUT} 1.8V range listed in the Performance Summary. Verify that the output ripple voltage is between 10mV and 50mV. Verify that PGV_{OUT} is high. Decrease LOAD1 to 5mA. Verify that PGV_{OUT} and EH_ON are high. Decrease PS1 to 2.0V. Verify that V_{OUT} is 0V.
5. Set JP1, JP2, JP3, JP4 to 1. Slowly increase PS1 to 16V and verify that V_{OUT} is off. Increase PS1 to 19V and verify that V_{OUT} is within the V_{OUT} 1.8V range listed in the Performance Summary. Decrease PS1 to 4.0V. Verify that V_{OUT} is 0V.
6. Decrease PS1 to 0V and disconnect PS1 from V_{IN}. Set the current limit of PS1 to 25mA as described above.
7. Move the connection for PS1 from V_{IN} to AC1. Slowly increase PS1 voltage to 2.0V while monitoring the input current. If the current remains less than 5mA, increase PS1 to 19V. Verify voltage on V_{OUT} is within the V_{OUT} 1.8V range listed in the Performance Summary. Decrease PS1 to 0V, swap the AC1 connection to AC2 and repeat the test. Decrease PS1 to 0V and move the connection for PS1 from AC2 to V_{IN}.
8. Set JP5 to 1, JP6 to 1, and JP7 to 1. Increase PS1 to 19V and set LOAD1 to 50mA. Verify voltage on V_{OUT} is within the V_{OUT} 5.0V range listed in the Performance Summary. Verify that the output ripple voltage is between 40mV and 90mV. Set PS1 to 0V.
9. Set the current limit of PS2 to 60mA as described above. Set JP1 to 0, JP2, JP3 and JP4 to 1, JP5–JP7 to 1 and JP8–JP10 to 0. Set JP12 to CHARGE. Increase PS1 to 12V and set LOAD1 to 0mA. Connect PS2 to the BAT_IN Terminals, then turn on PS2 and slowly increase voltage to 1.0V while monitoring the input current. If the current remains less than 15mA, increase PS2 until V_{M4} reads 2.7V. Verify that the current in AM2 is approximately 660µA. Increase PS2 to 3.5V and verify that V_{M4} is approximately 3.45V.
10. Set JP8–JP10 to 1. Increase PS1 to 12V and set LOAD1 to 0mA. Set PS2 to 3.7V. Verify that the current in AM2 is approximately 330µA. Increase PS2 to 4.3V and verify that V_{M4} is approximately 4.2V.
11. Set JP12 to FAST_CHRG. Set PS2 to 3.7V. Verify that the current in AM2 is approximately 10mA. Set JP12 to CHARGE
12. Set the current limit of PS2 to 100mA as described above. Set PS1 to 14V. Set JP1 to 1, JP2, JP3 and JP4 to 0, JP5 to 0, JP6 and JP7 to 1. Set JP8 to 0. Set PS2 to 3.2V. Set LOAD1 to 5mA. Remove PS1 lead from the V_{IN} turret. Verify voltage on V_{OUT} is within the V_{OUT} 3.0V range listed in Performance Summary. Verify that PGV_{OUT} is high and EH_ON is low. Decrease PS2 to 2.6V and verify that V_{OUT} is 0V. Increase PS2 to 3.8V. Press and release PB1. Verify the V_{OUT} is 3.0V.

QUICK START PROCEDURE

13. Reconnect PS1 to V_{IN} turret. Set PS1 to 14V. Set JP8 to 1. Set PS2 to 3.8V. Set LOAD1 to 5mA. Remove PS1 lead from the V_{IN} turret. Verify voltage on V_{OUT} is within the V_{OUT} 3.0V range listed in Performance Summary. Verify that PGV_{OUT} is high and EH_ON is low. Decrease PS2 to 3.1V and verify that V_{OUT} is 0V. Increase PS2 to 4.3V. Press and release PB1. Verify the V_{OUT} is 3.0V.
14. Set JP11 to SHIP and verify that V_{OUT} is approximately 0V.
15. Decrease PS2 to 0V and disconnect PS2.
16. Set the current limit of PS1 to 300mA as described above. Connect PS1 to the V_{IN} Terminals. Set JP5 to 1, JP6 to 1 and JP7 to 1. Set PS1 to 14V. Set LOAD1 to 50mA. Add a jumper lead from V_{OUT} to SCAP. Verify that BAL is approximately half of V_{OUT}.
17. Quickly remove PS1+ lead from V_{IN} and verify that V_{OUT} remains above 1.2V for approximately 5 seconds.
18. Turn off PS1, PS2 and LOAD1. Reinstall battery in battery holder.

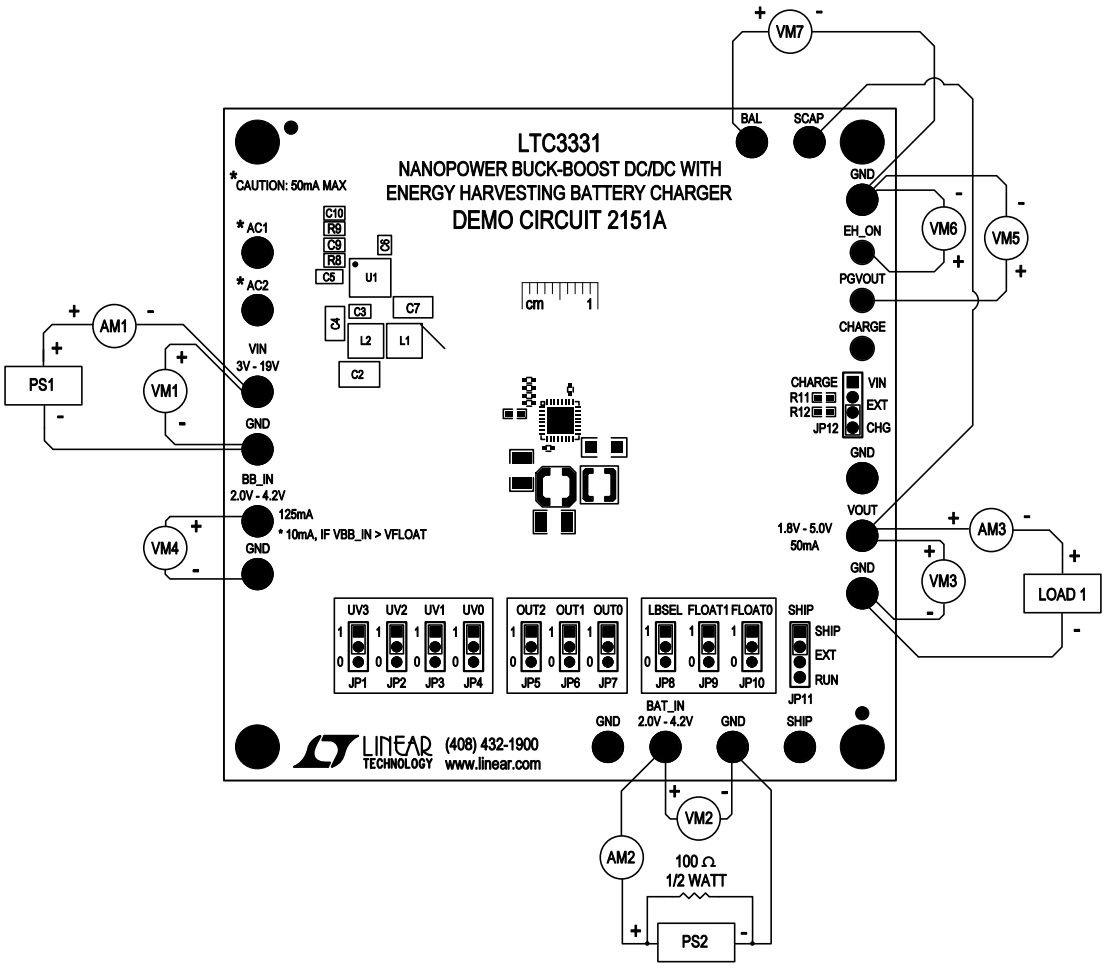

Figure 4. Proper Measurement Equipment Setup

CONNECTION TO A DUST MOTE (DC9003A-B)

Attach a Dust® Mote to J1 of the DC2151A, refer to Figure 5 for the proper setup. J1 is a keyed connector and is connected to the left side of the P1 connector on the DUST Mote. Figure 13 is a schematic of the Dust Mote and the DC2151A interconnections plus three extra connections which 1) connect the SCAP to V_{OUT}, 2) connect BAL to the middle of the supercapacitors and 3) connect EH_ON to OUT2. The DC2151A contains NC7SZ58P6X Universal Configurable 2-Input logic gates that are input voltage tolerant and allow level shifting between the LTC3331 and the Dust Mote.

Remove the battery from the BH1 holder on the bottom side of the DC2151A. On the DC2151A, set JP1 to 1, JP2 to 0, JP3 to 1, JP4 to 0, JP5 to1, JP6 to 0, JP7 to 0, JP8, JP9 and JP10 to 0, JP11 to RUN.

Piezoelectric Transducer Evaluation

Mount a series connected MIDE V25W to a vibration source and connect the electrical connections to the AC1 and AC2 turrets. Activate the vibration source to an acceleration of 1g and a frequency of 60Hz. Figure 6 shows an open-circuit voltage of 10.6V for the MIDE V25W piezoelectric device that was tuned to 60Hz. In order to set the VIN_UVLO_RISING and VIN_UVLO_FALLING thresholds, the open-circuit voltage of the piezoelectric device must be measured. The internal bridge network of the LTC3331 will have approximately 800mV drop at an input current of 300µA.

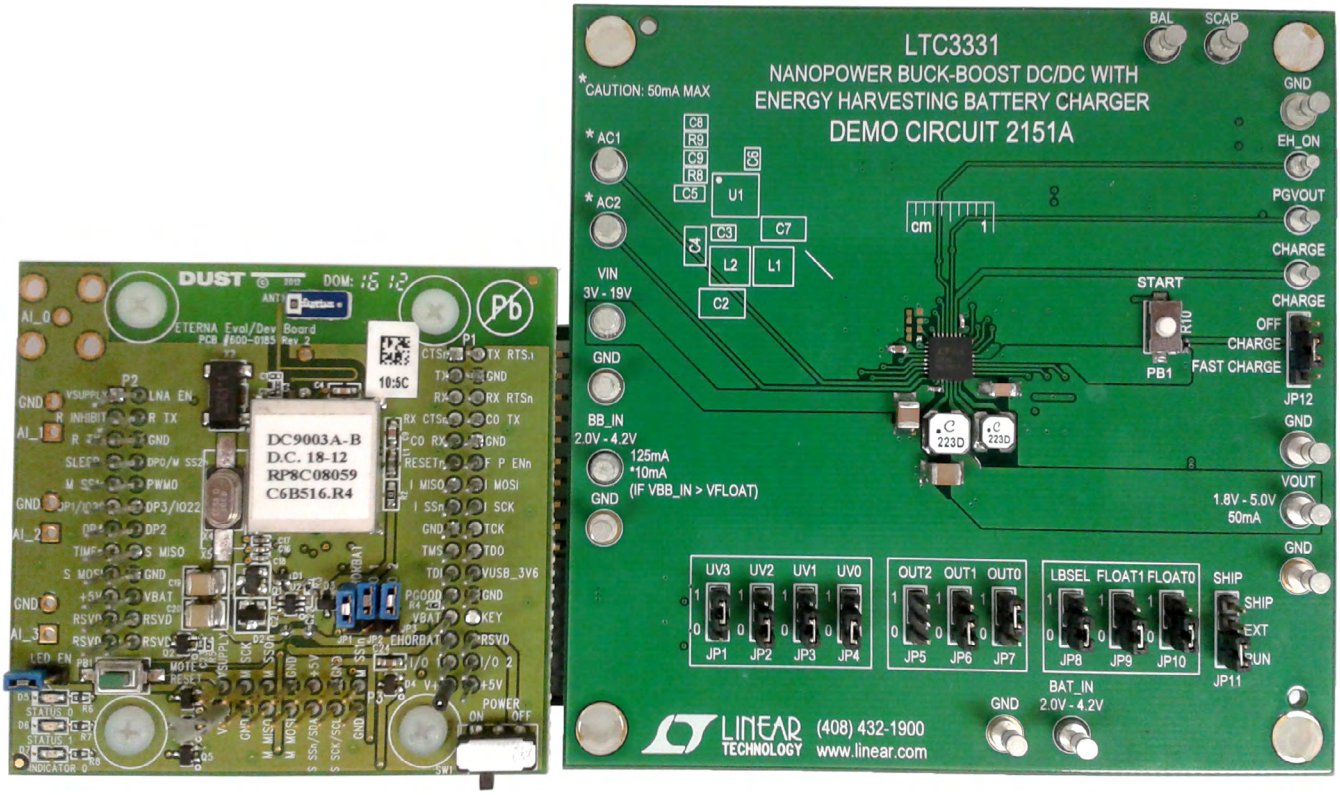

Figure 5. DC2151A with Dust Mote

CONNECTION TO A DUST MOTE (DC9003A-B)

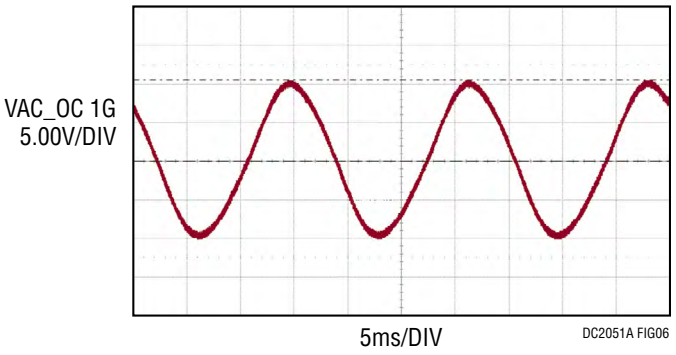

Figure 6. MIDE V25W Open-Circuit AC Voltage with 1grms, 60Hz Acceleration Applied

The peak-power-load voltage of a purely resistive source is at one-half of the rectified no-load voltage. In this case, the optimal average input-voltage regulation level would be 4.9V. Using a VIN_UVLO_RISING threshold of 6V and a VIN_UVLO_FALLING threshold of 5V (UV3 = 0, UV2 = 0, UV1 = 1, UV0 = 0) yields an average input voltage close to the theoretical optimal voltage.

Figure 7 is a plot of the output power and load voltage of the V25W piezoelectric transducer into a 42.2kΩ load for various rms acceleration levels. The output power

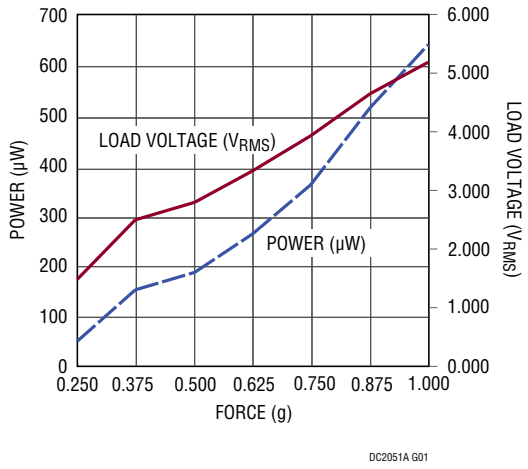

Figure 7. MIDE V25W Output Power into a 42.2kΩ Load with 1grms, 60Hz Acceleration Applied the MIDE V25W Piezoelectric Transducer, [$\sqrt{2}$ • sin(2π • 60Hz • t)]

compares well with the input power that is charging C_{IN} during the sleep cycle between VIN_UVLO_FALLING and VIN_UVLO_RISING thresholds at an acceleration force of $1g_{rms}$, shown in Figure 8 below.

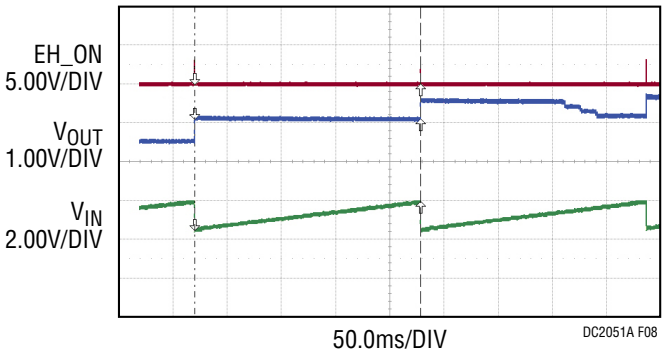

Figure 8. MIDE V25W Charging the 18µF input capacitance from 4.48V to 5.92V in 208ms

In Figure 8, the input capacitor is being recharged from the V25W piezoelectric transducer. The input capacitor is charging from 4.48V to 5.92V in 208 milliseconds. The power delivered from the V25W is 648µW.

$$P_{CIN} = \frac{C_{IN} \bullet (V_{IN1}^2 - V_{IN2}^2)}{2 \bullet \Delta t}$$

$$P_{CIN} = \frac{18\mu F \bullet (5.92^2 - 4.48^2)}{2 \bullet 208ms}$$

$$P_{CIN} = 648\mu W$$

Assuming that the circuit is configured as shown in Figure 9, it will take a significant amount of time for the piezo transducer to charge the 0.09F supercapacitor on the output of the LTC3331. As used above, the 22µF input capacitor is only 18µF at an applied voltage of 5V, so every VIN_UVLO_RISING and FALLING event produces 26 micro-coulombs [(5.92V – 4.48V) • 18µF)] that may be transferred from the input capacitor to the output capacitor,

CONNECTION TO A DUST MOTE (DC9003A-B)

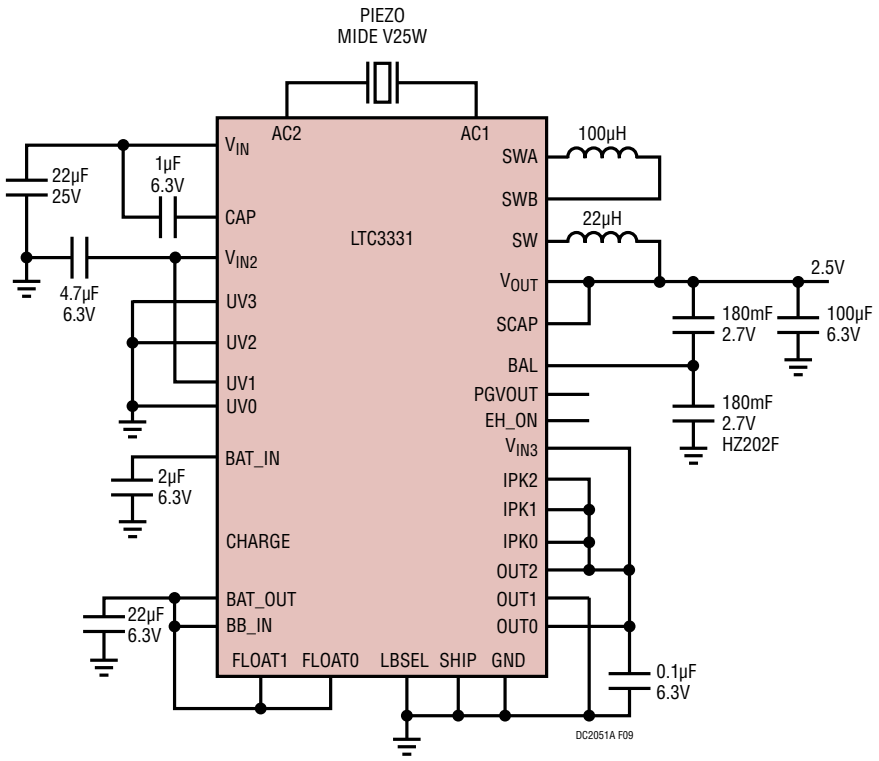

Figure 9. LTC3331 Circuit Charging Supercapacitor at No Load without a battery (Vout=3.6V)

minus the losses of the buck regulator in the LTC3331. The buck regulator efficiency is approximately 90% at V_{IN} equal to 5V and V_{OUT} between 2.5V and 3.6V. Thus, for every UVLO event, 23.3 micro-coulombs are added to the output supercapacitor. Given a 0.09F output supercapacitor charging to 3.6V, 324 milli-coulombs are required to fully charge the supercapacitor. Assuming no additional load on the output, it takes 13,906 (.324/23.3e^{-6}) UVLO events to charge the output supercapacitor to 3.6V. From Figure 8, it can be observed that each VIN_UVLO event takes 208ms, so the total time to charge the output capacitor from 0V to 3.6V will be greater than 2900 seconds. Figure 10 shows the no-load charging of the output supercapacitor, which takes approximately 3300 seconds. The above calculation neglects the lower efficiency at low output voltages and the time it takes to transfer the energy from the input capacitor to the output supercapacitor, so predicting the actual value within –12% is to be expected.

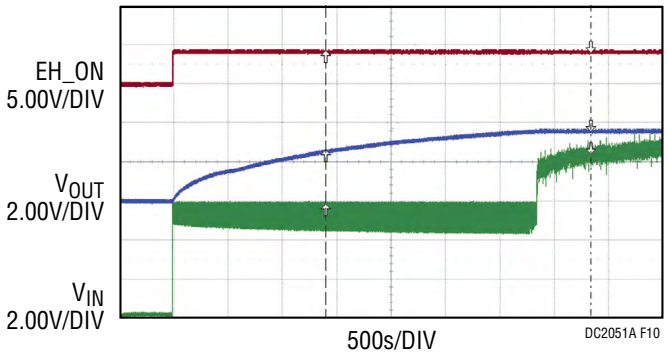

Figure 10. Scope Shots of LTC3331 Charging Supercapacitor at No Load without a Battery (V_{out} = 3.6V)

CONNECTION TO A DUST MOTE (DC9003A-B)

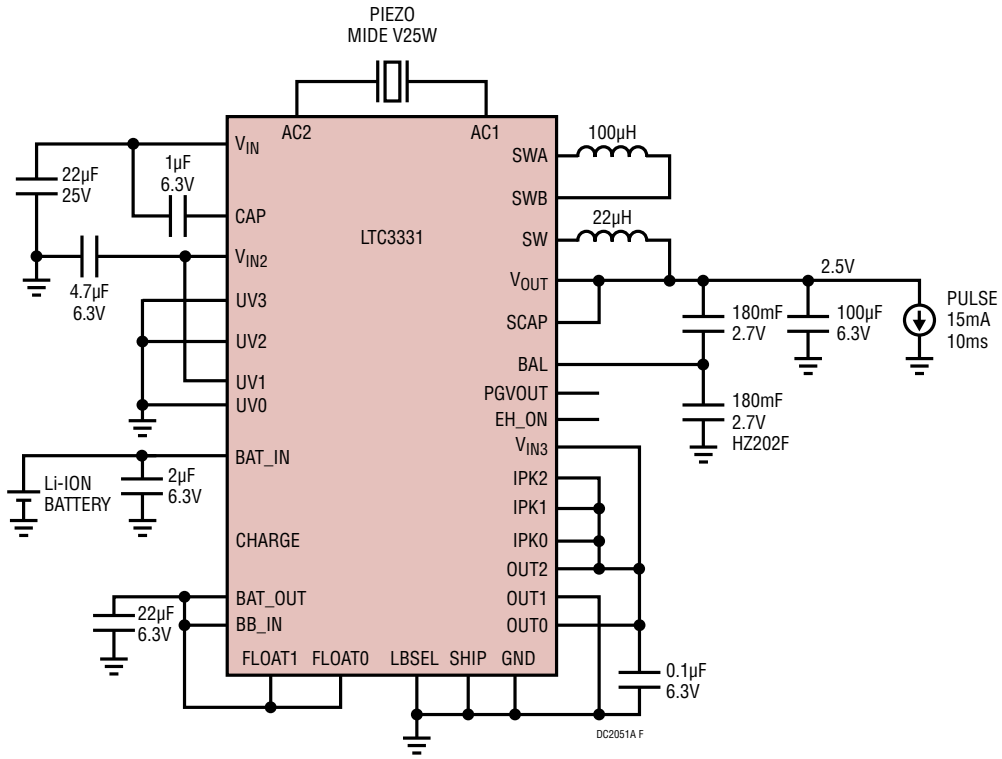

Figure 11. LTC3331 Circuit with a Supercapacitor, a Battery installed and a pulsed load applied (Vout=3.6V)

Figure 11 shows the LTC3331 with a supercapacitor on the output, a battery installed and the output voltage set to 3.6V. The scope shots in Figure 12 were taken after applying a pulsed load of 15mA for 10ms. With the battery attached and a pulsed load applied, the EH_ON signal will switch back and forth from high to low every time the V_{IN} voltage transitions from the VIN_UVLO_RISING to the VIN_UVLO_FALLING threshold. When the pulsed load is applied, the output capacitor is depleted slightly and the input capacitor must recharge the output cap. Because the input capacitance is much less then the output capacitance, the input capacitor will go through many UVLO transitions to charge the output capacitor back up to the sleep threshold. Once the output is charged to the output sleep threshold, the EH_ON signal will again be consistently high indicating that the energy harvesting source is powering the output.

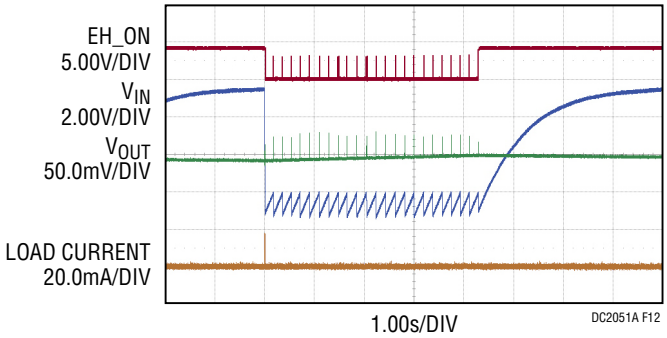

Figure 12. Charging a Supercapacitor with a battery installed and a pulsed load (Vout=3.6V)

CONNECTION TO A DUST MOTE (DC9003A-B)

Figure 13 shows the LTC3331 with an output supercapacitor, a Dust Mote attached, a battery installed and EH_ON connected to OUT2. In this configuration, when EH_ON is low, V_{OUT} will be set to 2.5V and when EH_ON is high, V_{OUT} will be set to 3.6V.

The first marker in Figure 14 is where the vibration source was activated; V_{IN} then rises above the VIN_UVLO_RISING threshold. EH_ON will then go high causing V_{OUT} to rise towards 3.6V (V_{OUT} started at 2.5V because the battery had charged it up initially). At the same time EH_ON goes high, PGVOUT will go low, since the new V_{OUT} level of 3.6V has not been reached. As the charge on V_{IN} is being transferred to V_{OUT}, V_{IN} is discharging and when V_{IN} reaches its UVLO_FALLING threshold, EH_ON will go

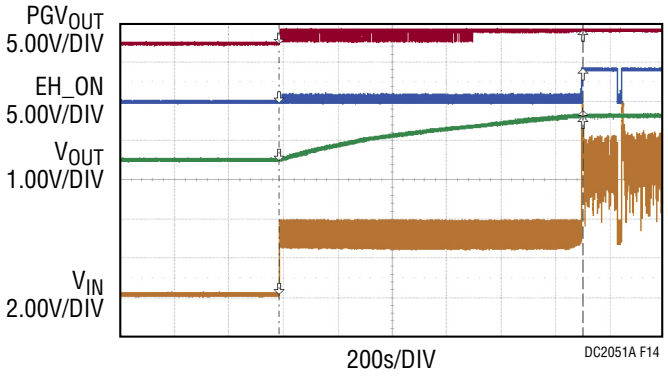

Figure 14. MIDE 25W Charging Output Supercapacitor from 2.5V to 3.6 V with DUST Mote Attached

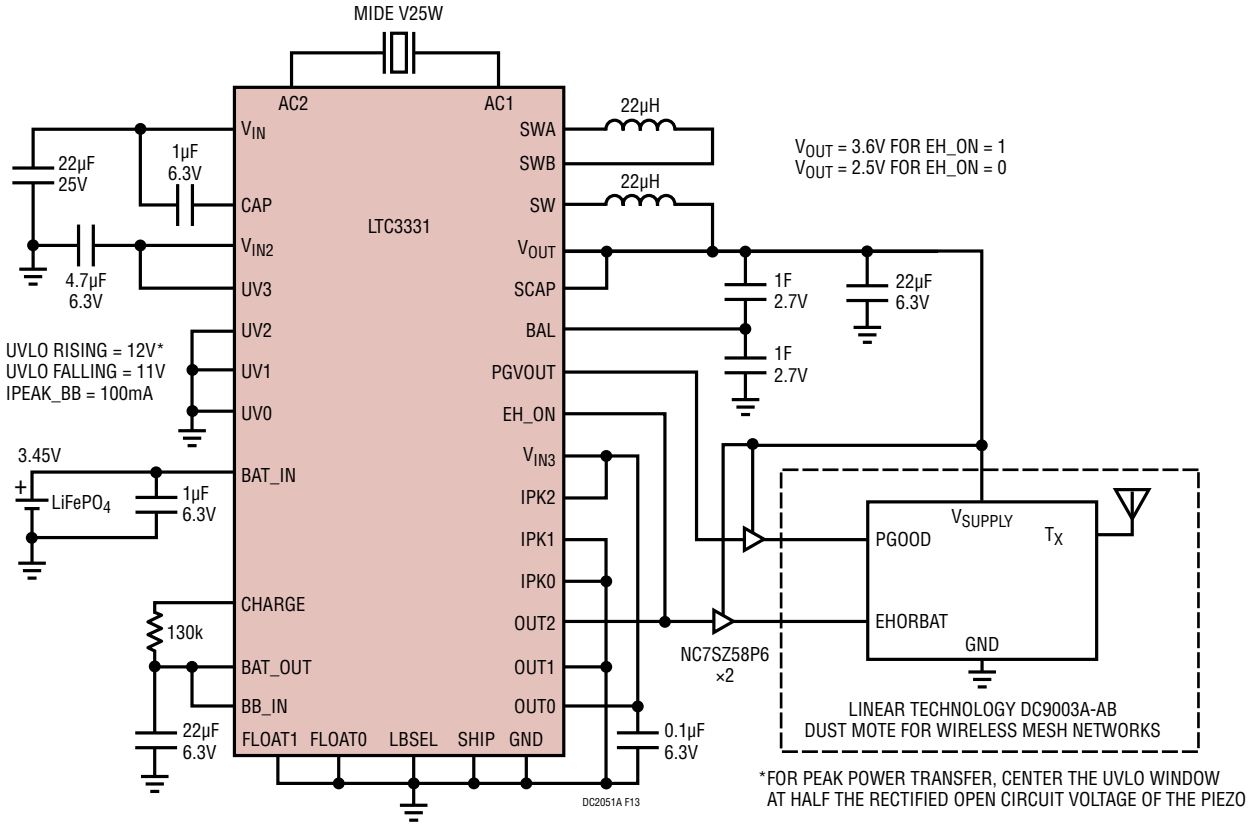

Figure 13. Dust Mote Setup with a Supercapacitor, a battery and EH_ON connected to OUT2

CONNECTION TO A DUST MOTE (DC9003A-B)

low, causing the targeted V_{OUT} to again be 2.5V. Given that the output capacitor is very large and the average load is less than the input power supplied by the MIDE piezoelectric transducer, the output voltage will increase to the higher setpoint of 3.6V over many cycles. During the transition from the BAT setpoint of 2.5V to the energy harvester setpoint of 3.6V, V_{OUT} is above the 2.5V PGVOUT threshold, hence, PGVOUT will go high every time EH_ON goes low. This cycle will be repeated until V_{OUT} reaches the PGVOUT threshold for the V_{OUT} setting of 3.6V. When a pulse load is applied that is greater than the energy supplied by the input capacitor, V_{IN} will drop below the VIN_UVLO_FALLING threshold, EH_ON will go low and the buck-boost regulator will be ready to support the load requirement from the battery, but will not start to switch until the supercapacitor is discharged to 2.5V. In this way, the circuit can store a lot of harvested energy and use it for an extended period of time before switching over to the battery energy. The supercapacitor could be sized to accommodate known repeated periods of time that the energy harvester source will not be available, such as overnight when a vibrating machine is turned off or, in the case of a solar application, when the lights are turned off or the sun goes down.

While the EH_ON signal is low, the buck-boost circuit will consume 750nA from the battery in the sleeping state. The effects of a pulsed load are shown in Figure 14 at approximately 1850 seconds, where V_{IN} is discharged and the EH_ON signal pulses low to high for a brief period of time, which occurred as a result of the Dust Mote radio making a data transmission.

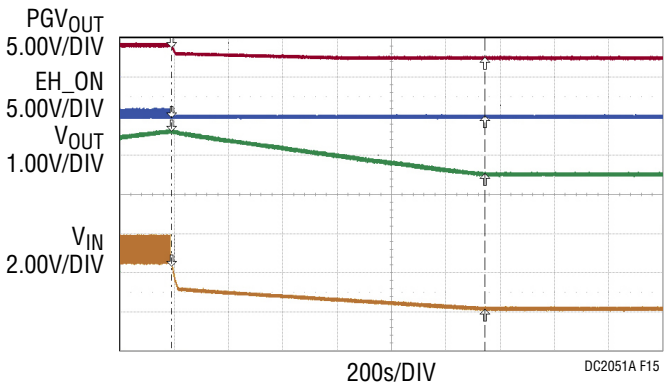

Figure 15. Output Supercapacitor Discharging when the vibration source is switched off

Figure 15 shows the discharging of V_{OUT} when the vibration source is removed and V_{IN} drops below the UVLO_FALLING threshold, causing EH_ON to go low. The supercapacitor on V_{OUT} will discharge down to the new target voltage of 2.5V, at which point the buck-boost regulator will turn on, supplying power to the Dust Mote. The discharging of the supercapacitor on V_{OUT} provides an energy source for short term loss of the vibration source and extends the life of the battery.

Figure 16 is the same Dust mote configuration as Figure 13 but without the output supercapacitor. Figure 17 shows the charging of the output without the supercapacitor attached.

CONNECTION TO A DUST MOTE (DC9003A-B)

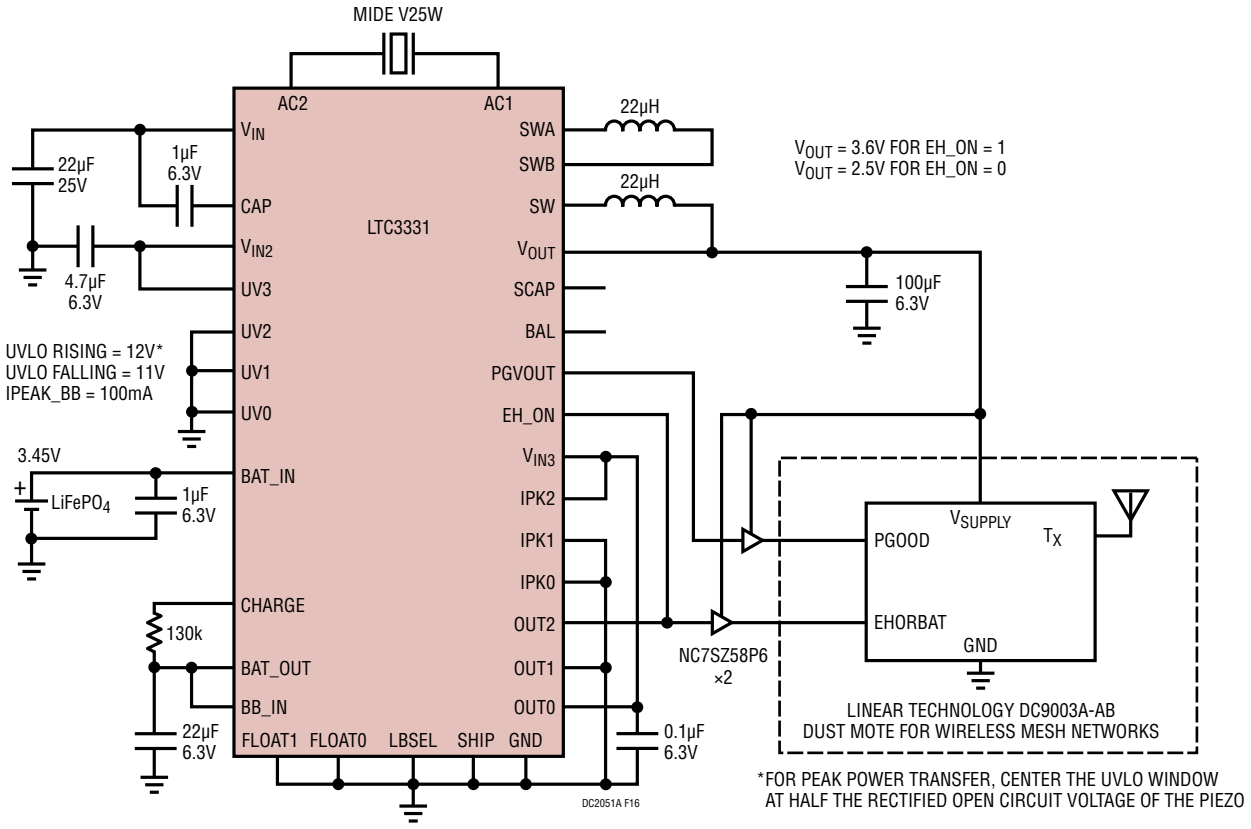

Figure 16. Dust Mote Setup without a Supercapacitor and with EH_ON Connected to OUT2

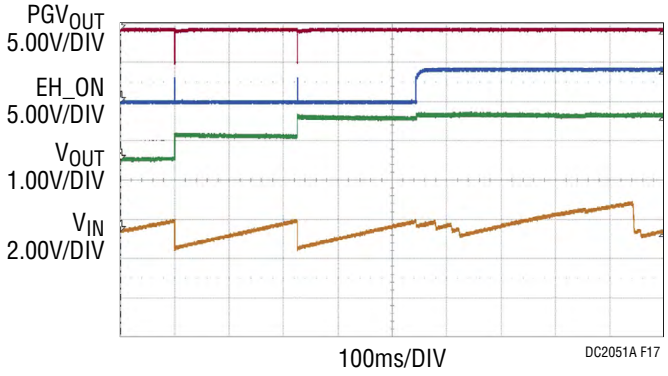

Figure 17. Output Voltage Charging with Dust Mote Attached without Supercapacitor

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	BAT1	CR2032 COIN LI-ION BATTERY	POWERSTREAM, Lir2032
2	1	BTH1	BATTERY HOLDER COIN CELL 2032 SMD	MPD INC, BU2032SM-HD-G
3	1	C1	SUPERCAP, 90mF, 5.5V, 20mm x 15mm	CAP-XX, HZ202F-1
4	1	C2	CAP, CHIP, X5R, 150µF, 20%, 6.3V, 1210	SAMSUNG, CL32A157MQVNNNE
5	1	C3	CAP, CHIP, X5R, 1µF, 10%, 6.3V, 0402	SAMSUNG, CL05A105KQ5NNNC
6	1	C4	CAP, CHIP, X5R, 22µF, 10%, 25V, 1210	SAMSUNG, CL32A226KAJNNNE
7	1	C5	CAP, CHIP, X5R, 4.7µF, 10%, 6.3V, 0603	SAMSUNG, CL10A475KQ8NNNC
8	1	C6	CAP, CHIP, X5R, 0.1µF, 10%, 10V, 0402	TDK, C1005X5R1A104K
9	1	C7	CAP, CHIP, X5R, 22µF, 20%, 6.3V, 1206	SAMSUNG, CL31A226MQHNNNE
10	1	L1	INDUCTOR, 22µH, 0.800A, 0.36Ω, 3.9mm x 3.9mm	COILCRAFT, LPS4018-223MLB
11	1	L2	INDUCTOR, 22µH, 0.75A, 0.19Ω, 4.8mm x 4.8mm	COILCRAFT, LPS5030-223MLB
12	3	R2, R4, R6	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0EA
13	1	R10	RES, CHIP, 3.01K, 1/16W, 1%, 0402	VISHAY, CRCW04023K01FKED
14	1	U1	NANOPOWER BUCK-BOOST DC/DC WITH EH BATTERY CHARGER	LINEAR TECHNOLOGY, LTC3331EUH#TRPBF
Additional Demo Board Circuit Components				
1	0	C8, C9	CAP, CHIP, X5R, 0.1µF, 10%, 10V, 0402 (OPT)	TDK, C1005X5R1A104K
2	0	C10	SUPERCAP/ULTRACAPACITOR, 330mF, 5.5V, 60mΩ DOUBLE CELL	MURATA, DMF3R5R5L334M3DTA0
3	1	D1	DIODE, SCHOTTKY, 30V, 0.1A, SOD-523	CENTRAL, CMOSH-3
4	0	BTH2	SMT, CR2477 BATTERY HOLDER	RENATA, SMTU2477-1
5	1	R1	RES, CHIP, 100Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402100RFKED
6	0	R3, R5, R7	RES, CHIP, 0Ω, 0603 (DNP)	VISHAY, CRCW06030000Z0EA
7	0	R8, R9	RES, CHIP, 7.5K, 1/16W, 1%, 0402	VISHAY, CRCW04027K50FKED
8	1	R11	RES, CHIP, 56.2Ω, 1/16W, 1%, 0402	VISHAY, CRCW040256R2FKED
9	2	R12, R14	RES, CHIP, 1.00M, 1/16W, 1%, 0402	VISHAY, CRCW04021M00FKED
10	1	R13	RES, CHIP, 100K, 1/16W, 1%, 0402	VISHAY, CRCW0402100KFKED
11	1	Q1	SMT, DUAL MOSFET, NCHANNET/PCHANNET, 60V, SuperSOT-6	FAIRCHILD, NDC7001C
12	1	Q2	SMT, BIPOLAR, PNP, 60V, SOT-23	CENTRAL, CMPT3906E
13	2	U2, U3	IC, UHS UNIV. CONFIG. TWO-INPUT GATES, SC70-6	FAIRCHILD, NC7SZ58P6X
1	13	E1-E6, E10-E17	TURRET, 0.09 DIA	MILL-MAX, 2501-2-00-80-00-00-07-0
2	3	E7-E9	TURRET, 0.061 DIA	MILL MAX, 2308-2-00-80-00-00-07-0
3	1	J1	HEADER, 12 PIN, DUST HEADER 2X6	SAMTEC, SMH-106-02-L-D-05
4	10	JP1-JP10	HEADER, 3 PIN 0.079 SINGLE ROW	WURTH, 62000311121
5	2	JP11, JP12	HEADER, 4 PIN 0.079 SINGLE ROW	WURTH, 62000411121
6	12	JP1-JP12	SHUNT, 2mm	WURTH, 60800213421

SCHEMATIC DIAGRAM

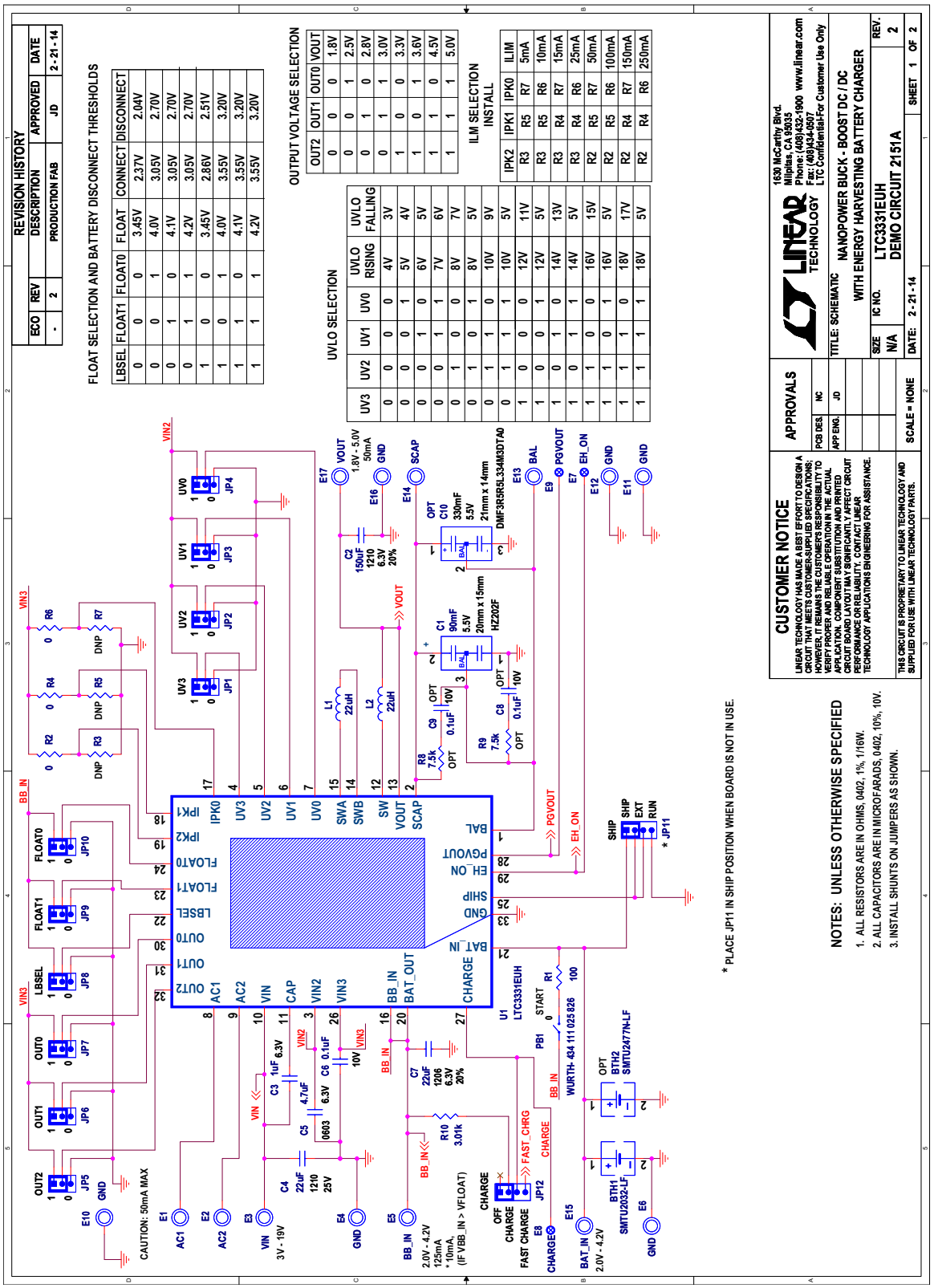

Figure 18. DC2151A Demo Circuit Schematic, Page 1

SCHEMATIC DIAGRAM

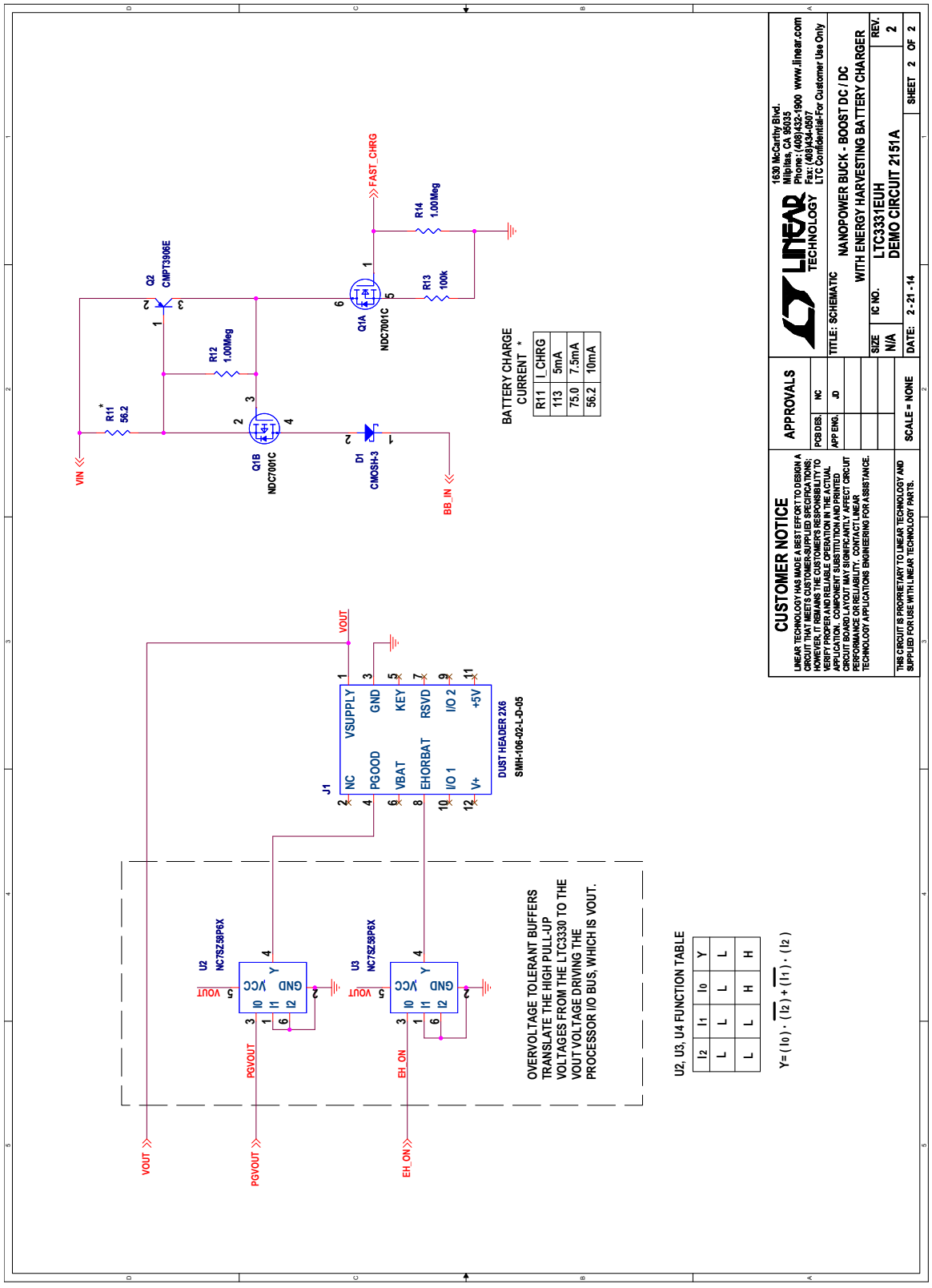

Figure 19. DC2151A Demo Circuit Schematic, Page 2

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