PE29101

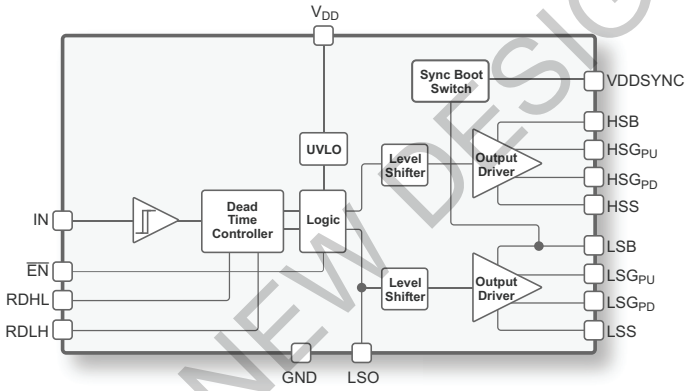
Document Category: Product Specification

UltraCMOS® High-speed FET Driver, 40 MHz

Features

- High- and low-side FET drivers
- Dead-time control
- Fast propagation delay, 11 ns
- Internal gate overvoltage management
- Sub-nanosecond rise and fall time
- 2A/4A peak source/sink current
- Package – flip chip

Figure 1 ▪ PE29101 Functional Diagram



Applications

- DC–DC conversions
- AC–DC conversions
- Wireless power
- LiDAR

Product Description

The PE29101 integrated high-speed driver is designed to control the gates of external power devices, such as enhancement mode gallium nitride (GaN) FETs. The outputs of the PE29101 are capable of providing switching transition speeds in the sub-nanosecond range for switching applications up to 40 MHz. High switching speeds result in smaller peripheral components and enable new applications such as wireless power charging.

The PE29101 operates from 4V to 6.5V and can support a high side floating supply voltage of 80V. An optional internal synchronous bootstrap circuit limits overcharging of the bootstrap capacitor during reverse body diode conduction, preventing the GaN FETs from exceeding their maximum gate-to-source voltage rating. The PE29101 also features a dead-time controller that allows timing of the LS and HS gates to eliminate any large shoot-through currents that could dramatically reduce the efficiency of the circuit and potentially damage the transistors.

The PE29101 is available in a flip chip package and is manufactured on Peregrine's UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ▪ Absolute Maximum Ratings for PE29101

Parameter/Condition	Min	Max	Unit
Low-side bias (LSB) to low-side source (LSS)	–0.3	7	V
High-side bias (HSB) to high-side source (HSS)	–0.3	7	V
Input signal	–0.3	7	V
HSS to LSS	–5	100	V
ESD voltage HBM(*), all pins		1000	V
Note: * Human body model (JEDEC JS–001, Table 2A).			

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE29101. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Conditions for PE29101

Parameter	Min	Typ	Max	Unit
Supply for driver front-end, V_{DD}	4.0	5.0	6.5	V
Supply for high-side bias (HSB) to high-side source (HSS)	4.0	5.0	6.5	V
Supply for low-side bias (LSB) to low-side source (LSS)	4.0	5.0	6.5	V
Logic HIGH for control input	1.6		6.5	V
Logic LOW for control input	0		0.6	V
HSS range	0		80	V
Operating temperature	–40		+105	°C
Junction temperature	–40		+125	°C

Electrical Specifications

Table 3 provides the key electrical specifications @ +25 °C, V_{DD} = 5V, 100 pF load; RDHL and RDLH are ±1% tolerance unless otherwise specified.

Table 3 ▪ DC Characteristics

Parameter	Condition	Min	Typ	Max	Unit
DC Characteristics					
V_{DD} quiescent current	V_{DD} = 5V, RDHL = RDLH = 80.6 kΩ		0.9		mA
HSB quiescent current	HSB = 5V		2.5		mA
LSB quiescent current	LSB = 5V		2.5		mA
Total quiescent current	V_{DD} =HSB=LSB=5V, RDHL = RDLH = 80.6 kΩ		5.9	8.0	mA
V_{DD} quiescent current	V_{DD} = 6.5V, RDHL = RDLH = 80.6 kΩ		1.3		mA
HSB quiescent current	HSB = 6.5V		3.8		mA
LSB quiescent current	LSB = 6.5V		3.9		mA
Total quiescent current	V_{DD} =HSB=LSB=6.5V, RDHL = RDLH = 80.6 kΩ		9.0	11.5	mA
Under Voltage Lockout					
Under voltage release (rising)			3.6	3.9	V
Under voltage hysteresis			400		mV
Gate Drivers					
HSG_{PU}/LSG_{PU} pull-up resistance	V_{DD} = 6.5V, RDHL = RDLH = 80.6 kΩ		1.8		Ω
HSG_{PD}/LSG_{PD} pull-down resistance	V_{DD} = 6.5V		1.5		Ω
VDDSYNC resistance			4.5		Ω
HSG_{PU}/LSG_{PU} leakage current	HSB–HSG_{PU} = 5V, LSB–LSG_{PU} = 5V		10		µA
HSG_{PD}/LSG_{PD} leakage current	HSG_{PD}–HSS = 5V/LSG_{PD}–HSS = 5V		50		µA
Dead-time Control					
Dead-time control voltages	HSB=LSB, 80.6 kΩ resistor to GND		1.4		V
Dead-time from HSG going low to LSG going high	RDHL = 30 kΩ		0.8		ns
	RDHL = 80.6 kΩ		3.3		ns
	RDHL = 150 kΩ		6.5		ns
	RDHL = 255 kΩ		11.1		ns

Table 3 ▪ DC Characteristics (Cont.)

Parameter	Condition	Min	Typ	Max	Unit
Dead-time from LSG going low to HSG going high	RDLH = 30 kΩ		0.2		ns
	RDLH = 80.6 kΩ		2.6		ns
	RDHL = 150 kΩ		5.6		ns
	RDHL = 255 kΩ		10.0		ns
Switching Characteristics					
LSG turn-off propagation delay			11.0		ns
HSG rise time	10%–90% with 100pF load		1.0		ns
LSG rise time	10%–90% with 100pF load		1.0		ns
HSG fall time	10%–90% with 100pF load		1.0		ns
LSG fall time	10%–90% with 100pF load		1.0		ns
Minimum output pulse width	RDLH = RDLH = 30 kΩ		2.0	4.0	ns
Max switching frequency @ 50% duty cycle	RDHL = RDLH = 80.6 kΩ	40	47		MHz

Control Logic

Table 4 provides the control logic truth table for the PE29101.

Table 4 ▪ Truth Table for PE29101

$\overline{EN}$	IN	HSG_{PU}–HSS	HSG_{PD}–HSS	LSG_{PU}–LSS	LSG_{PD}–LSS
L	L	Hi–Z	L	H	Hi–Z
L	H	H	Hi–Z	Hi–Z	L
H	L	Hi–Z	L	Hi–Z	L
H	H	Hi–Z	L	Hi–Z	L

Typical Performance Data

Figure 2 through **Figure 4** show the typical performance data @ +25 °C, VDD = 5V, load = 100 pF capacitor, unless otherwise specified.

Figure 2 ▪ Total Quiescent Current

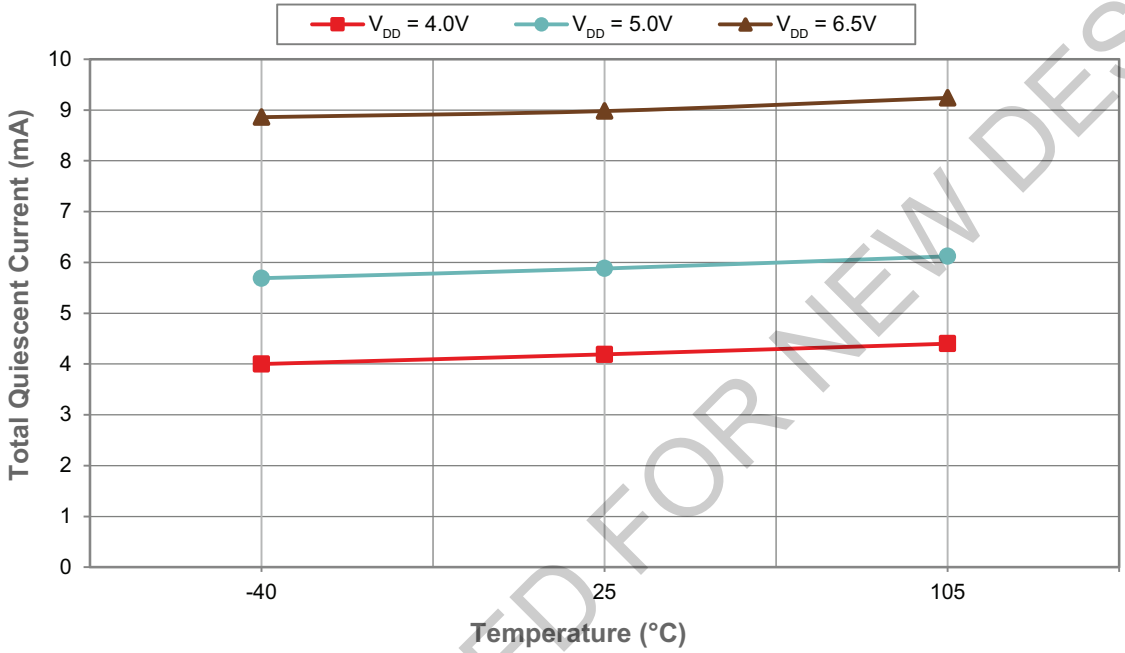


Figure 3 ▪ UVLO Threshold

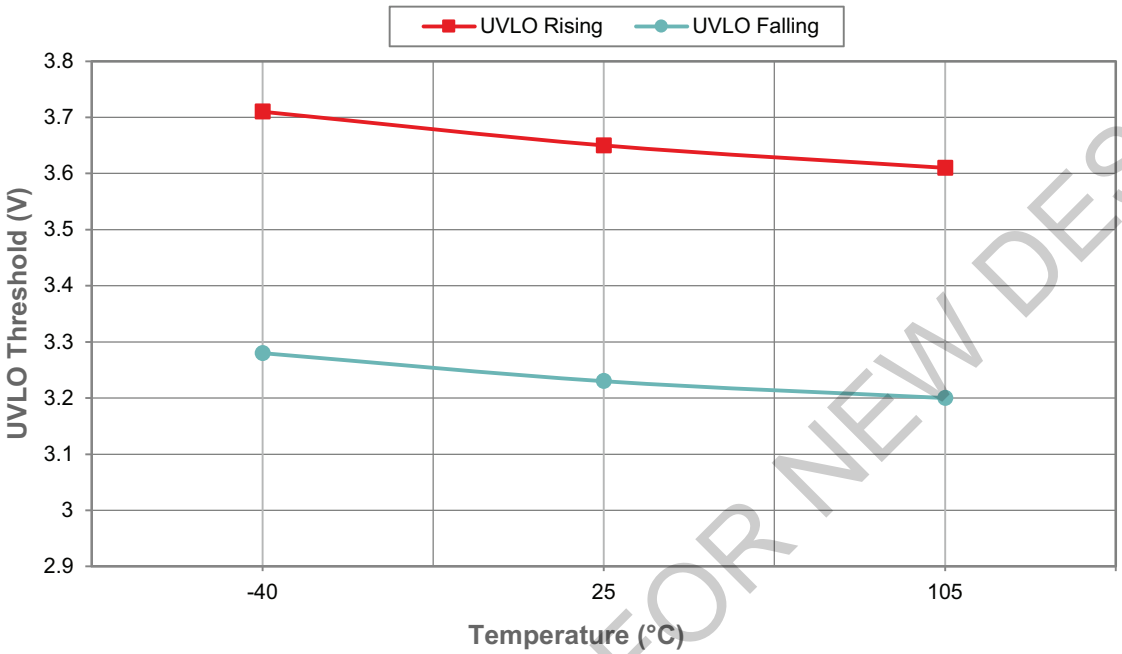
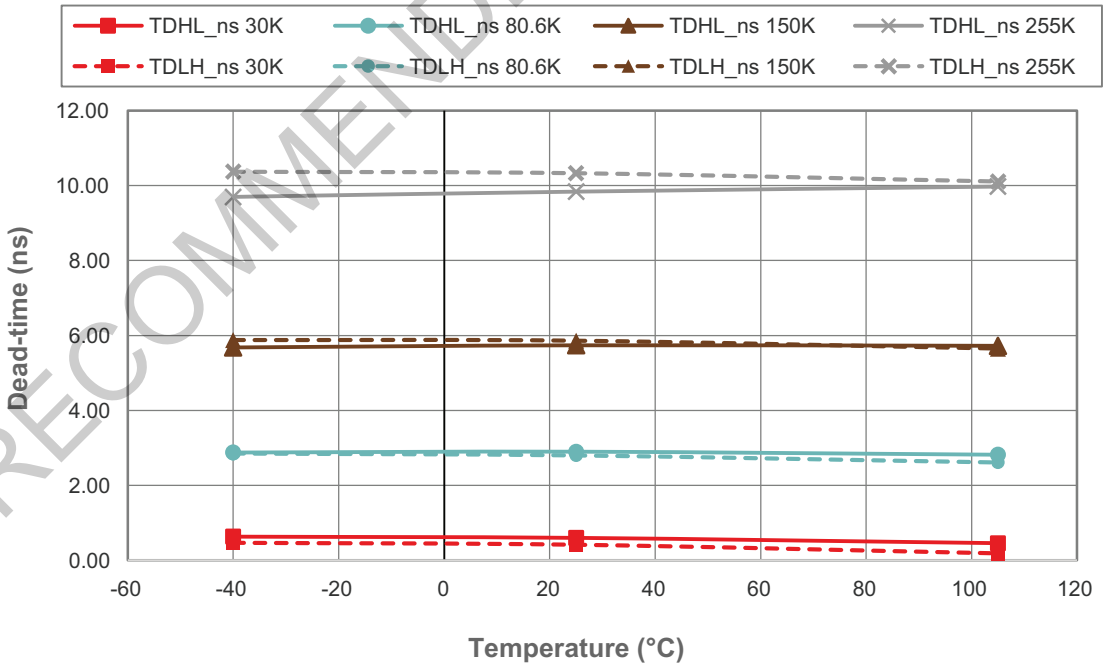


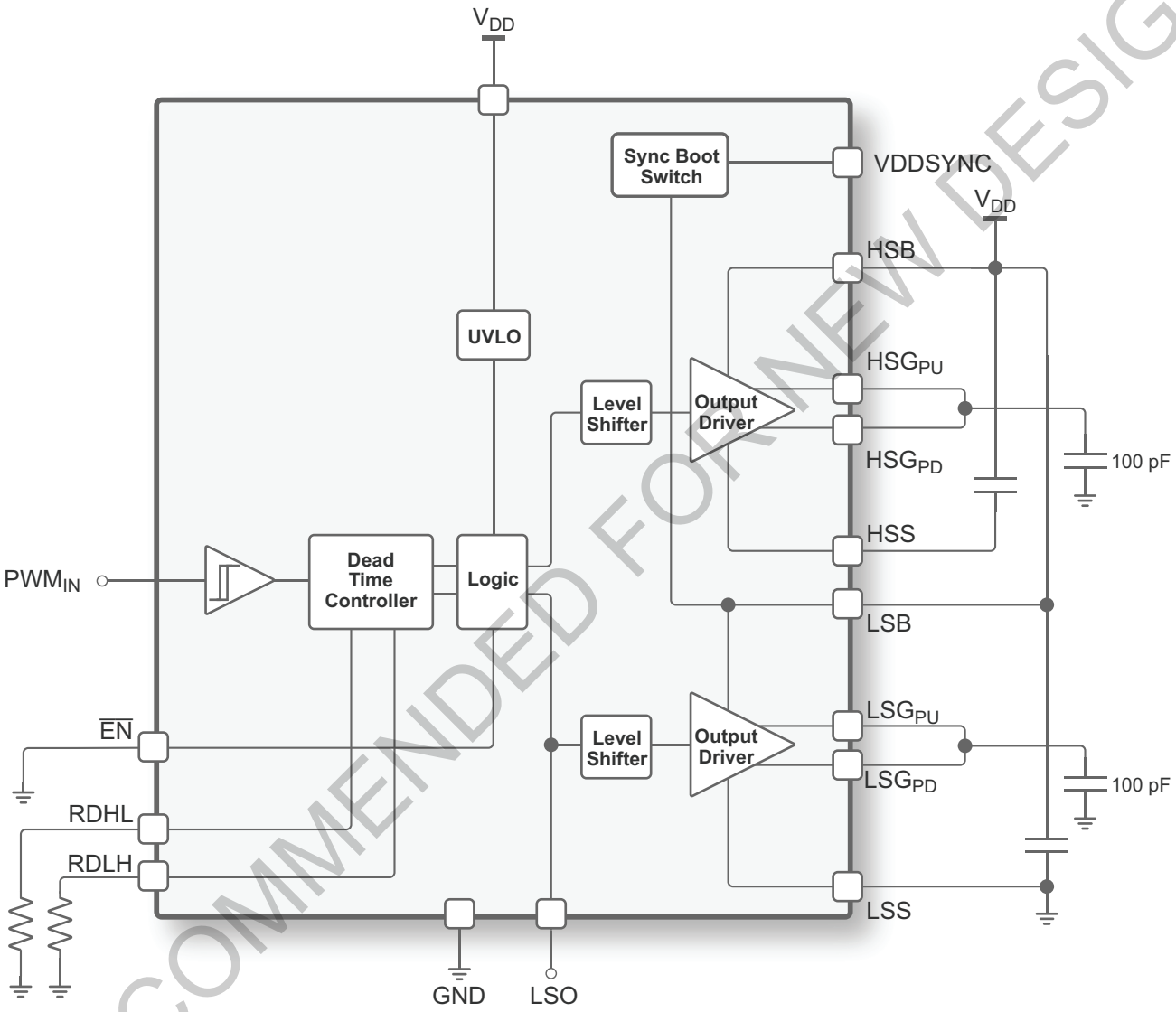
Figure 4 ▪ Dead Time



Test Diagram

Figure 5 shows the test circuit used to characterize the PE29101.

Figure 5 ▪ Test Circuit for PE29101



Theory of Operation

General

The PE29101 is intended to drive both the high-side (HS) and the low-side (LS) gates of external power transistors, such as enhancement-mode GaN FETs, for power management applications. The PE29101 is suited for applications requiring higher switching speeds due to the reduced parasitic properties of the high resistivity insulating substrate inherent with Peregrine's UltraCMOS process.

The driver uses a single-ended pulse width modulation (PWM) input that feeds a dead-time controller, capable of generating a small and accurate dead-time. The propagation delay of the dead-time controller must be small to meet the fast switching requirements when driving GaN FETs. The differential outputs of the dead-time controller are then level-shifted from a low-voltage domain to a high-voltage domain required by the output drivers.

Each of the output drivers includes two separate pull-up and pull-down outputs allowing independent control of the turn-on and turn-off gate loop resistance. The low impedance output of the drivers improves external power FETs switching speed and efficiency, and minimizes the effects of the voltage rise time (dv/dt) transients.

Under-voltage Lockout

An internal under-voltage lockout (UVLO) feature prevents the PE29101 from powering up before input voltage rises above the UVLO threshold of 3.6V (typ), and 400 mV (typ) of hysteresis is built in to prevent false triggering of the UVLO circuit. The UVLO must be cleared and the $\overline{EN}$ pin must be released before the part will be enabled.

Dead-time Adjustment

The PE29101 features a dead-time adjustment that allows the user to control the timing of the LS and HS gates to eliminate any large shoot-through currents, which could dramatically reduce the efficiency of the circuit and potentially damage the GaN FETs. Two external resistors control the timing of outputs in the dead-time controller block. The timing waveforms are illustrated in **Figure 6**.

The dead-time resistors only affect the LS output; the HS output will always equal the duty-cycle of the input. The HS FET gate node will track the duty cycle of the PWM input, as both rising and falling edges are shifted in the same direction. The LS FET gate node duty cycle can be controlled with the dead-time resistors as each resistor will move the rising and falling edges in opposite directions. RDLH will change the dead-time from low-side gate (LSG) falling to high-side gate (HSG) rising and RDHL will change the dead-time from HSG falling to LSG rising. **Figure 7** shows the resulting dead-time versus the external resistor values

High-side Gate Overvoltage Protection

In cases where the GaN transistor body diode conduction is significantly longer than the bootstrap diode turn-on time, overcharging of the bootstrap capacitor can develop. The resulting overvoltage on the high-side supply may exceed the specified operating range of the transistor. The PE29101 features an internal synchronous bootstrap protection circuit (pin 4) designed to limit overcharging of the bootstrap capacitor during reverse body diode conduction.

Figure 6 and **Figure 7** provide the dead-time description for the PE29101.

Figure 6 ▪ Typical Dead-time Description

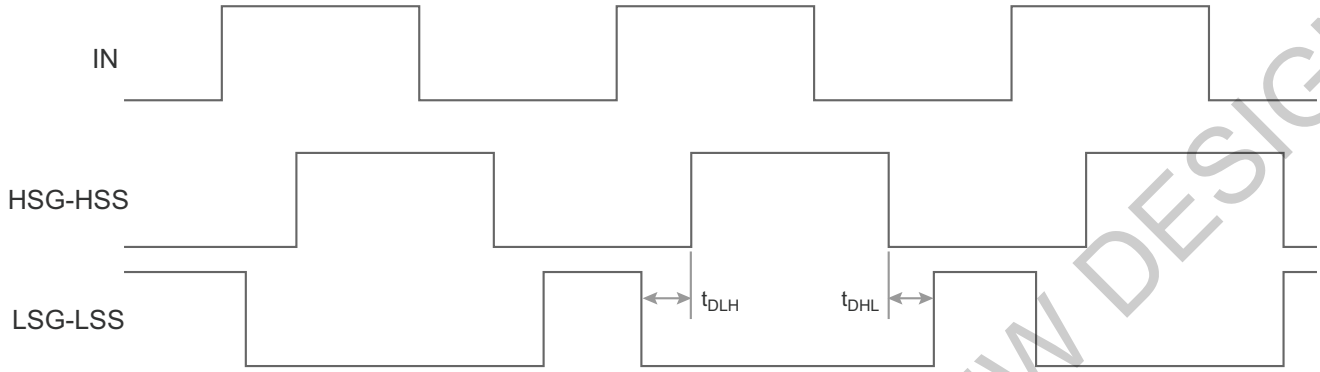
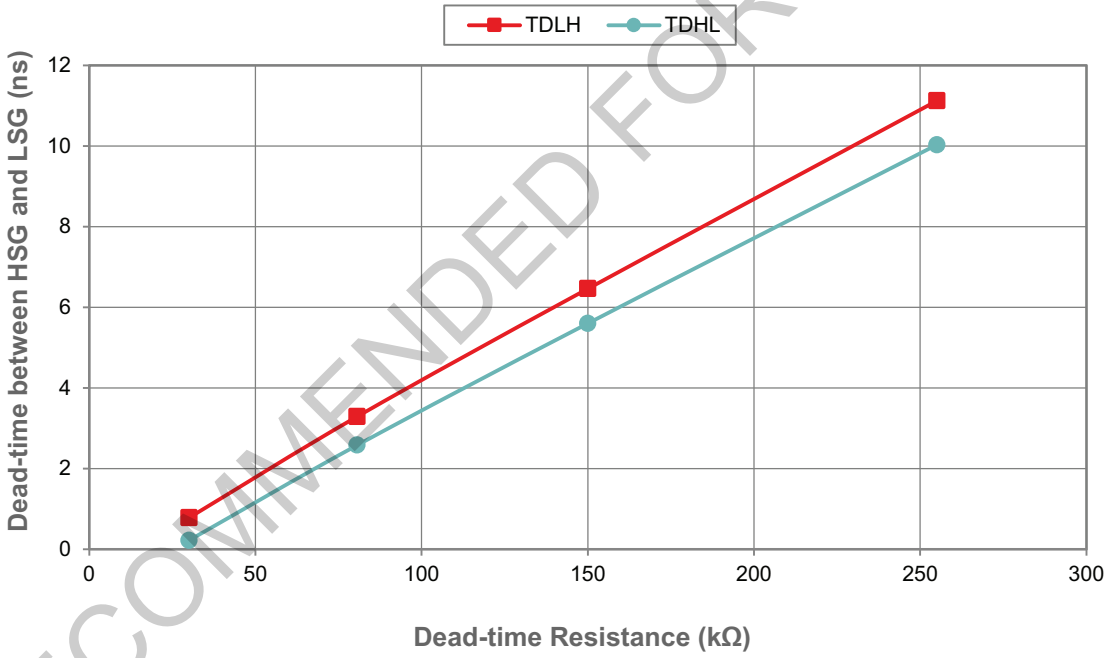


Figure 7 ▪ Dead-time vs. Dead-time Resistor

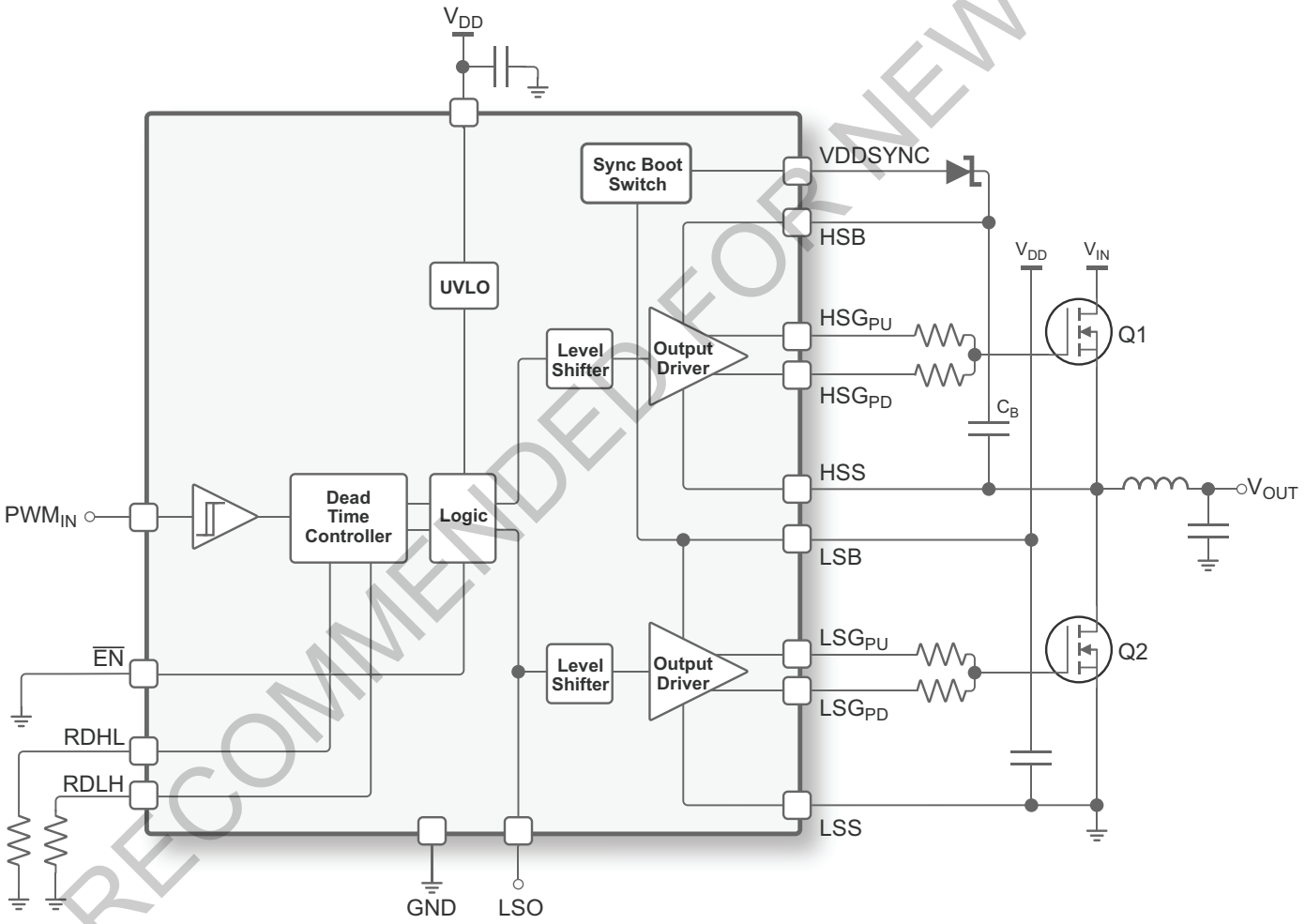


Application Circuit

Figure 8 shows a typical application diagram of the PE29101 and its external components in a half-bridge, open-loop configuration. The PE29101 drives the low-side gate of Q2 referenced to ground, and the floating high-side gate of Q1 referenced to the switch node (HSS). Pin 4 of the PE29101 is connected to an external Schottky bootstrap diode with fast recovery time. The internal synchronous boot circuit limits overcharging of the bootstrap capacitor during reverse body diode conduction, which could potentially damage Q1 by exceeding its specified gate-to source voltage.

The external gate resistors are required to de-Q the inductance in the gate loop and dampen any ringing on the FET gates and the SW node. Dead-time resistors RDHL and RDLH can be adjusted to fine-tune the dead time and to reduce unwanted losses during dead-time periods.

Figure 8 ▪ Applications Diagram for PE29101



Pin Configuration

This section provides pin information for the PE29101. **Figure 9** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 9 ▪ Pin Configuration (Top View—Bumps Down)

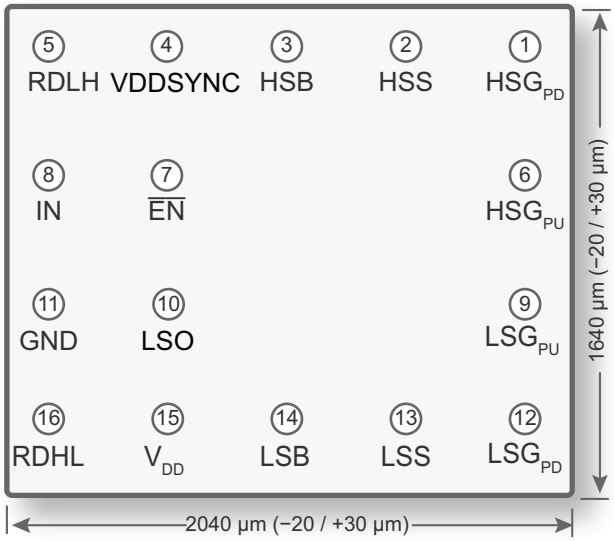


Table 5 ▪ Pin Descriptions for PE29101

Pin No.	Pin Name	Description
1	HSG_{PD}	High-side gate drive pull-down
2	HSS	High-side source
3	HSB	High-side bias
4	VDDSYNC	High-side gate synchronous boot control. Connect to anode of external Schottky diode.
5	RDLH	Dead-time control resistor sets LSG falling to HSG rising delay (external resistor to GND)
6	HSG_{PU}	High-side gate drive pull-up
7(*)	$\overline{EN}$	Enable active low, tri-state outputs when high
8(*)	IN	Control input
9	LSG_{PU}	Low-side gate drive pull-up
10(*)	LSO	Look ahead for LSG_{PU}. LSO precedes LSG_{PU} and LSG_{PD} by 4 ns. Leave open if unused.
11	GND	Ground
12	LSG_{PD}	Low-side gate drive pull-down
13	LSS	Low-side source
14	LSB	Low-side bias
15	V_{DD}	+5V supply voltage
16	RDHL	Dead-time control resistor sets HSG falling to LSG rising delay (external resistor to ground)

Note: * Internal 100k pull down resistor

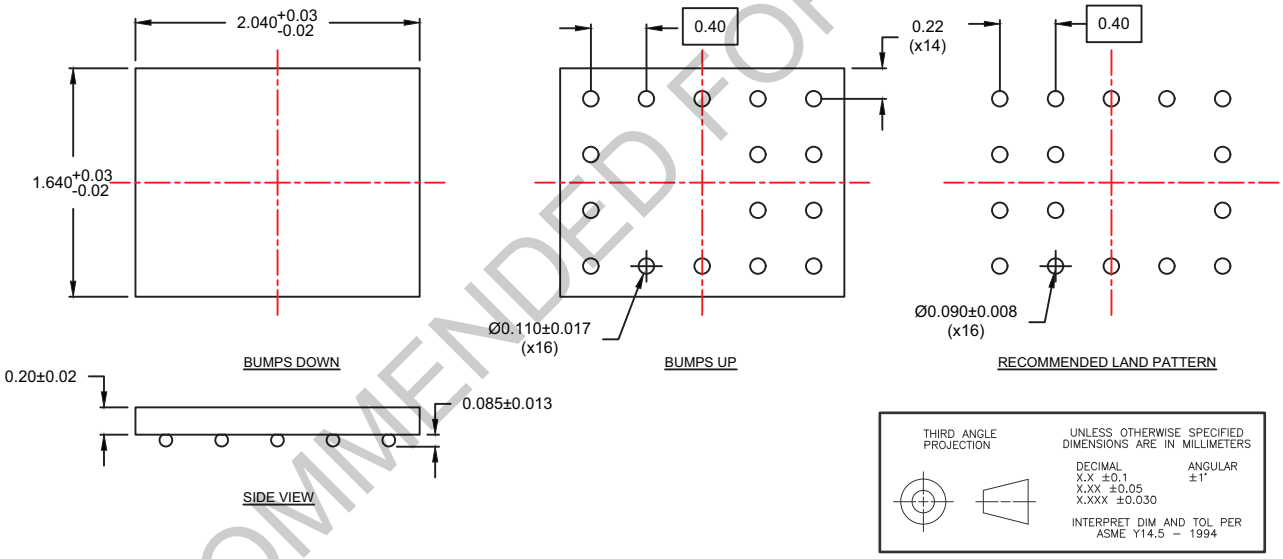
Die Mechanical Specifications

This section provides the die mechanical specifications for the PE29101.

Table 6 ▪ Die Mechanical Specifications for PE29101

Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x,y)		2040 × 1640		µm	Including sapphire, max tolerance = –20/+30
Wafer thickness	180	200	220	µm	
Wafer size				µm	
Bump pitch		400		µm	
Bump height		85		µm	
Bump diameter		110		µm	max tolerance = ±17

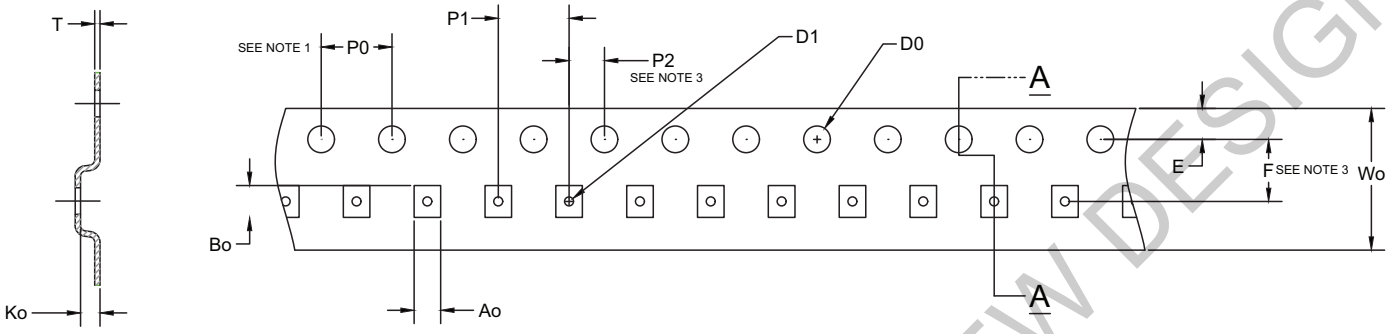
Figure 10 ▪ Recommended Land Pattern for PE29101



Tape and Reel Specification

This section provides tape-and-reel information for the PE29101.

Figure 11 ▪ Tape and Reel Specifications for the PE29101

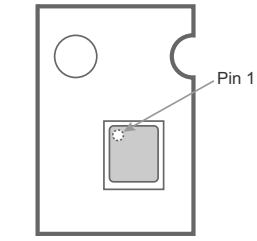


Direction of Feed

Pocket	Nominal	Tolerance
Ao	1.9	+/- 0.05
Bo	2.3	+/- 0.05
Ko	0.4	+/- 0.05
P1	4.0	+/- 0.1
Wo	8.0	+0.3 / -0.1
F	3.5	+/- 0.05
D1	0.5	+/- 0.05
D0	1.5	+ 0.1 / - 0
E	1.8	+/- 0.1
P0	4.0	+/- 0.1
P2	2.0	+/- 0.05
T	0.2	+/- 0.05

Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.



Device Orientation in Tape

Ordering Information

Table 7 lists the available ordering codes for the PE29101.

Table 7 ▪ Order Codes for PE29101

Order Codes	Description	Packaging	Shipping Method
PE29101A-X	PE29101 flip chip	Die on tape and reel	500 units/T&R
PE29101A-Z	PE29101 flip chip	Die on tape and reel	3000 units/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Specification

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Sales Contact

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