Data sheet acquired from Harris Semiconductor
SCHS217B

February 1998 - Revised July 2003

High-Speed CMOS Logic BCD to 7-Segment Latch/Decoder/Driver for LCDs

Features

- **Input Latches for BCD Code Storage**
- **Blanking Capability**
- **Phase Input for Complementing Outputs**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{O}C to 125^{O}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

Description

The CD74HC4543 high-speed silicon-gate device is a BCD to 7-segment latch/decoder/driver designed primarily for directly driving liquid-crystal displays. It has an active-high disable input (LD), an active-high blanking input (BI) and a phase input (PH) to which a square wave is applied for liquid-crystal applications. This square wave also is applied to the backplane of the liquid-crystal display.

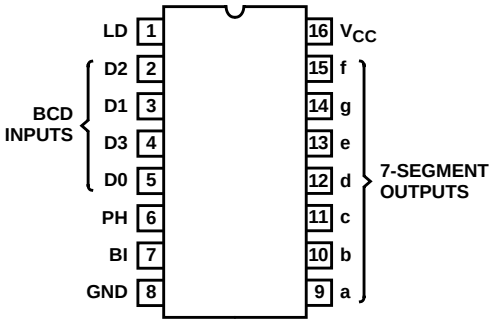
This device also can be used, in conjunction with current amplifying devices, for driving LEDs, incandescent, fluorescent, and gas-discharge displays. For these applications the phase input provides a means to obtain active-high or active-low segment outputs. (See the Function Table.)

Ordering Information

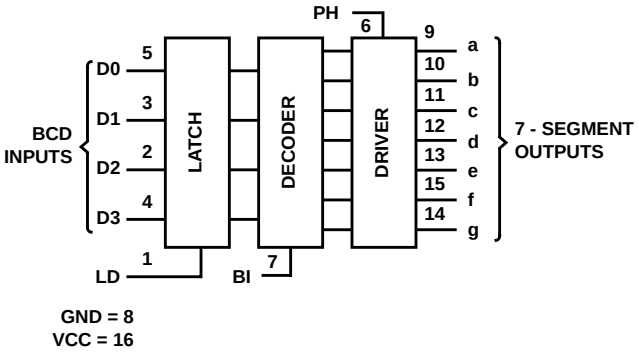
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD74HC4543E	-55 to 125	16 Ld PDIP

Pinout

CD74HC4543
(PDIP)
TOP VIEW



Functional Diagram



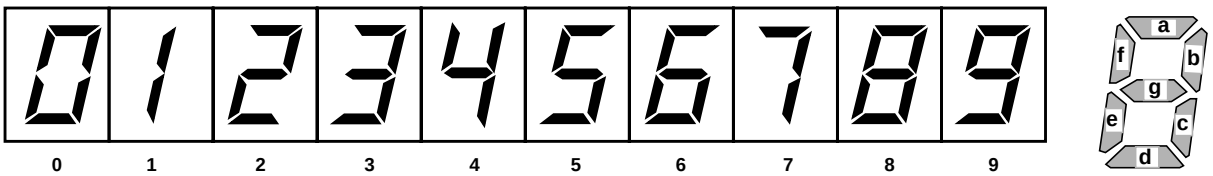
FUNCTION TABLE

INPUTS							OUTPUTS							
LD	BI	PH	D3	D2	D1	D0	a	b	c	d	e	f	g	DISPLAY
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	Note 1							Note 1
As Above		H	As Above				Inverse of Above							As Above

NOTE:

1. Depends on BCD code previously applied when LD = high.

DISPLAY



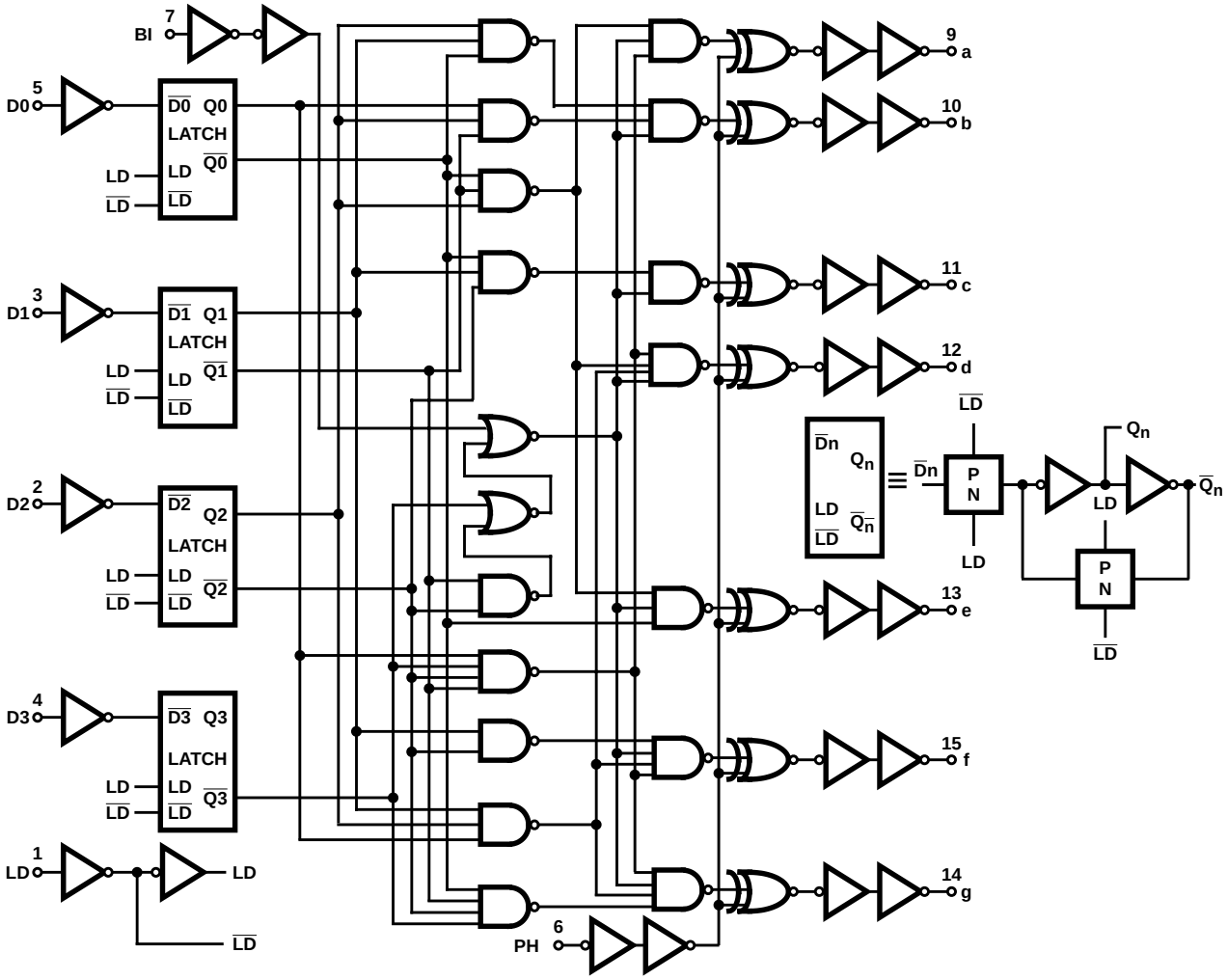


FIGURE 1. LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC} . . . . . 2V to 6V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
E (PDIP) Package 67
Maximum Junction Temperature (Hermetic Package or Die) . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads (Non-Standard)			-	-	-	-	-	-	-	-	-	V
			-1	4.5	3.98	-	-	3.84	-	3.7	-	V
			-1.3	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads (Standard Output)			-	-	-	-	-	-	-	-	-	V
			1	4.5	-	-	0.26	-	0.33	-	0.4	V
			1.3	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Setup Time Dn to LD	t_{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Dn to LD	t_H	2	30	-	-	40	-	-	45	-	-	ns
		4.5	6	-	-	8	-	-	9	-	-	ns
		6	5	-	-	7	-	-	8	-	-	ns
Latch Disable Pulse Width	t_W	2	50	-	-	65	-	-	75	-	-	ns
		4.5	10	-	-	13	-	-	15	-	-	ns
		6	9	-	-	11	-	-	13	-	-	ns

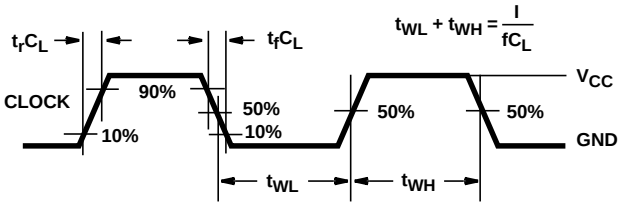
Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Dn to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	340	-	425	-	510	ns
			4.5	-	-	68	-	85	-	102	ns
			6	-	-	58	-	72	-	87	ns
		C_L = 15pF	5	-	28	-	-	-	-	-	ns
Propagation Delay, LD to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	370	-	465	-	555	ns
			4.5	-	-	74	-	93	-	111	ns
			6	-	-	63	-	79	-	94	ns
		C_L = 15pF	5	-	31	-	-	-	-	-	ns
Propagation Delay, BI to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	265	-	330	-	400	ns
			4.5	-	-	53	-	66	-	80	ns
			6	-	-	45	-	56	-	68	ns
		C_L = 15pF	5	-	22	-	-	-	-	-	ns
Propagation Delay, PH to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	200	-	250	-	300	ns
			4.5	-	-	40	-	50	-	60	ns
			6	-	-	34	-	43	-	51	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
			6	-	-	43	-	54	-	64	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	52	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.
4. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

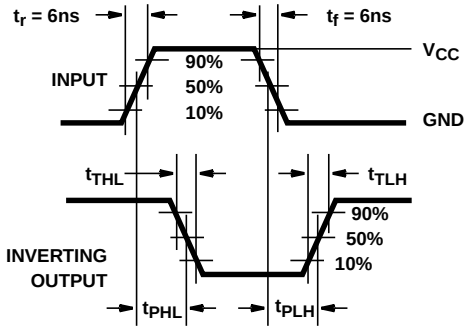


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

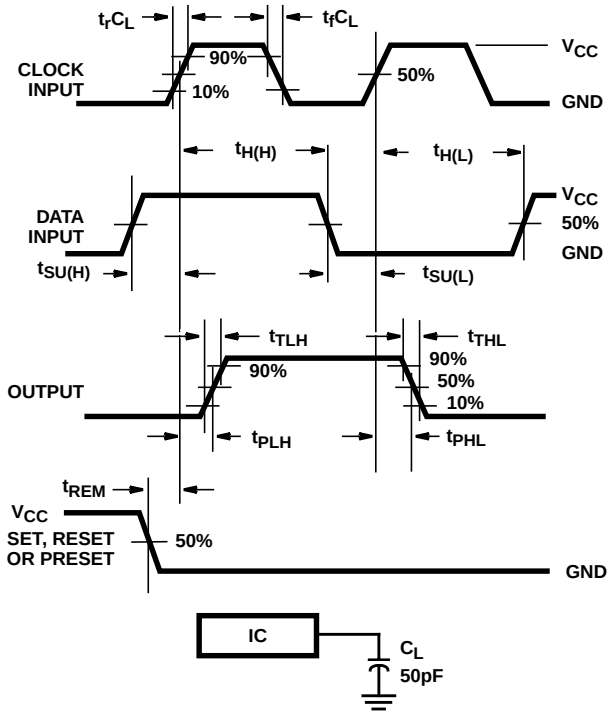


FIGURE 4. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Application Circuits

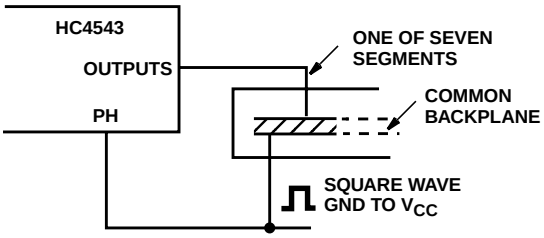


FIGURE 5. CONNECTION TO LIQUID-CRYSTAL (LCD) DISPLAY READOUT

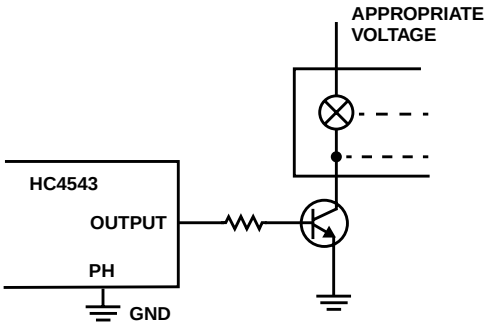


FIGURE 6. CONNECTION TO INCANDESCENT DISPLAY READOUT

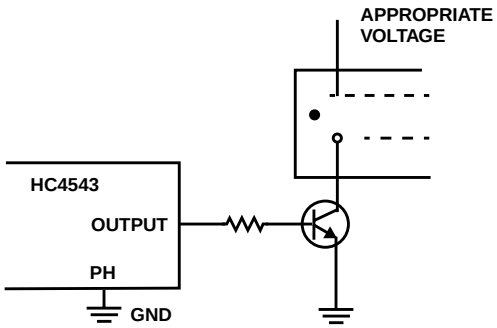


FIGURE 7. CONNECTION TO GAS-DISCHARGE DISPLAY READOUT

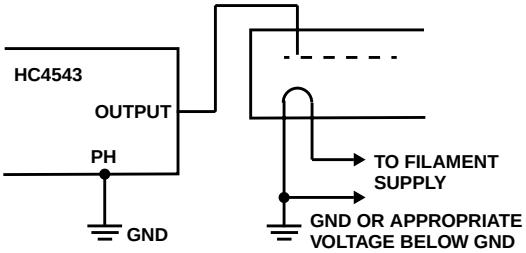


FIGURE 8. CONNECTION TO FLUORESCENT DISPLAY READOUT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4543E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4543E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

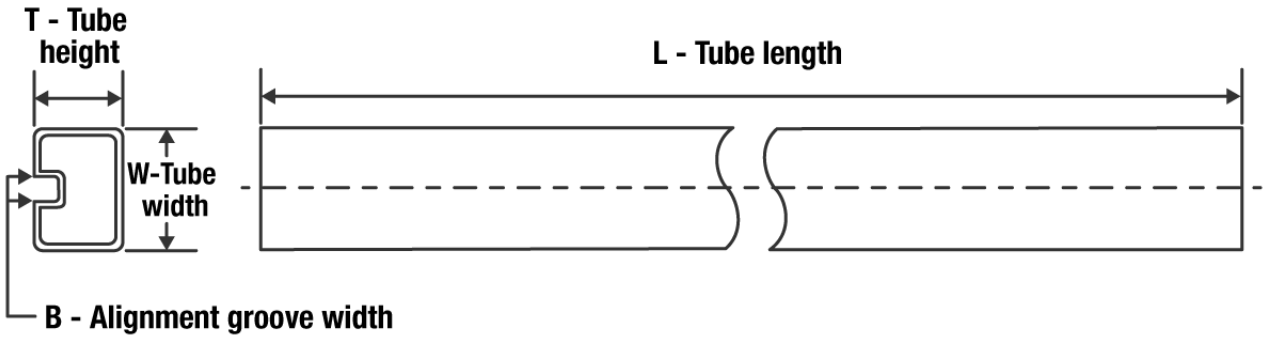
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



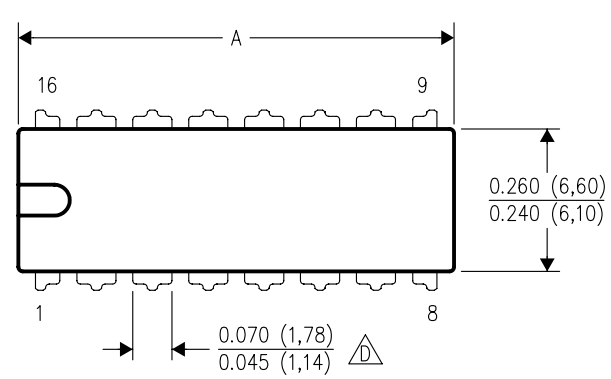
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4543E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4543E	N	PDIP	16	25	506	13.97	11230	4.32

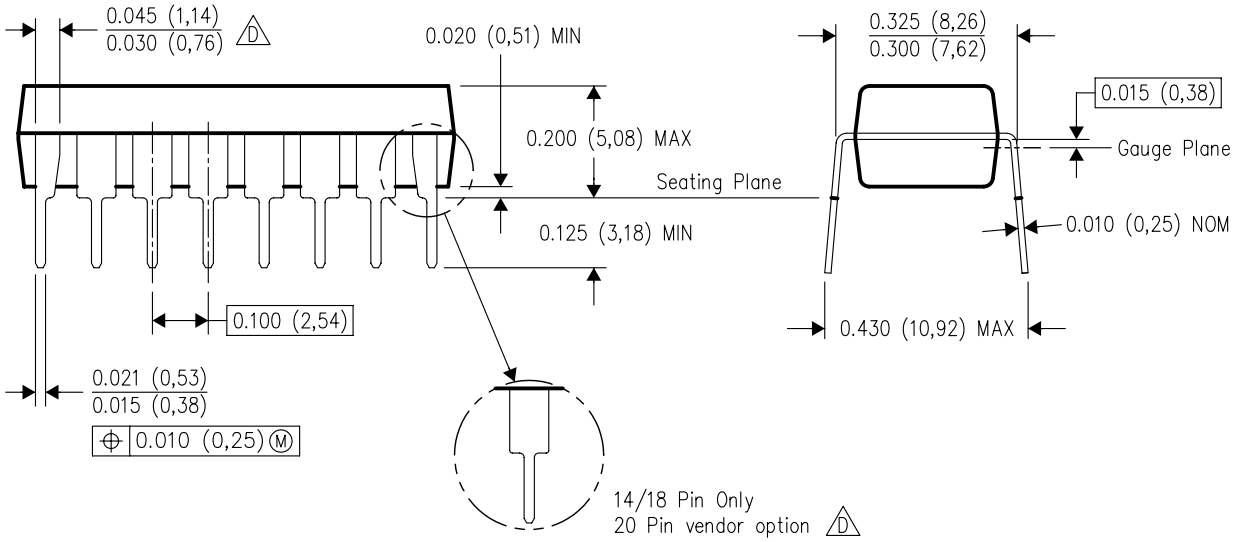
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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