PLL Model: PT626-13

Issue 2; 28th April 2022

Features

- Temperature stability to ± 5ppb
- Very Low phase noise options
- Standard frequency range (1 to 500) MHz
- Low pre-aged options available
- Reference 10 MHz to 500 MHz, 10 MHz standard.
- Low phase noise frequency translation.
- Holdover dependant on option A, B or C
- The flexible nature of the design means that variations to suit almost any application can be developed to meet individual customer requirements

Option A

- Temperature stability ±5ppb over (0 to 50)°C
- Output: CMOS 15pF, 45% 55% or Sinewave 0dBm
- Voltage: 5.0V 12.0V
- Warm up Current: 560mA 390mA
- Quiescent current: 320mA 170mA

Option B

- Temperature stability : ±10ppb over (–20 to 70)°C
- Output: CMOS 15pF, 45% 55% or Sinewave 0dBm
- Voltage: 5.0V 12.0V
- Warm up Current: 560mA 390mA
- Quiescent current: 320mA 170mA

Option C

- Temperature stability : ±20ppb over (–40 to 70)°C
- Output: CMOS 15pF, 45% 55% or Sinewave 0dBm
- Voltage: 5.0V 12.0V
- Warm up Current: 560mA 390mA
- Quiescent current: 320mA 170mA

Phase Noise (typical)

- FO_0+10Hz -125 dBc/Hz
- FO_0+100Hz -145 dBc/Hz
- FO_0+1KHz -155 dBc/Hz
- FO_0+10KHz -160 dBc/Hz
- FO_0+100KHz -165 dBc/Hz

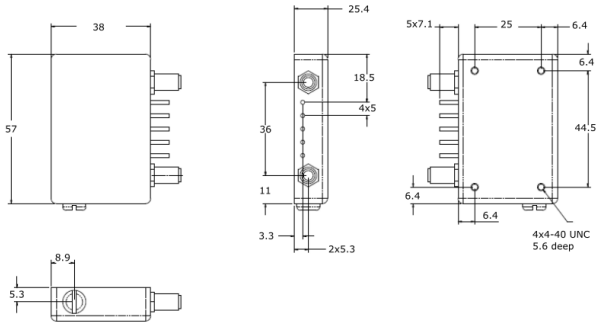
Values based on a 10MHz unit

Phase noise locked dependant on reference.

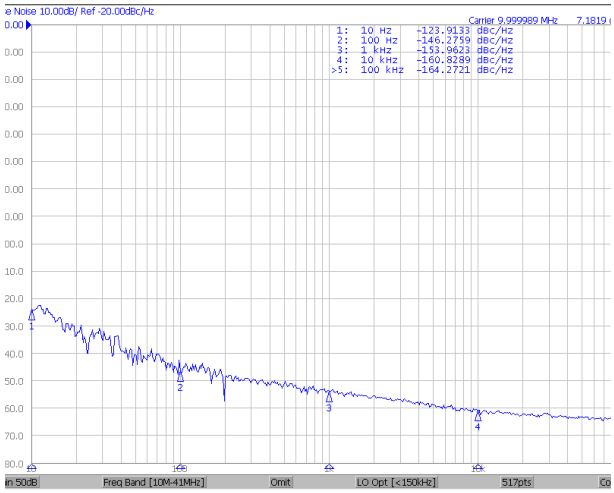
Voltage / Load change

- ±5% supply voltage change: ±2ppb
- ±10% load change: ±10ppb

Dimensions (mm)



Phase Noise Plot



Ageing:

Based on 10MHz unit after 30 days continuous operation:

- Per day: ±0.1ppb max.
- Per year: ±50ppb max.
- Warm up time: 2 minutes to within 0.1 ppm

Voltage Trim:

- 0.5ppm minimum
- Fine adjust through side screw.

Reference Options:

- N/A

Environmental

- Electrostatic-Sensitive Device (ESD)
- Storage Temperature Range: (-40 to +125)°C
- Mechanical shock: MIL standard 202F, method 213, condition J
- Thermal shock: MIL standard 202F, method 107, condition A
- Vibration: MIL standard 202F, method 204, condition B
- Solderability: 5 seconds maximum at 230°C
- 3 seconds maximum at 350°C

Compliance

- RoHS Status (2011/65/EU) - Compliant
- REACH Status - Compliant

Packaging

- Pack Style: Bulk

Ordering Information

- Unique customer part number and custom specification issued with each application
- PLL model: PT626-13
- Frequency: (1 to 500) MHz
- Stability/Output/Voltage Option: A, B or C
- Supply voltage code: V2= +5Vd.c. supply
- V3= +12Vd.c. supply

Connections

Reference Input
#1 Lock Detect
#2 Reference Detect
#3 Vcc
#4 Tune
#5 ground
RF out

Reference input > -10 dBm

Lock Status

Ref DT	Lock DT	
high	low	Reference present, no lock
low	high	Spurious lock
high	high	Full operational lock

Test Circuit - Sinewave