

# 8-Input Data Selector/ Multiplexer with 3-State Outputs

## High-Performance Silicon-Gate CMOS



ON Semiconductor®

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### MC74HC251A

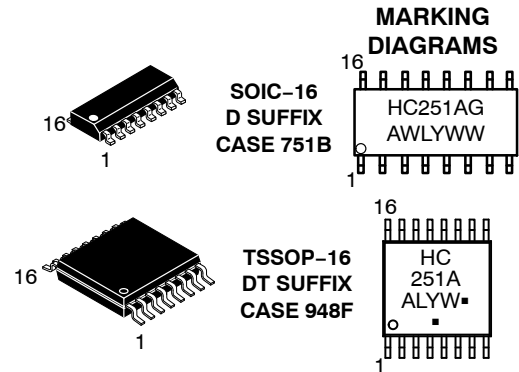
The MC54/74HC251 is identical in pinout to the LS251. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects one of the eight binary Data Inputs, as determined by the Address Inputs. The Output Enable pin must be a low level for the selected data to appear at the outputs. If Output Enable is high, both the Y and the  $\bar{Y}$  outputs are in the high-impedance state. This 3-state feature allows the HC251 to be used in bus-oriented systems.

The HC251 is similar in function to the HC251 which does not have 3-state outputs.

#### Features

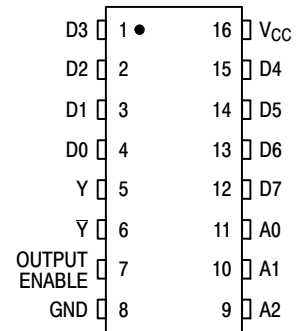
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or  $\blacksquare$  = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC74HC251A

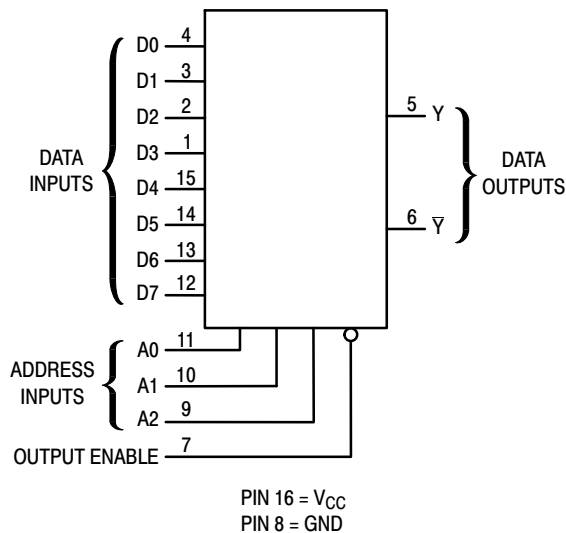


Figure 1. Logic Diagram

## FUNCTION TABLE

| Inputs |    |    |                | Outputs |            |
|--------|----|----|----------------|---------|------------|
| A2     | A1 | A0 | Output Enabled | Y       | $\bar{Y}$  |
| X      | X  | X  | H              | Z       | $\bar{Z}$  |
| L      | L  | L  | L              | D0      | $\bar{D0}$ |
| L      | L  | H  | L              | D1      | $\bar{D1}$ |
| L      | H  | L  | L              | D2      | $\bar{D2}$ |
| L      | H  | H  | L              | D3      | $\bar{D3}$ |
| H      | L  | L  | L              | D4      | $\bar{D4}$ |
| H      | L  | H  | L              | D5      | $\bar{D5}$ |
| H      | H  | L  | L              | D6      | $\bar{D6}$ |
| H      | H  | H  | L              | D7      | $\bar{D7}$ |

Z = high impedance  
D0, D1, ..., D7 = the level of the respective D input.

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                  | Unit        |
|-----------|---|------------------------|-------------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                           | -0.5 to +7.0           | V           |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                            | -1.5 to $V_{CC} + 1.5$ | V           |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                           | -0.5 to $V_{CC} + 0.5$ | V           |
| $I_{in}$  | DC Input Current, per Pin                                       | $\pm 25$               | mA          |
| $I_{out}$ | DC Output Current, per Pin                                      | $\pm 50$               | mA          |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                        | $\pm 75$               | mA          |
| $P_D$     | Power Dissipation in Still Air<br>SOIC Package<br>TSSOP Package | 500<br>TBD             | mW          |
| $T_{stg}$ | Storage Temperature   | -65 to +150            | $^{\circ}C$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min | Max      | Unit        |
|-------------------|--|-----|----------|-------------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0 | 6.0      | V           |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0   | $V_{CC}$ | V           |
| $T_A$             | Operating Temperature, All Package Types             | -55 | +125     | $^{\circ}C$ |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 2)               |     |          | ns          |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0   | 1000     |             |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0   | 500      |             |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0   | 400      |             |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
|                 |  |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |  |   | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |  |   | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.3              | 0.3    | 0.3     | V    |
|                 |  |   | 4.5                  | 0.9              | 0.9    | 0.9     |      |
|                 |  |   | 6.0                  | 1.2              | 1.2    | 1.2     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |  |   | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |  |   | 6.0                  | 5.9              | 5.9    | 5.9     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA                   | 4.5                  | 3.98             | 3.84   | 3.70    |      |
| 6.0             | 5.48   | 5.34  | 5.20                 |                  |        |         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |   | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  |   | 6.0                  | 0.1              | 0.1    | 0.1     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA                   | 4.5                  | 0.26             | 0.33   | 0.40    |      |
| 6.0             | 0.26   | 0.33  | 0.40                 |                  |        |         |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 6.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0                  | ± 0.5            | ± 5.0  | ± 10    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA   | 6.0                  | 8                | 80     | 160     | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Symbol                   | Parameter   | $V_{CC}$<br>V     | Guaranteed Limit |                 |                 | Unit |
|--------------------------|---|-------------------|------------------|-----------------|-----------------|------|
|                          |   |                   | - 55 to<br>25°C  | ≤ 85°C          | ≤ 125°C         |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Input D to Output Y or $\bar{Y}$<br>(Figures 2, 3 and 6) | 2.0<br>4.5<br>6.0 | 185<br>37<br>31  | 230<br>46<br>39 | 280<br>56<br>48 | ns   |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y or $\bar{Y}$<br>(Figures 3 and 6)    | 2.0<br>4.5<br>6.0 | 205<br>41<br>35  | 255<br>51<br>43 | 310<br>62<br>53 | ns   |
| $t_{PLZ}$ ,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 5 and 7)           | 2.0<br>4.5<br>6.0 | 195<br>39<br>33  | 245<br>49<br>42 | 295<br>59<br>50 | ns   |
| $t_{PZL}$ ,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 5 and 7)           | 2.0<br>4.5<br>6.0 | 145<br>29<br>25  | 180<br>36<br>31 | 220<br>44<br>38 | ns   |
| $t_{PLZ}$ ,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output $\bar{Y}$<br>(Figures 5 and 7)   | 2.0<br>4.5<br>6.0 | 220<br>44<br>37  | 275<br>55<br>47 | 330<br>66<br>56 | ns   |
| $t_{PZL}$ ,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output $\bar{Y}$<br>(Figures 5 and 7)   | 2.0<br>4.5<br>6.0 | 150<br>30<br>26  | 190<br>38<br>33 | 225<br>45<br>38 | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 2 and 6)                     | 2.0<br>4.5<br>6.0 | 75<br>15<br>13   | 95<br>19<br>16  | 110<br>22<br>19 | ns   |
| $C_{in}$                 | Maximum Input Capacitance   | –                 | 10               | 10              | 10              | pF   |
| $C_{out}$                | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State)          | –                 | 15               | 15              | 15              | pF   |

| $C_{PD}$ | Power Dissipation Capacitance (Per Package) | Typical @ 25°C, $V_{CC} = 5.0$ V |  |  | pF |
|----------|---|----------------------------------|--|--|----|
|          |   | 36                               |  |  |    |
|          |   |                                  |  |  |    |

## PIN DESCRIPTIONS

### INPUTS

#### D0, D1, ..., D7 (Pins 4, 3, 2, 1, 15, 14, 13, 12)

Data inputs. Data on one of these eight binary inputs may be selected to appear on the output.

### CONTROL INPUTS

#### A0, A1, A2 (Pins 11, 10, 9)

Address inputs. The data on these pins are the binary address of the selected input (see the Function Table).

### Output Enable (Pin 7)

Output Enable. This input pin must be at a low level for the selected data to appear at the outputs. If the Output Enable pin is high, both the Y and  $\bar{Y}$  outputs are taken to the high-impedance state.

### OUTPUTS

#### Y, $\bar{Y}$ (Pins 5, 6)

Data outputs. The selected data is presented at these pins in both true (Y output) and complemented ( $\bar{Y}$  output) forms.

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## SWITCHING WAVEFORMS

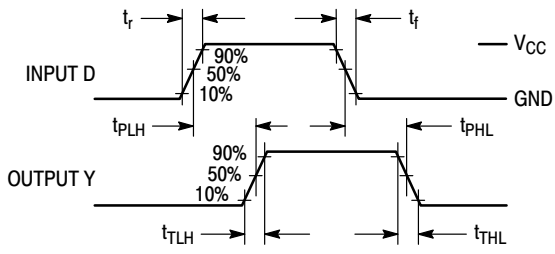


Figure 2.

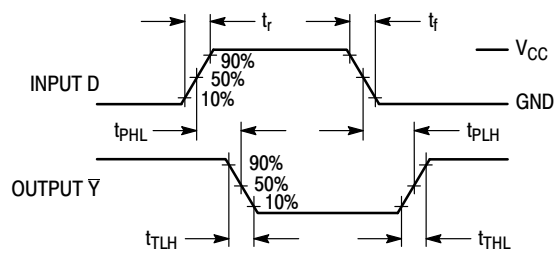


Figure 3.

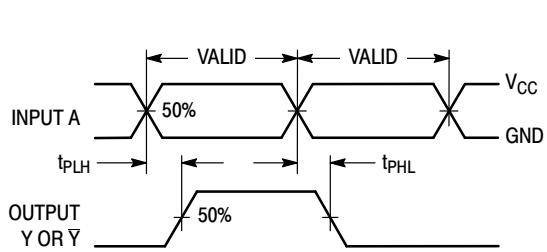


Figure 4.

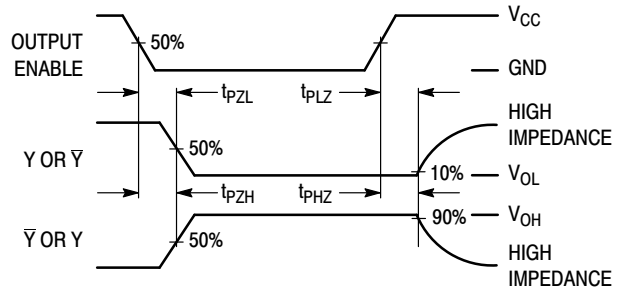
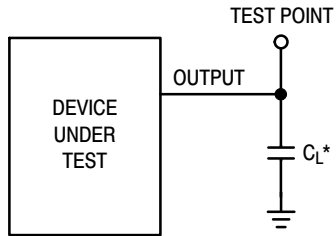


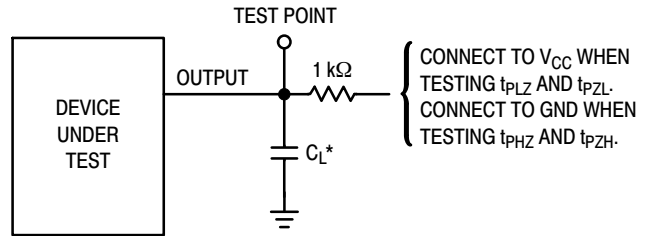
Figure 5.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 6.



\*Includes all probe and jig capacitance

Figure 7.

# MC74HC251A

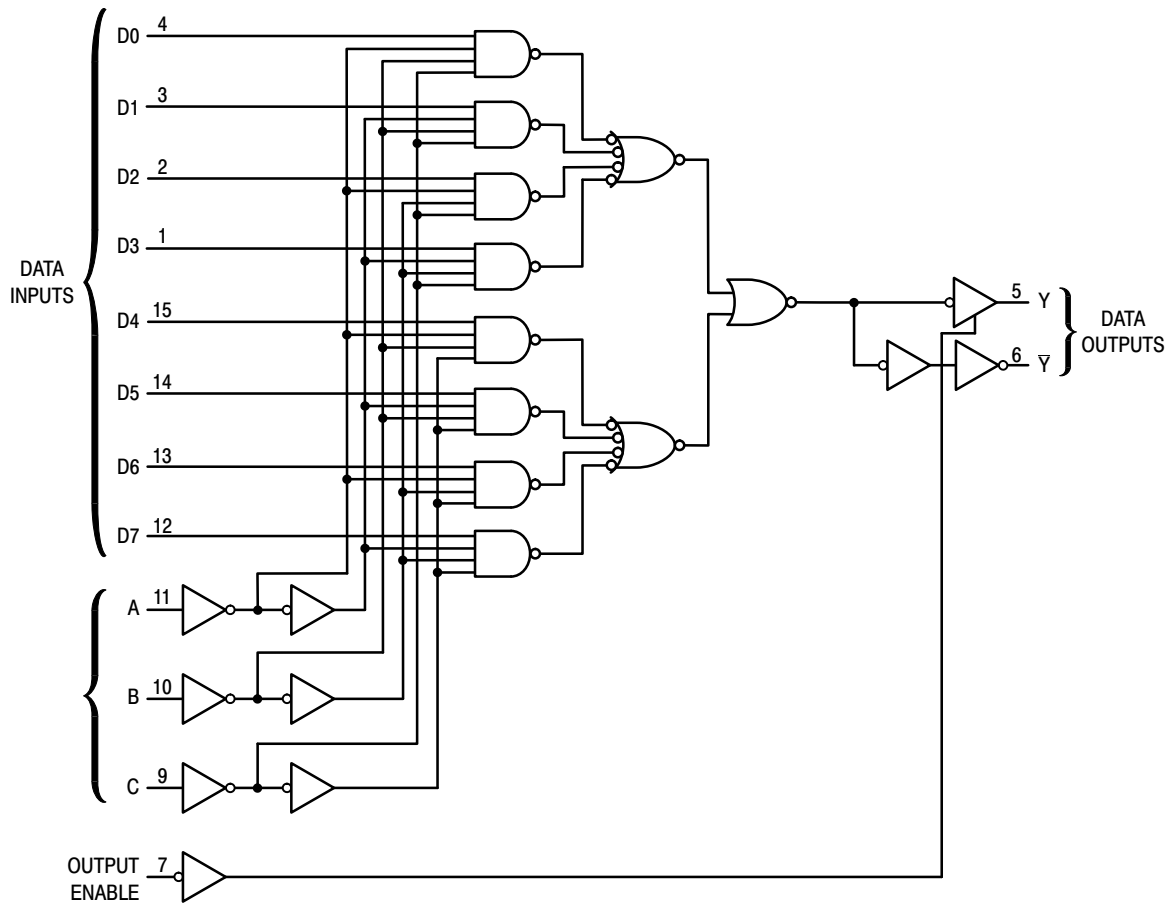


Figure 8. Expanded Logic Diagram

## ORDERING INFORMATION

| Device           | Package               | Shipping†        |
|------------------|-----------------------|------------------|
| MC74HC251ADG     | SOIC-16<br>(Pb-Free)  | 48 Units / Rail  |
| MC74HC251ADR2G   |                       | 2500 Tape & Reel |
| NLV74HC251ADR2G* |                       | 2500 Tape & Reel |
| MC74HC251ADTG    | TSSOP-16<br>(Pb-Free) | 96 Units / Rail  |
| MC74HC251ADTR2G  |                       | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

## SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

- |  |  |  |  |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p>                           | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p>   | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p>                                 | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> |  |

### SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

|                  |             |  |
|------------------|-------------|--|
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| DESCRIPTION:     | SOIC-16     | PAGE 1 OF 1  |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16  
CASE 948F-01  
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

|                  |             |  |
|------------------|-------------|--|
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