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NTE74C240 & NTE74C244
Integrated Circuit
TTL– CMOS Octal Buffers and Line Drivers
w/3–State Outputs
20–Lead DIP

Description:

The NTE74C240 (Inverting) and NTE74C244 (Non–Inverting) octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits in a 20–Lead DIP type package with 3–state outputs. These outputs have been specially designed to drive highly capacitive loads such as bus–oriented systems. These devices have a fan out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

Features:

- Wide Supply Range: 3V to 15V
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power Consumption
- High Capacitive Load Drive Capability
- 3–State Outputs
- Input Protection
- TTL Compatible
- High Speed: 25ns (typ.) at 10V, 50pF (NTE74C244 **ONLY**)

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . . 3V to 15V
Maximum V_{CC} Voltage 18V
Operating Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V	I_O = −10μA	4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V	I_O = 10μA	–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		–1.0	–0.005	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.05	300	μA
CMOS/LPTTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V	I_O = −450μA	V_{CC}–0.4	–	–	V
			I_O = −2.2mA	2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 2.2mA		–	–	0.4	V
Output Drive							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	V_{OUT} = 0, T_A = +25°C	–14	–30	–	mA
		V_{CC} = 10V		–36	–70	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	V_{OUT} = V_{CC}, T_A = +25°C	12	20	–	mA
		V_{CC} = 10V		48	70	–	mA

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay (Data In to Out) NTE74C240	$t_{PD(1)}$, $t_{PD(0)}$	V_{CC} = 5V		–	60	90	ns
			C_L = 150pF	–	80	110	ns
		V_{CC} = 10V		–	40	70	ns
			C_L = 150pF	–	60	90	ns
NTE74C244		V_{CC} = 5V		–	45	70	ns
			C_L = 150pF	–	60	90	ns
		V_{CC} = 10V		–	25	50	ns
			C_L = 150pF	–	40	70	ns
Propagation Delay Output Disable to High Impedance State (from a Logic Level)	t_{1H}, t_{0H}	V_{CC} = 5V	R_L = 1kΩ	–	45	80	ns
		V_{CC} = 10V		–	35	60	ns
Propagation Delay Output Disable to Logic Level (from High Impedance State)	t_{H1}, t_{H0}	V_{CC} = 5V	R_L = 1kΩ	–	50	90	ns
		V_{CC} = 10V		–	30	60	ns
Transition Time	$t_{T(HL)}$, $t_{T(LH)}$	V_{CC} = 5V		–	45	80	ns
			C_L = 150pF	–	75	140	ns
		V_{CC} = 10V		–	30	60	ns
			C_L = 150pF	–	50	100	ns

Note 2. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Dissipation Capacitance (Output Enabled Buffer)	C_{PD}	Note 4	–	100	–	pF
Power Dissipation Capacitance (Output Disabled Buffer) NTE74C240	C_{PD}	Note 4	–	10	–	pF
NTE74C244			–	0	–	pF
Input Capacitance (Any Input)	C_{IN}	V_{IN} = 0V, f = 1Mhz, T_A = +25°C	–	10	–	pF
Output Capacitance (Output Disabled)	C_O		–	10	–	pF

Note 2. AC Parameters are guaranteed by DC correlated testing.
Note 3. Capacitance is guaranteed by periodic testing.
Note 4. C_{pd} determines the no load AC power consumption of any CMOS device.

Truth Table (NTE74C240):

ODA	IA	OA	ODB	IA	OB
1	X	Z	1	X	Z
1	X	Z	1	X	Z
0	0	1	0	0	1
0	1	0	0	1	0

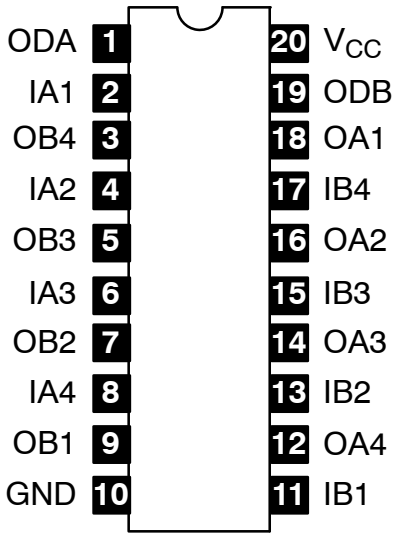
1 = High Level
0 = Low Level
X = Don't Care
Z = 3−State

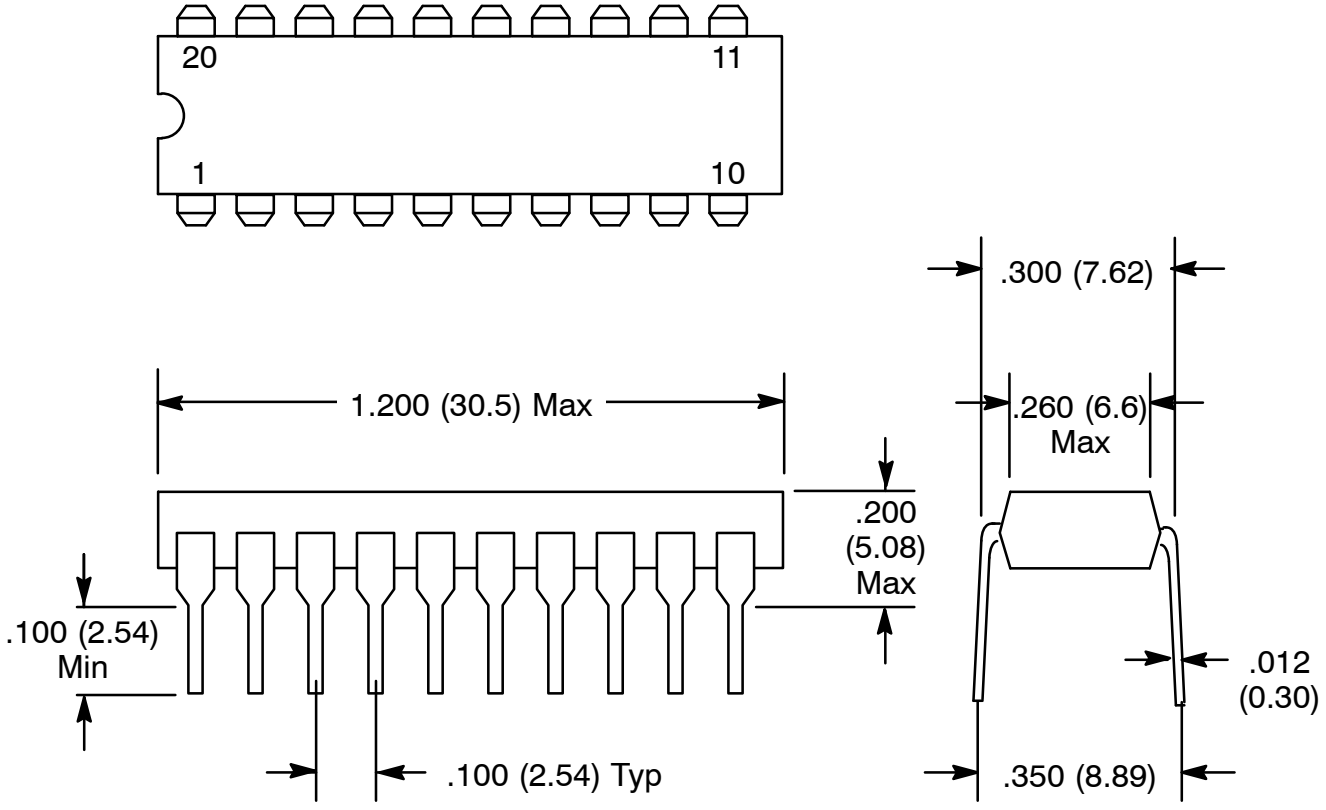
Truth Table (NTE74C244):

ODA	IA	OA	ODB	IA	OB
1	X	Z	1	X	Z
1	X	Z	1	X	Z
0	0	0	0	0	0
0	1	1	0	1	1

1 = High Level
0 = Low Level
X = Don't Care
Z = 3−State

Pin Connection Diagram




20
11
1
10
.300 (7.62)
1.200 (30.5) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
Min
.012
(0.30)
.100 (2.54) Typ
.350 (8.89)