LX7219

Datasheet

6A Hysteretic Synchronous Buck Regulator with I2C

Production

July 2018

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in July 2018. In this revision, the format of the document was updated to the latest template.

1.2 Revisions Prior to 2.0

Prior to revision 2.0, this datasheet was maintained in a different document control system. The last revision of this document prior to 2.0 was revision 1.3, published in March 2018.

2 LX7219 Overview

The LX7219 is a digitally controlled step-down regulator IC with an integrated 22 mΩ high-side P-channel MOSFET and a 13 mΩ low-side N-channel MOSFET. It features Microsemi's proprietary constant-frequency hysteretic control engine for near-instantaneous correction to line/load transients for a voltage range of 2.7 V to 5.5 V, and 6 A constant frequency . It does not require high-ESR output capacitors and incorporates energy-saving power save or pulse skip mode (PSM) at light loads, to extend battery life in mobile applications. The LX7219 has an I²C serial interface port for output voltage margining and monitoring, if required (it can also operate in default mode). In addition it includes robust fault monitoring functions. The LX7219 is available in 0.9 V single slave address and 0.8 V default output voltage (no voltage divider is necessary) with four slave addresses. The output voltage can be adjusted with an external voltage divider up to 3.3 V.

2.1 Features

The following features are supported in LX7219.

- Constant frequency hysteretic control
- Extremely fast line/load transient response
- I²C for output adjustment (3.4 Mbps)
- 1.2 MHz switching frequency
- Extremely low-R_{DSON} MOSFETS
- Input voltage rail 2.7 V to 5.5 V
- Greater than 6 A output current
- Power save mode for light-load efficiency
- UVLO, OVP, and OCP
- –40 °C to 85 °C ambient temperature
- Available in VQFN 2mm x 3mm 14L package
- RoHS compliant

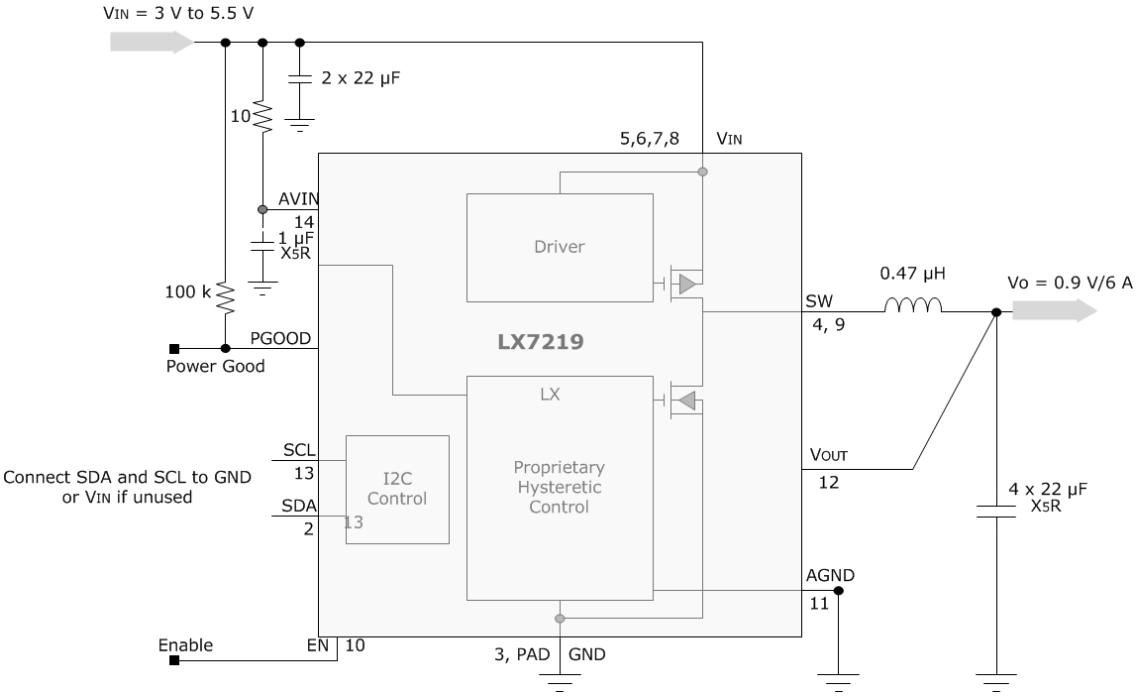
2.2 Applications

The following list of applications use LX7219.

- High performance hard disk drive (HDD)
- Solid-state drive
- Data center applications
- Raid/host bus adaptors
- Optical transceivers

The following figure shows the block diagram of LX7219.

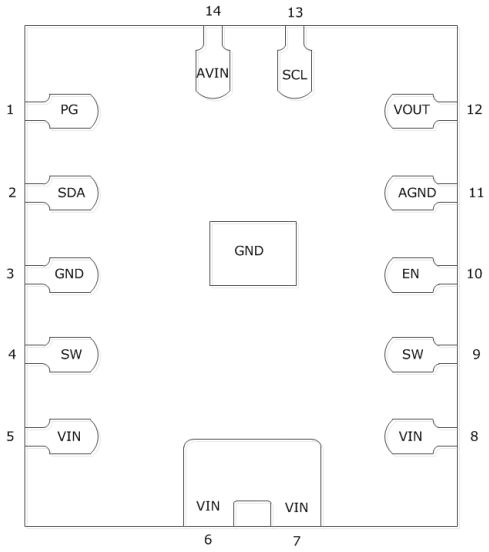
Figure 1 • Typical 5 V to 0.9 V at 6 A Schematic



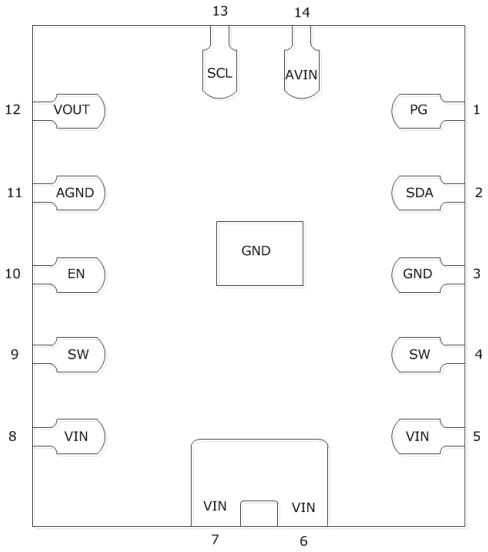
3 Pin/Ball Configuration

The following figure shows the top view and bottom view of LX7219 VQFN 2×3 14L package, pin/ball configuration.

Figure 2 • LX7219 Pinout Details



LX7219
Top View
VQFN 2x3 14L Package



LX7219
Bottom View
VQFN 2x3 14L Package

3.1 Ordering Information

The following table gives the ordering information details for LX7219.

Table 1 • Ordering Information Details

Ambient Temperature	Package	Part Marking	Output Voltage	Slave Address	Part Number	Packaging Type
–40°C to 85°C	VQFN 2x3 14L RoHS compliant, Pb-free	MSCJ 7219 YWWL	0.9 V	E0h	LX7219-02ILQ Bulk	LX7219-02ILQ-TR Tape and Reel
		MSCA 7219 YWWL	0.8 V	E0h	LX7219-01ILQ Bulk	LX7219-01ILQ-TR Tape and Reel
		MSCB 7219 YWWL		E2h	LX7219-11ILQ Bulk	LX7219-11ILQ-TR Tape and Reel
		MSCC 7219 YWWL		E4h	LX7219-21ILQ Bulk	LX7219-21ILQ-TR Tape and Reel
		MSCD 7219 YWWL		E6h	LX7219-31ILQ Bulk	LX7219-31ILQ-TR Tape and Reel

3.2 Pin/Ball Description

The following table gives pin/ball numbers and their respective descriptions.

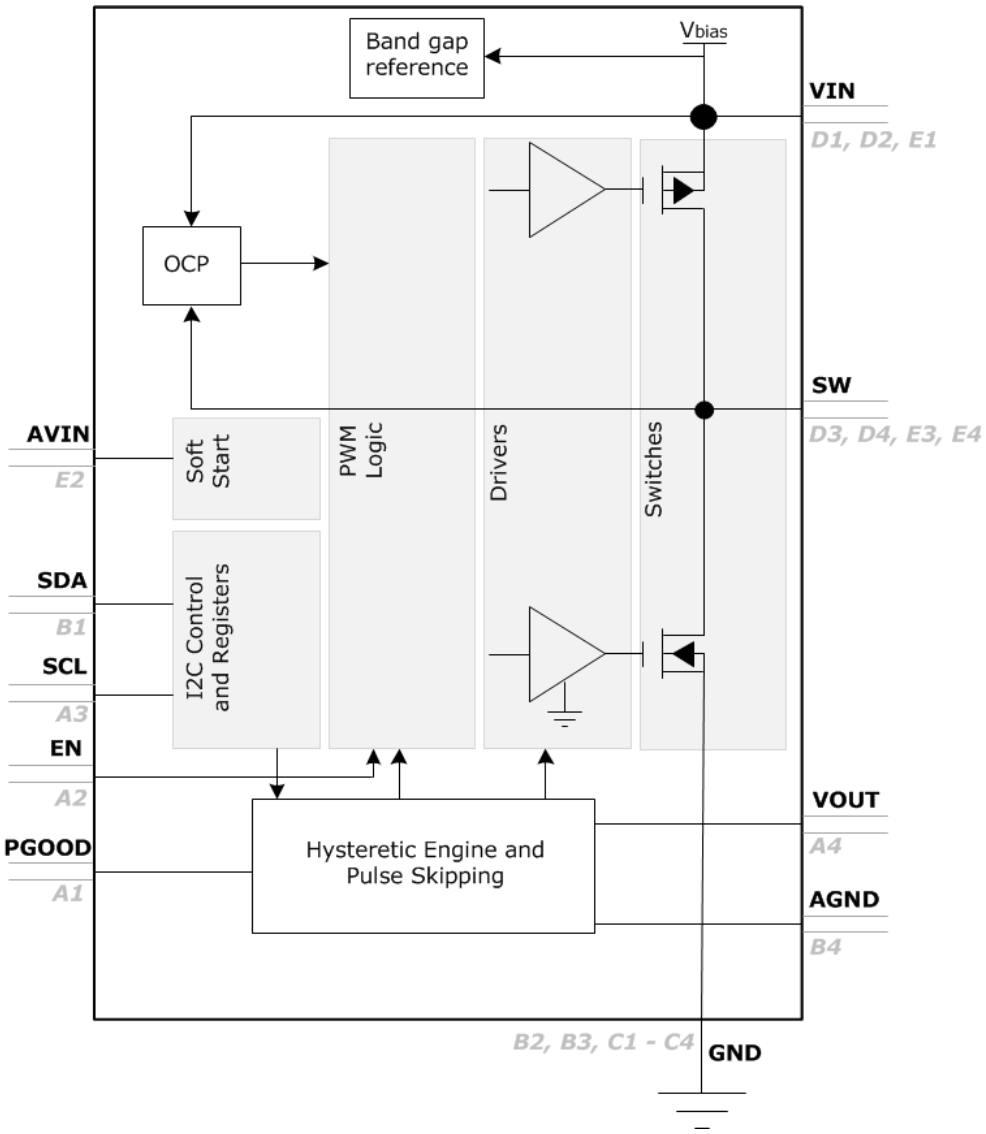
Table 2 • Pin/Ball Details

Pin /Ball Number	Pin/Ball Designator	Description
1	PGOOD	Open drain status output, requires external pull-up resistor. This pin goes low, when V_{OUT} exceeds the defined power good range, when the die is hotter than the thermal shutdown threshold and, when PVIN is above the over voltage threshold, or when PVIN is below the under voltage threshold. PGOOD goes high after the last of these fault conditions clear.
10	EN	Enable for switching regulator. Force high to enable, force low to disable the IC.
13	SCL	Serial clock input for I²C. Connect directly to GND, if unused.
12	VOUT	Output voltage sense. Connect directly to output rail or resistive voltage divider output.
2	SDA	Serial data bus (bidirectional) for I²C. Connect directly to GND, if unused.
3, PAD	GND	Ground. Connect to ground plane.
11	AGND	Analog ground. Connect to ground plane.
5,6,7,8	VIN	Input of IC and buck stage. Connect to input rail VIN (between 2.7 V and 5.5 V). A minimum input capacitance of one 1 µF and one 22 µF of X5R or a multilayer ceramic, should be placed very close to IC between this node and GND.
14	AVIN	Analog VIN voltage input pin.
4,9	SW	Switching node. Drives the external L-C low pass filter.

3.3 Functional Block Diagram

The following figure shows the functional block diagram.

Figure 3 • Functional Block Diagram



4 Electrical Specifications

The following sections provide details of the electrical specifications for LX7219.

4.1 Absolute Maximum Ratings

The following table gives absolute maximum ratings for LX7219. Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact the long-term operating reliability.

Table 3 • Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN, SW to GND	–0.3	7	V
AVIN, VOUT, SDA, SCL, EN, PGOOD to GND	–0.3	7	V
SW to GND (shorter than 50 ns)	–2	7	V
Maximum junction temperature		150	°C
Lead soldering temperature (30 s, reflow)		260 (+0, –5)	°C
Storage temperature	–65	150	°C

4.2 Electrical Characteristics

The following tables provide operating ratings and typical electrical characteristics.

4.2.1 Operating Ratings

Performance is generally guaranteed over the ranges mentioned in the following table, further detailed in Typical Electrical Characteristics (see page 7).

Table 4 • LX7219 Operating Ratings

Parameter	Minimum	Maximum	Unit
V_{IN}	2.7	5.5	V
Ambient Temperature	–40	85	°C
Output Current	0	6	A

Note: Corresponding absolute maximum junction temperature is 150 °C.

4.2.2 Typical Electrical Characteristics

The following specifications apply over the operating ambient temperature of –40°C ≤ TA ≤ 85°C except when the test conditions are V_{IN} = 5 V, EN = 5 V, SCL = 5 V, SDA = 5 V or default register settings. The typical values stated are either by design or by production testing at 25 °C ambient temperature.

Table 5 • LX7219 Typical Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Input Voltage						
I_Q	Input current	I_{LOAD} = 0, PSM enabled	200	440	600	µA
I_{IN}	Input current at shut down	EN = GND, T_A = 25 °C		0.1	14	µA
$I_{IN\_I^2C}$	Input current I²C shut down	V_{SEL}(7) = low, EN = high		100	120	µA

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
UVLO	Under voltage rising threshold	V_{IN} rising		2.6	2.89	V
$UVLO_{HYST}$	UVLO hysteresis			0.26		V
OVP_R	Over voltage rising threshold		5.90		6.30	V
OVP_F	Over voltage falling hysteresis			0.2		V
V_{REF}						
T_{SS}	V_{REF} slew rate	SLEW: Ctrl2(2:1) = 01		0.8		mV /µs
T_{HICCUP}	Hiccup time	V_{OUT} = 0.2V		9.8		ms
Output Voltage						
V_{OUT}	Default V_{OUT}	V_{OUT} = 0.9 V, (V_{IN} = 2.7 V – 5 V), V_{SEL} = 40 h	0.891	0.9	0.909	V
	V_{OUT} I^2C V_{SEL}	V_{OUT} = 0.75 V, (V_{IN} = 2.7 V – 5 V), V_{SEL} = 20 h	0.743	0.75	0.758	V
		V_{OUT} = 0.75 V, (V_{IN} = 2.7 V – 5 V), V_{SEL} = 20 h, –10 °C ≤ T_A ≤ 85 °C	0.741	0.75	0.759	V
		V_{OUT} = 1.197 V, (V_{IN} = 2.7 V – 5 V), V_{SEL} = 7Fh	1.183	1.195	1.207	V
	Line regulation	V_{IN} from 3 V to 5.5 V, I_{LOAD} = 1A[1]		0.1		%
	Load regulation	I_{LOAD} = 0 A to 5 A[1]		–0.23		%/A
	V_{OUT} input current			0	1	µA
V_{OUV}	V_{OUT} under voltage threshold	V_{OUT} below this threshold will initiate a hiccup sequence	77	82	85	%V_{REF}
Switch (SW)						
R_{DSON_H}	High side on resistance	V_{IN} = 5 V		22		mΩ
R_{DSON_L}	Low side on resistance	V_{IN} = 5 V		13		mΩ
OCP	Current limit[1]		7.5	8.5	10.0	A
T_{SH}	Thermal shut down threshold[1]			150		°C
T_H	Hysteresis[1]			20		°C
F_{SW}	PWM switching frequency		1.0	1.2	1.4	MHz
R_{SWDISC}	SW discharge resistance	EN = low; Discharge: Ctrl2(4) = 1	80	200	1400	Ω
EN, SDA (as input), and SCL						
V_{IH}	Input high		1.1			V
V_{IL}	Input low				0.4	V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_H	Hysteresis		0.05	0.15		V
I_{II}	Input current			0	1.1	µA
V_{OL}	Low level output voltage	Logic0 output voltage, Isink = 2 mA[1]	0		0.2 * VDD	V
I_{OL}	Low level output current	V_{OL} = 0.4 V[1]	3			mA
PGOOD						
V_{PG90}	PGOOD V_{OUT} lower threshold	V_{OUT} rising, percentage of V_{REF}	82	85	88	%V_{REF}
V_{PG110}	PGOOD V_{OUT} upper threshold	V_{OUT} falling, percentage of V_{REF}	105	110	115	%V_{REF}
V_{PGHY}	Hysteresis	Percentage of V_{REF}		5		%V_{REF}
PG_{RDSON}	PGOOD pull down resistance			13	20	Ω
	PGOOD leakage current			0	1	µA
	PGOOD delay	PGOOD rising edge delay	25	45	78	ms
7 Bit DAC						
	Differential linearity	Monotonicity assured by design			0.8	LSB

Note 1: These values are guaranteed by design.

4.2.3 Thermal Properties

The following table gives the thermal properties of LX7219. The θ_{JA} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The typical value in the following table is for a four-layer board in accordance with JESD-51 (JEDEC).

Table 6 • Thermal Resistance

Thermal Resistance		Typical	Units
θ_{JA}	VQFN	49	°C/W

4.2.4 Application Specifications

The following table describes the application specific parameters and their values.

Table 7 • LX7219 Application Specifications Details

Efficiency	I_{OUT} = 2.0 A, VCC = 5 V, V_{OUT} = 3.3 V	95%
	I_{OUT} = 4.0 A, VCC = 5 V, V_{OUT} = 0.9 V, Inductor (IHLP-2020CZ-01)	> 84%
	I_{OUT} = 4.0 A, VCC = 5 V, V_{OUT} = 0.9 V, Inductor (SPM5015)	> 83%

V_{OUT} Max Transient	100 mA ↔ 4A, 1 A/2 µs, C_{LOAD} = 4 x 22 µF ceramic caps, 0.47 µH inductor Step Duration 1 – 50 µs	Peak to peak < 80 mV
Typical Load Inductance	IHLP2020CZ (DCR = 6.7 mΩ, IDC = 12.2 A, ISAT = 16 A) SPM5015 (DCR = 16.3 mΩ, IDC = 7 A, ISAT = 13.8 A)	0.47 µH
Typical Load Capacitance	6.3 V, X5R	4 x 22 µF

4.3 I2C Timing Specifications

The following table gives the details of I²C timing specifications. All values are referred to V_{IH} (minimum) and V_{IL} (maximum) levels.

Table 8 • I2C Timing Specifications Details

Symbol	Parameter	Conditions	C_b = 100 pF (max)[2]		C_b = 400 pF		Unit
			Minimum	Maximum	Minimum	Maximum	
f_{SCHL}	SCL clock frequency		0	3.4	0	0.4	MHz
$t_{SU;STA}$	Set–up time for a repeated START condition		160	–	600	–	ns
$t_{HD;STA}$	Hold time (repeated) START condition		160	–	600	–	ns
t_{LOW}	LOW period of the SCL clock		160	–	1300	–	ns
t_{HIGH}	HIGH period of the SCL clock		60	–	600	–	ns
$t_{SU;DAT}$	Data set–up time		10	–	100	–	ns
$t_{HD;DAT}$	Data hold time		0	70	0	–	ns
t_{rCL}	Rise time of SCL signal		10	40	20 * 0.1C_b	300	ns
t_{rCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit		10	80	20 * 0.1C_b	300	ns
t_{fCL}	Fall time of SCL signal		10	40	20 * 0.1C_b	300	ns
t_{rDA}	Rise time of SDA signal		10	80	20 * 0.1C_b	300	ns
t_{fDA}	Fall time of SDA signal		10	80	20 * 0.01 C_b	300	ns
$t_{SU;STO}$	Set–up time for STOP condition		160	–	600	–	ns
t_{BUF}	Bus free time between a STOP and START condition		160	–	1300	–	ns
$t_{VD;DAT}$	Data valid time		–	160	–	900	ns
$t_{VD;ACK}$	Data valid acknowledge time		–	160	–	900	ns
C_b	Capacitive load for each bus line	SDA and SCL lines	–	100		400	pF

Note: 2. Loads in excess of 100 pF will restrict bus operation speed to < 3.4 MHz

5 Operation Theory

The following sections describe the operating conditions for LX7219.

5.1 Basic Operation

The LX7219 compares V_{OUT} voltage to an internal reference (V_{REF}). When V_{OUT} is lower than V_{REF}, the upper switch turns on and the lower switch turns off. When V_{OUT} is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp helps to keep the switching frequency constant over a wide range of output capacitor values and parasitic components (that is, ESR, ESL). In addition, a frequency control loop keeps the switching frequency constant during continuous conduction mode. At light loads, if enabled, the converter automatically reduces the switching frequency and enters discontinuous conduction to optimize efficiency, while ensuring low V_{OUT} ripple voltage. An integrated I^2C bus interface, operating up to 3.4 Mbps, adds the following use programmability to the converter:

1. On the fly programming of the output voltage in 4.7 mV increments.
2. Enable/disable the regulator.
3. Allow PSM or limit operation to only PWM mode.
4. Set the V_{REF} slew rate.
5. Switch node slew rate control.

5.2 Setting the Output Voltage

The output voltage is set with the reference voltage and how the VOUT pin (12) is connected to the output. With a direct connection (See Typical 5 V to 0.9 V at 6 A Schematic (see page 3)), the reference voltage equals the output voltage. When the VOUT pin (12) is connected to a resistor divider, it determines the output voltage. At startup, the reference voltage is 0.9 V for LX7219-02 or 0.8 V for LX7219-01. After startup, the reference voltage can be programmed with the I^2C bus V_{SEL} register value using the following equation.

$$V_{REF} = 0.6\ V + N_{SEL} \times 0.0046875\ V$$

Where, N_{SEL} is the decimal value of the 7 V_{SEL} bits.
Use the following equation to calculate the output voltage.

$$V_{OUT} = V_{REF} \times (1 + R_{TOP}/R_{BOTTOM})$$

Where, R_{TOP} is the resistor connected from VOUT pin to output. R_{BOTTOM} is the resistor connected from VOUT pin to GND.

5.3 Startup

If the LX7219 is enabled, when V_{IN} rises above the UVLO threshold, the regulator will initiate a startup sequence. The serial port registers are initialized to their default values and all internal bias voltages and currents are allowed to stabilize. V_{REF} then ramps up from 0 V to the default voltage at the default slew rate. At the end of the ramp time, PGOOD is allowed to go high after V_{OUT} has reached the PGOOD rising threshold. During the ramp time, the LX7219 switches to PSM to allow discontinuous operation. This switchover is independent of the MODE bit setting.

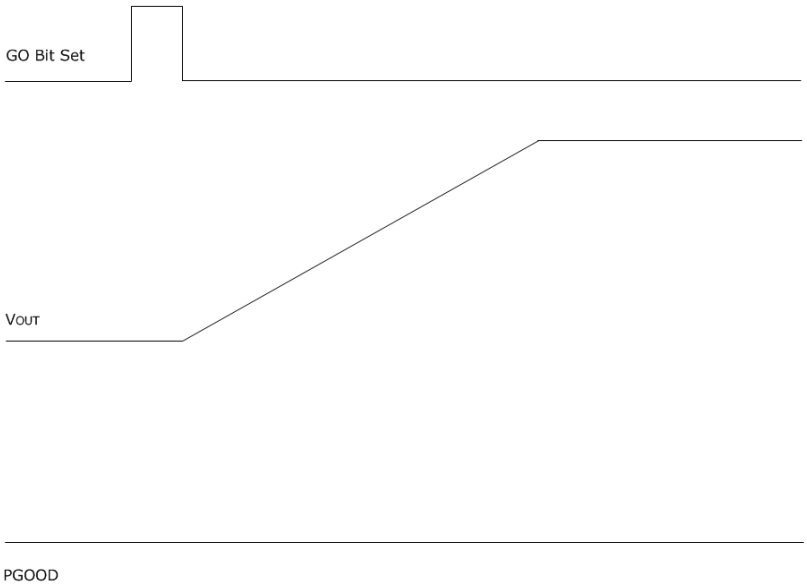
5.4 Over Current Protection

The LX7219 protects against all types of short circuit conditions. Cycle by cycle, over current protection turns off the upper switch when the current exceeds the OCP threshold. When this occurs, the upper switch is held off for at least 350 ns, before being allowed to turn on again. After startup, if V_{OUT} drops below the V_{OUT} under voltage threshold, a hiccup sequence will be initiated, where both output switches are shut off for 1.5 ms before initiating another soft start cycle. This protects against a crowbar short circuit. The V_{OUT} under voltage detection is not active during start up.

5.5 Positive Voltage Transitions

After the initial startup sequence, the output voltage can be programmed to a new value by programming the V_{SEL} register bits and then asserting the GO bit. V_{REF} transitions to the new value at the programmed slew rate. The PGOK monitor bit is deasserted during the V_{REF} ramp time, or when V_{OUT} is outside the error envelope.

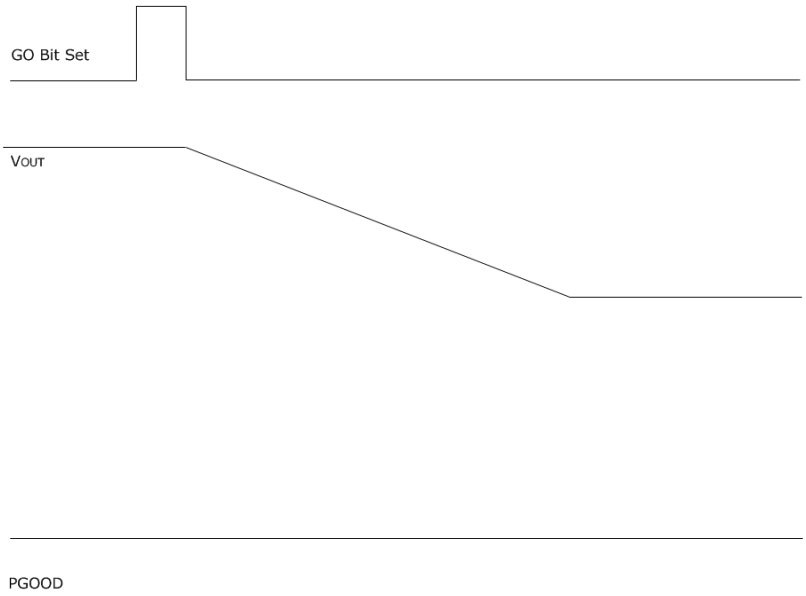
Figure 4 • Positive Voltage Transition



5.6 Negative Voltage Transitions

A negative voltage transition occurs when a lower output voltage is programmed into the V_{SEL} register, and initiated by asserting the GO bit. In PSM, the LX7219 will not discharge the output filter capacitor.

Figure 5 • Negative Voltage Transition



5.7 Enabling Regulator from I2C Bus

In addition to the EN pin, the regulator can be enabled and disabled through the I²C bus by programming the control register. During disable, the regulator and most of the support circuitry is turned off. However, the I²C bus circuitry is still active and may be programmed.

5.8 Switch Node Rise Rate Adjustment

The LX7219 can be programmed to operate in a lower emissions mode by slowing down the switch node rise rate. In this mode, the switch node rise rate slows down by 25%, reducing the switching frequency harmonic content.

6 I2C Interface

This section describes details of I²C interface.

6.1 I2C Port Functional Description

The following list describes functional characteristics of I²C interface.

- Simple two wire, bidirectional, and serial communication port.
- Multiple devices on same bus speeds from 400 Kbps (FS-Mode) to 3.4 Mbps (HS-Mode).
- SOC master controls bus.
- Device listens for the unique address that precedes data.

6.2 I2C Port Description

The LX7219 includes an I²C compatible serial interface, using two dedicated pins: SCL and SDA for I²C clock and data respectively. Each line is externally pulled up to a logic voltage, when they are not being controlled by a device on the bus. The LX7219 interface acts as an I²C slave that is clocked by the incoming SCL clock. The LX7219 I²C port supports both the fast mode (400 kHz maximum) and typically the high speed mode (3.4 MHz maximum). The data on the SDA line must be stable during the high period of the clock signal (SCL). The state of the SDA line can only be changed when SCL is LOW (except for start, stop, and restart).

6.3 Register Map

The LX7219 has five 8-bit user-accessible registers. See Control Register Bit Definitions (see page 18).

6.4 Slave Address

In the following table, the binary values of the address given to the part number with address (E0h) is described.

Table 9 • I2C Slave Address

7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	R/W

6.5 Start and Stop Commands

When the bus is idle, both SCL and SDA must be high, except in the power up case where they may be held high or low during the system power up sequence. The STX SOC (bus master) signals; start and stop bits signify the beginning and the end of the I2C transfer. The start condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. The stop condition is defined as the SDA transitioning from LOW to HIGH while the SCL is HIGH. The STX SOC acts as the I2C master and always generates the start and stop bits. The I2C bus is considered to be busy after start condition and free after stop condition. During data transfer, STX SOC master can generate repeated start conditions. The start and the repeated start conditions are functionally equivalent.

6.6 Data Transfers

Data is transferred in 8 bit bytes by SDA with the MSB transferred first. Each byte of data has to be followed by an acknowledge (ACK) bit. The acknowledged related clock pulse is generated by the master. The acknowledge occurs when the transmitter master releases the SDA line to a high state during the acknowledge clock. The SDA line must be pulled down by the receiver slave during the 9th clock pulse to signify acknowledgment. A receiver slave which has been addressed, must generate an acknowledgement ("ACK") after each byte has been received.

After the start condition, the STX SOC (I2C) master sends a chip address. The standard I2C address is seven bits long. The eighth bit is a data direction bit (R/W). For the eighth bit (LSB), a "0" indicates a WRITE and a "1" indicates a READ. (For clarification, communications are broken up into 9-bit segments, one byte followed by one bit for acknowledging.) The second byte selects the register to which the data is written. The third byte contains data to write to the selected register. When a receiver slave doesn't acknowledge the slave address, the data line must be left high by the slave. The master can then generate a stop command to abort the transfer. If a slave receiver acknowledges the slave address but sometime later during the transfer it cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave, generating the not acknowledge on the first byte to follow. The slave leaves the data line high and the master generates the stop command. In a read operation, the data line is left high by the slave and master after the slave has transmitted a byte of data to the master, but this is a *not acknowledge* that indicates that the data transfer is successful.

6.6.1 Data Transfer Timing for Write Commands

Transfer timing is designed to ensure that the bad data is not written into the registers. Data from a write command is only stored after a valid stop command has been performed.

6.7 I2C Electrical Characteristics

The minimum high and low periods of the SCL clock specified in the I²C Timing Specification (see page 10), determine the maximum bit transfer rates of 400 Kbits/s for fast-mode devices, and 3.4 Mbits/s for HS-mode Plus. Devices must follow the transfers at their own maximum bit rates, either by transmitting or receiving at that speed or by applying the I²C clock synchronization procedure, which forces the master into a wait state and stretch the low period of the SCL signal. In the latter case, the bit transfer rate is reduced.

Definition for FS-Mode Devices on the I2C Port (see page 16) and Timing Definition for HS-Mode Devices on the I²C Port (see page 17) show all timing parameters for the HS and FS-mode timing. The 'normal' start condition S does not exist in HS-mode. Timing parameters for address bits, R/W bit, acknowledge bit, and data bits are all the same. Only the rising edge of the first SCL clock signal, after an acknowledge bit has a larger value, it is because the external Rp has to pull-up SCL without the help of an internal current-source.

The HS and FS-mode timing parameters for the bus lines are specified in the I²C Timing Specification (see page 10). The minimum high and low periods and the maximum rise and fall times of the SCL clock signal determine the highest bit rate. With an internally generated SCL signal with low and high level periods of 200 ns and 100 ns respectively, an HS-mode master fulfills the timing requirements for the external SCL clock pulses (taking the rise and fall times into account) for the maximum bit rate of 3.4 Mbit/s. A basic frequency of 10 MHz, or a multiple of 10 MHz, can be used by an HS-mode master to generate the SCL signal. There are no limits for maximum high and low periods of the SCL clock, and there is no limit for a lowest bit rate.

Timing parameters are independent for capacitive load, up to 100 pF for each bus line allowing the maximum possible bit rate of 3.4 Mbit/s. At a higher capacitive load on the bus lines, the bit rate decreases gradually. The timing parameters for a capacitive bus load of 400 pF are specified in I²C Timing Specification (see page 10), allowing a maximum bit rate of 1.7 Mbit/s. For capacitive bus loads between 100 pF and 400 pF, the timing parameters must be interpolated linearly. Rise and fall times are in accordance with the maximum propagation time of the transmission lines SDA and SCL to prevent reflections of the open ends.

The following figures give details of read and write protocols.

Figure 6 • Write Protocol

1	7	1	1	8	1	8	1	1
Start	XXXXXXXX Device Address	0 Write	ACK	XXXXXXXX Register Address	ACK	XXXXXXXX Data	ACK	Stop

Figure 7 • Read Protocol

1	7	1	1	8	1	1	7	1	1	8	1	1
Start	XXXXXXXX Device Address	0 Write	ACK	XXXXXXXX Register Address	ACK	Repeated Start	XXXXXXXX Device Address	Read	ACK	XXXXXXXX Data	Master ACK	Stop

The following figures show the timing definitions for FS-mode and HS-mode devices on the I²C port.

Figure 8 • Definition for FS-Mode Devices on the I2C Port

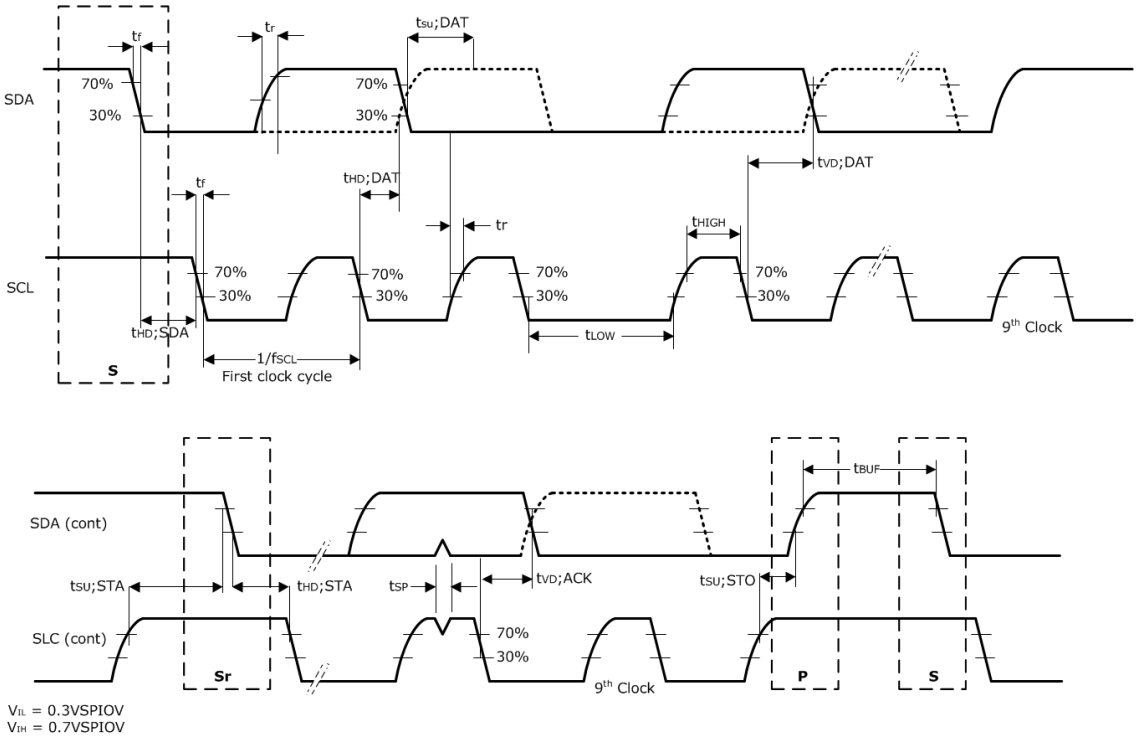
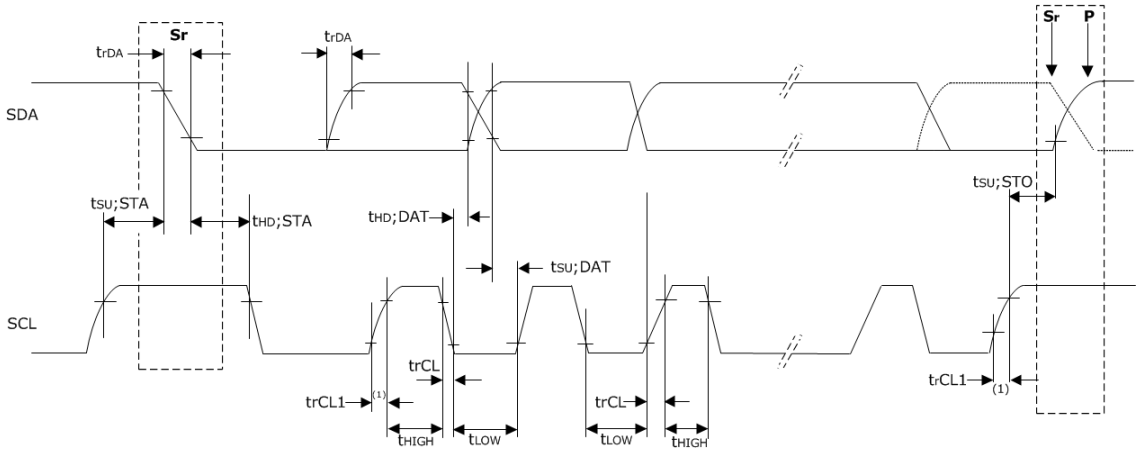


Figure 9 • Timing Definition for HS-Mode Devices on the I2C Port



= MCS current source pull-up

= RIP resistor pull-up

(1) First rising edge of the SCL signal after Sr and after each acknowledge bit

The following diagrams show write and read cycles.

Figure 10 • Write Cycle Diagram

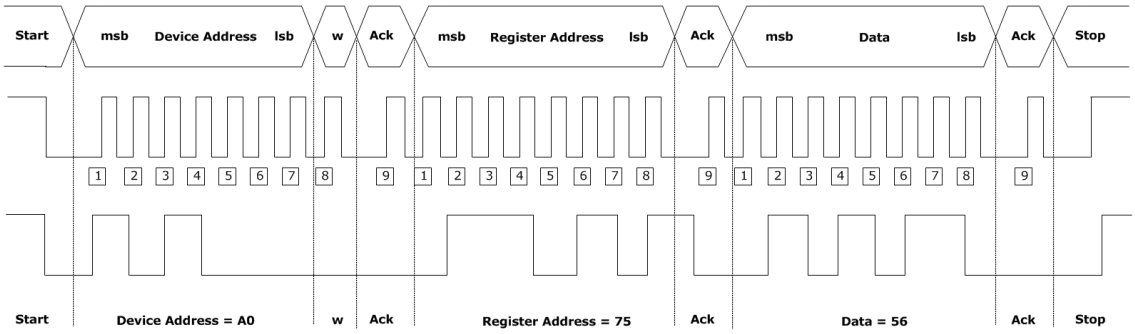
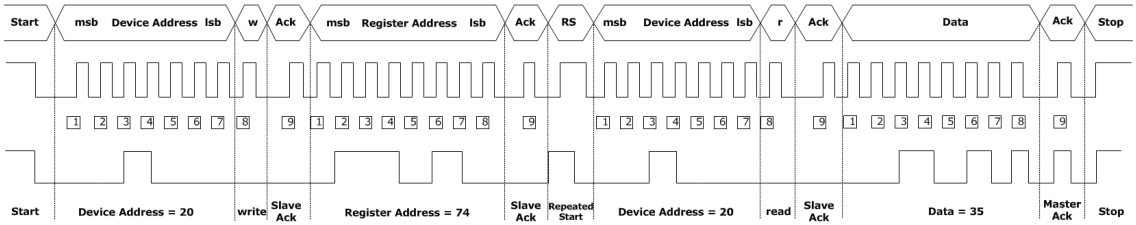


Figure 11 • Read Cycle Diagram



6.8 Control Register Bit Definitions

The following table describes the control register bits and their descriptions.

Table 10 • Control Register Bits and Definitions

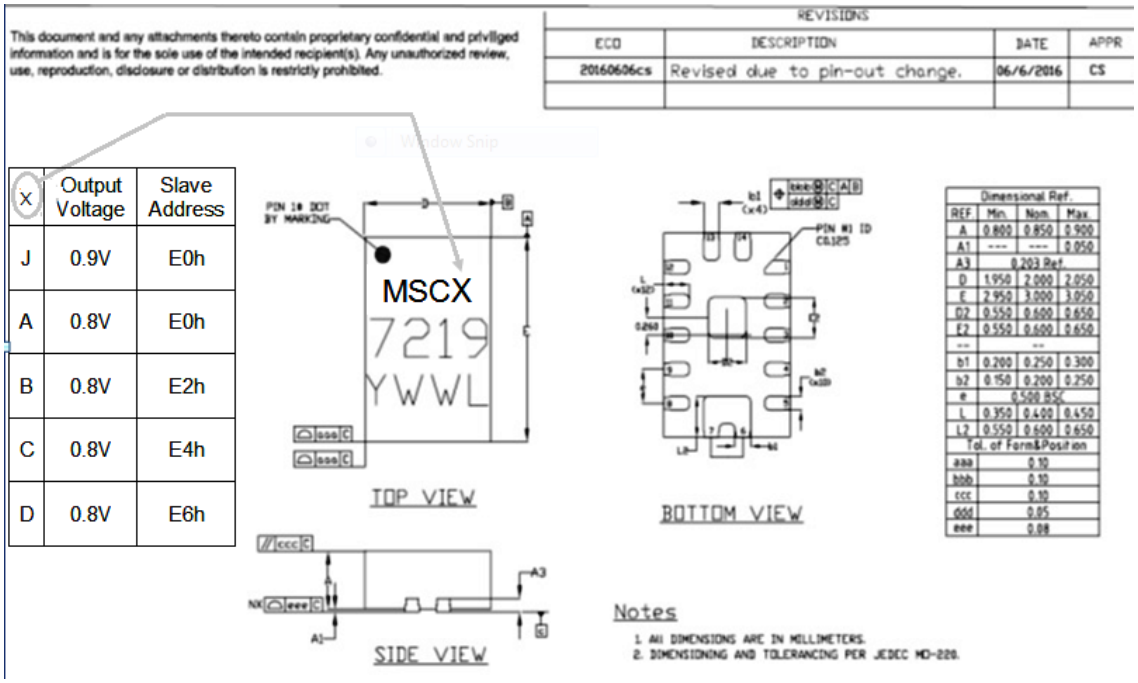
Bit	Name	Value	Description
Status, Address 00h			
7:3	Reserved		
2	OCP		Latched to 1 if the over current limit is reached. Write a "1" to reset the status flag.
1	OTP		Latched to 1 if an over temperature event occurs. Write a "1" to reset the status flag.
0	FB_UVLO		Latched to 1 if a FB_UVLO event occurs. Write a "1" to reset the status flag.
V_{SEL}, Address 01h, (DAC)			
7	EN	1-d	Device enabled.
		0	Device disabled.
6:0	V_{SEL}[6:0]		7-bit DAC value to set V_{REF}. The default value is determined by the part ordering code.
Ctrl1, Address 02h, (reg2)			
7:6	Reserved	00-d	
5	ctrl1	1-d	
4	DLY_DIS	1	45 ms delay on PGOOD is enabled.
		0-d	Disable 45 ms delay on PGOOD.
3	SW_RATE	0	High switch node rise rate.

		1-d	Reduced switch node rise rate.
2	Reserved	1-d	
		0	
1	Reserved	1-d	
		0	
0	MODE	0	PWM mode only – NO PSM.
		1-d	Power saving mode – allows discontinuous conduction.
Vendor ID, Address 03h (Read Only)			
7:4	VID[3:0]	0010	Microsemi vendor ID
3:2	A1A0	00	Designates the slave address version. These bits correspond to the two LSB bits.
1:0	V_{OUT}	XX	XX designates the default output voltage version: 01 = 0.8 V, 10 = 0.9 V.
Ctrl2, Address 04h, (reg4)			
7:6	Reserved		
5	GO	1	Writing to this bit, starts a V_{OUT} transition regardless of its initial value.
		0-d	The V_{OUT} is ramped to the default V_{SEL} value.
4	Discharge	1	When the regulator is disabled, the output voltage is discharged through the SW pin.
		0-d	When the regulator is disabled, the output voltage is not discharged.
3	PGOK (read only)	1	This bit is high when output is in regulation and V_{REF} has stabilized.
		0	This bit is low during an output voltage transition or when the output is not in regulation.
2:1	SLEW		
		01-d	V_{REF} slews at 0.8 mV/µs.
		10	V_{REF} slews at 2.2 mV/µs.
		11	V_{REF} slews at 8.4 mV/µs.
0	Reserved		

7 Package Markings and Dimensions

The following figure shows the outline diagram and the dimensions of LX7219.

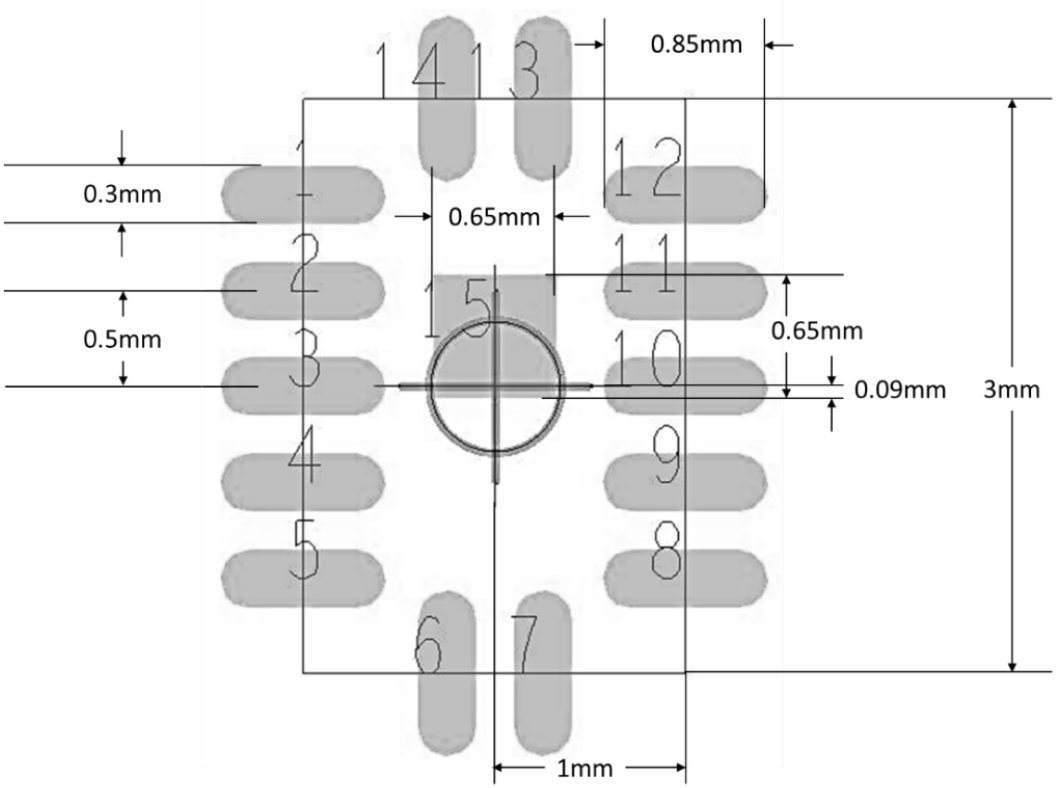
Figure 12 • Package Markings and Dimensions



8 Land Pattern Recommendation

The following figure shows the land pattern recommendation for Lx7219.

Figure 13 • LQ 14-Pin and Gnd Pad (15) VQFN Package Land Pattern



Disclaimer:
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