

## N-Channel Power MOSFET

600V, 3A, 1.5Ω

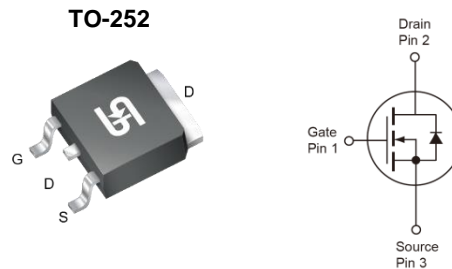
### FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- 100% UIS & Rg tested
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

### APPLICATIONS

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	600	V
$R_{DS(on)}$ (max)	1.5	Ω
$Q_g$	8	nC



**Note:** MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current <sup>(Note 1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	3
		$T_C = 100^\circ\text{C}$	2
Pulsed Drain Current <sup>(Note 2)</sup>	$I_{DM}$	9	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	55	W
Single Pulse Avalanche Energy <sup>(Note 3)</sup>	$E_{AS}$	100	mJ
Single Pulse Avalanche Current <sup>(Note 3)</sup>	$I_{AS}$	2	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	2.2	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	52	°C/W

**Thermal Performance Note:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

<b>ELECTRICAL SPECIFICATIONS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1mA$	$BV_{DSS}$	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1mA$	$V_{GS(TH)}$	3.5	4.2	5.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V$	$I_{DSS}$	--	--	100	$\mu\text{A}$
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1A$	$R_{DS(on)}$	--	1.3	1.5	$\Omega$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 300V, I_D = 3A,$ $V_{GS} = 10V$	$Q_g$	--	8.1	--	nC
Gate-Source Charge		$Q_{gs}$	--	2.5	--	
Gate-Drain Charge		$Q_{gd}$	--	3.4	--	
Input Capacitance	$V_{DS} = 300V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	$C_{iss}$	--	235	--	pF
Output Capacitance		$C_{oss}$	--	16	--	
Reverse Transfer Capacitance		$C_{rss}$	--	10	--	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	0.84	2.8	5.6	$\Omega$
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 300V, R_G = 10\Omega,$ $I_D = 1.5A, V_{GS} = 10V$	$t_{d(on)}$	--	18	--	ns
Turn-On Rise Time		$t_r$	--	17	--	
Turn-Off Delay Time		$t_{d(off)}$	--	33	--	
Turn-Off Fall Time		$t_f$	--	40	--	
<b>Source-Drain Diode</b> (Note 4)						
Body-Diode Continuous Forward Current		$I_S$	--	--	3	A
Body-Diode Pulsed Current		$I_{SM}$	--	--	9	A
Forward Voltage	$I_S = 3A, V_{GS} = 0V$	$V_{SD}$	--	--	1.5	V
Reverse Recovery Time	$V_{DD} = 300V, I_S = 3A$ $di_f/dt = 100A/\mu\text{s}$	$t_{rr}$	--	250	--	ns
Reverse Recovery Charge		$Q_{rr}$	--	1.9	--	$\mu\text{C}$

**Notes:**

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3.  $L = 50\text{mH}, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse test:  $PW \leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

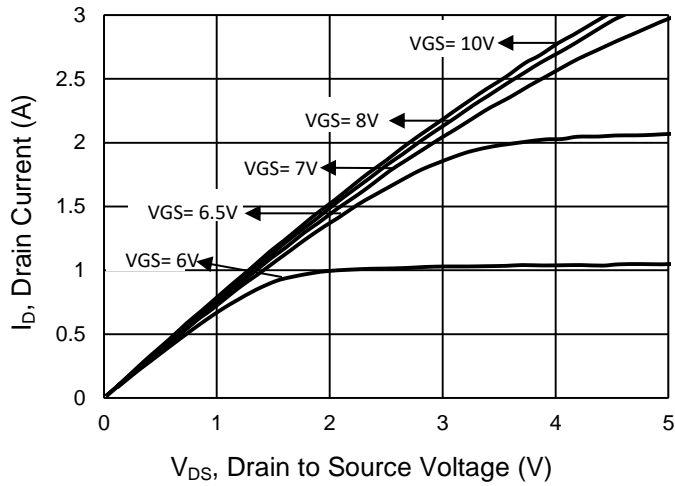
**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TSM60NC1R5CP ROG	TO-252 (DPAK)	2500pcs / 13"Reel

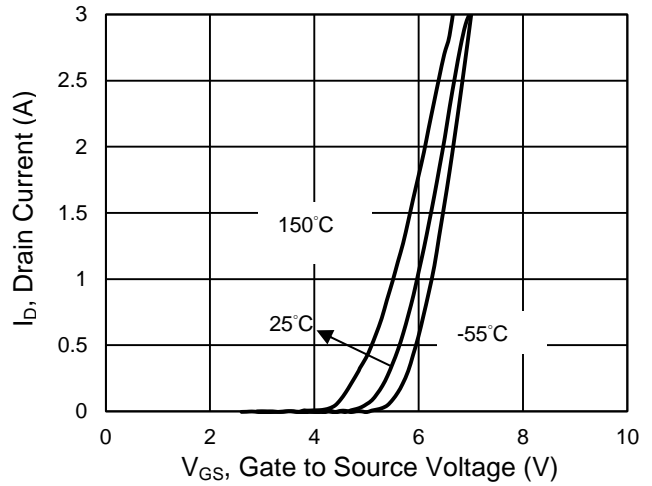
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

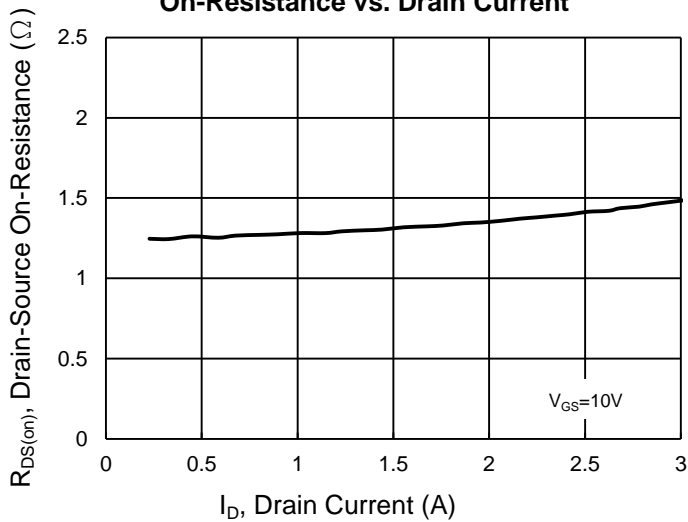
**Output Characteristics**



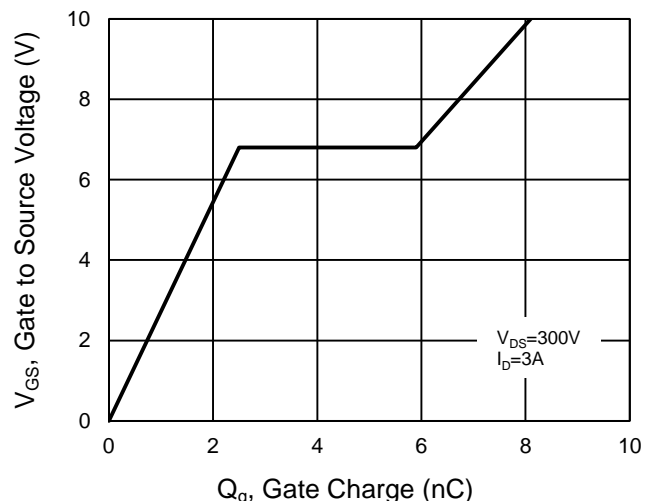
**Transfer Characteristics**



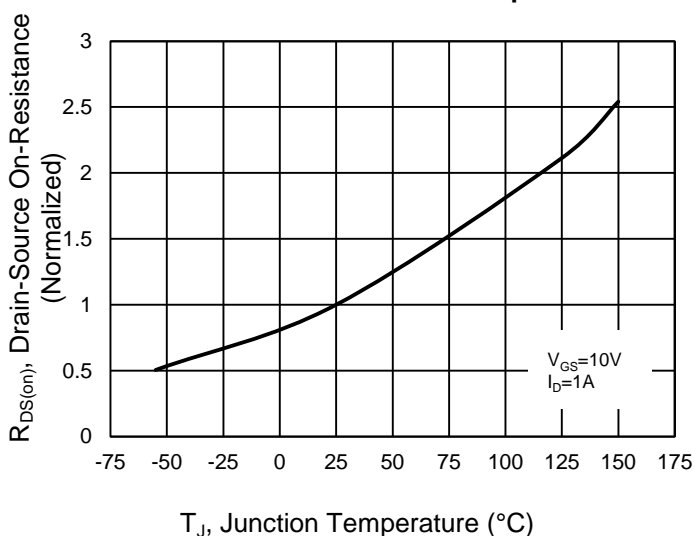
**On-Resistance vs. Drain Current**



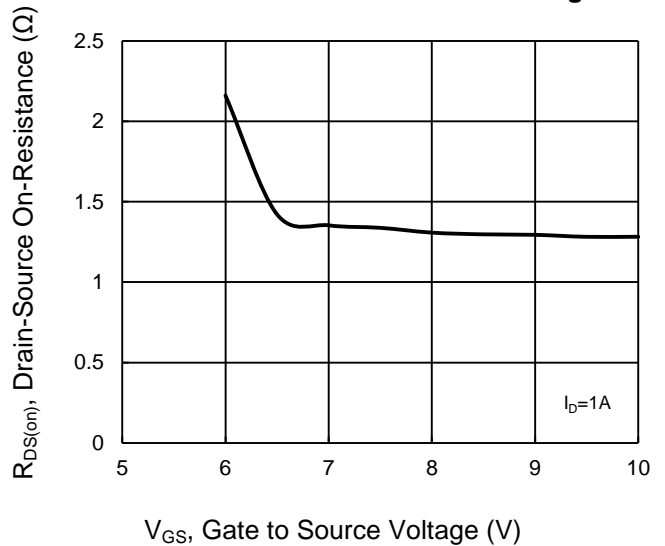
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**



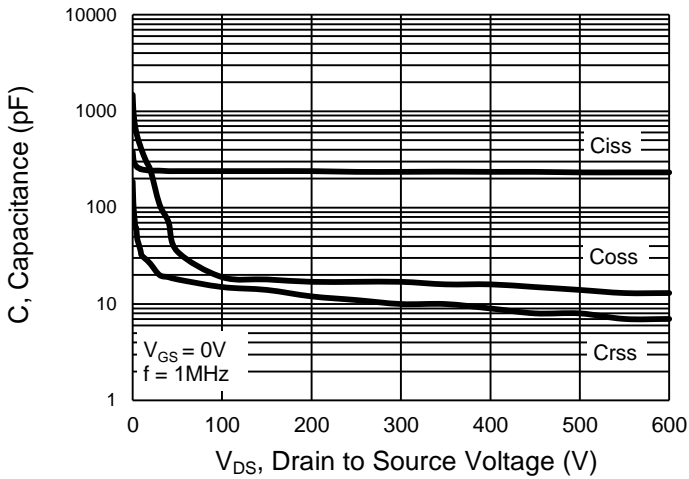
**On-Resistance vs. Gate-Source Voltage**



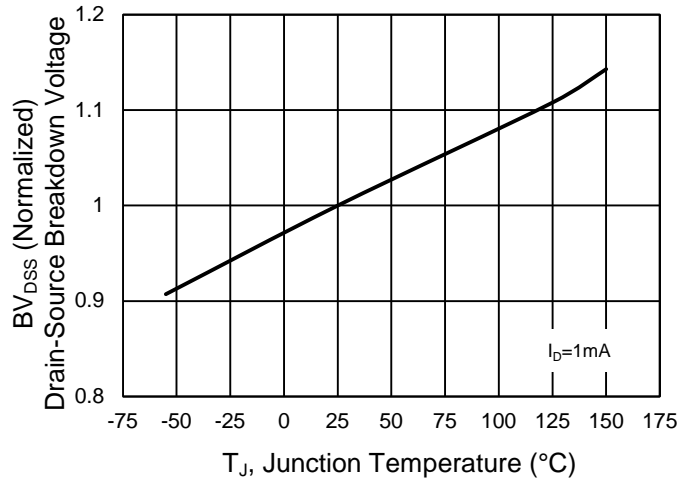
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

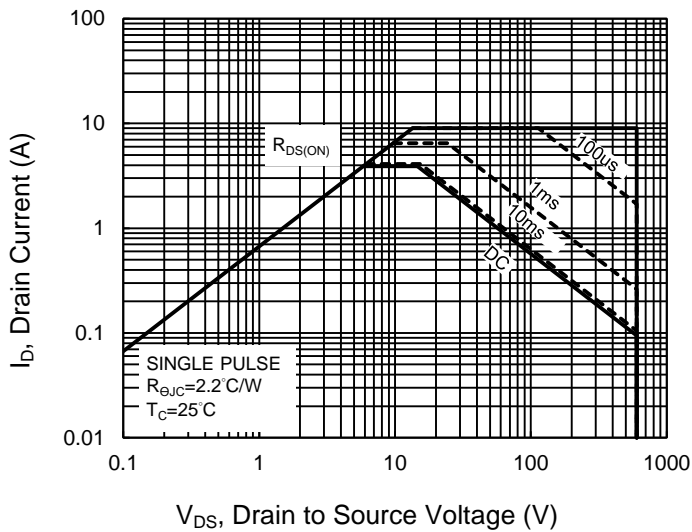
**Capacitance vs. Drain-Source Voltage**



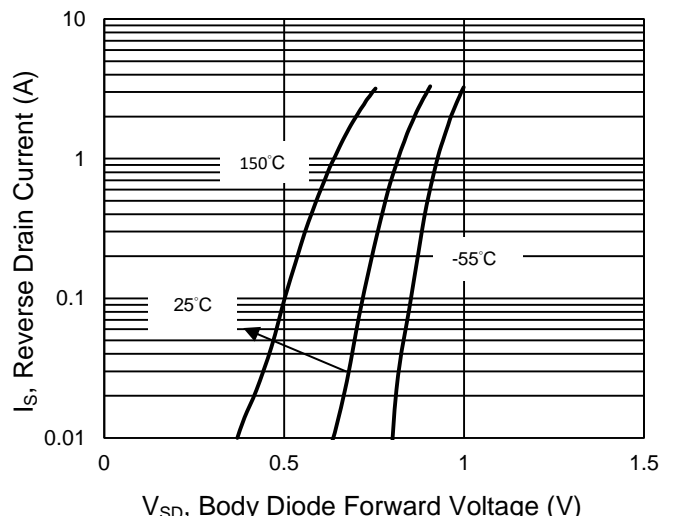
**$BV_{DSS}$  vs. Junction Temperature**



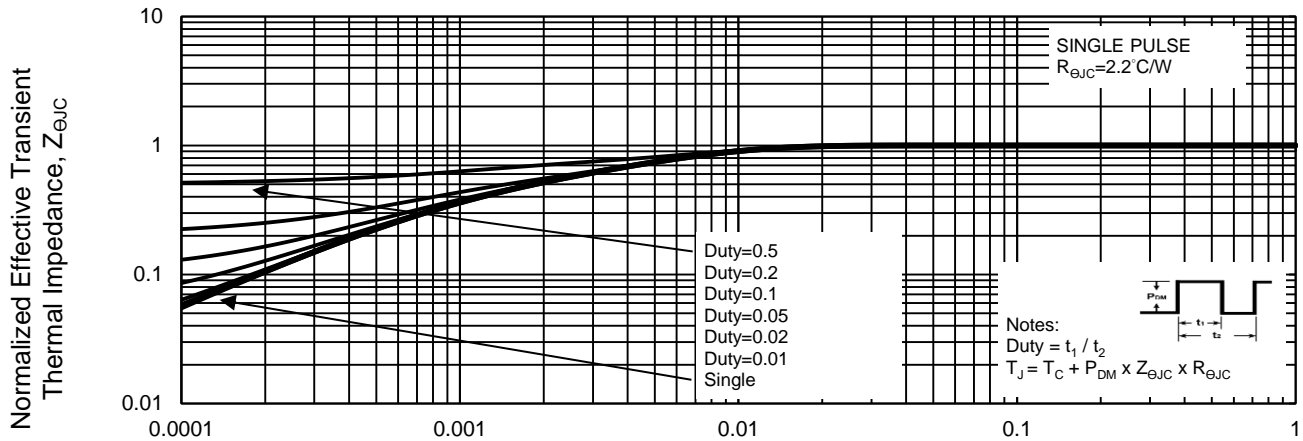
**Maximum Safe Operating Area, Junction-to-Case**



**Source-Drain Diode Forward Current vs. Voltage**



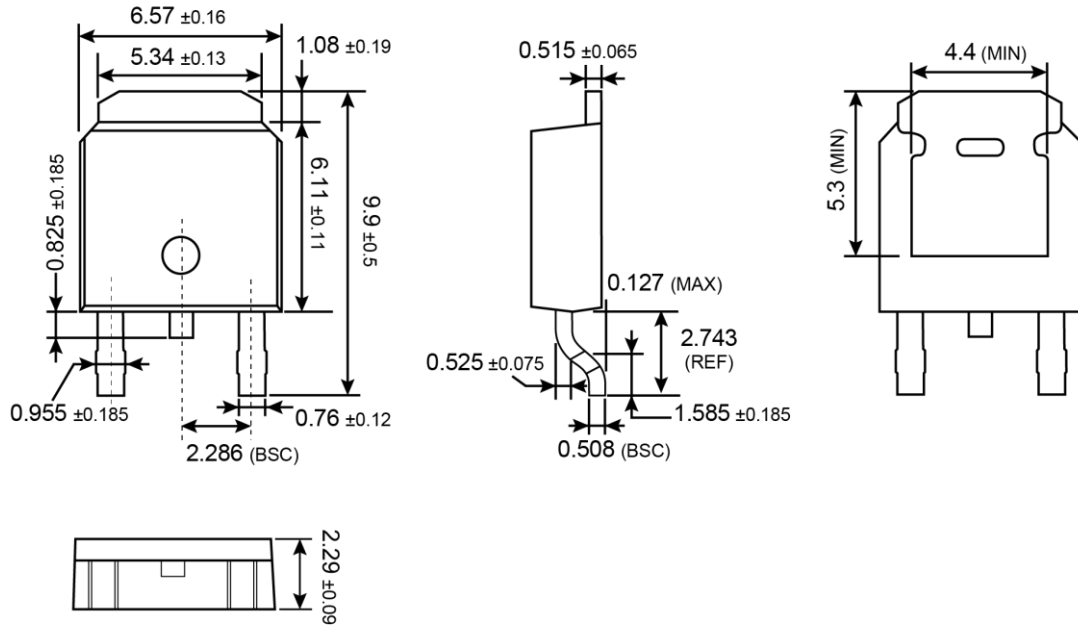
**Normalized Thermal Transient Impedance, Junction-to-Case**



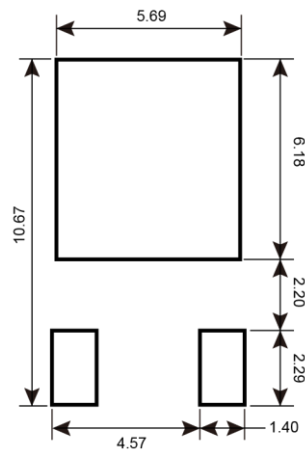
t, Square Wave Pulse Duration (sec)

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

**TO-252**



**SUGGESTED PAD LAYOUT** (Unit: Millimeters)



**MARKING DIAGRAM**



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9,A~Z)
- F** = Factory Code

#1

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