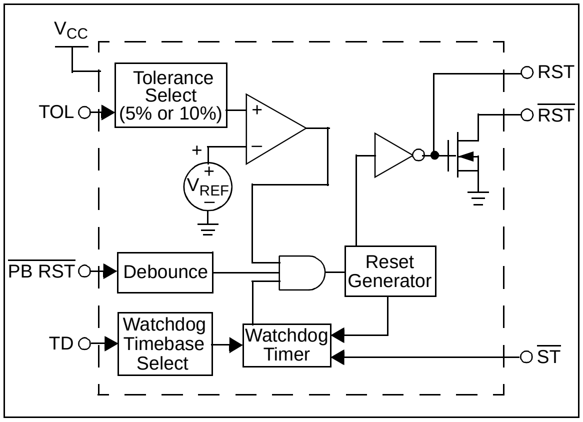
TC1232

Microprocessor Monitor

Features:

- Precision Voltage Monitor:
  - Adjustable +4.5V or +4.75V
- Reset Pulse Width – 250 ms minimum
- No External Components
- Adjustable Watchdog Timer:
  - 150 ms, 600 ms or 1.2s
- Operating Voltage 4.0V to 5.5V
- Debounced Manual Reset Input for External Override

Block Diagram



General Description:

The TC1232 is a fully-integrated processor supervisor that provides three important functions to safeguard processor sanity: precision power on/off Reset control, Watchdog Timer and external Reset override.

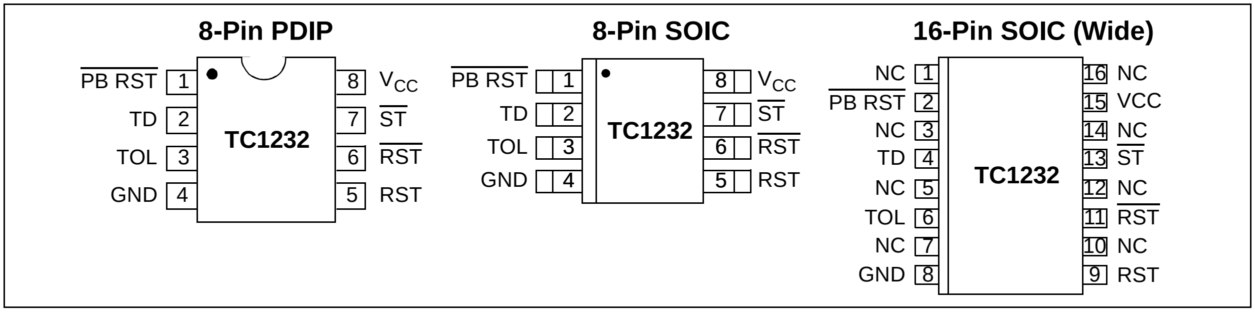
On power-up, the TC1232 holds the processor in the Reset state for a minimum of 250 ms after V_{CC} is within tolerance to ensure a stable system start-up.

Microprocessor sanity is monitored by the on-board watchdog circuit. The microprocessor must provide a periodic low-going signal on the $\overline{\text{ST}}$ input. Should the processor fail to supply this signal within the selected time-out period (150 ms, 600 ms or 1200 ms), an out-of-control processor is indicated and the TC1232 issues a processor Reset as a result.

The outputs of the TC1232 are immediately driven active when the PB input is brought low by an external push button switch or other electronic signal. When connected to a push button switch, the TC1232 provides contact debounce.

The TC1232 is packaged in a space-saving 8-Pin PDIP or SOIC package, a 16-Pin SOIC (wide) package and requires no external components.

Package Types



Device Features

Device	$\overline{\text{RST}}$ pin			RST pin		Trip Points (Max)	Minimum Reset Active Time (ms)	WDI Input Typical Timeouts (ms)	MR Input
	Type	Pull-up Resistor	Active Level	Type	Active Level				
TC1232	Open-drain	External	Low	Push-pull	High	4.75V or 4.5V	250	150, 600 or 1200	Yes

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Voltage on Any Pin (With Respect to GND)
.... -0.3V to +5.8V

Operating Temperature Range:
C-Version .... 0°C to +70°C
E-Version..................................... -40°C to +85°C

Storage Temperature Range: ....-65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{CC}	4.0	5.0	5.5	V	
$\overline{\text{ST}}$ and $\overline{\text{PB RST}}$ Input High Level	V_{IH}	2.0	—	V_{CC} +0.3	V	**Note 1**
$\overline{\text{ST}}$ and $\overline{\text{PB RST}}$ Input Low Level	V_{IL}	-0.3	—	+0.8	V	
Input Leakage $\overline{\text{ST}}$, TOL	I_L	-1.0	—	+1.0	µA	
Output Current RST	I_{OH}	-1.0	-12	—	mA	V_{OH} = 2.4V
Current RST, $\overline{\text{RST}}$	I_{OL}	2.0	10	—	mA	V_{OL} = 0.4V
Operating Current	I_{CC}	—	50	200	µA	Note 2
V_{CC} 5% Trip Point	V_{CCTP}	4.50	4.62	4.74	V	TOL = GND **(Note 3)**
V_{CC} 10% Trip Point	V_{CCTP}	4.25	4.37	4.49	V	TOL = V_{CC} **(Note 3)**
Capacitance Electrical Characteristics: Unless otherwise noted, T_A = +25°C**. (Note 4)**						
Input Capacitance $\overline{\text{ST}}$, TOL	C_{IN}	—	—	5	pF	
Output Capacitance RST, $\overline{\text{RST}}$	C_{OUT}	—	—	7	pF	

Note 1: $\overline{\text{PB RST}}$ is internally pulled up to V_{CC} with an internal impedance of typically 40 kΩ.
2: Measured with outputs open.
3: All voltages referenced to GND.
4: Ensured by design.

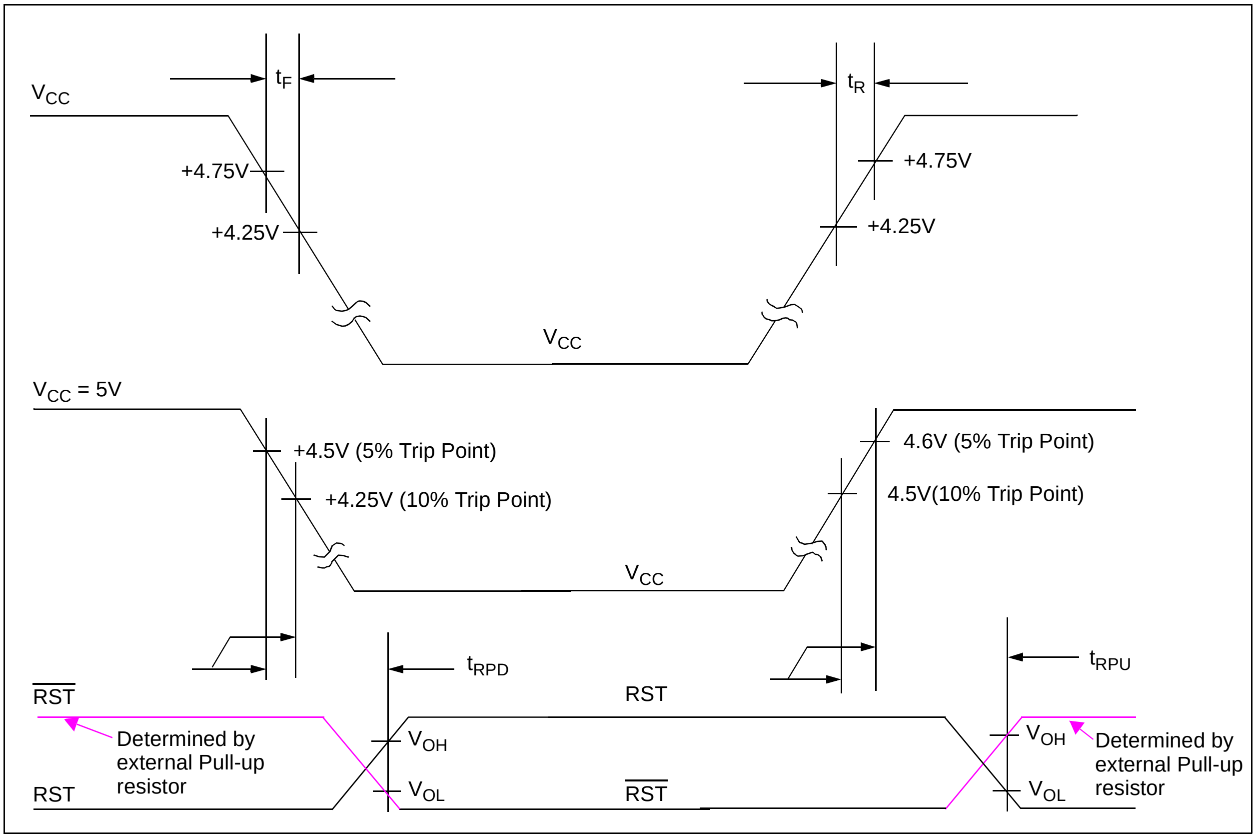


FIGURE 1-1: *Rise Time, Fall Time and Reset Detected to Reset Active Timing Waveforms.*

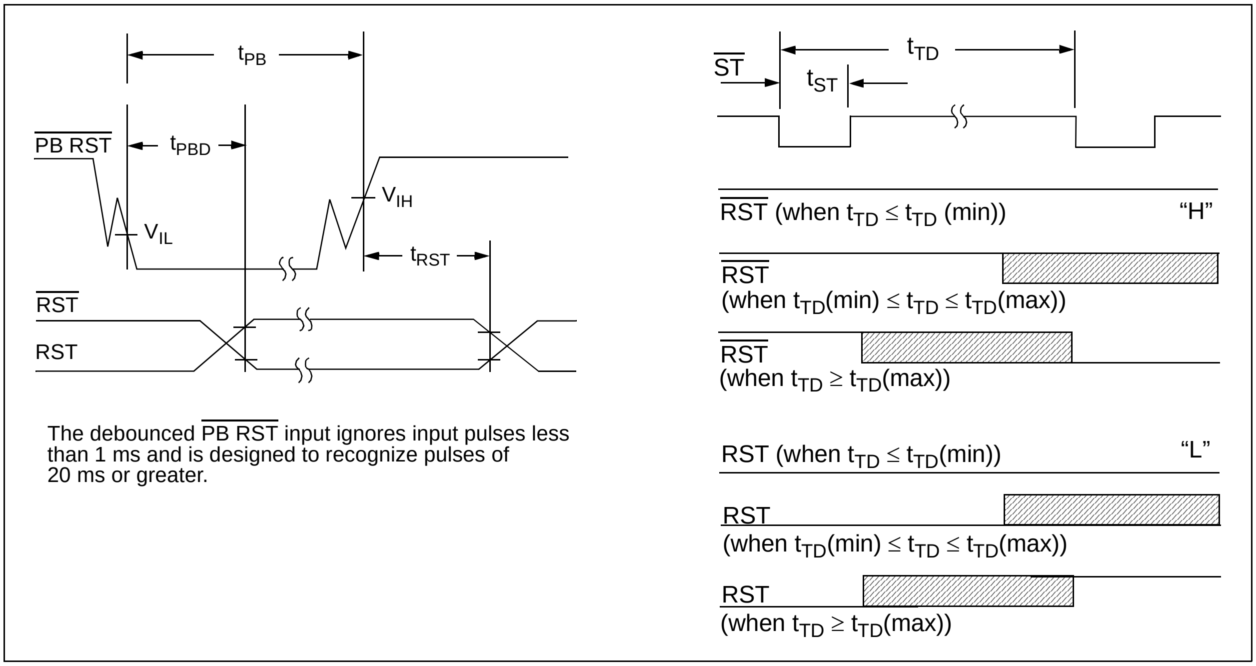
AC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{CC} Fall Time	t_F	10	—	—	µs	**Note 1**
V_{CC} Rise Time	t_R	0	—	—	µs	**Note 1**
V_{CC} Trip Point Detected to RST High and $\overline{\text{RST}}$ Low	t_{RPD}	—	—	100	ns	V_{CC} falling
V_{CC} Trip Point Detected to RST High and $\overline{\text{RST}}$ Open	t_{RPU}	250	610	1000	ms	V_{CC} rising (**Note 2**)

Note 1: Ensured by design.

2: t_R = 5 µs.



The debounced $\overline{\text{PB RST}}$ input ignores input pulses less than 1 ms and is designed to recognize pulses of 20 ms or greater.

FIGURE 1-2: *Push Button Reset and Watchdog Timer Reset Timing Waveforms.*

AC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.0V to 5.5V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
$\overline{\text{PB RST}}$ Pulse Width	t_{PB}	20	—	—	ms	Note 1
$\overline{\text{PB RST}}$ Falling Edge Low to Reset Active	t_{PBD}	1	4	20	ms	
$\overline{\text{PB RST}}$ Rising Edge High to Reset Inactive	t_{RST}	250	610	1000	ms	
$\overline{\text{ST}}$ Pulse Width	t_{ST}	20	—	—	ns	
$\overline{\text{ST}}$ Time-out Period	t_{TD}	62.5	150	250	ms	TD Pin = 0V
		250	600	1000	ms	TD Pin = Open
		500	1200	2000	ms	TD Pin = V_{CC}

Note 1: $\overline{\text{PB RST}}$ must be held low for a minimum of 20 ms to ensure a Reset.

2.0 TYPICAL PERFORMANCE CURVES

Performance Graphs are not available.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLES

Pin No.		Symbol	Pin Type	Buffer/ Driver Type	Function
8-pin PDIP, SOIC	16-pin SOIC				
1	2	$\overline{\text{PB RST}}$	I	ST	Push Button Reset Input. Input for a Manual Reset Switch. This input debounces (ignores) pulses less than 1 ms in duration and is ensured to recognize inputs of 20 ms or greater. L = Manual Reset Switch is Active, Force RST/$\overline{\text{RST}}$ pins Active H = Manual Reset Switch is Inactive. State of RST/$\overline{\text{RST}}$ pins determined by other system conditions.
2	4	TD	I	ST	Time Delay Input. The voltage level on this input determines the Watchdog Timer Time-out period. TD = 0V → t_{TD} = 150 ms TD = Open → t_{TD} = 600 ms TD = V_{CC} → t_{TD} = 1.2s
3	6	TOL	I	ST	Tolerance Input. TOL = GND, Max Voltage Trip Point (V_{CCTP}) = 4.75V (5% tolerance) TOL = V_{CC}, Max Voltage Trip Point (V_{CCTP}) = 4.5V (10% tolerance)
4	8	GND	—	P	The ground reference for the device.
5	9	RST	O	Push Pull	Reset Output (Active-High) Goes active (High) if one of these conditions occurs: 1. If V_{CC} falls below the selected Reset voltage threshold. 2. If $\overline{\text{PB RST}}$ pin is forced low. 3. If $\overline{\text{ST}}$ pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up.
6	11	$\overline{\text{RST}}$	O	Open Drain	Reset Output (Active-Low) Goes active (Low) if one of these conditions occurs: 1. If V_{CC} falls below the selected Reset voltage threshold. 2. If $\overline{\text{PB RST}}$ pin is forced low. 3. If $\overline{\text{ST}}$ pin is not strobed within the minimum selected time-out period. (see TD pin) 4. During power-up.
7	13	$\overline{\text{ST}}$	I	ST	Strobe Input Input for Watchdog Timer. WDT period determined by state of TD pin Falling Edge → Resets Watchdog Timer counter (no time-out)
8	15	V_{CC}	—	P	The positive supply (+5V) for the device.
—	1,3,5, 7,10,12,16	NC	—	—	No internal connection.

4.0 OPERATIONAL DESCRIPTION

4.1 Power Monitor

The TC1232 provides the function of warning the processor of a power failure. When V_{CC} is detected as being below the voltage levels defined by the TOL pin, the TC1232's comparator outputs the RST and $\overline{\text{RST}}$ signals to a logic level that warns the system of an out-of-tolerance power supply. The RST and $\overline{\text{RST}}$ signals switch at a threshold value of 4.5V if TOL is tied to V_{CC}, and at a value of 4.75V if TOL is grounded. The RST and $\overline{\text{RST}}$ signals are held active for a minimum of 250 ms to ensure that the power supply voltage has been stabilized.

Figure 4-1 shows the V_{CC} fall time.

Figure 4-2 shows the V_{CC} rise time.

Figure 4-3 shows the time from when the voltage trip point is detected to the Reset output pin going active.

Figure 4-4 shows the time from when the voltage trip point is exited to the Reset output pin going inactive.

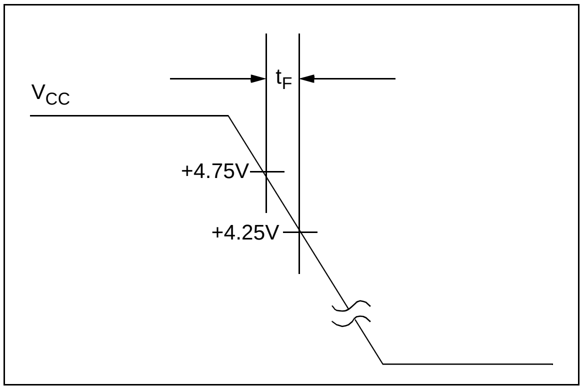


FIGURE 4-1: *Power-Down Slew Rate.*

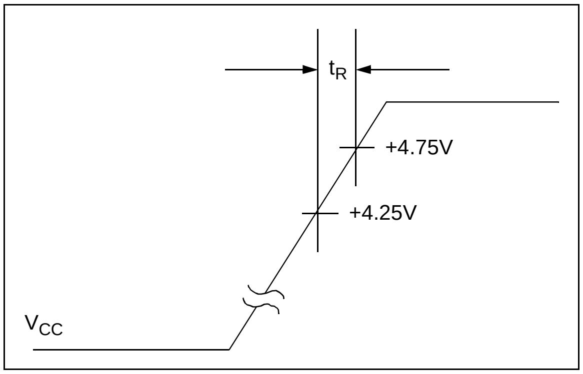


FIGURE 4-2: *Power-up Slew Rate.*

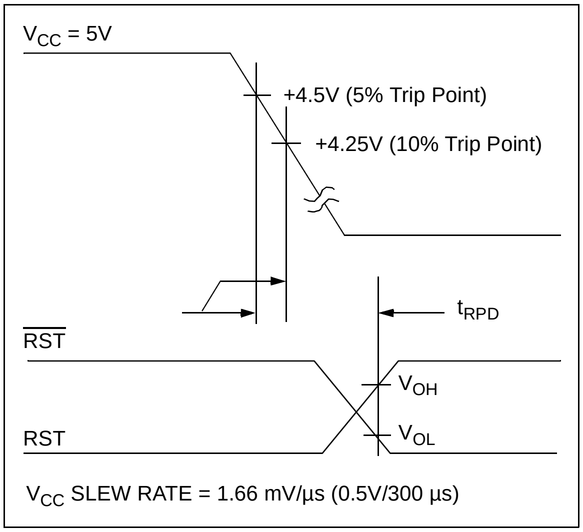


FIGURE 4-3: *V_{CC} Detect Reset Output Delay (Power-Down).*

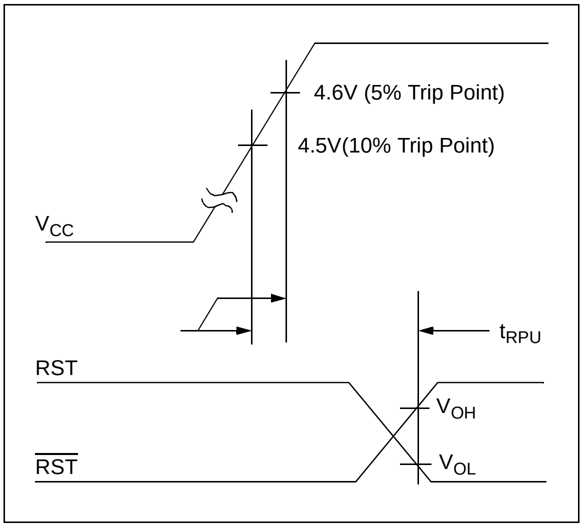


FIGURE 4-4: *V_{CC} Detect Reset Output Delay (Power-Up).*

4.2 Push Button Reset Input

The debounced manual Reset input ($\overline{\text{PB RST}}$) manually forces the Reset outputs into their active states. Figure 4-5 shows a block diagram for using the TC1232 with a push button switch.

Once $\overline{\text{PB RST}}$ has been low for a time t_{PBD} (the push button delay time), the Reset outputs go active. The Reset outputs remain in their active states for a minimum of 250 ms after $\overline{\text{PB RST}}$ rises above V_{IH}. Figure 4-6 shows a waveform for the push button switch input and the Reset pins output.

A mechanical push button or active logic signal can drive the $\overline{\text{PB RST}}$ input. The debounced input ignores input pulses less than 1 ms and recognizes pulses of 20 ms or greater. No external pull-up resistor is required because the $\overline{\text{PB RST}}$ input has an internal pull-up to V_{CC} of approximately 100 µA.

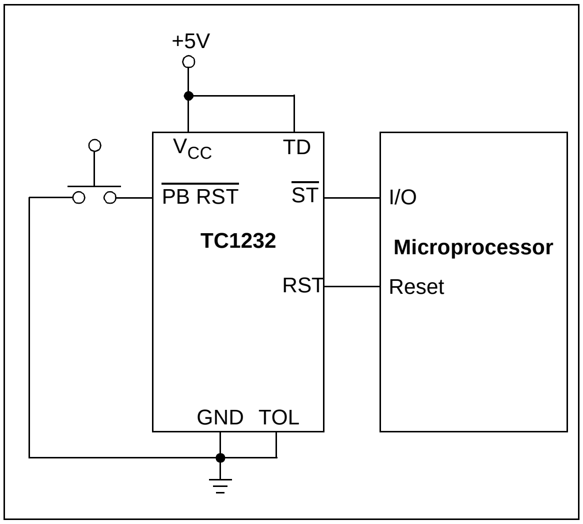
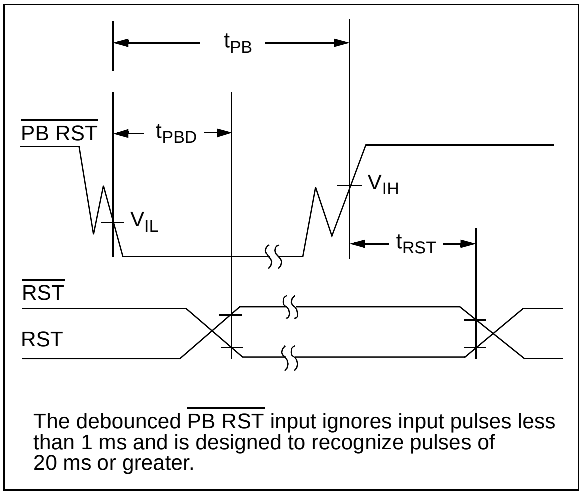


FIGURE 4-5: *Push Button Reset and Watchdog Timer.*



The debounced $\overline{\text{PB RST}}$ input ignores input pulses less than 1 ms and is designed to recognize pulses of 20 ms or greater.

FIGURE 4-6: *Push Button Reset – $\overline{\text{PB RST}}$ Input.*

4.3 Watchdog Timer

When the $\overline{ST}$ input is not stimulated for a preset time period, the Watchdog Timer function forces RST and $\overline{RST}$ signals to the active state. The preset time period is determined by the $\overline{TD}$ inputs to be 150 ms with TD connected to ground, 600 ms with TD floating or 1200 ms with TD connected to V_{CC} (typ.). The Watchdog Timer starts timing-out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the Watchdog Timer is reset and begins to time-out again. If the Watchdog Timer is allowed to time-out, the RST and $\overline{RST}$ signals are driven to the active state for 250 ms, minimum (Figure 4-7).

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that is executed frequently enough so the time between toggles is less than the Watchdog Time-out period. One common technique controls the microprocessor I/O line from two sections of the program. The software might set the I/O line high while operating in the Foreground mode and set it low while in the Background or Interrupt modes. If both modes do not execute correctly, the Watchdog Timer issues Reset pulses.

t_{TD} is the maximum elapsed time between $\overline{ST}$ high-to-low transitions ($\overline{ST}$ is activated by falling edges only), which will keep the Watchdog Timer from forcing the Reset outputs active for a time of t_{RST}. t_{TD} is a function of the voltage at the TD pin, as tabulated below:

TABLE 4-1: WATCHDOG TIMER PERIODS

Condition	t_{TD}		
	Min.	**Typ.**	**Max.**
TD pin = 0V	62.5 ms	150 ms	250 ms
TD pin = Open	250 ms	600 ms	1000 ms
TD pin = V_{CC}	500 ms	1200 ms	2000 ms

Figure 4-7 shows a block diagram for using the TC1232 with a PIC® MCU and the Watchdog input.

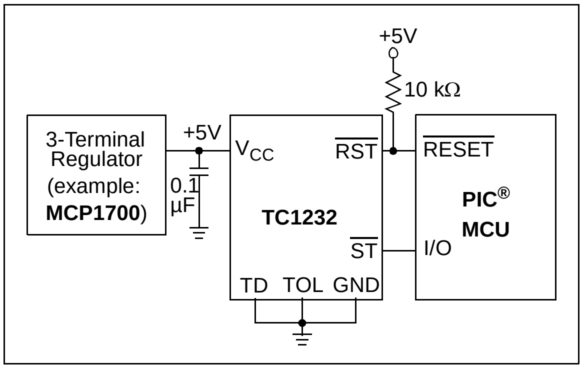


FIGURE 4-7: Watchdog Timer.

Figure 4-8 shows the expected Reset output pin waveforms depending on the period of the $\overline{ST}$ pin falling edge and the state of the TD input pin.

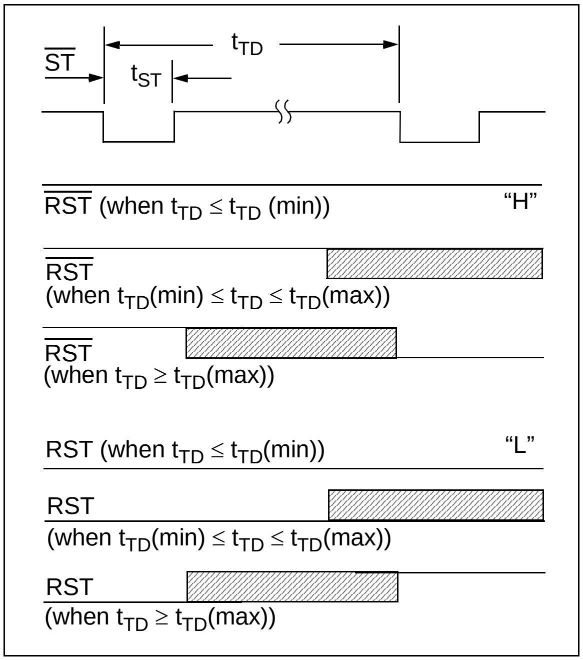


FIGURE 4-8: Strobe Input.

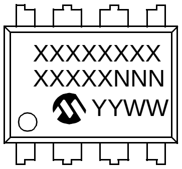
4.4 Supply Monitor Noise Sensitivity

The TC1232 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays) may require a 0.01 µF or 0.1 µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC1232 as possible to keep the capacitor lead length short.

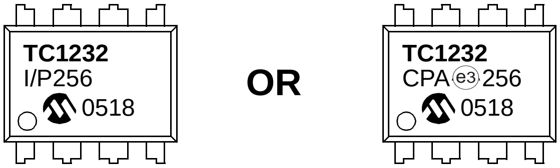
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

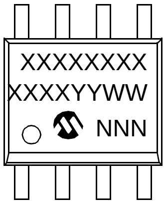
8-Lead PDIP (300 mil)



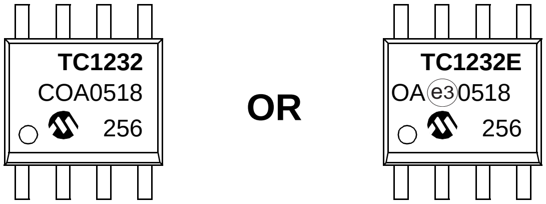
Examples:



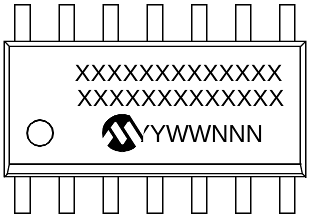
8-Lead SOIC (150 mil)



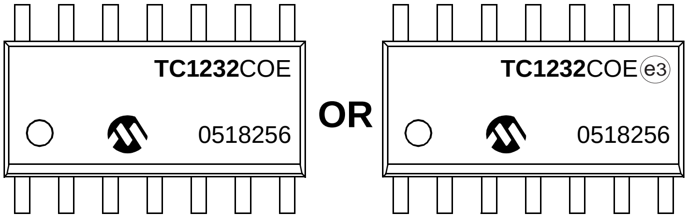
Examples:



16-Lead SOIC (150 mil)



Examples:

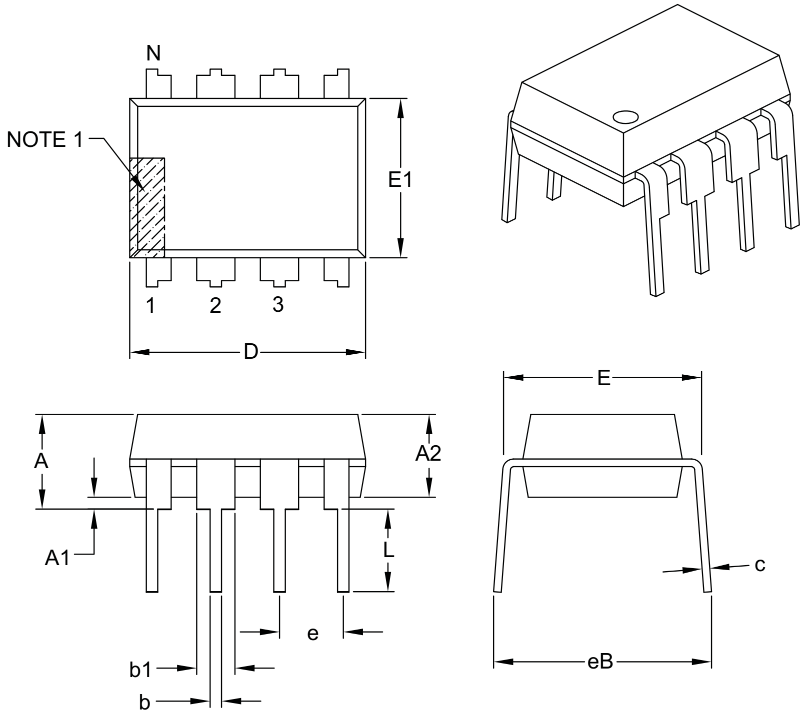


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (PA) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

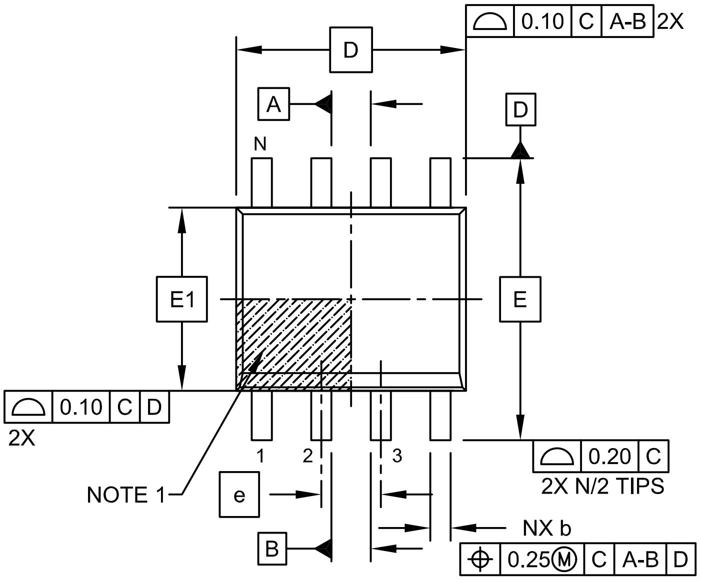
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

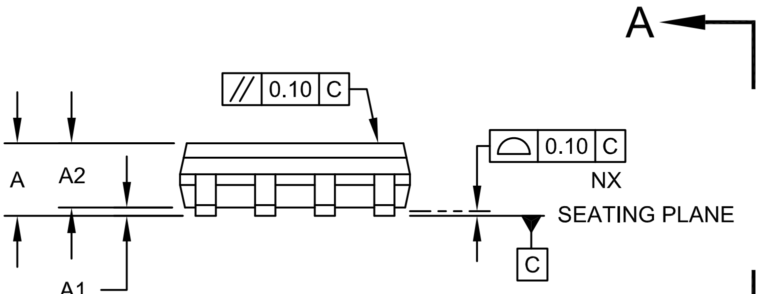
Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

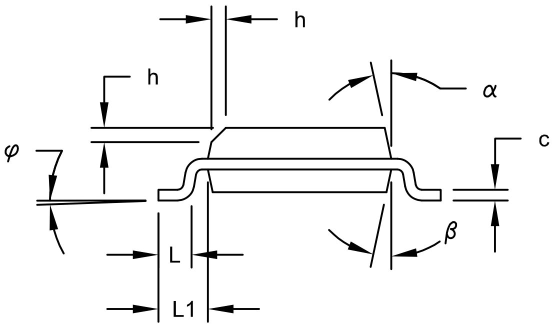
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

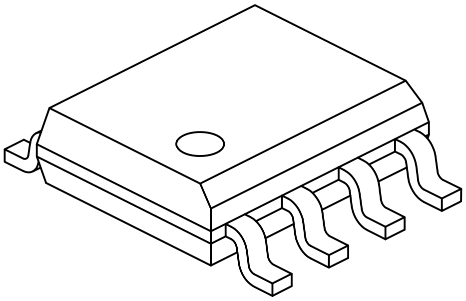


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

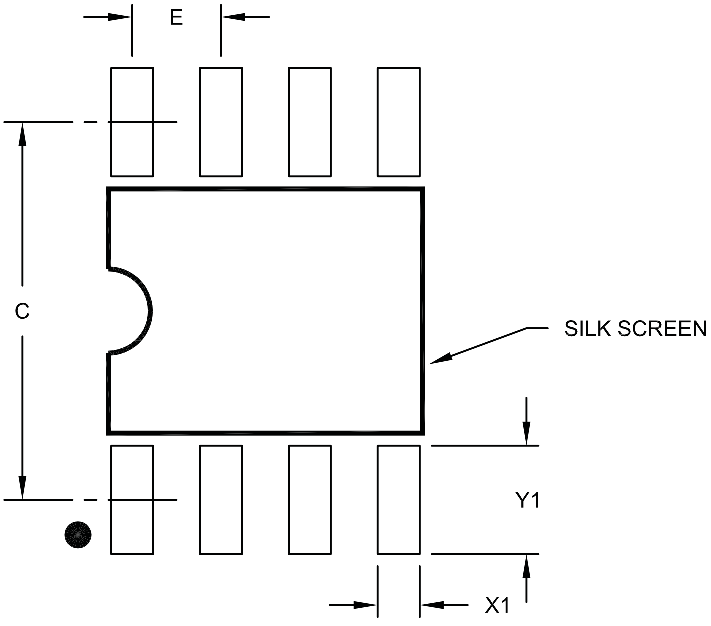
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

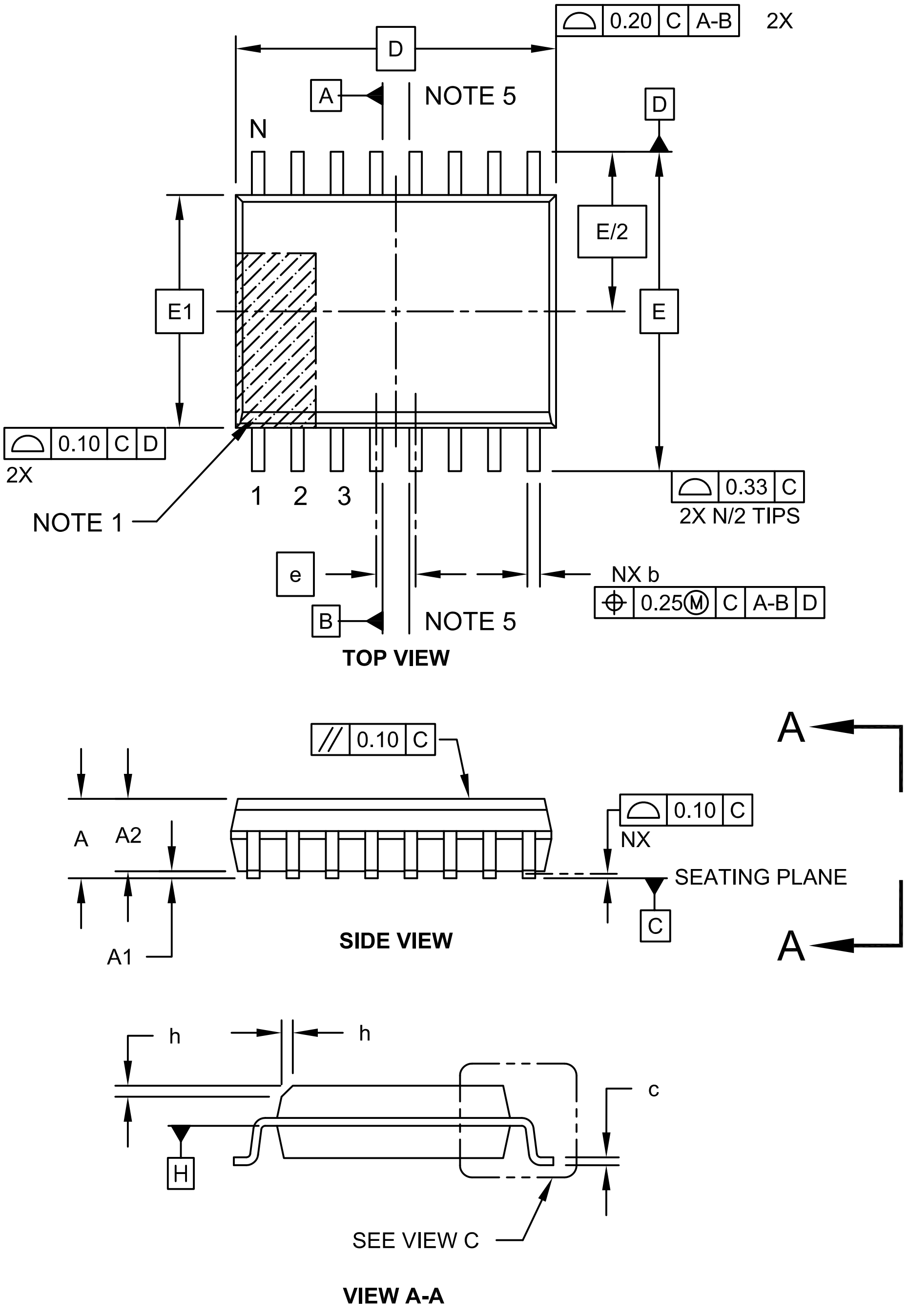
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

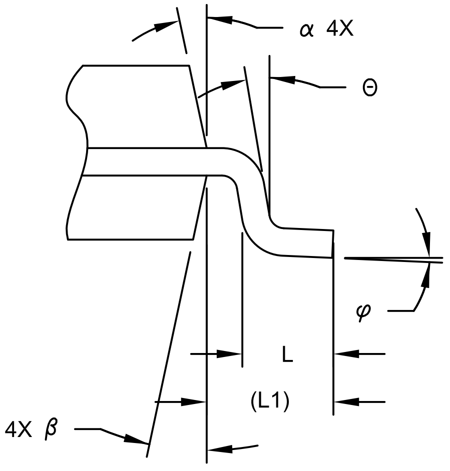
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



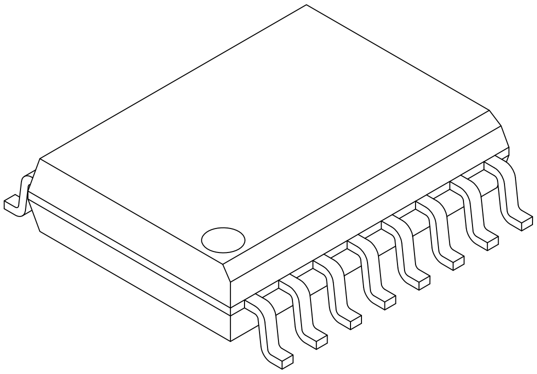
Microchip Technology Drawing C04-102C Sheet 1 of 2

16-Lead Plastic Small Outline (OE) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	16		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	10.30 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

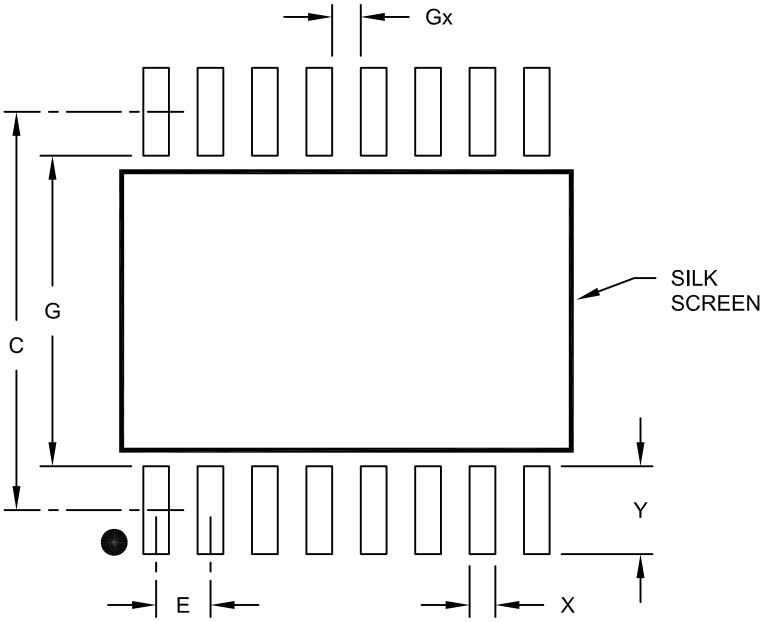
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-102C Sheet 2 of 2

16-Lead Plastic Small Outline (OE) – Wide, 7.50 mm Body [SOIC] Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.30	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.05
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2102A

NOTES:

APPENDIX A: REVISION HISTORY

Revision E (February 2014)

- Removed the “Preliminary” watermark.

Revision D (November 2012)

- Added a note to the package outline drawing.

Revision C (June 2005)

The following is the list of modifications:

1. Since no data is given in **Section 2.0 “Typical Performance Curves”**, “Preliminary” was added to the bottom of this document.
2. Corrected Operating Voltage in the Electrical Specifications.
3. General Data Sheet Enhancements.
4. Added Revision History Appendix Section.

Revision B (March 2003)

- Not logged

Revision A (March 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	**Temperature Range**	**Package**

Device: TC1232: Microprocessor Monitor

Temperature Range:
C = 0°C to +70°C
E = -40°C to +85°C

Package:
PA = Plastic DIP (300 mil Body), 8-lead
OA = Plastic SOIC, (150 mil Body), 8-lead
OA713 = Plastic SOIC, (150 mil Body), 8-lead Tape and Reel
OE = Plastic SOIC (300 mil Body), 16-lead
OE713 = Plastic SOIC (300 mil Body), 16-lead Tape and Reel

Examples:

a) TC1232COA: 0°C to +70°C, 8L-SOIC
b) TC1232COA713: 0°C to +70°C, 8L-SOIC, Tape and Reel
c) TC1232COE: 0°C to +70°C, 16L-SOIC
d) TC1232COE713: 0°C to +70°C, 16L-SOIC Tape and Reel
e) TC1232CPA: 0°C to +70°C, 8L-PDIP
f) TC1232EOA: -40°C to +85°C, 8L-SOIC
g) TC1232EOA713: -40°C to +85°C, 8L-SOIC, Tape and Reel
h) TC1232EOE: -40°C to +85°C, 16L-SOIC
i) TC1232EOE713: -40°C to +85°C, 16L-SOIC, Tape and Reel
j) TC1232EPA: -40°C to +85°C, 8L-PDIP

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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