19-4571; Rev 0; 4/09

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

General Description

The MAX3677 is a low-jitter, precision clock generator optimized for network applications. The device integrates a crystal oscillator and a phase-locked loop (PLL) to generate high-frequency clock outputs for Ethernet applications.

This proprietary PLL design features ultra-low jitter (0.4psRMS) and excellent power-supply noise rejection (PSNR), minimizing design risk for network equipment. The MAX3677 contains seven LVDS outputs and one LVCMOS output. The output frequency is 125MHz.

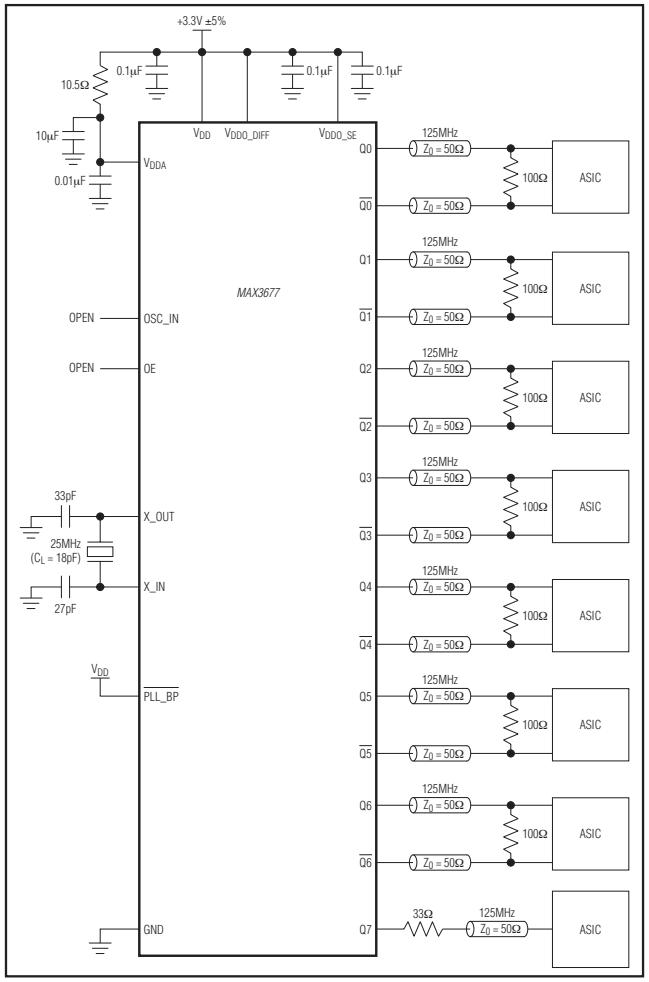
Applications

Ethernet Networking Equipment

Features

- **Crystal Oscillator Interface: 25MHz**
- **OSC_IN Interface**
  - **PLL Enabled: 25MHz**
  - **PLL Disabled: 20MHz to 320MHz**
- **Outputs**
  - **Seven LVDS Outputs at 125MHz**
  - **One LVCMOS Output at 125MHz**
- **Low Phase Jitter**
  - **0.4psRMS (12kHz to 20MHz)**
  - **0.2psRMS (1.875MHz to 20MHz)**
- **Excellent PSNR: -66dBc at 125MHz with 40mVP-P Supply Noise at 100kHz**
- **Operating Temperature Range: 0°C to +70°C**

Typical Operating Circuit

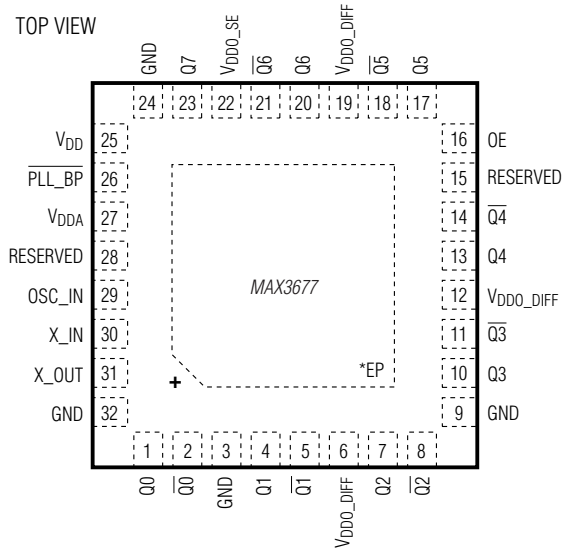


Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3677CTJ+	0°C to +70°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



THIN QFN (5mm × 5mm)

*EXPOSED PAD CONNECTED TO GROUND.

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range at V_{DD}, V_{DDA}, V_{DDO_SE}, V_{DDO_DIFF} ..... -0.3V to +4.0V
Voltage Range at Q0, $\overline{Q0}$, Q1, $\overline{Q1}$, Q2, $\overline{Q2}$, Q3, $\overline{Q3}$, Q4, $\overline{Q4}$, Q5, $\overline{Q5}$, Q6, $\overline{Q6}$, Q7, $\overline{PLL_BP}$, OE, OSC_IN ..... -0.3V to (V_{DD} + 0.3V)
Voltage Range at X_IN ..... -0.3V to +1.2V
Voltage Range at X_OUT ..... -0.3V to (V_{DD} - 0.6V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2759mW
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +160°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT input, no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL_BP}$ = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current (Note 2)	I_{DD}	PLL enabled		190	256	mA
		PLL bypassed		175		
LVDS OUTPUTS (Q0, $\overline{Q0}$, Q1, $\overline{Q1}$, Q2, $\overline{Q2}$, Q3, $\overline{Q3}$, Q4, $\overline{Q4}$, Q5, $\overline{Q5}$, Q6, $\overline{Q6}$)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage Amplitude	$\lvert V_{OD}\rvert$	Figure 1	250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\lvert V_{OD}\rvert$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{OS}\rvert$				25	mV
Differential Output Impedance			80	105	140	Ω
Output Current		Shorted together		5		mA
		Short to ground (Note 3)		8		
Clock Output Rise/Fall Time	t_r, t_f	20% to 80%, R_L = 100Ω	100	200	330	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 4)	46	50	54	
LVCMOS/LVTTL OUTPUT (Q7)						
Output Frequency					160	MHz
Output High Voltage	V_{OH}	I_{OH} = -12mA	2.6		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.4	V
Output Rise/Fall Time	t_r, t_f	20% to 80% at 125MHz (Note 5)	0.15	0.4	0.8	ns
Output Duty-Cycle Distortion		PLL enabled	46	50	54	%
		PLL bypassed (Note 4)	45	50	55	
Output Impedance	R_{OUT}			15		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT input, no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL_BP}$ = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SPECIFICATIONS ($\overline{PLL_BP}$, OE)						
Input-Voltage High	V_{IH}		2.0		V_{DD}	V
Input-Voltage Low	V_{IL}		0		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			80	µA
Input Low Current	I_{IL}	V_{IN} = 0	-80			µA
LVCMOS/LVTTL INPUT SPECIFICATIONS (OSC_IN) (Note 6)						
Input Clock Frequency		PLL enabled		25		MHz
		PLL bypassed	20		320	
Input Amplitude Range		(Note 7)	1.2		3.6	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			80	µA
Input Low Current	I_{IL}	V_{IN} = 0	-80			µA
Reference Clock Duty Cycle			40	50	60	%
Input Capacitance	C_{IN}			1.5		pF
CLOCK OUTPUT AC SPECIFICATIONS						
VCO Center Frequency				625		MHz
Output Frequency with PLL Enabled				125		MHz
Output Frequency with PLL Disabled		LVDS outputs	20		320	MHz
		LVCMOS output	20		160	
Integrated Phase Jitter	RJ_{RMS}	12kHz to 20MHz, $\overline{PLL_BP}$ = high (Note 8)		0.4	1.0	ps_{RMS}
		12kHz to 20MHz, $\overline{PLL_BP}$ = high-Z (Note 9)		0.4		
Power-Supply Noise Rejection (Note 10)	PSNR	LVDS outputs		-66		dBc
		LVCMOS output		-49		
Deterministic Jitter Due to Supply Noise (Note 11)		LVDS outputs		2.5		ps_{P-P}
		LVCMOS output		18		
Nonharmonic and Subharmonic Spurs		(Note 12)		-90		dBc
LVDS Clock Output SSB Phase Noise (Note 13)		f = 100Hz		-115		dBc/Hz
		f = 1kHz		-124		
		f = 10kHz		-126		
		f = 100kHz		-130		
		f = 1MHz		-143		
		f > 10MHz		-149		
LVCMOS Clock Output SSB Phase Noise (Note 13)		f = 100Hz		-113		dBc/Hz
		f = 1kHz		-123		
		f = 10kHz		-126		
		f = 100kHz		-130		
		f = 1MHz		-144		
		f > 10MHz		-151		

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT input, no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL_BP}$ = low.) (Note 1)

Note 1: A series resistor of up to 10.5Ω is allowed between V_{DD} and V_{DDA} for filtering supply noise when system power-supply tolerance is V_{DD} = 3.3V ±5%. See Figure 4.
Note 2: All outputs unloaded.
Note 3: The current when an LVDS output is shorted to ground is the steady-state current after the detection circuitry has settled. It is expected that the LVDS output short to ground condition is short-term only.
Note 4: Measured with OSC_IN input with 50% duty cycle.
Note 5: Measured with a series resistor of 33Ω to a load capacitance of 3.0pF. See Figure 2.
Note 6: The OSC_IN input can be DC- or AC-coupled.
Note 7: Must be within the absolute maximum rating of V_{DD} + 0.3V.
Note 8: Measured with 25MHz crystal (with OSC_IN left open).
Note 9: Measured with 25MHz reference clock applied to OSC_IN.
Note 10: Measured at 125MHz output with 40mV_{P-P} sinusoidal signal on the supply at 100kHz. Measured with a 10.5Ω resistor between V_{DD} and V_{DDA}.
Note 11: Parameter calculated based on PSNR.
Note 12: Measurement includes XTAL oscillator feedthrough, crosstalk, intermodulation spurs, etc.
Note 13: Measured with 25MHz XTAL oscillator.

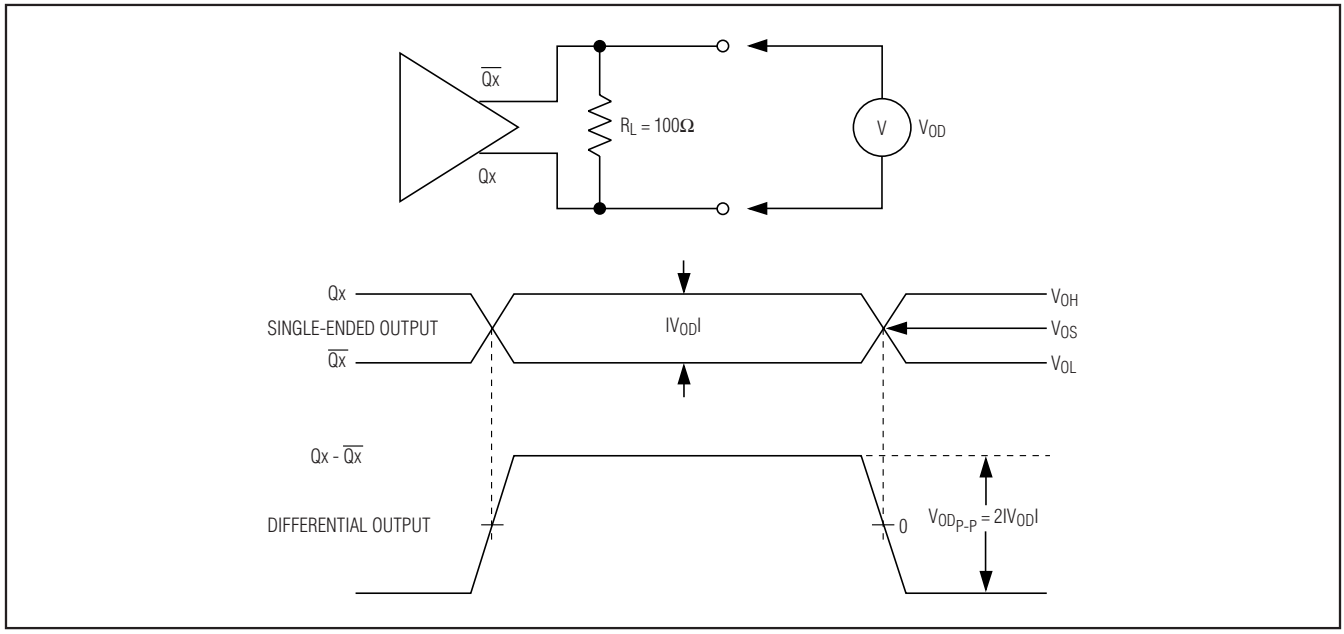


Figure 1. Driver Output Levels

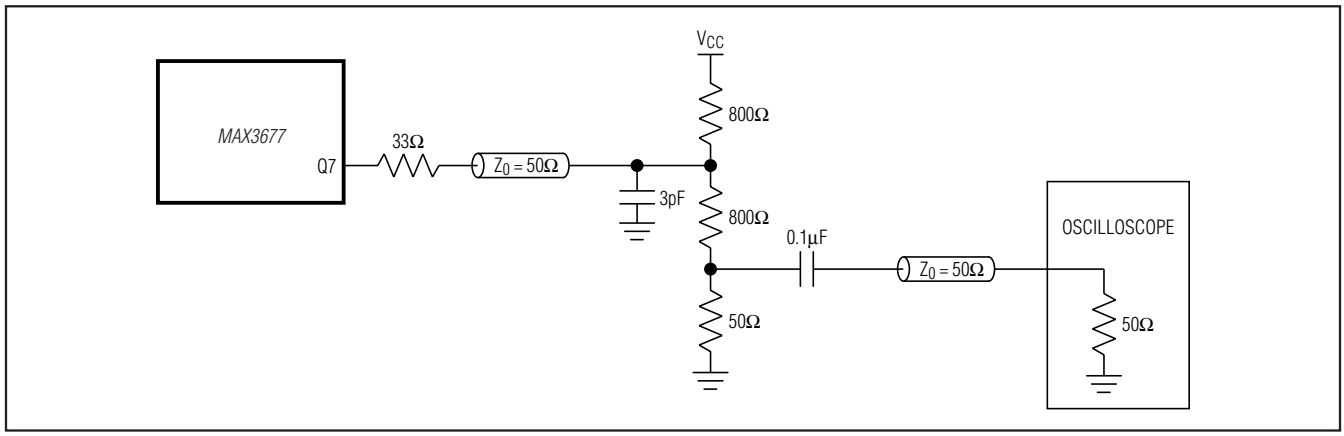


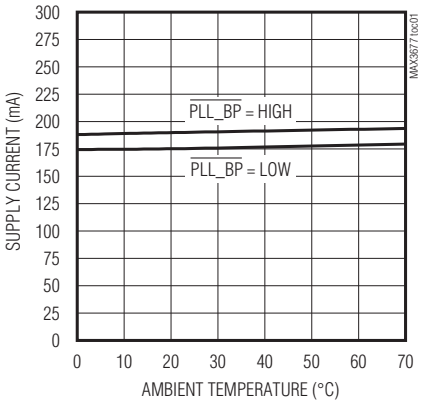
Figure 2. LVCMOS Output Measurement Setup

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

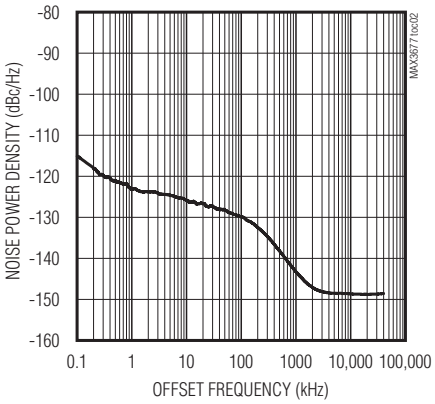
Typical Operating Characteristics

(Typical values are at V_{DD} = +3.3V, T_A = +25°C, crystal frequency = 25MHz.)

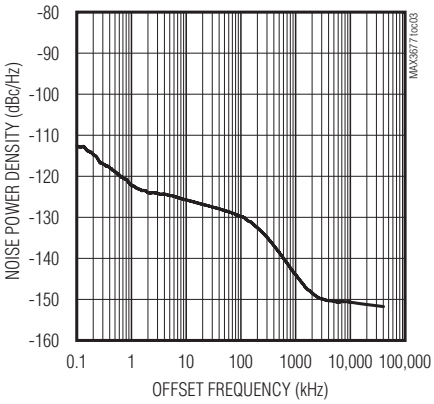
SUPPLY CURRENT vs. TEMPERATURE



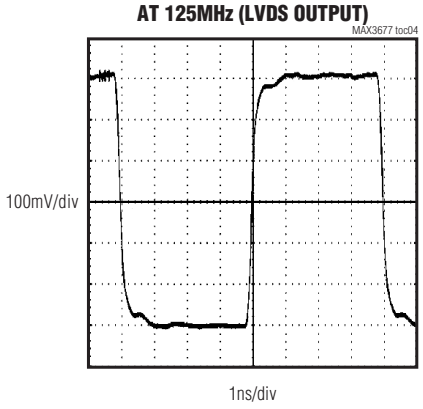
PHASE NOISE AT 125MHz CLOCK FREQUENCY (Q0)



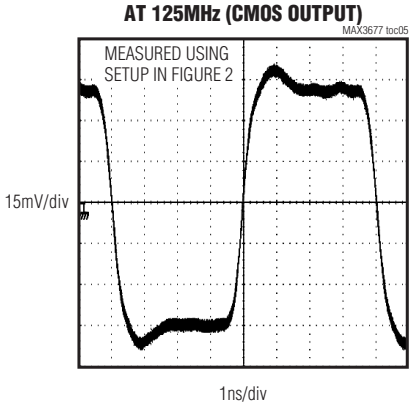
PHASE NOISE AT 125MHz CLOCK FREQUENCY (Q7)



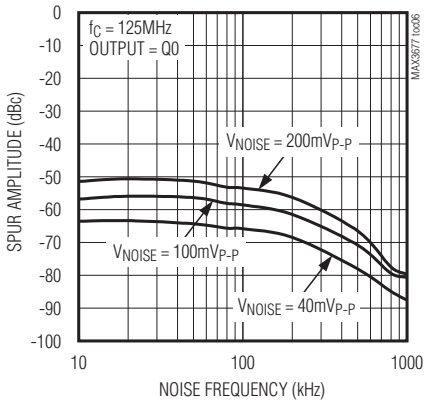
DIFFERENTIAL OUTPUT WAVEFORM AT 125MHz (LVDS OUTPUT)



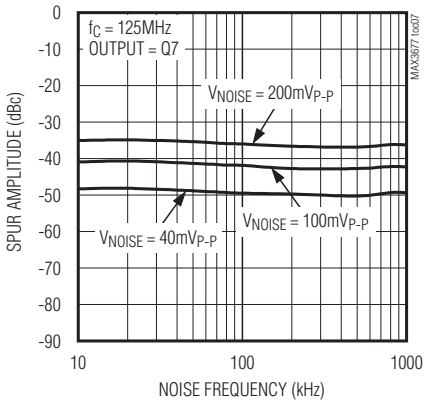
OUTPUT WAVEFORM AT 125MHz (CMOS OUTPUT)



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	Q0	LVDS, Noninverting Clock Output
2	$\overline{Q0}$	LVDS, Inverting Clock Output
3, 9, 24, 32	GND	Supply Ground
4	Q1	LVDS, Noninverting Clock Output
5	$\overline{Q1}$	LVDS, Inverting Clock Output
6, 12, 19	V_{DDO_DIFF}	Power Supply for Q0, Q1, Q2, Q3, Q4, Q5, and Q6 Clock Outputs. Connect to +3.3V.
7	Q2	LVDS, Noninverting Clock Output
8	$\overline{Q2}$	LVDS, Inverting Clock Output
10	Q3	LVDS, Noninverting Clock Output
11	$\overline{Q3}$	LVDS, Inverting Clock Output
13	Q4	LVDS, Noninverting Clock Output
14	$\overline{Q4}$	LVDS, Inverting Clock Output
15, 28	RESERVED	Reserved. Connect to GND.
16	OE	LVCMOS/LVTTL Input. Enable/disable control for the Q4, Q5, and Q6 outputs. The OE pin has an internal 75kΩ pullup resistor. When OE is connected to V_{DD} or left open, Q4, Q5, and Q6 are enabled. When OE is connected to GND, Q4, Q5, and Q6 are disabled to reduce power consumption. When disabled, Q4, Q5, and Q6 are high impedance.
17	Q5	LVDS, Noninverting Clock Output
18	$\overline{Q5}$	LVDS, Inverting Clock Output
20	Q6	LVDS, Noninverting Clock Output
21	$\overline{Q6}$	LVDS, Inverting Clock Output
22	V_{DDO_SE}	Power Supply for Q7 Clock Output. Connect to +3.3V.
23	Q7	LVCMOS Clock Output
25	V_{DD}	Core Power Supply. Connect to +3.3V.
26	$\overline{PLL_BP}$	Three-State LVCMOS/LVTTL Input (Active Low). When connected to logic-high, the PLL locks to the crystal interface (25MHz typical at X_IN and X_OUT). When left open (high-Z), the PLL locks to the OSC_IN input (25MHz typical). When connected to logic-low, the PLL is bypassed and the OSC_IN input is selected. When bypass mode is selected, the VCO/PLL is disabled to save power and eliminate intermodulation spurs.
27	V_{DDA}	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can be connected to V_{DD} through a 10.5Ω resistor as shown in Figure 4.
29	OSC_IN	LVCMOS Input. Self-biased to allow AC- or DC-coupling. When $\overline{PLL_BP}$ is open, the OSC_IN input frequency should be 25MHz. When the PLL is in bypass mode ($\overline{PLL_BP}$ = low), the OSC_IN input frequency can be between 20MHz and 320MHz. When $\overline{PLL_BP}$ is high, OSC_IN should be disconnected.
30	X_IN	Crystal Oscillator Input
31	X_OUT	Crystal Oscillator Output
—	EP	Exposed Pad. Connect to GND for proper electrical and thermal performance.

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

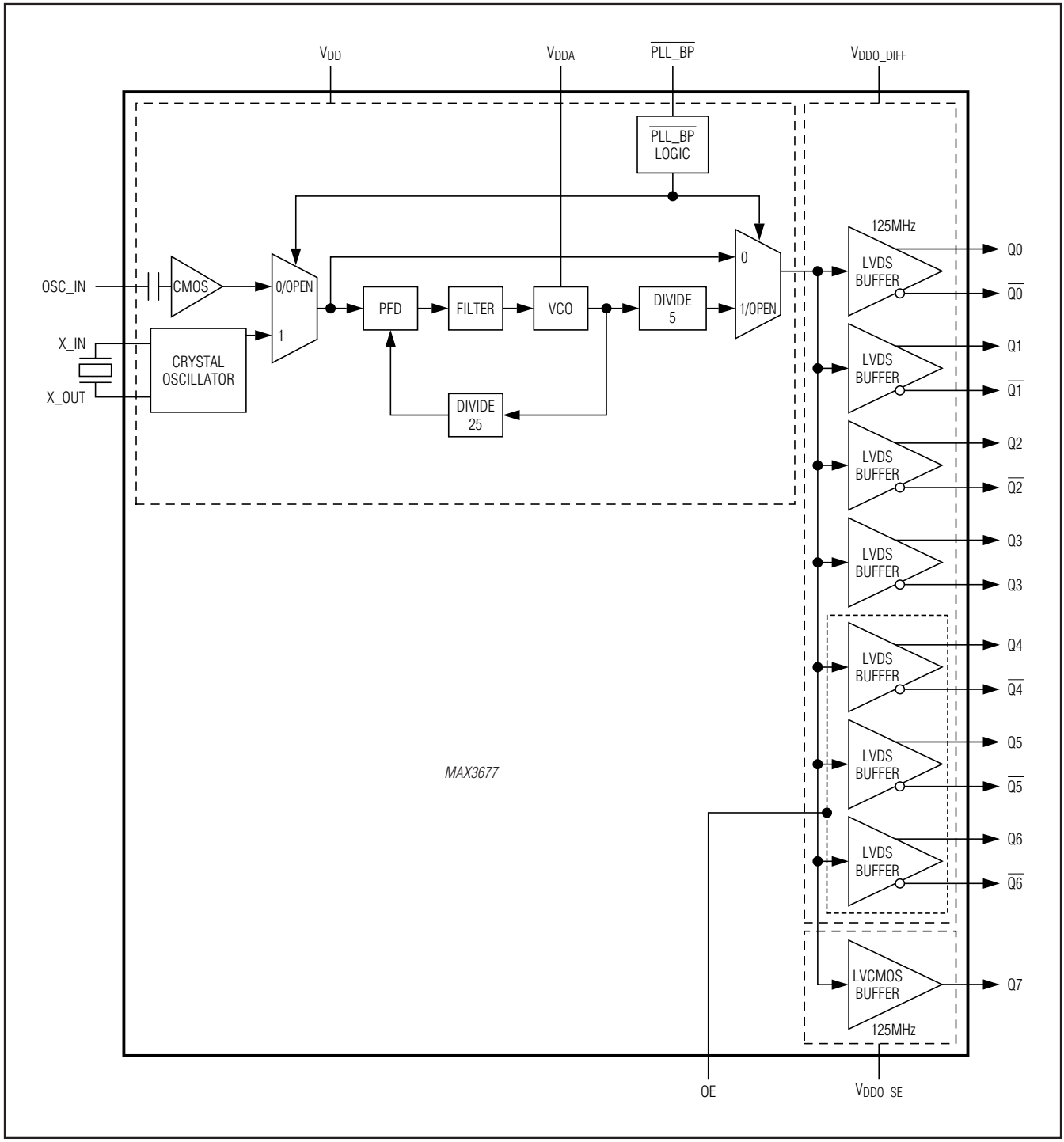


Figure 3. Functional Diagram

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Detailed Description

The MAX3677 is a frequency generator designed to operate at Ethernet frequencies. It consists of an on-chip crystal oscillator, PLL, LVCMOS output buffer, and LVDS output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency 125MHz output clock with excellent jitter performance.

Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X_IN and X_OUT. The crystal frequency is 25MHz. See the *Applications Information* section for more information.

OSC_IN Buffer

The LVCMOS OSC_IN buffer is internally biased to allow AC- or DC-coupling. This input is internally AC-coupled, and is designed to operate at 25MHz when the PLL is enabled ($\overline{PLL_BP}$ is left open). When the PLL is bypassed ($\overline{PLL_BP}$ is set low), the OSC_IN buffer can be operated from 20MHz to 320MHz.

PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency 125MHz clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO) that operates at 625MHz. The PLL bandwidth is tuned to 150kHz typical to optimize both phase noise and power-supply noise rejection (PSNR). The VCO output is connected to the PFD input through a feedback divider that divides the VCO frequency by 25 to lock onto the 25MHz reference clock or oscillator. To minimize the jitter induced by power-supply noise, the VCO supply (V_{DDA}) is isolated from the core logic and output buffer supplies.

LVDS Drivers

The high-frequency outputs—Q0, Q1, Q2, Q3, Q4, Q5, and Q6—are differential LVDS buffers designed to drive 100Ω.

LVCMOS Driver

LVCMOS output Q7 is provided on the MAX3677. It is designed to drive single-ended high-impedance loads. The output specifications are only valid up to 160MHz.

Applications Information

Power-Supply Filtering

The MAX3677 is a mixed analog/digital IC. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation, in addition to excellent on-chip power-supply rejection, this part provides a separate power-supply pin, V_{DDA}, for the VCO circuitry. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. Figure 4 illustrates the recommended power-supply filter network for V_{DDA}. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins and placed as close as possible to the pins for best performance.

Crystal Input Layout and Frequency Stability

The MAX3677 features an integrated on-chip crystal oscillator to minimize system implementation cost. The integrated crystal oscillator is a Pierce-type that uses the crystal in its parallel resonance mode. It is recommended to use a 25MHz crystal with a load specification of C_L = 18pF. See Table 1 for the recommended crystal specifications.

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X_IN and X_OUT pins to minimize the board parasitic capacitance and prevent active signals from coupling into the oscillator.

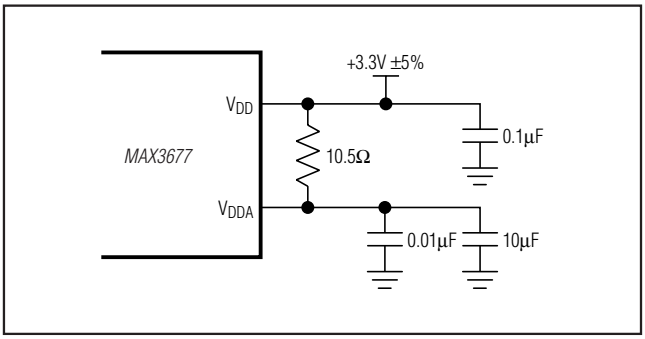


Figure 4. Analog Supply Filtering

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Table 1. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f_{OSC}		25		MHz
Shunt Capacitance	C_O			7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S			50	Ω
Maximum Crystal Drive Level				300	µW

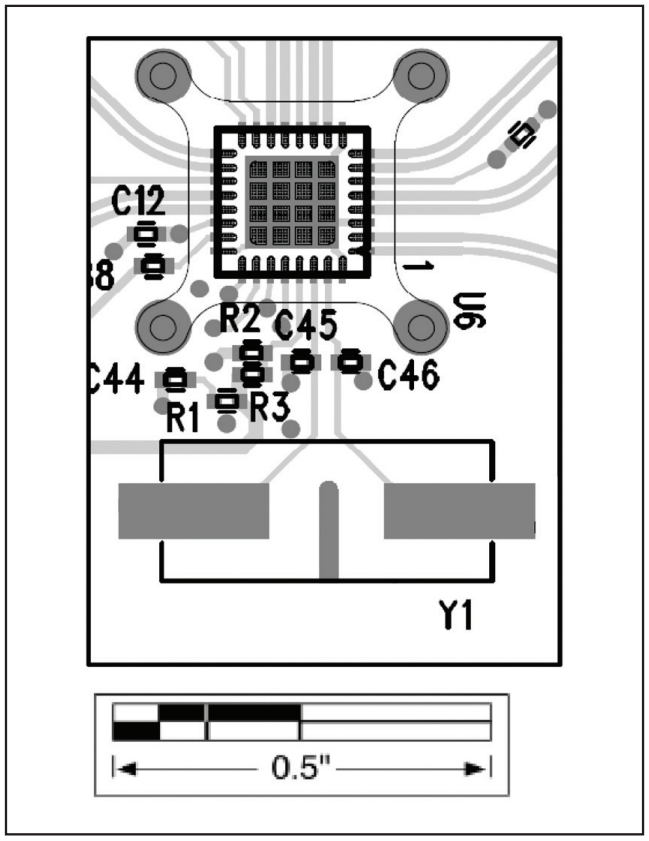


Figure 5. Crystal Layout

The layout shown in Figure 5 gives approximately 2pF of trace plus footprint capacitance per side of the crystal (Y1). The dielectric material is FR4, and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C45 = 27pF and C46 = 33pF, the measured output frequency accuracy is -1ppm at +25°C ambient temperature.

Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 1 for recommended crystal specifications. See Figure 6 for external capacitance connection.

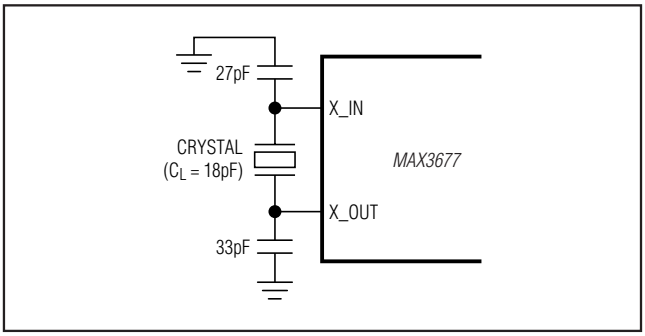


Figure 6. Crystal, Capacitors Connection

Interface Models

Figures 7, 8, and 9 show examples of interface models.

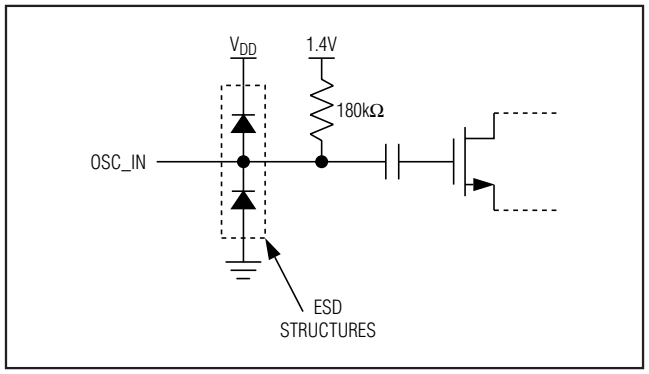


Figure 7. Simplified OSC_IN Pin Circuit Schematic

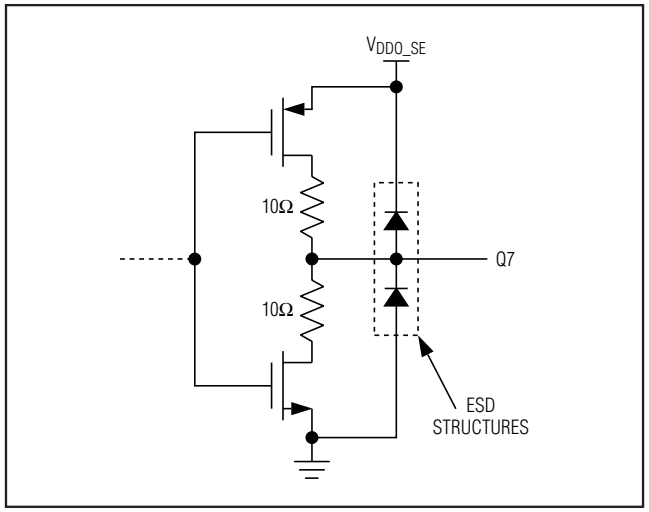


Figure 8. Simplified LVCMOS Output Circuit Schematic

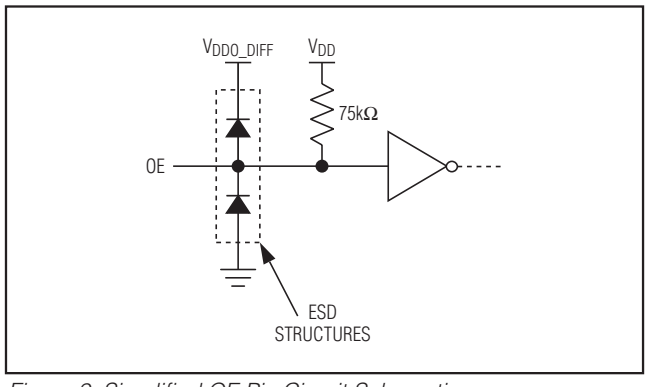


Figure 9. Simplified OE Pin Circuit Schematic

Layout Considerations

The inputs and outputs are the most critical paths for the MAX3677 and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3677:

- An uninterrupted ground plane should be positioned beneath the clock outputs. The ground plane under the crystal should be removed to minimize capacitance.
- Ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3677 and the receive devices.
- Supply decoupling capacitors should be placed close to the supply pins, preferably on the same layer as the MAX3677.
- Take care to isolate crystal input traces from the MAX3677 outputs.
- The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X_IN and X_OUT pins.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance into and out of the part.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3677 evaluation kit for more information.

Exposed-Pad Package

The exposed pad on the 32-pin TQFN package provides a very low inductance path for return current traveling to the PCB ground plane. The pad is thermal and electrical ground on the MAX3677 and must be soldered to the circuit board ground for proper electrical performance.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **http://www.microsemi.com**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
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