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FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16503-5E

32-bit Microcontroller

CMOS

FR60 MB91350A Series

MB91F355A/F353A/F356B/F357B/355A/354A/ MB91353A/352A/351A/V350A

■ DESCRIPTION

The FR family* is a series of standard single-chip microcontrollers that feature a variety of built-in I/O resources and bus control functions, and that employ a high-performance 32-bit RISC CPU for embedded control applications that demand powerful and fast CPU processing capabilities.

This product is one of the FR60 family based on the FR30/40 family CPU with enhanced bus access. The FR60 family is a line of single-chip oriented microcontrollers that incorporate a wealth of peripheral resources.

The FR60 family is optimized for embedded control applications that require high CPU processing power, such as DVD players, navigation equipment, high performance fax machines, and printer controllers.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

1. FR CPU

- 32-bit RISC, load/store architecture with a five-stage pipeline
- Maximum operating frequency : 50 MHz (using the PLL at an oscillation frequency of 12.5 MHz)
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instruction set optimized for embedded applications : Memory-to-memory transfer, bit manipulation, barrel shift etc.
- Instructions adapted for high-level languages : Function entry/exit instructions, multiple-register load/store instructions
- Register interlock functions : Facilitate coding in assemblers

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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2008.11

- On-chip multiplier supported at the instruction level.
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instructions compatible with the FR family

2. Bus interface

- Maximum operating frequency : 25 MHz
- 24-bit address full output (16 Mbyte address space) capability
  (21-bit address full output (2 Mbyte address space) capability : MB91F353A/353A/352A/351A)
- 8,16-bit data output
- Built-in prefetch buffer
- Unused data and address pins can be used as general I/O ports.
- Able to output chip-select for 4 completely independent areas that can be configured in units of 64 Kbytes
- Support for various memory interfaces :
  SRAM, ROM/Flash
  page mode Flash ROM, page mode ROM interface
- Basic bus cycle : 2 cycles
- Programmable automatic wait cycle generator capable of inserting wait cycles for each area
- RDY input for external wait cycles
- DMA support of fly-by transfer capable of wait control for independent I/O
  (The MB91F353A/353A/352A/351A does not support fly-by transfer.)

3. Built-in memory

D-bus memory	MB91V350A	MB91F353A MB91F355A MB91F357B	MB91F356B	MB91353A MB91355A	MB91352A MB91354A	MB91351A
ROM	No	512 Kbytes	256 Kbytes	512 Kbytes	384 Kbytes	384 Kbytes
RAM (Stack)	16 Kbytes	16 Kbytes	16 Kbytes	16 Kbytes	8 Kbytes	16 Kbytes
RAM (Execute instruction)	16 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes

4. DMAC (DMA Controller)

- Capable of simultaneous operation of up to 5 channels (external → external : 3 channels)
- 3 transfer sources (external pin, internal peripheral or software) :
  Activation sources are software-selectable (transfer can be activated by UART0/1/2).
- Addressing using 32-bit full addressing mode (increment, decrement, fixed)
- Transfer modes (demand transfer, burst transfer, step transfer, block transfer)
- Fly-by transfer support (between external I/O and memory)
- Selectable transfer data size : 8, 16, or 32-bit
- Multi-byte transfer capability (selected by software)
- DMAC descriptor in IO areas (200_H to 240_H, 1000_H to 1024_H)
  (The MB91F353A/353A/352A/351A does not have an external interface.)
  External pin transfer is not supported. Demand transfer and fly-by transfer cannot be used.

5. Bit search module (for REALOS)

- Search a single word starting from the MSB for the position of the first bit changed from 1 to 0.

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6. Various timers

- 4 channels of 16-bit reload timer (including 1 channel for REALOS) :
  Internal clock frequency divider selectable from 2/8/32 (division by 64/128 selectable only for ch.3)
- 16-bit free-run timer : 1 channel
  Output compare : 8 channels (MB91F353A/353A/352A/351A : 2 channels)
  Input capture : 4 channels
- 16-bit PPG timer : 6 channels (MB91F353A/353A/352A/351A : 3 channels)

7. UART

- UART full duplex double buffer : 5 channels (MB91F353A/353A/352A/351A : 4 channels)
- Selectable parity on/off
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
- Built-in dedicated baud rate timer
- External clock can be used as transfer clock
- Assorted error detection functions (for parity, frame, and overrun errors)
- Support for 115 kbps

8. SIO

- 8-bit data serial transfer : 3 channels (MB91F353A/353A/352A/351A : 2 channels)
- Shift clock selectable from among three internal and one external
- Shift direction selectable (transfer from LSB or MSB)

9. Interrupt controller

- Total number of external interrupts : 17 (MB91F353A/353A/352A/351A : 9)
  (One non-maskable interrupt pin and 16/8 ordinary interrupt pins that can be used for wakeup in stop mode.)
- Interrupts from internal peripherals
- Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt

10. D/A converter

- 8-bit resolution : 3 channels (MB91F353A/353A/352A/351A : 2 channels)

11. A/D converter

- 10-bit resolution : 12 channels (MB91F353A/353A/352A/351A : 8 channels)
- Serial/parallel conversion type Conversion time : 1.48 µs
- Conversion mode (one shot conversion mode, continuous conversion mode)
- Activation source (software, external trigger, peripheral interrupt)

12. Other interval timer/counter

- 8/16-bit up/down counter
  The MB91F353A/353A/352A/351A supports only an 8-bit up/down counter.
- 16-bit timer (U-TIMER) : 5 channels (MB91F353A/353A/352A/351A : 4 channels)
- Watch dog timer

13. I^2C bus interface (supports 400 kbps)

- 1 channel master/slave transmission and reception
- Arbitration and clock synchronization functions

14. I/O ports

- 3 V I/O ports
  (5 V input is supported for those ports that are also used for external interrupts (16 ports, MB91F353A/353A/352A/351A : 8 ports).
- Up to 126 ports (MB91F353A/353A/352A/351A : Up to 84 ports)

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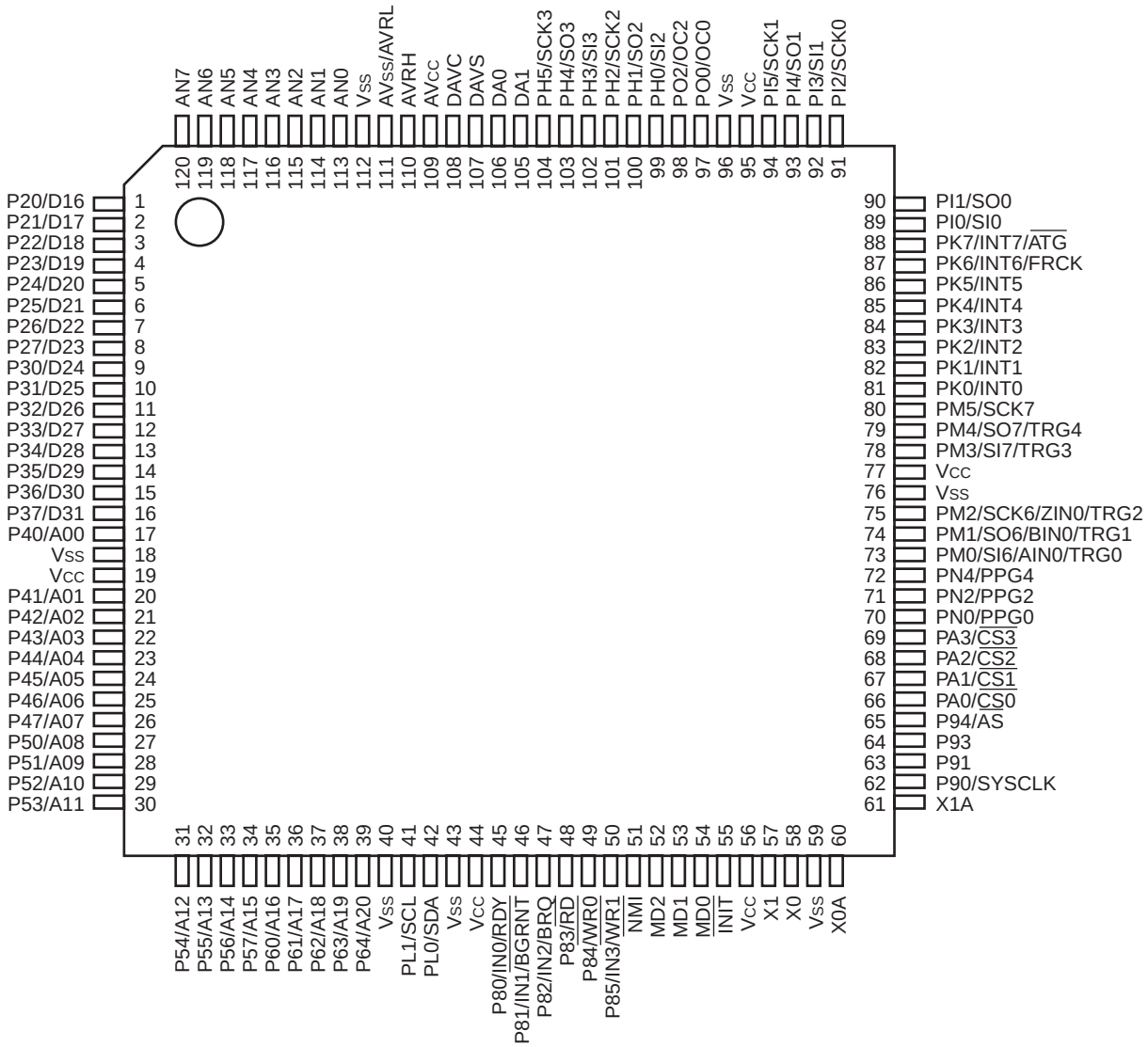
15. Other features

- Internal oscillator circuit as clock source, and PLL multiplication can be selected
- $\overline{\text{INIT}}$ pin provided as a reset pin (the oscillation stabilization wait time when the $\overline{\text{INIT}}$ pin is reset is clock cycle $\times$ 2.)
- Watch dog timer reset and software reset are also provided.
- Support for stop and sleep modes for low power consumption, capable of saving power by operating the CPU at 32 kHz.
- Gear function
- Built-in time base timer
- Package : MB91F355A/F356B/355A/354A/F357B : LQFP-176 (lead pitch 0.50 mm)
  MB91F353A/353A/352A/351A : LQFP-120 (lead pitch 0.50 mm)
- CMOS technology(0.35 µm)
- Power supply voltage : 3.3 V $\pm$ 0.3 V
  2.7 V to 3.6 V (MB91F356B/F357B only)

■ PIN ASSIGNMENTS

• MB91F353A/353A/352A/351A

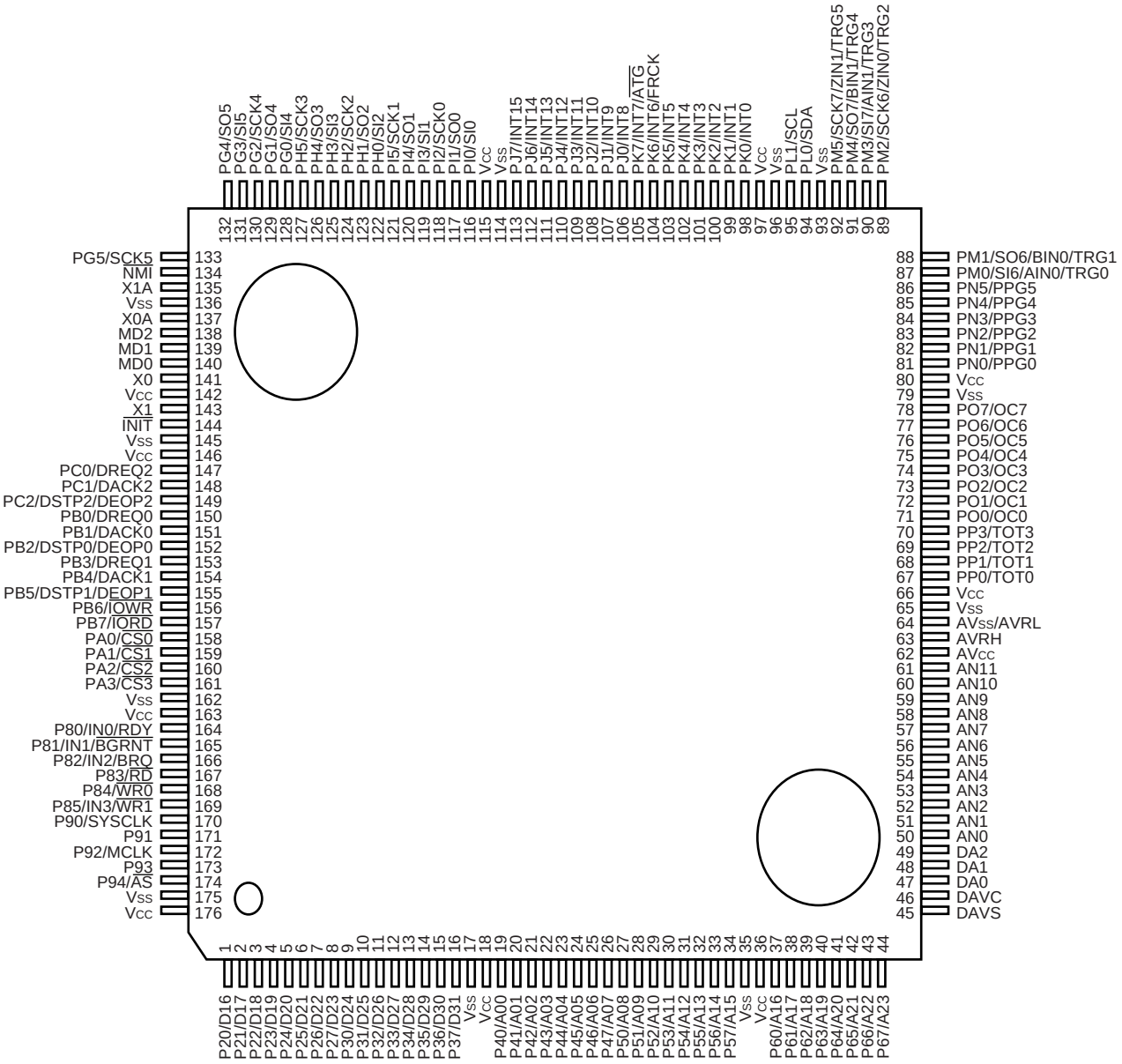
(TOP VIEW)



(FPT-120P-M21)

- MB91F355A/F356B/F357B/355A/354A

(TOP VIEW)



(FPT-176P-M02)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
1 to 8	1 to 8	D16 to D23	C	Bit 16 to bit 23 of the external data bus. Valid only in external bus mode.
		P20 to P27		Can be used as ports while in external bus 8-bit mode.
9 to 16	9 to 16	D24 to D31	C	Bit 24 to bit 31 of the external data bus. Valid only in external bus mode.
		P30 to P37		Can be used as ports while in single-chip mode.
19 to 26	17, 20 to 26	A00 to A07	C	Bit 0 to bit 7 of the external address bus. Valid only in external bus mode.
		P40 to P47		Can be used as ports while in single-chip mode.
27 to 34	27 to 34	A08 to A15	C	Bit 8 to bit 15 of the external address bus. Valid only in external bus mode.
		P50 to P57		Can be used as ports while in single-chip mode.
37 to 41	35 to 39	A16 to A20	C	Bit 16 to bit 20 of the external address bus. Valid only in external bus mode.
		P60 to P64		Can be used as ports while in single-chip mode or when the external address bus is not used.
42 to 44	—	A21 to A23	C	Bit 21 to bit 23 of the external address bus. Valid only in external bus mode.
		P65 to P67		Can be used as ports while in single-chip mode or when the external address bus is not used.
47, 48	106,105	DA0, DA1	—	D/A converter output pins
49	—	DA2	—	D/A converter output pin
50 to 57	113 to 120	AN0 to AN7	G	Analog input pins
58 to 61	—	AN8 to AN11	G	Analog input pins
67 to 70	—	TOT0 to TOT3	D	Reload timer output ports. This pin is valid when timer output is enabled.
		PP0 to PP3		General-purpose I/O ports. This pin is valid when the timer output function is disabled.
71	97	OC0	D	Output compare output pin
		PO0		General-purpose I/O port. This pin can be used as a port when the output compare output is not used.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
72	—	OC1	D	Output compare output pin
		PO1		General-purpose I/O port. This pin can be used as a port when the output compare output is not used.
73	98	OC2	D	Output compare output pin
		PO2		General-purpose I/O port. This pin can be used as a port when the output compare output is not used.
74 to 78	—	OC3 to OC7	D	Output compare output pins
		PO3 to PO7		General-purpose I/O ports. These pins can be used as ports when the output compare outputs are not used.
81	70	PPG0	D	PPG timer output pin
		PN0		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.
82	—	PPG1	D	PPG timer output pin
		PN1		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.
83	71	PPG2	D	PPG timer output pin
		PN2		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.
84	—	PPG3	D	PPG timer output pin
		PN3		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.
85	72	PPG4	D	PPG timer output pin
		PN4		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.
86	—	PPG5	D	PPG timer output pin
		PN5		General-purpose I/O port. This pin can be used as a port when the PPG timer output is not used.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
87	73	SI6	D	Data input for serial I/O6. Since this input is always used when serial I/O6 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		AIN0		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG0		External trigger input for PPG timer 0. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM0		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.
88	74	SO6	D	Data output from serial I/O6. This function is valid when data output from serial I/O6 is enabled.
		BIN0		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG1		External trigger input for PPG timer 1. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM1		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.
89	75	SCK6	D	Clock I/O for serial I/O 6. This function is valid when clock output from serial I/O6 is enabled or when an external shift clock input is used.
		ZIN0		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG2		External trigger input for PPG timer 2. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM2		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
90	78	SI7	D	Data input for serial I/O7. Since this input is always used when serial I/O7 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		AIN1*4		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG3		External trigger input for PPG timer 3. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM3		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.
91	79	S07	D	Data output from serial I/O7. This function is valid when data output from serial I/O7 is enabled.
		BIN1*4		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG4		External trigger input for PPG timer 4. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM4		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.
92	80	SCK7	D	Clock I/O for serial I/O7. This function is valid when clock output from serial I/O7 is enabled or when an external shift clock input is used.
		ZIN1*4		Input for the up/down counter. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		TRG5*4		External trigger input for PPG timer 5. Since this input is always used when input is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		PM5		General-purpose I/O port. This pin can be used as a port when serial I/O, up/down counter, and PPG timer output are not used.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
94	42	SDA	F	DATA I/O pin for the I²C bus. This pin is valid when standard mode I²C operation is enabled. Output using the port must be stopped beforehand unless this operation is intended (open drain output).
		PL0		General-purpose I/O port. This pin can be used as a port when I²C operation is disabled (open drain output).
95	41	SCL	F	Clock I/O pin for the I²C bus. This pin is valid when standard mode I²C operation is enabled. Output using the port must be stopped beforehand unless this operation is intended (open drain output).
		PL1		General-purpose I/O port. This pin can be used as a port when I²C operation is disabled (open drain output).
98 to 103	81 to 86	INT0 to INT5	E	External interrupt inputs. Since these inputs are always used when the corresponding external interrupts are enabled, output using the ports must be stopped beforehand unless this operation is the intended operation.
		PK0 to PK5		General-purpose I/O ports
104	87	INT6	E	External interrupt input. Since this input is always used when the corresponding external interrupt is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		FRCK		External clock input pin for the free-run timer. Since this input is always used when it is selected as the external clock input for the free-run timer, output using the port must be stopped beforehand unless this operation is the intended operation.
		PK6		General-purpose I/O port
105	88	INT7	E	External interrupt input. Since this input is always used when the corresponding external interrupt is enabled, output using the port must be stopped beforehand unless this operation is the intended operation.
		$\overline{\text{ATG}}$		External trigger for the A/D converter. Since this input is always used when it is selected as the A/D activation source, output using the port must be stopped beforehand unless this operation is the intended operation.
		PK7		General-purpose I/O port

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
106 to 113	—	INT8 to INT15	E	External interrupt inputs. Since these inputs are always used when the corresponding external interrupts are enabled, output using the ports must be stopped beforehand unless this operation is the intended operation.
		PJ0 to PJ7		General-purpose I/O ports
116	89	SI0	D	Data input for UART0. Since this input is always used when UART0 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PI0		General-purpose I/O port
117	90	SO0	D	Data output from UART0. This function is valid when UART0 data output is enabled.
		PI1		General-purpose I/O port. This function is valid when UART0 data output is disabled.
118	91	SCK0	D	Clock I/O for UART0. This function is valid when UART0 clock output is enabled or when an external clock input is used.
		PI2		General-purpose I/O port. This function is valid when UART0 clock output is disabled or when an external clock input is not used.
119	92	SI1	D	Data input for UART1. Since this input is always used when UART1 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PI3		General-purpose I/O port
120	93	SO1	D	Data output from UART1. This function is valid when UART1 data output is enabled.
		PI4		General-purpose I/O port. This function is valid when UART1 data output is disabled.
121	94	SCK1	D	Clock I/O for UART1. This function is valid when UART1 clock output is enabled or when an external clock input is used.
		PI5		General-purpose I/O port. This function is valid when UART1 clock output is disabled or when an external clock input is not used.
122	99	SI2	D	Data input for UART2. Since this input is always used when UART2 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PH0		General-purpose I/O port

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
123	100	SO2	D	Data output from UART2. This function is valid when UART2 data output is enabled.
		PH1		General-purpose I/O port. This function is valid when UART2 data output is disabled or when an external shift clock input is used.
124	101	SCK2	D	Clock I/O for UART2. This function is valid when UART2 clock output is enabled or when an external clock input is used.
		PH2		General-purpose I/O port. This function is valid when UART2 clock output is disabled or when an external clock input is not used.
125	102	SI3	D	Data input for UART3. Since this input is always used when UART3 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PH3		General-purpose I/O port
126	103	SO3	D	Data output from UART3. This function is valid when UART3 data output is enabled.
		PH4		General-purpose I/O port. This function is valid when UART3 data output is disabled.
127	104	SCK3	D	Clock I/O for UART3. This function is valid when UART3 clock output is enabled or when an external clock input is used.
		PH5		General-purpose I/O port. This function is valid when UART3 clock output is disabled or when an external clock input is not used.
128	—	SI4	D	Data input for UART4. Since this input is always used when UART4 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PG0		General-purpose I/O port
129	—	SO4	D	Data output from UART4. This function is valid when serial I/O4 data output is enabled.
		PG1		General-purpose I/O port. This function is valid when serial I/O4 data output is disabled.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
130	—	SCK4	D	Clock I/O for UART4. This function is valid when serial I/O4 clock output is enabled or when an external clock input is used.
		PG2		General-purpose I/O port. This function is valid when serial I/O4 clock output is disabled or when an external clock input is not used.
131	—	SI5	D	Data input for serial I/O5. Since this input is always used when serial I/O5 input is operating, output using the port must be stopped beforehand unless this operation is the intended operation.
		PG3		General-purpose I/O port
132	—	SO5	D	Data output from serial I/O5. This function is valid when serial I/O5 data output is enabled.
		PG4		General-purpose I/O port. This function is valid when serial I/O5 data output is disabled.
133	—	SCK5	D	Clock I/O for serial I/O5. This function is valid when serial I/O5 clock output is enabled or when an external shift clock input is used.
		PG5		General-purpose I/O port. This function is valid when serial I/O5 clock output is disabled or when an external clock input is not used.
134	51	$\overline{\text{NMI}}$	H	NMI (non-maskable interrupt) input
135	61	X1A	B	Clock (oscillation) output (sub clock)
137	60	X0A	B	Clock (oscillation) input (sub clock)
138 to 140	52 to 54	MD2 to MD0	H J	Mode pins 2 to 0. These pins set the basic operating mode. Connect the pins to V_{CC} or V_{SS}. Input circuit type : The production version (MASK ROM version) is the "H" type. The Flash ROM version is the "J" type.
141	58	X0	A	Clock (oscillation) input (main clock)
143	57	X1	A	Clock (oscillation) output (main clock)
144	55	$\overline{\text{INIT}}$	I	External reset input
147	—	DREQ2	C	DMA external transfer request input. Since this input is always used when it is selected as the DMA activation source, output using the port must be stopped beforehand unless this operation is the intended operation.
		PC0		General-purpose I/O port

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
148	—	DACK2	C	DMA external transfer request acceptance output. This function is valid when DMA transfer request acceptance output is enabled.
		PC1		General-purpose I/O port. This function is valid when DMA transfer request acceptance output is enabled.
149	—	DEOP2	C	DMA external transfer end output. This function is valid when DMA external transfer end output is enabled.
		DSTP2		DMA external transfer stop input. This function is valid when DMA external transfer stop input is enabled.
		PC2		General-purpose I/O port. This function is valid when DMA external transfer end output and external transfer stop input are disabled.
150	—	DREQ0	C	DMA external transfer request input. Since this input is always used when it is selected as the DMA activation source, output using the port must be stopped beforehand unless this operation is the intended operation.
		PB0		General-purpose I/O port
151	—	DACK0	C	DMA external transfer request acceptance output. This function is valid when DMA transfer request acceptance output is enabled.
		PB1		General-purpose I/O port. This function is valid when DMA transfer request acceptance output is disabled.
152	—	DEOP0	C	DMA external transfer end output. This function is valid when DMA external transfer end output is enabled.
		DSTP0		DMA external transfer stop input. This function is valid when DMA external transfer stop input is enabled.
		PB2		General-purpose I/O port. This function is valid when DMA external transfer end output and external transfer stop input are disabled.
153	—	DREQ1	C	DMA external transfer request input. Since this input is always used when it is selected as the DMA activation source, output using the port must be stopped beforehand unless this operation is the intended operation.
		PB3		General-purpose I/O port.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
154	—	DACK1	C	DMA external transfer request acceptance output. This function is valid when DMA transfer request acceptance output is enabled.
		PB4		General-purpose I/O port. This function is valid when DMA external transfer request acceptance output is disabled.
155	—	DEOP1	C	DMA external transfer end output. This function is valid when DMA external transfer end output is enabled.
		DSTP1		DMA external transfer stop input. This function is valid when DMA external transfer stop input is enabled.
		PB5		General-purpose I/O port. This function is valid when DMA external transfer end output and external transfer stop input are disabled.
156	—	$\overline{\text{IOWR}}$	C	Write strobe output for DMA fly-by transfer. This function is valid when write strobe output for DMA fly-by transfer is enabled.
		PB6		General-purpose I/O port. This function is valid when write strobe output for DMA fly-by transfer is disabled.
157	—	$\overline{\text{IORD}}$	C	Read strobe output for DMA fly-by transfer. This function is valid when read strobe output for DMA fly-by transfer is enabled.
		PB7		General-purpose I/O port. This function is valid when read strobe output for DMA fly-by transfer is disabled.
158	66	$\overline{\text{CS0}}$	C	Chip select 0 output. This function is valid in external bus mode.
		PA0		General-purpose I/O port. This function is valid in single-chip mode.
159	67	$\overline{\text{CS1}}$	C	Chip select 1 output. This function is valid when chip select 1 output is enabled.
		PA1		General-purpose I/O port. This function is valid when chip select 1 output is disabled.
160	68	$\overline{\text{CS2}}$	C	Chip select 2 output. This function is valid when chip select 2 output is enabled.
		PA2		General-purpose I/O port. This function is valid when chip select 2 output is disabled.

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
161	69	$\overline{CS3}$	C	Chip select 3 output. This function is valid when chip select 3 output is enabled.
		PA3		General-purpose I/O port. This function is valid when chip select 3 output is disabled.
164	45	RDY	D	External ready input. This function is valid when external ready input is enabled.
		IN0		Input capture input pin. Since this input is always used when it is selected for input capture input, output using the port must be stopped beforehand unless this operation is the intended operation.
		P80		General-purpose I/O port. This function is valid when external ready input is disabled.
165	46	$\overline{BGRNT}$	D	External bus open acceptance output. Outputs an “L” level when the external bus is open. This function is valid when output is enabled.
		IN1		Input capture input pin. Since this input is always used when it is selected for input capture input, output using the port must be stopped beforehand unless this operation is the intended operation.
		P81		General-purpose I/O port. This function is valid when external bus open acceptance is disabled.
166	47	BRQ	D	External bus open request input. A high level is input to this pin to request for the external bus to be made open. This function is valid when input is enabled.
		IN2		Input capture input pin. Since this input is always used when it is selected for input capture input, output using the port must be stopped beforehand unless this operation is the intended operation.
		P82		General-purpose I/O port. This function is valid when external bus open request is disabled.
167	48	$\overline{RD}$	D	External bus read strobe output. This function is valid in external bus mode.
		P83		General-purpose I/O port. This function is valid in single-chip mode.

(Continued)

(Continued)

Pin no.		Pin name	I/O circuit type*3	Function
LQFP*1	LQFP*2			
168	49	$\overline{WR0}$	D	External bus write strobe output. This function is valid in external bus mode.
		P84		General-purpose I/O port. This function is valid in single-chip mode.
169	50	$\overline{WR1}$	D	External bus write strobe output. This function is valid when $\overline{WR1}$ output in external bus mode is enabled.
		IN3		Input capture input pin. Since this input is always used when it is selected for input capture input, output using the port must be stopped beforehand unless this operation is the intended operation.
		P85		General-purpose I/O port. This function is valid when external bus write enable output is disabled.
170	62	SYSCLK	C	System clock output. This function is valid when system clock output is enabled. A clock having the same frequency as the external bus operating frequency is output (stopped in stop mode).
		P90		General-purpose I/O port. This function is valid when system clock output is disabled.
171	63	P91	C	General-purpose I/O port
172	—	MCLK	C	Memory clock output. This function is valid when memory clock output is enabled. A clock having the same frequency as the external bus operating frequency is output (stopped in sleep mode).
		P92		General-purpose I/O port. This function is valid when memory clock output is disabled.
173	64	P93	C	General-purpose I/O port
174	65	$\overline{AS}$	C	Address strobe output. This function is valid when address strobe output is enabled.
		P94		General-purpose I/O port. This function is valid when address load output is disabled.

*1 : FPT-176P-M02

*2 : FPT-120P-M21

*3 : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

*4 : These functions are not supported on the FPT-120P-M21.

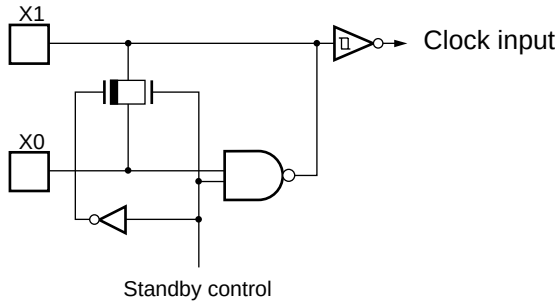
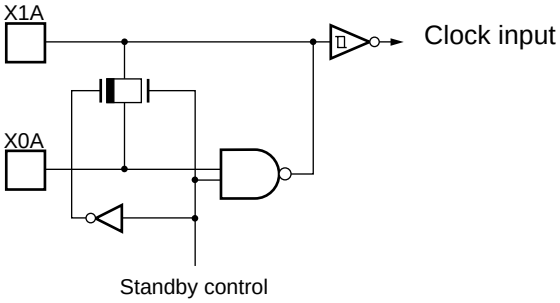
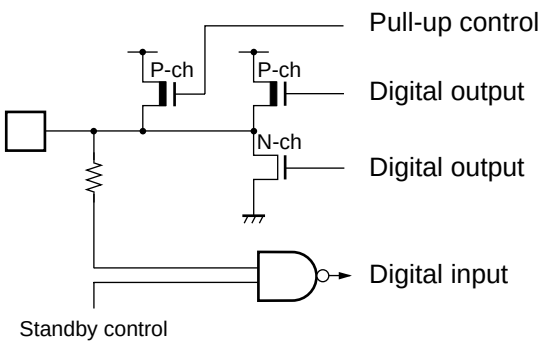
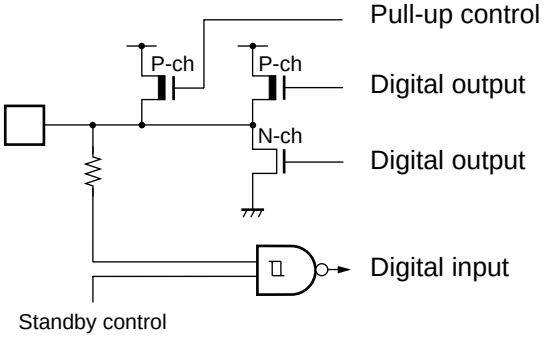
[Power supply and GND pins]

Pin number		Pin name	Function
LQFP*1	LQFP*2		
17, 35, 65, 79, 93, 96, 114, 136, 145, 162, 175	18, 40, 43, 59, 76, 96, 112	V_{SS}	GND pins. Use the same potential for all pins.
18, 36, 66, 80, 97, 115, 142, 146, 163, 176	19, 44, 56, 77, 95	V_{CC}	3.3 V power supply pins. Use the same potential for all pins.
45	107	DAVS	D/A converter GND pin
46	108	DAVC	D/A converter power supply pin
62	109	AV_{CC}	A/D converter analog power supply pin
63	110	AVRH	A/D converter reference power supply pin
64	111	AV_{SS}/AVRL	A/D converter analog GND pin

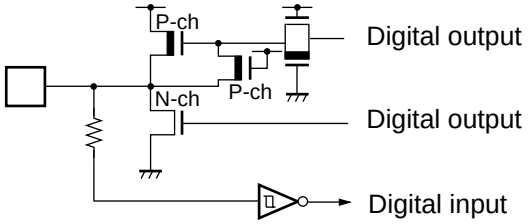
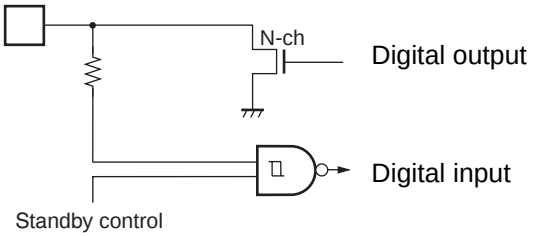
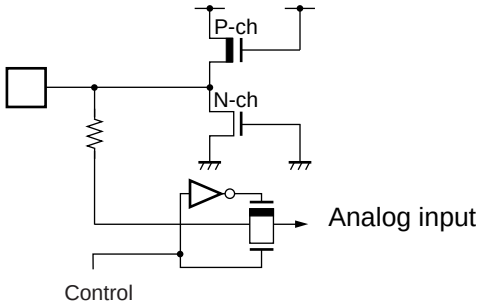
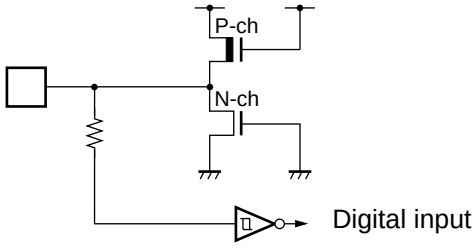
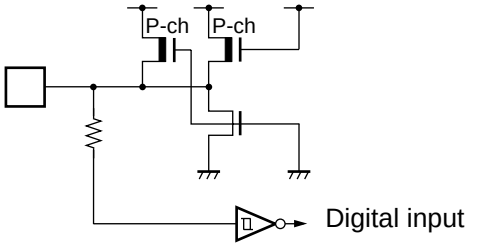
*1 : FPT-176P-M02

*2 : FPT-120P-M21

■ I/O CIRCUIT TYPE

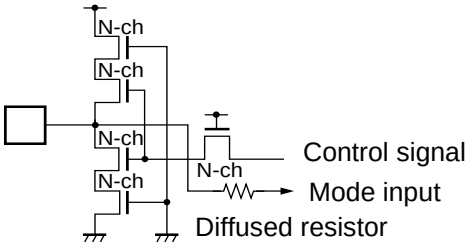
Type	Circuit type	Remarks
A		Oscillation feedback resistance : approx. 1 MΩ
B		Oscillation feedback resistance for low speed (sub clock oscillation) : approx. 7 MΩ
C		• CMOS level output • CMOS level input With standby control With pull-up control
D		• CMOS level output • CMOS level hysteresis input With standby control With pull-up control

(Continued)

Type	Circuit type	Remarks
E		• CMOS level output • CMOS level hysteresis input Withstand voltage of 5 V
F		• N-ch (Open drain input) • CMOS level hysteresis input With standby control Withstand voltage of 5 V
G		Analog input With switch
H		CMOS level hysteresis input
I		CMOS level hysteresis input With pull-up resistor

(Continued)

(Continued)

Type	Circuit type	Remarks
J		• CMOS level input • MB91F353A/F355A/F356B/F357B only

■ HANDLING DEVICES

• Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} and V_{SS}. A latch-up,if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, don't exceed the absolute maximum rating.

• Treatment of Unused Pins

Do not leave unused input pins open, as this may cause a malfunction. Handle by using a pull-up or pull-down resistor.

• Power Supply Pins

In products with multiple V_{CC} and V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to the external power supply and ground lines in order to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source to the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} and V_{SS} pins near this device.

• Crystal Oscillator Circuit

Noise near the X0, X1, X0A and X1A pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, X0A, X1A, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located close to the device as possible.

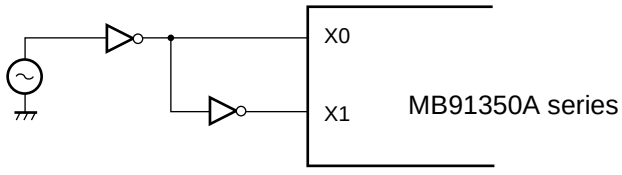
It is strongly recommended that the PC board artwork be designed such that the X0, X1, X0A and X1A pins are surrounded by ground plane, as stable operation can be obtained by using this layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• Notes on Using an External Clock

When using an external clock, as a general rule you should simultaneously supply the clock signal to X0 and a clock signal with the reverse phase to X1. However, the stop mode (oscillator stop mode) must not be used under this configuration (This is because the X1 pin stops at High level output in STOP mode) .

Using an external clock (normal)



Note : STOP mode (oscillation stop mode) cannot be used.

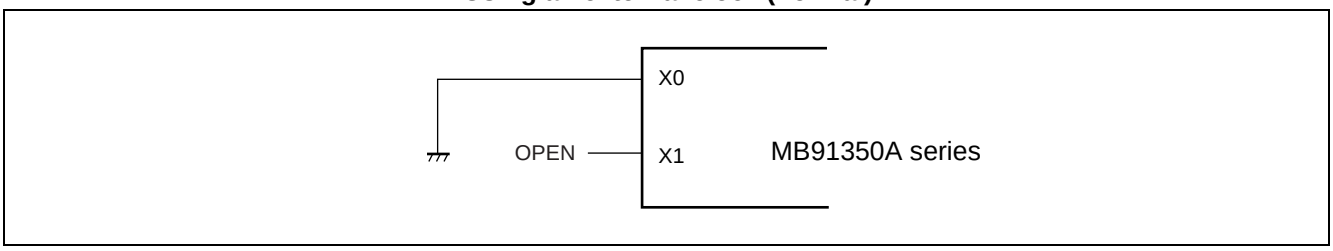
• Clock Control Block

Hold the signal for the oscillation stabilization wait time when inputting a Low level to the $\overline{INIT}$ pin.

• Notes on Using the Sub Clock

When the X0A and X1A pins are not connected to an oscillator, pull down the X0A pin and leave the X1A pin open.

Using an external clock (normal)



• Treatment of NC and OPEN Pins

Pins marked as NC and OPEN must be left open.

• Mode Pins (MD0 to MD2)

These pins should be connected directly to the V_{CC} or V_{SS} pins.

To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} pins is as short as possible and the connection impedance is low.

• Operation at Start-up

The $\overline{INIT}$ pin must be at Low level when the power supply is turned on.

Immediately after the power supply is turned on, the Low level input needs to be held to the $\overline{INIT}$ pin for the oscillation stabilization wait time of the oscillator circuit to ensure that the oscillator has time to settle (For INIT via the $\overline{INIT}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value).

• Oscillation Input at Power On

When the power is turned on, maintain the clock input until the device is released from the oscillation stabilization wait state.

• Precautions While Operating in PLL Clock Mode

On this microcontroller, if the crystal oscillator is disconnected or the external reference clock input stops while PLL clock mode is selected, the microcontroller may continue to operate at the free-run frequency of the self-oscillating circuit within the PLL. However, Fujitsu does not guarantee this operation.

• External Bus Setting

This model guarantees an external bus frequency of 25 MHz.
If the base clock frequency is set to 50 MHz when the DIVR1 (external bus base clock division setting register) register is still set to the default value, the external bus frequency will be set to 50 MHz. When you change the base clock frequency, change the base clock frequency after setting the external bus within 25 MHz.

• MCLK and SYSCLK

The difference between MCLK and SYSCLK is that MCLK stops in SLEEP/STOP mode but SYSCLK stops only in STOP mode. Use the clock that is appropriate for each application.
Upon initialization, MCLK is disabled (PORT) and SYSCLK is enabled. To use MCLK, the port function register (PFR) needs to be set to enable the use of the clock.

• Pull-up Control

If a pull-up resistor is provided to a pin that is used as an external bus pin, there is no guarantee that the pin will conform to the specifications given in "■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4) Normal Bus Access Read/Write Operation, (5) Multiplex Bus Access Read/Write operation and (7) Hold Timing". Furthermore, even if a port has been configured to use a pull-up resistance, this setting is invalid during stop mode with HIZ=1 and during hardware standby mode.

• Sub Clock Select

At least one NOP instruction needs to be executed immediately after switching the clock source from main clock mode to sub clock mode.

```
(Idi    #0x0b, r0)
(Idi    #_CLKR, r12)
 stb    r0, @r12        // sub-clock mode
 nop                    // Must insert NOP instruction
```

• Bit Search Module

The BSD0, BSD1, and BDSC registers can only be accessed in words.

• D-bus Memory

Do not set the code area to memory on the D-bus because instructions cannot be fetched from the D-bus. Executing an instruction fetch to the D-bus area will cause incorrect data to be interpreted as code, possibly causing the device to run out of control.

• Low Power Consumption Mode

When entering sleep or stop mode, be sure to read the standby control register (STCR) immediately after writing to it.
More specifically, use the following sequence.
Furthermore, after recovering from standby mode, set the I flag, ILM, and ICR registers such that the CPU branches to the interrupt handler for the interrupt that triggered the controller to recover from standby mode.

```
(Idi    #value_of_standby, r0)
(Idi    #_STCR, r12)
 stb    r0, @r12        // set STOP/SLEEP bit
 Idub   @r12, r0        // Must read STCR
 Idub   @r12, r0        // after reading, go into standby mode
 NOP                    // Must insert NOP × 5
 NOP
 NOP
 NOP
 NOP
```

• Switching the Function of Shared Ports

Use the Port Function Register (PFR) to switch between using an external pin as a port or a shared pin. Note, however, that bus pins are switched depending on the external bus settings.

• Prefetch

If prefetch is enabled in a area that is configured as little endian, limit access to the corresponding area to word-length (32-bit) access.
Byte or halfword does not allow a proper access to data.

• I/O Port Access

Ports can only be accessed in bytes.

• Built-in RAM

Immediately after a reset is released, the internal RAM capacity restriction function begins operating, allowing only 4 Kbytes to be used for both data and program execution irrespective of the on-chip RAM capacity. Update the setting to clear the restriction function.
At least one NOP instruction is required immediately after updating this setting.

Please refer to the “MB91350A Series HARDWARE MANUAL CHAPTER 19 DATA INTERNAL RAM/INSTRUCTION INTERNAL RAM ACCESS RESTRICTION FUNCTIONS” for the details.

• Flash Memory

In programming mode, Flash memory cannot be used for the interrupt vector table (However, a reset can be performed) .

• Notes on the PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the following exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

1. The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction :
   (a) a user interrupt or NMI is accepted; (b) single-step execution is performed; or (c) execution breaks due to a data event or from the emulator menu.
   - The D0 and D1 flags are updated in advance.
   - An EIT handling routine (user interrupt, NMI, or emulator) is executed.
   - Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as in (1).
2. The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.
   - The PS register is updated in advance.
   - The EIT handling routine (user interrupt, NMI, or emulator) is executed.
   - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1).

[Note on Debugger]

- Single-Step Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler) .
Disable the corresponding interrupt when the corresponding interrupt handling routine no longer needs debugging.

- Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including event breaks).

- Internal ROM area

Do not set DMAC transfer destination to an address in the internal ROM area.

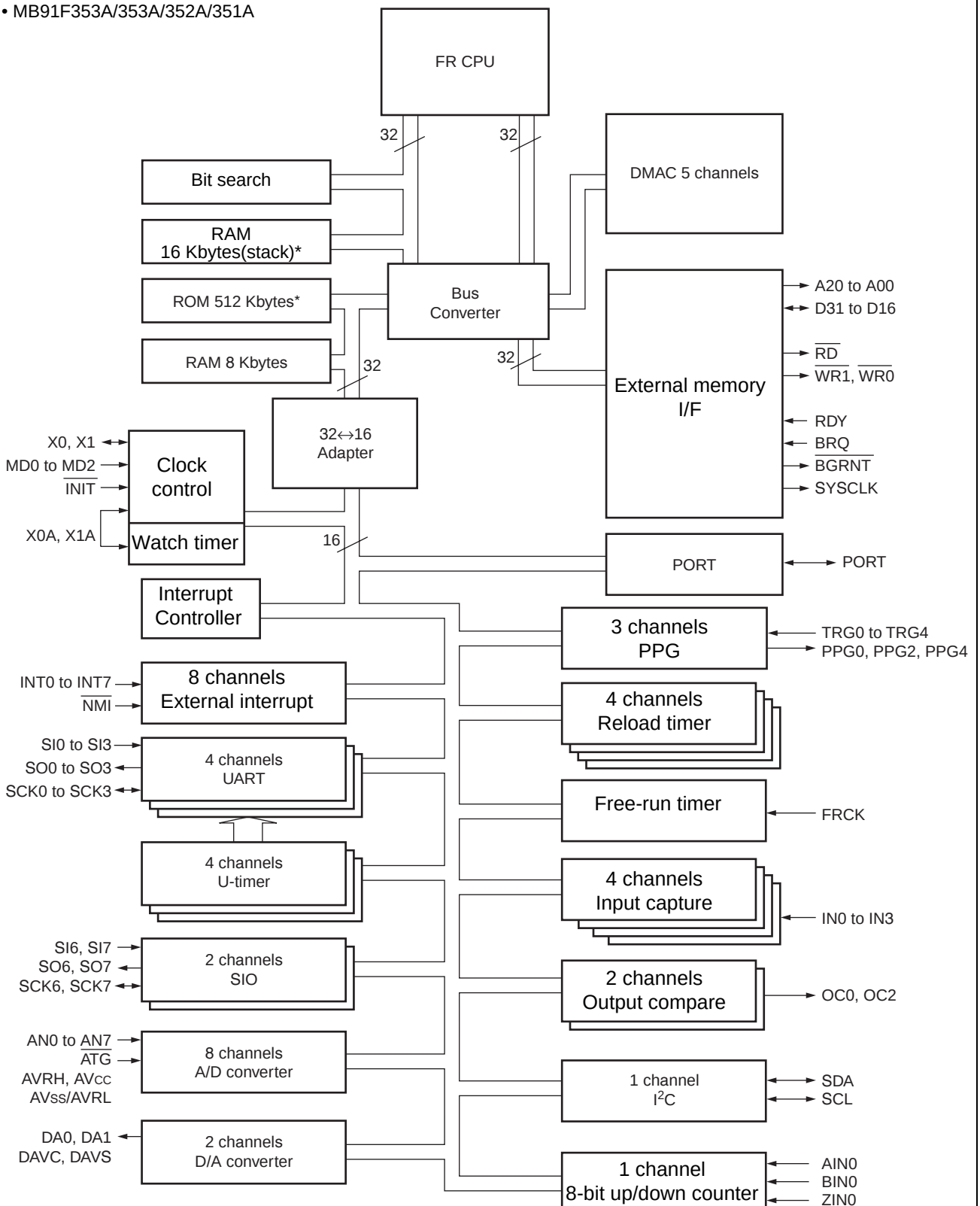
- Simultaneous Occurrence of a Software Break (INTE instruction) and a User Interrupt/NMI

When a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may react as follows.

- The debugger stops pointing to a location other than a programmed breakpoint.
- The program does not resume execution correctly after breaking.
  If this symptom occurs, use a hardware break in place of the software break. When using a monitor debugger, do not set a break at the relevant location.
- A malfunction may occur if the stack pointer is in an area that is configured for DSU operand break. Do not set a data event breaks that apply to accesses to an area that contains the address of the system stack pointer.

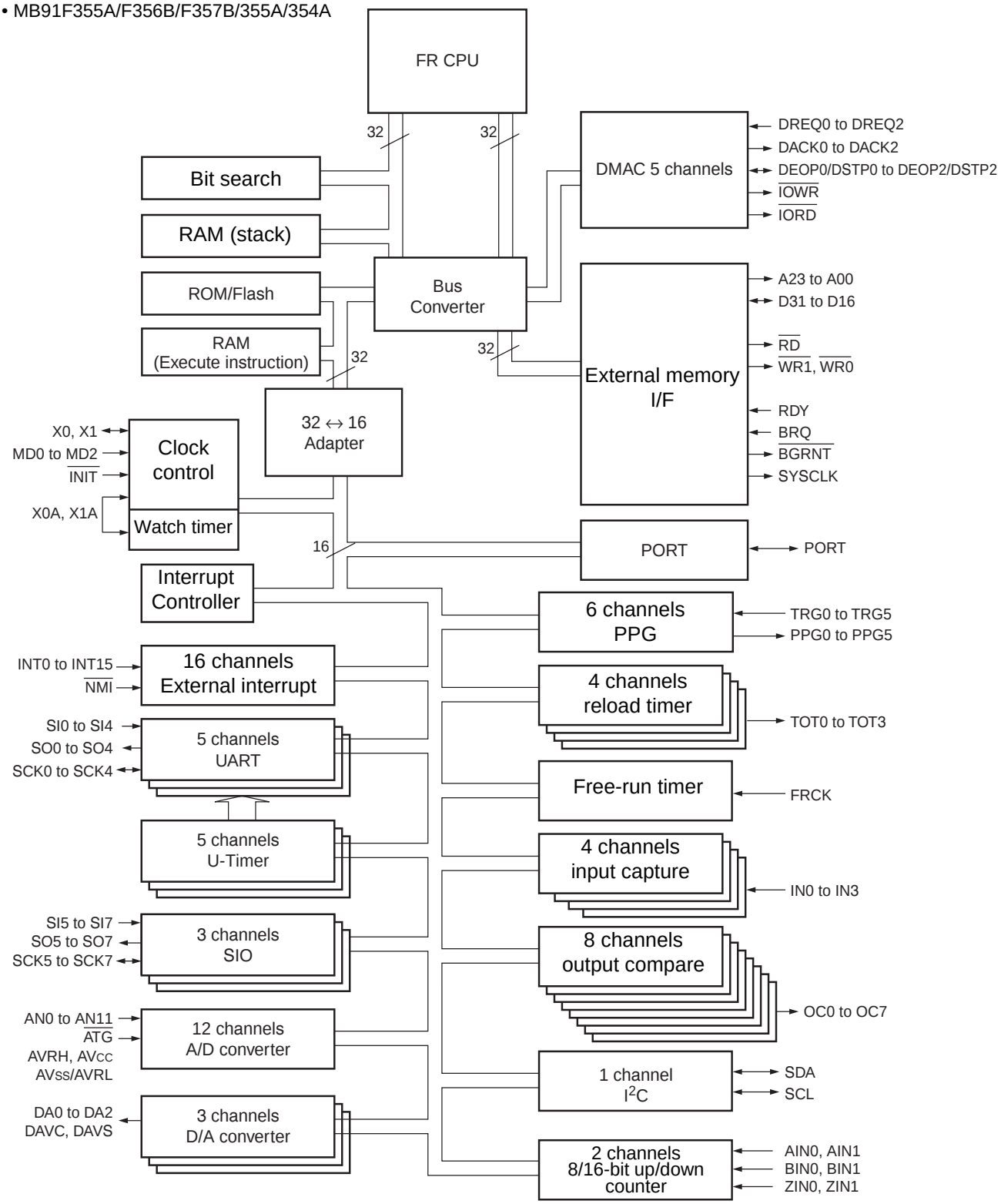
■ BLOCK DIAGRAMS

• MB91F353A/353A/352A/351A



* : MB91352A : RAM 8 Kbytes (stack) , ROM 384 Kbytes
MB91351A : RAM 16 Kbytes (stack) , ROM 384 Kbytes

• MB91F355A/F356B/F357B/355A/354A



	MB91F355A/MB91F357B	MB91F356B	MB91355A	MB91354A
ROM/Flash	512 Kbytes (Flash)	256 Kbytes (Flash)	512 Kbytes	384 Kbytes
RAM (stack)	16 Kbytes	16 Kbytes	16 Kbytes	8 Kbytes
RAM (Execute instruction)	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes

■ CPU AND CONTROL UNIT

Internal architecture

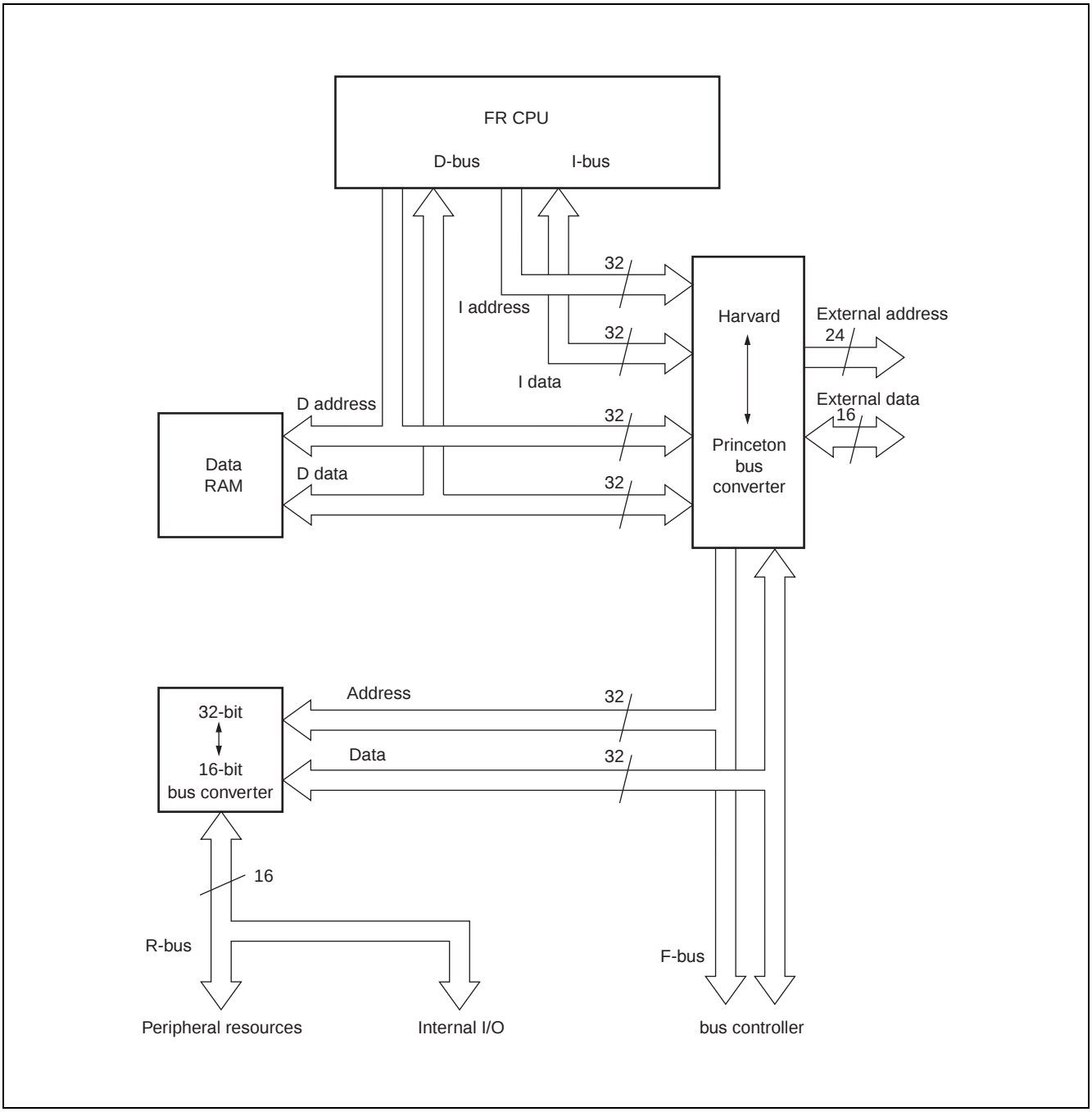
The FR family CPU is a high performance core based on a RISC architecture while incorporating advanced instructions for embedded controller applications.

1. Features

- RISC architecture
  Basic instructions : Executed at 1 instruction per cycle
- 32-bit architecture
  General-purpose registers : 32-bit × 16 registers
- 4GB linear memory space
- Built-in multiplier
  32-bit × 32-bit multiplication : 5 cycles
  16-bit × 16-bit multiplication : 3 cycles
- Enhanced interrupt handling
  Fast response speed (6 cycles)
  Multiple interrupts supported
  Level masking (16 levels)
- Enhanced I/O manipulation instructions
  Memory-to-memory transfer instructions
  Bit manipulation instructions
- High code efficiency
  Basic instruction word length : 16-bit
- Low-power consumption
  Sleep mode and stop mode
- Gear function

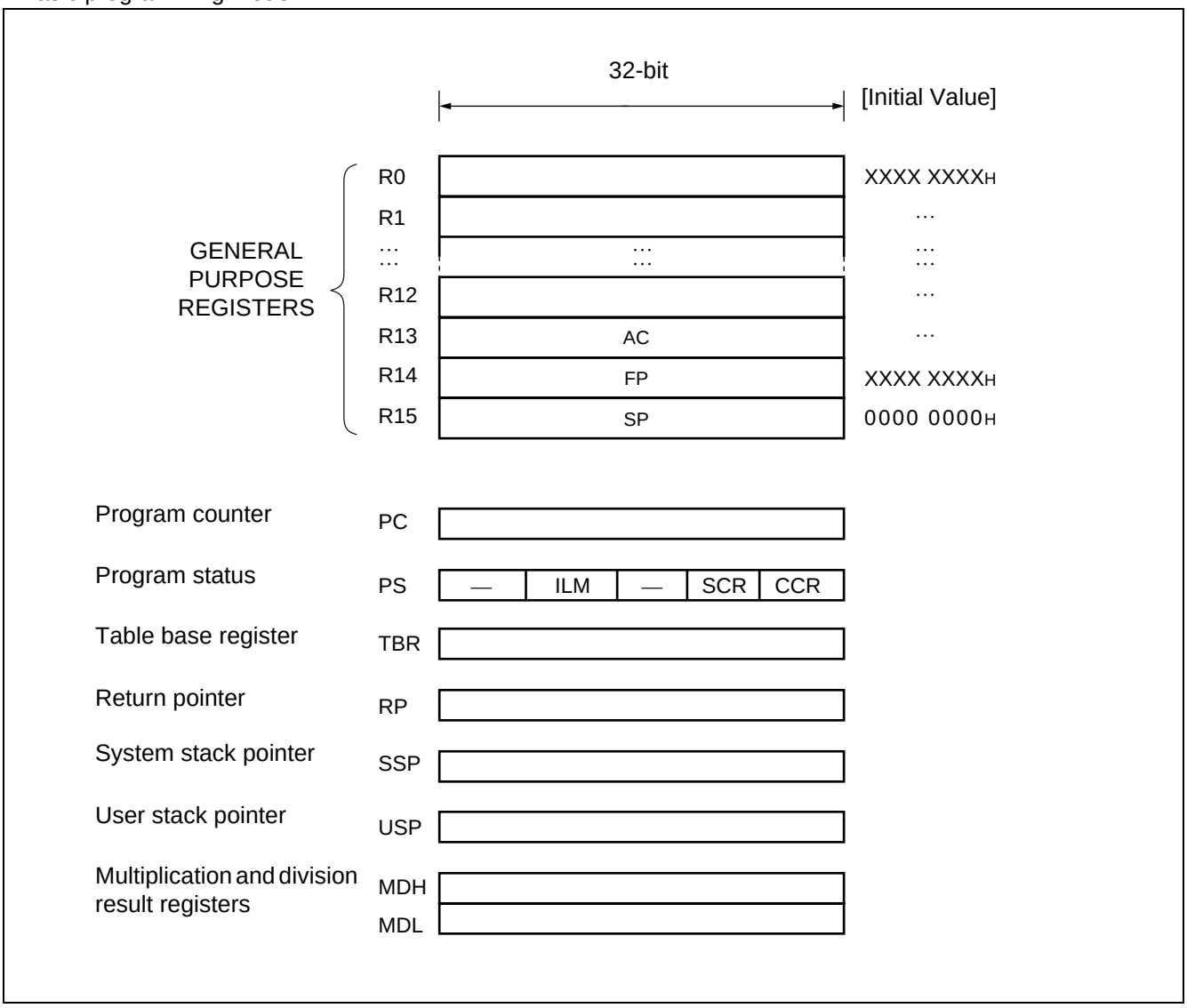
2. Internal architecture

The FR-family CPU has a Harvard architecture in which the instruction and data buses are separated. A 32-bit ↔ 16-bit bus converter is connected to the 32-bit bus (F-bus), providing an interface between the CPU and peripheral resources. A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus, providing an interface between the CPU and the bus controller.



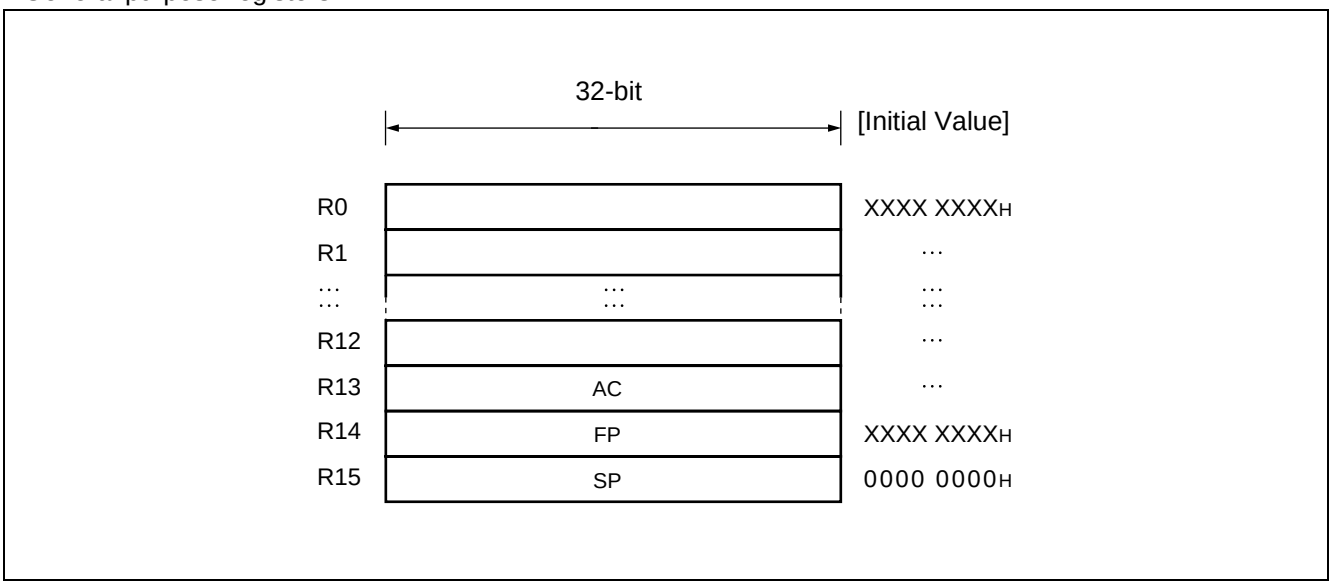
3. Programming model

• Basic programming model



4. Registers

• General purpose registers



Registers R0 to R15 are general-purpose registers. The registers are used as the accumulator and memory access pointers for CPU operations.

Of these 16 registers, the registers listed below are intended for special applications. Some instructions have been enhanced for this purpose.

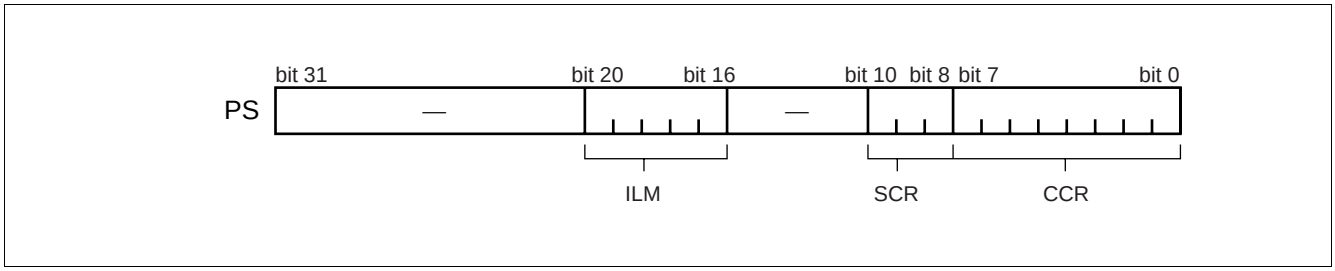
R13 : Virtual accumulator
R14 : Frame pointer
R15 : Stack pointer

The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 00000000H (SSP value).

• PS (Program Status)

This register holds the program status and is divided into the ILM, SCR, and CCR.

The undefined bits in the following illustration are all reserved bits. Reading these bits always returns “0”. Writing to them has no effect.



• CCR (Condition Code Register)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial Value
CCR	—	—	S	I	N	Z	V	C	- - 00XXXX$_B$

S : Stack flag. Cleared to “0” by a reset.
I : Interrupt enable flag. Cleared to “0” by a reset.
N : Negative flag. The initial value after a reset is indeterminate.
Z : Zero flag. The initial value after a reset is indeterminate.
V : Overflow flag. The initial value after a reset is indeterminate.
C : Carry flag. The initial value after a reset is indeterminate.

• SCR (System Condition Code Register)

	bit 10	bit 9	bit 8	Initial Value
SCR	D1	D0	T	XX0$_B$

Flag for stepwise division

Stores intermediate data for stepwise division operations.

Step trace trap flag

A flag specifying whether the step trace trap function is enabled or not.
The step trace trap function is used by the emulator. This function cannot be used by a user program while using the emulator.

• ILM

	bit 20	bit 19	bit 18	bit 17	bit 16	Initial Value
ILM	ILM4	ILM3	ILM2	ILM1	ILM0	01111$_B$

This register stores the interrupt level mask value. The value in the ILM register is used as the level mask.
Initialized to “15” (01111$_B$) by a reset.

• PC (Program Counter)

	bit 31	bit 0	Initial Value
PC			XXXXXXXX$_H$

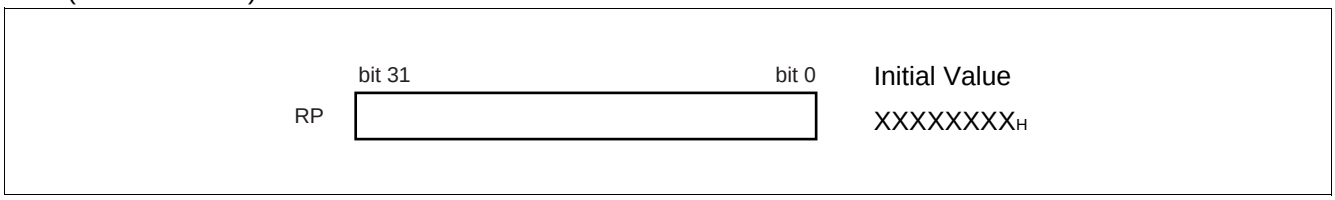
The program counter contains the address of the instruction currently being executed.
The initial value after a reset is indeterminate.

• TBR (Table Base Register)

	bit 31	bit 0	Initial Value
TBR			000FFC00$_H$

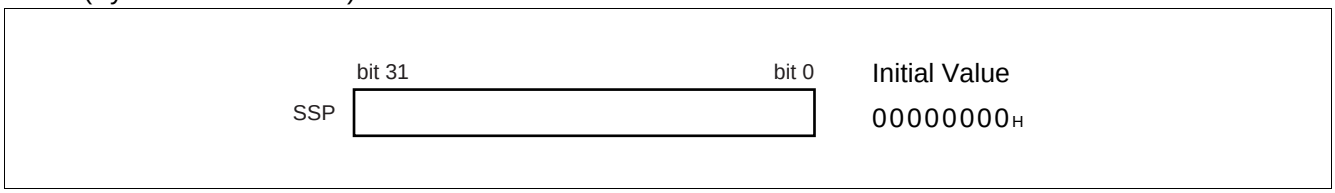
The table base register contains the start address of the vector table used for handling EIT events.
The initial value after a reset is 000FFC00$_H$.

• RP (Return Pointer)



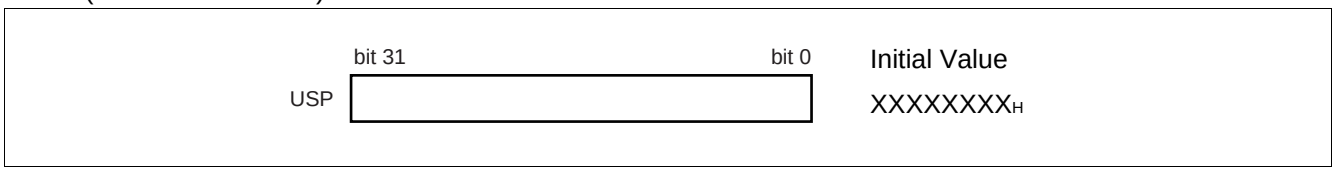
The return pointer contains the address to which to return from a subroutine.
When the CALL instruction is executed, the value in the PC is transferred to the RP.
When the RET instruction is executed, the value in the RP is transferred to the PC.
The initial value after a reset is indeterminate.

• SSP (System Stack Pointer)



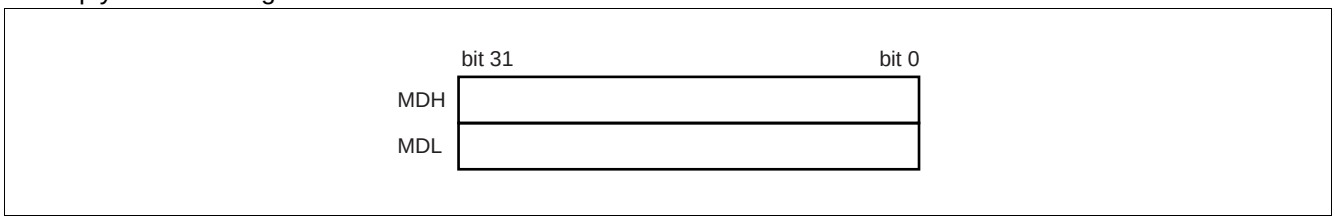
The SSP is the system stack pointer and functions as R15 when the S flag is “0”.
The SSP can be specified explicitly.
The SSP is also used as the stack pointer that specifies the stack for saving the PS and PC when an EIT event occurs.
The initial value after a reset is 00000000_H.

• USP (User Stack Pointer)



The USP is the user stack pointer and functions as R15 when the S flag is “1”.
The USP can be specified explicitly.
The initial value after a reset is indeterminate.
This pointer cannot be used by the RETI instruction.

• Multiply & Divide Registers



These registers are 32-bit wide registers that store the results of multiplication and division operations.
The initial value after a reset is indeterminate.

■ MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and a mode register (MODR) to set the operation mode.

1. Mode Pins

The MD2, MD1, and MD0 pins specify how the mode vector fetch is performed.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	internal ROM mode vector	Internal	
0	0	1	external ROM mode vector	External	The bus width is specified by the mode register.

Values other than those listed in the table are prohibited.

2. Mode Register (MODR)

The data that is written to the mode register from the address at 000F FFF8$_H$ by the mode vector fetch is called the mode data.
After the mode register (MODR) , has been set, the device operates according to the configured operating mode.
The mode register is set by all of the reset sources. User programs cannot write to the mode register.

Note : No data exists at the address (0000 07FF$_H$) of the mode register in the previous FR family.

[Register description]

MODR
000F FFF8$_H$

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	0	0	ROMA	WTH1	WTH0
					← Operating mode setting bits →		

Initial Value
XXXXXXXX$_B$

[bit7-bit3] Reserved bit

Always set these bits to “00000$_B$”. Operation is not guaranteed if these bits are set to a value other than “00000$_B$”.

[bit2] ROMA (internal ROM enable bit)

The ROMA bit is used to set whether to enable the internal F-bus RAM and F-bus ROM areas.

ROMA	Function	Remarks
0	External ROM mode	Internal F-bus RAM is valid; the area (8 0000$_H$ to 10 0000$_H$) of internal ROM is used as an external area.
1	Internal ROM mode	Internal F-bus RAM and F-bus ROM are valid.

[bit1, bit0] WTH1, WTH0 (Bus width setting bits)

Used to set the bus width to be used in external bus mode.
In external bus mode, the BW1 and BW0 bits of AMD0 (CS0 area) are set to the value of these bits.

WTH1	WTH0	function	Remarks
0	0	8-bit bus width	external bus mode
0	1	16-bit bus width	
1	0	—	Setting prohibited
1	1	single chip mode	single chip mode

■ MEMORY SPACE

1. Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

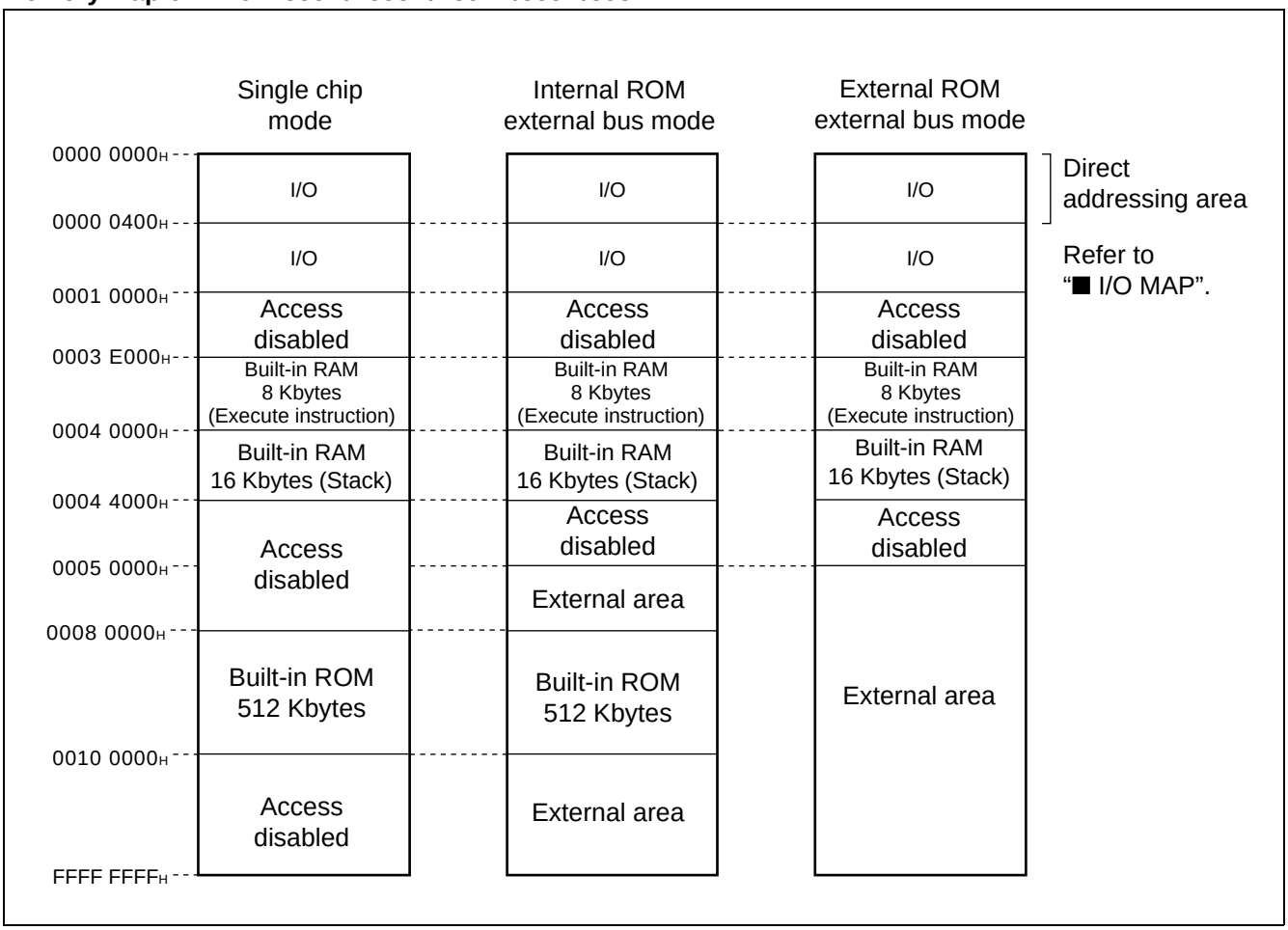
• Direct Addressing Areas

The following address space areas are used as I/O areas.
These areas are called direct addressing areas. The addresses of operands in these areas can be specified directly within an instruction.
The size of the directly addressable areas depends on the size of the data being accessed as shown below.

→ Byte data access : 000H to 0FFH
→ Half word data access : 000H to 1FFH
→ Word data access : 000H to 3FFH

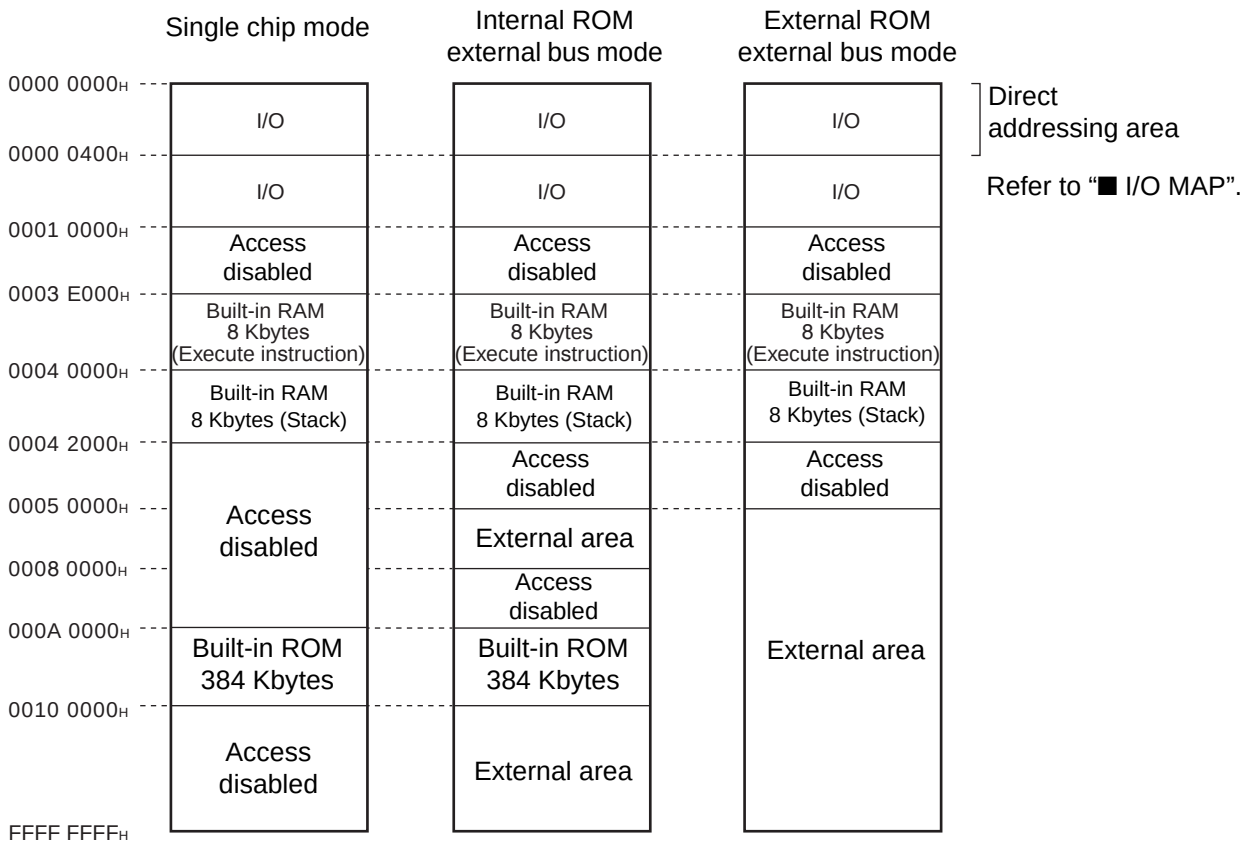
2. Memory Map

Memory Map of MB91F355A/F353A/F357B/355A/353A



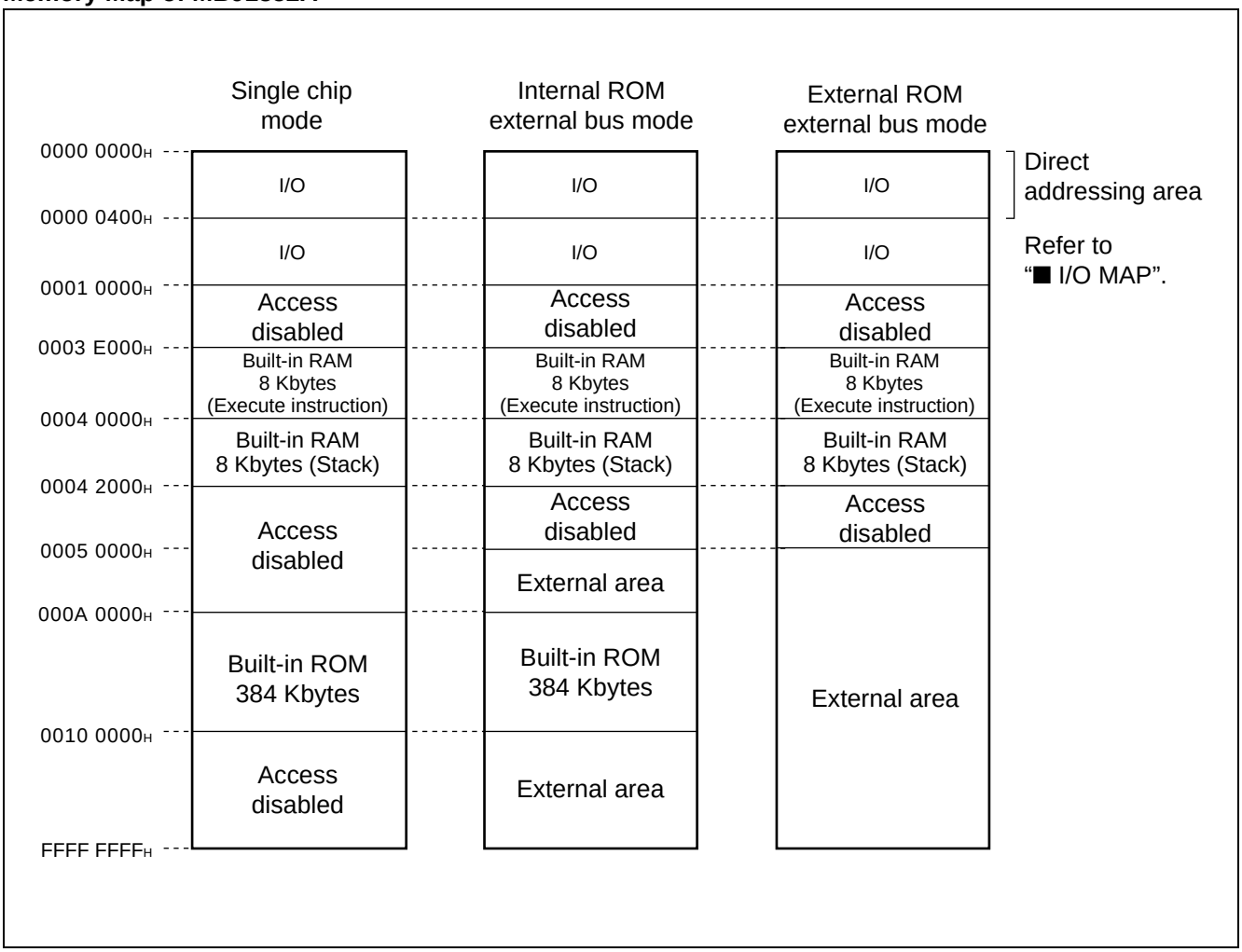
- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is released. At least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

Memory Map of MB91354A



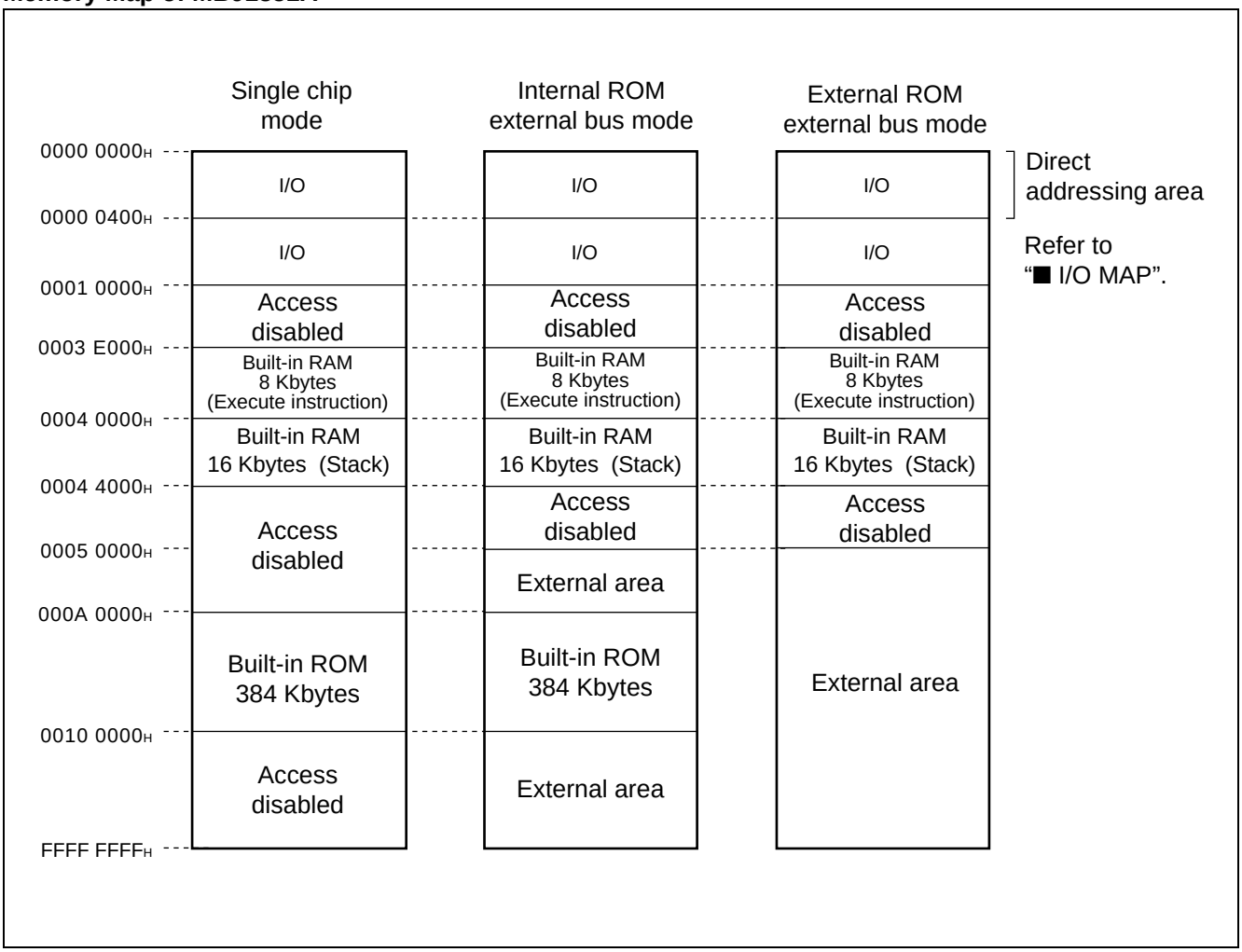
- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is released. At least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

Memory Map of MB91352A



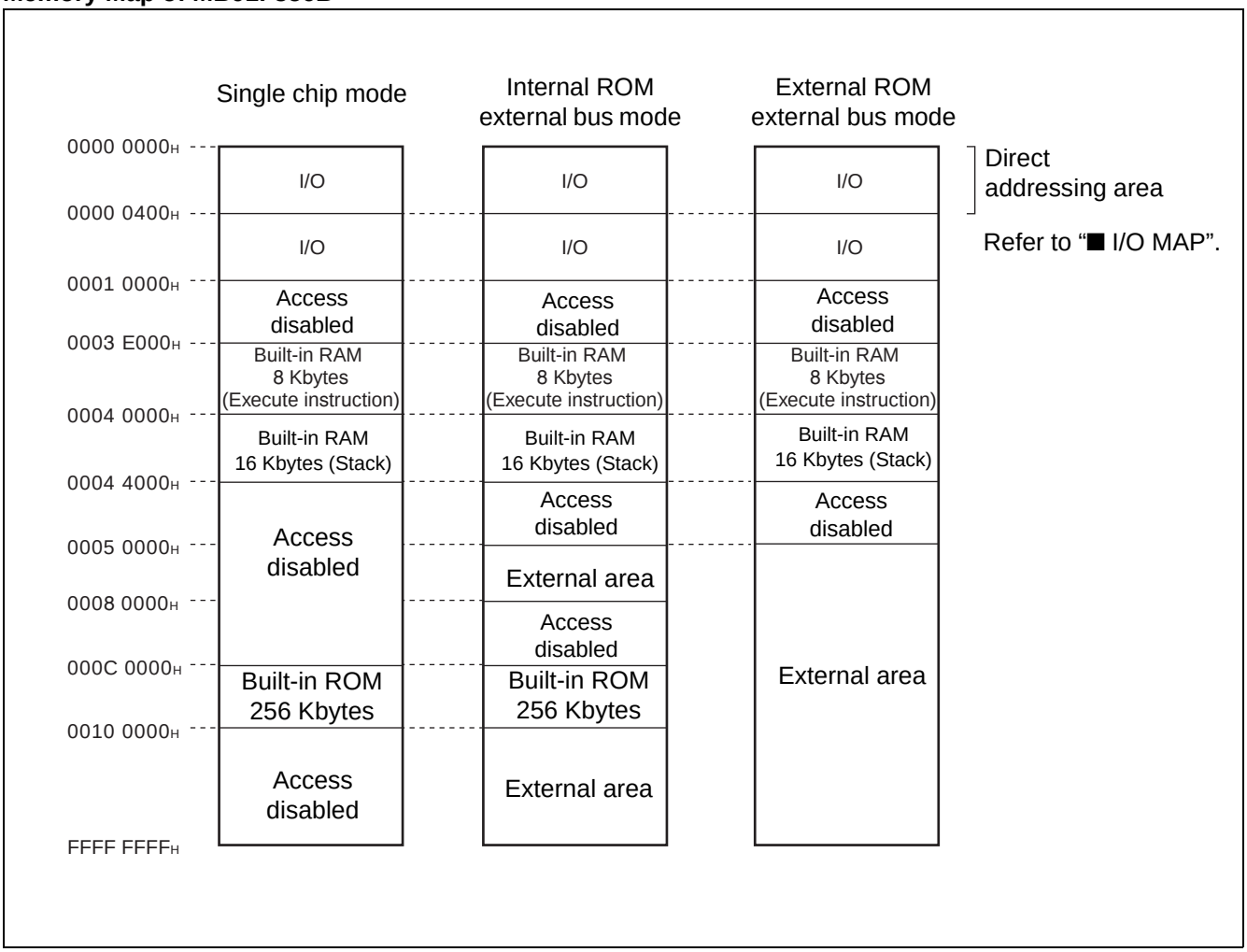
- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is released. At least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

Memory Map of MB91351A



- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is released. At least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

Memory Map of MB91F356B



- Each mode is set depending on the mode vector fetch after $\overline{\text{INIT}}$ is negated.
- The available area of internal RAM is restricted immediately after a reset is released. At least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

■ I/O MAP

This shows the locations of each of the registers for the peripheral resources in memory space.

[How to read the table]

Address	Register				Block diagram
	+ **0**	+ **1**	+ **2**	+ **3**	
000000H	PDR0 [R/W] B XXXXXXXX	PDR1 [R/W] B XXXXXXXX	PDR2 [R/W] B XXXXXXXX	PDR3 [R/W] B XXXXXXXX	T-unit Port Data Register

Read/write attribute, Access unit
(B : Byte, H : Half Word, W : Word)

Initial value after a reset

Register name (First-column register at address 4n; second-column register at address 4n + 2)

Location of left-most register (When using word access, the register in column 1 is the MSB side of the data.)

Note : Initial values of register bits are represented as follows :

“1” : Initial value is “1”.

“0” : Initial value is “0”.

“X” : Initial value is “X”.

“–” : No physical register at this location

Address	Register				Block
	+0	+1	+2	+3	
000000H	————	————	PDR2[R/W]B XXXXXXXX	PDR3[R/W]B XXXXXXXX	T-unit port data register*3
000004H	PDR4[R/W]B XXXXXXXX	PDR5[R/W]B XXXXXXXX	PDR6[R/W]B XXXXXXXX	————	
000008H	PDR8[R/W]B --XXXXXX	PDR9[R/W]B ---XXXXX	PDRA[R/W]B ----XXXX	PDRB[R/W]B*3 XXXXXXXX	
00000CH	PDRC[R/W]B*3 -----XXX	————			
000010H	PDRG[R/W]B*3 --XXXXXX	PDRH[R/W]B --XXXXXX	PDRI[R/W]B --XXXXXX	PDRJ[R/W]B*3 XXXXXXXX	R-bus port data register*3
000014H	PDRK[R/W]B XXXXXXXX	PDRL[R/W]B ------XX	PDRM[R/W]B --XXXXXX	PDRN[R/W]B --XXXXXX	
000018H	PDRO[R/W]B XXXXXXXX	PDRP[R/W]B*3 ----XXXX	————	————	
00001CH	————				
000020H	————	————	————	————	Reserved
000024H	SMCS5[R/W]B,H*3 00000010_----00--		SES5[R/W]B*3 ------00	SDR5[R/W]B*3 XXXXXXXX	SIO5*3
000028H	SMCS6[R/W]B,H 00000010_----00--		SES6[R/W]B ------00	SDR6[R/W]B XXXXXXXX	SIO6
00002CH	SMCS7[R/W]B,H 00000010_----00--		SES7[R/W]B ------00	SDR7[R/W]B XXXXXXXX	SIO7
000030H	————	————	CDCR5[R/W]B*3 0---1111	———— *1	SIO prescaler 5*3
000034H	CDCR6[R/W]B 0---1111	———— *1	CDCR7[R/W]B 0---1111	———— *1	SIO prescaler 6, 7
000038H	————	SRCL5[W]B*3 --------	SRCL6[W]B --------	SRCL7[W]B --------	SIO5 to SIO7*3
00003CH	————	————	————	————	Reserved
000040H	EIRR0[R/W]B,H,W 00000000	ENIR0[R/W]B,H,W 00000000	ELVR0[R/W]B,H,W 00000000		External interrupts (INT0 to INT7)
000044H	DICR[R/W]B,H,W -------0	HRCL[R/W]B,H,W 0--11111	————		Delay interrupt
000048H	TMRLR[W]H,W XXXXXXXX_XXXXXXXX		TMR[R]H,W XXXXXXXX_XXXXXXXX		Reload timer 0
00004CH	————		TMCSR[R/W]B,H,W ----0000_00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000050H	TMRLR[W]H,W XXXXXXXX_XXXXXXXX		TMR[R]H,W XXXXXXXX_XXXXXXXX		Reload timer 1
000054H	————		TMCSR[R/W]B,H,W ----0000_00000000		
000058H	TMRLR[W]H,W XXXXXXXX_XXXXXXXX		TMR[R]H,W XXXXXXXX_XXXXXXXX		Reload timer 2
00005CH	————		TMCSR[R/W]B,H,W ----0000_00000000		
000060H	SSR[R/W]B,H,W 00001000	SIDR[R/W]B,H,W XXXXXXXX	SCR[R/W]B,H,W 00000100	SMR[R/W]B,H,W 00--0---	UART0
000064H	UTIM[R]H(UTIMR[W]H) 00000000_00000000		DRCL[W]B --------	UTIMC[R/W]B 0--00001	U-TIMER/ UART0
000068H	SSR[R/W]B,H,W 00001000	SIDR/SODR [R/W]B,H,W XXXXXXXX	SCR[R/W]B,H,W 00000100	SMR[R/W]B,H,W 00--0---	UART1
00006CH	UTIM[R]H(UTIMR[W]H) 00000000_00000000		DRCL[W]B --------	UTIMC[R/W]B 0--00001	U-TIMER/ UART1
000070H	SSR[R/W]B,H,W 00001000	SIDR[R/W]B,H,W XXXXXXXX	SCR[R/W]B,H,W 00000100	SMR[R/W]B,H,W 00--0---	UART2
000074H	UTIM[R]H(UTIMR[W]H) 00000000_00000000		DRCL[W]B --------	UTIMC[R/W]B 0--00001	U-TIMER/ UART2
000078H	ADCS2[R/W]B,H,W X000XX00	ADCS1[R/W]B,H,W 000X0000	ADCT[R/W]H,W XXXXXXXX_XXXXXXXX		A/D converter successive approxima-tions
00007CH	ADTH0[R]B,H,W XXXXXXXX	ADTL0[R]B,H,W 000000XX	ADTH1[R]B,H,W XXXXXXXX	ADTL1[R]B,H,W 000000XX	
000080H	ADTH2[R]B,H,W XXXXXXXX	ADTL2[R]B,H,W 000000XX	ADTH3[R]B,H,W XXXXXXXX	ADTL3[R]B,H,W 000000XX	
000084H	————	DACR2 [R/W]B,H,W*3 -------0	DACR1[R/W]B,H,W -------0	DACR0[R/W]B,H,W -------0	D/A converter*3
000088H	————	DADR2 [R/W]B,H,W*3 XXXXXXXX	DADR1[R/W]B,H,W XXXXXXXX	DADR0[R/W]B,H,W XXXXXXXX	
00008CH	————	————	————	————	Reserved
000090H	————	————	————	———— *1	Reserved
000094H	IBCR[R/W]B,H,W 00000000	IBSR[R]B,H,W 00000000	ITBA[R/W]B,H,W ------00_00000000		I2C interface
000098H	ITMK[R/W]B,H,W 00----11_11111111		ISMK[R/W]B,H,W 01111111	ISBA[R/W]B,H,W -0000000	
00009CH	———— *2	IDAR[R/W]B,H,W 00000000	ICCR[R/W]B,H,W 0-011111	IDBL[R/W]B,H,W -------0	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000A0H	————	————*1	————	————*1	Reserved
0000A4H	————	————*1	————*1	————*1	
0000A8H	TMRLR[W]H,W XXXXXXXX_XXXXXXXX		TMR[R]H,W XXXXXXXX_XXXXXXXX		Reload timer 3
0000ACH	————		TMCSR[R/W]B,H,W ----0000_00000000		
0000B0H	RCR1[W]B,H,W*3 00000000	RCR0[W]B,H,W 00000000	UDCR1[R]B,H,W*3 00000000	UDCR0[R]B,H,W 00000000	8/16-bit Up/Down counter 0, 1*3
0000B4H	CCRH0[R/W]B,H,W 00000000	CCRL0[R/W]B,H,W 00001000	————	CSR0[R/W]B,H,W 00000000	
0000B8H	CCRH1[R/W]B,H,W*3 00000000	CCRL1[R/W]B,H,W*3 00001000	————	CSR1[R/W]B,H,W*3 00000000	
0000BCH	————	————	————	————	Reserved
0000C0H	SSR[R/W]B,H,W 00001000	SIDR[R/W]B,H,W XXXXXXXX	SCR[R/W]B,H,W 00000100	SMR[R/W]B,H,W 00--0---	UART3
0000C4H	UTIM[R]H(UTIMR[W]H) 00000000_00000000		————	UTIMC[R/W]B 0--00001	U-TIMER/ UART3
0000C8H	SSR[R/W]B,H,W*3 00001000	SIDR[R/W]B,H,W*3 XXXXXXXX	SCR[R/W]B,H,W*3 00000100	SMR[R/W]B,H,W*3 00--0---	UART4*3
0000CCH	UTIM[R]H(UTIMR[W]H)*3 00000000_00000000		————	UTIMC[R/W]B*3 0--00001	U-TIMER/ UART4*3
0000D0H	EIRR1[R/W]B,H,W*3 00000000	ENIR1[R/W]B,H,W*3 00000000	ELVR1[R/W]B,H,W*3 00000000		External interrupts (INT8 to INT15)*3
0000D4H	TCDT[R/W]H,W 00000000_00000000		————	TCCS[R/W]B,H,W 00000000	16-bit free-run timer
0000D8H	IPCP1[R]H,W XXXXXXXX_XXXXXXXX		IPCP0[R]H,W XXXXXXXX_XXXXXXXX		16-bit input capture
0000DCH	IPCP3[R]H,W XXXXXXXX_XXXXXXXX		IPCP2[R]H,W XXXXXXXX_XXXXXXXX		
0000E0H	————	ICS23[R/W]B,H,W 00000000	————	ICS01[R/W]B,H,W 00000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000E4H	OCCP1[R/W]H,W*3 XXXXXXXX_XXXXXXXX		OCCP0[R/W]H,W XXXXXXXX_XXXXXXXX		16-bit output compare*3
0000E8H	OCCP3[R/W]H,W*3 XXXXXXXX_XXXXXXXX		OCCP2[R/W]H,W XXXXXXXX_XXXXXXXX		
0000ECH	OCCP5[R/W]H,W*3 XXXXXXXX_XXXXXXXX		OCCP4[R/W]H,W*3 XXXXXXXX_XXXXXXXX		
0000F0H	OCCP7[R/W]H,W*3 XXXXXXXX_XXXXXXXX		OCCP6[R/W]H,W*3 XXXXXXXX_XXXXXXXX		
0000F4H	OCS23[R/W]B,H,W 11101100_00001100		OCS01[R/W]B,H,W 11101100_00001100		
0000F8H	OCS67[R/W]B,H,W*3 11101100_00001100		OCS45[R/W]B,H,W*3 11101100_00001100		
0000FCH	————	————	————	————	Reserved
000100H to 000114H	————	————	————	————	Reserved
000118H	GCN10[R/W]H 00110010_00010000		————	GCN20[R/W]B 00000000	PPG control 0
00011CH	————		————		Reserved
000120H	PTMR0[R]H,W 11111111_11111111		PCSR0[W]H,W XXXXXXXX_XXXXXXXX		PPG0
000124H	PDUT0[W]H,W XXXXXXXX_XXXXXXXX		PCNH0[R/W]B,H,W 00000000	PCNL0[R/W]B,H,W 00000000	
000128H	PTMR1[R]H,W*3 11111111_11111111		PCSR1[W]H,W*3 XXXXXXXX_XXXXXXXX		PPG1*3
00012CH	PDUT1[W]H,W*3 XXXXXXXX_XXXXXXXX		PCNH1[R/W]B,H,W*3 00000000	PCNL1[R/W]B,H,W*3 00000000	
000130H	PTMR2[R]H,W 11111111_11111111		PCSR2[W]H,W XXXXXXXX_XXXXXXXX		PPG2
000134H	PDUT2[W]H,W XXXXXXXX_XXXXXXXX		PCNH2[R/W]B,H,W 00000000	PCNL2[R/W]B,H,W 00000000	
000138H	PTMR3[R]H,W*3 11111111_11111111		PCSR3[W]H,W*3 XXXXXXXX_XXXXXXXX		PPG3*3
00013CH	PDUT3[W]H,W*3 XXXXXXXX_XXXXXXXX		PCNH3[R/W]B,H,W*3 00000000	PCNL3[R/W]B,H,W*3 00000000	
000140H	PTMR4[R]H,W 11111111_11111111		PCSR4[W]H,W XXXXXXXX_XXXXXXXX		PPG4
000144H	PDUT4[W]H,W XXXXXXXX_XXXXXXXX		PCNH4[R/W]B,H,W 00000000	PCNL4[R/W]B,H,W 00000000	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000148H	PTMR5[R]H,W*3 11111111_11111111		PCSR5[W]H,W*3 XXXXXXXX_XXXXXXXX		PPG5*3
00014CH	PDUT5[W]H,W*3 XXXXXXXX_XXXXXXXX		PCNH5[R/W]B,H,W*3 00000000	PCNL5[R/W]B,H,W*3 00000000	
000150H to 0001FCH	————				Reserved
000200H	DMACA0[R/W]B,H,W *4 00000000_0000XXXX_XXXXXXXX_XXXXXXXX				DMAC
000204H	DMACB0[R/W]B,H,W 00000000_00000000_XXXXXXXX_XXXXXXXX				
000208H	DMACA1[R/W]B,H,W *4 00000000_0000XXXX_XXXXXXXX_XXXXXXXX				
00020CH	DMACB1[R/W]B,H,W 00000000_00000000_XXXXXXXX_XXXXXXXX				
000210H	DMACA2[R/W]B,H,W *4 00000000_0000XXXX_XXXXXXXX_XXXXXXXX				
000214H	DMACB2[R/W]B,H,W 00000000_00000000_XXXXXXXX_XXXXXXXX				
000218H	DMACA3[R/W]B,H,W *4 00000000_0000XXXX_XXXXXXXX_XXXXXXXX				
00021CH	DMACB3[R/W]B,H,W 00000000_00000000_XXXXXXXX_XXXXXXXX				
000220H	DMACA4[R/W]B,H,W *4 00000000_0000XXXX_XXXXXXXX_XXXXXXXX				
000224H	DMACB4[R/W]B,H,W 00000000_00000000_XXXXXXXX_XXXXXXXX				
000228H	————				
00022CH to 00023CH	————				Reserved
000240H	DMACR[R/W]B 0XX00000_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
000244H to 00027CH	————				Reserved
000280H	FRLR[R/W]B,H,W*2 ------01	————	————	————	Limit on F-bus RAM capacity

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000284H to 00038CH	————				Reserved
000390H	DRLR[R/W]B,H,W*2 ------01	————	————	————	Limit on D-bus RAM capacity
000394H to 0003ECH	————				Reserved
0003F0H	BSD0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				Bit search module
0003F4H	BSD1[R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
0003F8H	BSDC[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
0003FCH	BSRR[R] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000400H	DDRG[R/W]B*3 --000000	DDRH[R/W]B --000000	DDRI[R/W]B --000000	DDRJ[R/W]B*3 00000000	R-bus data direction register*3
000404H	DDRK[R/W]B 00000000	DDRL[R/W]B ------00	DDRM[R/W]B --000000	DDRN[R/W]B --000000	
000408H	DDRO[R/W]B 00000000	DDRP[R/W]B*3 ----0000	————		
00040CH	————				
000410H	PFRG[R/W]B*3 --00-00-	PFRH[R/W]B --00-00-	PFRI[R/W]B --00-00-	————	R-bus port function register*3
000414H	————	PFRL[R/W]B ------00	PFRM[R/W]B --00-00-	PFRN[R/W]B --000000	
000418H	PFRO[R/W]B 00000000	PFRP[R/W]B*3 ----0000	————		
00041CH	————				Reserved
000420H	PCRG[R/W]B*3 --000000	PCRH[R/W]B --000000	PCRI[R/W]B --000000	————	R-bus pull-up control register*3
000424H	————	————	PCRM[R/W]B --000000	PCRN[R/W]B --000000	
000428H	PCRO[R/W]B 00000000	PCRP[R/W]B*3 ----0000	————	————	
00042CH to 00043CH	————				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000440H	ICR00[R/W]B,H,W ---11111	ICR01[R/W]B,H,W ---11111	ICR02[R/W]B,H,W ---11111	ICR03[R/W]B,H,W ---11111	Interrupt controller unit
000444H	ICR04[R/W]B,H,W ---11111	ICR05[R/W]B,H,W ---11111	ICR06[R/W]B,H,W ---11111	ICR07[R/W]B,H,W ---11111	
000448H	ICR08[R/W]B,H,W ---11111	ICR09[R/W]B,H,W ---11111	ICR10[R/W]B,H,W ---11111	ICR11[R/W]B,H,W ---11111	
00044CH	ICR12[R/W]B,H,W ---11111	ICR13[R/W]B,H,W ---11111	ICR14[R/W]B,H,W ---11111	ICR15[R/W]B,H,W ---11111	
000450H	ICR16[R/W]B,H,W ---11111	ICR17[R/W]B,H,W ---11111	ICR18[R/W]B,H,W ---11111	ICR19[R/W]B,H,W ---11111	
000454H	ICR20[R/W]B,H,W ---11111	ICR21[R/W]B,H,W ---11111	ICR22[R/W]B,H,W ---11111	ICR23[R/W]B,H,W ---11111	
000458H	ICR24[R/W]B,H,W ---11111	ICR25[R/W]B,H,W ---11111	ICR26[R/W]B,H,W ---11111	ICR27[R/W]B,H,W ---11111	
00045CH	ICR28[R/W]B,H,W ---11111	ICR29[R/W]B,H,W ---11111	ICR30[R/W]B,H,W ---11111	ICR31[R/W]B,H,W ---11111	
000460H	ICR32[R/W]B,H,W ---11111	ICR33[R/W]B,H,W ---11111	ICR34[R/W]B,H,W ---11111	ICR35[R/W]B,H,W ---11111	
000464H	ICR36[R/W]B,H,W ---11111	ICR37[R/W]B,H,W ---11111	ICR38[R/W]B,H,W ---11111	ICR39[R/W]B,H,W ---11111	
000468H	ICR40[R/W]B,H,W ---11111	ICR41[R/W]B,H,W ---11111	ICR42[R/W]B,H,W ---11111	ICR43[R/W]B,H,W ---11111	
00046CH	ICR44[R/W]B,H,W ---11111	ICR45[R/W]B,H,W ---11111	ICR46[R/W]B,H,W ---11111	ICR47[R/W]B,H,W ---11111	
000470H to 00047CH	————				
000480H	RSRR[R/W]B,H,W 10000000	STCR[R/W]B,H,W 00110011	TBCR[R/W]B,H,W 00XXXX00	CTBR[W]B,H,W XXXXXXXX	Clock control unit
000484H	CLKR[R/W]B,H,W 00000000	WPR[W]B,H,W XXXXXXXX	DIVR0[R/W]B,H,W 00000011	DIVR1[R/W]B,H,W 00000000	
000488H	————		OSCCR[R/W]B XXXXXXX0	————	
00048CH	WPCR[R/W]B 00---000	————	————	————	Watch timer
000490H	OSCR[R/W]B 00---000	————	————	————	Main clock oscillation stabilization wait timer
000494H	RSTOP0[W]B 00000000	RSTOP1[W]B 00000000	RSTOP2[W]B 00000000	RSTOP3[W]B -----000	Peripheral stop control

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000498H	————	————	————	————	Reserved
00049CH to 0005FCH	————				Reserved
000600H	————	————	DDR2[R/W]B 00000000	DDR3[R/W]B 00000000	T-unit data direction register*3
000604H	DDR4[R/W]B 00000000	DDR5[R/W]B 00000000	DDR6[R/W]B 00000000	————	
000608H	DDR8[R/W]B --000000	DDR9[R/W]B ---00000	DDRA[R/W]B ----0000	DDRB[R/W]B*3 00000000	
00060CH	DDRC[R/W]B*3 -----000	————			
000610H	————	————	————	————	T-unit port function register*3
000614H	————	————	PFR6[R/W]B 11111111	————	
000618H	PFR8[R/W]B --1--0--	PFR9[R/W]B ---010-1	PFRA[R/W]B ----1111	PFRB1[R/W]B*3 00000000	
00061CH	PFRB2[R/W]B*3 00----00	PFRC[R/W]B*3 ---00000	————	————	
000620H	————	————	PCR2[R/W]B 00000000	PCR3[R/W]B 00000000	T-unit pull-up control register*3
000624H	PCR4[R/W]B 00000000	PCR5[R/W]B 00000000	PCR6[R/W]B 00000000	————	
000628H	PCR8[R/W]B --000000	PCR9[R/W]B 00000000	PCRA[R/W]B 00000000	PCRB[R/W]B*3 00000000	
00062CH	PCRC[R/W]B*3 -----000	————	————	————	
000630H to 00063CH	————				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000640H	ASR0[R/W]H,W 00000000_00000000		ACR0[R/W]B,H,W 1111XX00_00000000		T-unit
000644H	ASR1[R/W]H,W 00000000_00000000		ACR1[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000648H	ASR2[R/W]H,W 00000000_00000000		ACR2[R/W]B,H,W XXXXXXXX_XXXXXXXX		
00064CH	ASR3[R/W]H,W 00000000_00000000		ACR3[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000650H	ASR4[R/W]H,W 00000000_00000000		ACR4[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000654H	ASR5[R/W]H,W 00000000_00000000		ACR5[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000658H	ASR6[R/W]H,W 00000000_00000000		ACR6[R/W]B,H,W XXXXXXXX_XXXXXXXX		
00065CH	ASR7[R/W]H,W 00000000_00000000		ACR7[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000660H	AWR0[R/W]B,H,W 01111111_11111111		AWR1[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000664H	AWR2[R/W]B,H,W XXXXXXXX_XXXXXXXX		AWR3[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000668H	AWR4[R/W]B,H,W XXXXXXXX_XXXXXXXX		AWR5[R/W]B,H,W XXXXXXXX_XXXXXXXX		
00066CH	AWR6[R/W]B,H,W XXXXXXXX_XXXXXXXX		AWR7[R/W]B,H,W XXXXXXXX_XXXXXXXX		
000670H	————				
000674H	————				
000678H	IOWR0[R/W]B,H,W XXXXXXXX	IOWR1[R/W]B,H,W XXXXXXXX	IOWR2[R/W]B,H,W XXXXXXXX	————	
00067CH	————				
000680H	CSER[R/W]B,H,W 00000001	————	————	TCR[W]B,H,W 0000XXXX	
000684H to 0007F8H	————				Reserved
0007FCH	————	MODR[W] *5 XXXXXXXX	————	————	Mode register
000800H to 000AFCH	————				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000B00H	ESTS0[R/W] X0000000	ESTS1[R/W] XXXXXXXX	ESTS2[R] 1XXXXXXX	———————	DSU (EVA chip only)
000B04H	ECTL0[R/W] 0X000000	ECTL1[R/W] 00000000	ECTL2[W] 000X0000	ECTL3[R/W] 00X00X11	
000B08H	ECNT0[W] XXXXXXXX	ECNT1[W] XXXXXXXX	EUSA[W] XXX00000	EDTC[W] 0000XXXX	
000B0CH	EWPT[R] 00000000_00000000		———————		
000B10H	EDTR0[W] XXXXXXXX_XXXXXXXX		EDTR1[W] XXXXXXXX_XXXXXXXX		
000B14H to 000B1CH	———————				
000B20H	EIA0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B24H	EIA1[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B28H	EIA2[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B2CH	EIA3[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B30H	EIA4[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B34H	EIA5[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B38H	EIA6[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B3CH	EIA7[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B40H	EDTA[R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B44H	EDTM[R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B48H	EOA0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B4CH	EOA1[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B50H	EPCR[R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000B54H	EPSR[R/W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DSU (EVA chip only)
000B58H	EIAM0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B5CH	EIAM1[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B60H	EOAM0/EODM0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B64H	EOAM1/EODM1[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B68H	EOD0[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B6CH	EOD1[W] XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
000B70H to 000BFCH	————				Reserved
000C00H	Test register (access is not allowed.)				Interrupt controller unit
000C04H to 000C14H	Test register (access is not allowed.)				R-bus test
000C18H to 000FFCH	————				Reserved
001000H	DMASA0[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
001004H	DMADA0[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001008H	DMASA1[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00100CH	DMADA1[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001010H	DMASA2[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001014H	DMADA2[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001018H	DMASA3[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00101CH	DMADA3[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
001020H	DMASA4[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
001024H	DMADA4[R/W]W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001028H to 001FFCH	————				Reserved
007000H	FLCR[R/W] 0110X000	————	————	————	Flash memory
007004H	FLWC[R/W] 00010011	————	————	————	
007008H	————	————	————	————	
00700CH	————	————	————	————	
007010H	————	————	————	————	
007014H to 0070FFH	————				Reserved

*1 : This is a test register. Access is disabled.

*2 : The available area of internal RAM is restricted immediately after a reset is released. This setting therefore needs to be changed before using the internal RAM.
In addition, at least one NOP instruction is required immediately after overwriting the setting for the available RAM area.

*3 : This register does not exist on the MB91F353A/353A/352A/351A. Access is disabled.

*4 : The 16 low-order bits (DTC [15 : 0]) of DMACA0 to DMACA4 cannot be byte-accessed.

*5 : This register is accessed by the mode vector fetch. It cannot be accessed during normal operation.

3. Vector table

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	Resource number
	10	16				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
System reserved	10	0A	—	3D4$_H$	000FFFD4$_H$	—
System reserved	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	15 (F$_H$) fixed	3C0$_H$	000FFFC0$_H$	—
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$	6
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$	7
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$	11
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$	—
External interrupt 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	8
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	9
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	10
UART0 (Reception completed)	27	1B	ICR11	390$_H$	000FFF90$_H$	0
UART1 (Reception completed)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	1
UART2 (Reception completed)	29	1D	ICR13	388$_H$	000FFF88$_H$	2
UART0 (Transmission completed)	30	1E	ICR14	384$_H$	000FFF84$_H$	3
UART1 (Transmission completed)	31	1F	ICR15	380$_H$	000FFF80$_H$	4
UART2 (Transmission completed)	32	20	ICR16	37C$_H$	000FFF7C$_H$	5
DMAC0 (end, error)	33	21	ICR17	378$_H$	000FFF78$_H$	—
DMAC1 (end, error)	34	22	ICR18	374$_H$	000FFF74$_H$	—

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	Resource number
	10	16				
DMAC2 (end, error)	35	23	ICR19	370H	000FFF70H	—
DMAC3 (end, error)	36	24	ICR20	36CH	000FFF6CH	—
DMAC4 (end, error)	37	25	ICR21	368H	000FFF68H	—
A/D	38	26	ICR22	364H	000FFF64H	15
I^2C	39	27	ICR23	360H	000FFF60H	—
System reserved	40	28	ICR24	35CH	000FFF5CH	—
System reserved	41	29	ICR25	358H	000FFF58H	12
SIO 6	42	2A	ICR26	354H	000FFF54H	13
SIO 7	43	2B	ICR27	350H	000FFF50H	14
UART3 (Reception completed)	44	2C	ICR28	34CH	000FFF4CH	—
UART3 (Transmission completed)	45	2D	ICR29	348H	000FFF48H	—
Reload timer 3/main oscillation stabilization wait timer	46	2E	ICR30	344H	000FFF44H	—
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H	—
System reserved	48	30	ICR32	33CH	000FFF3CH	—
Watch counter	49	31	ICR33	338H	000FFF38H	—
U/D Counter 0	50	32	ICR34	334H	000FFF34H	—
System reserved	51	33	ICR35	330H	000FFF30H	—
PPG 0	52	34	ICR36	32CH	000FFF2CH	—
PPG 2	53	35	ICR37	328H	000FFF28H	—
PPG 4	54	36	ICR38	324H	000FFF24H	—
16-bit free-run timer	55	37	ICR39	320H	000FFF20H	—
ICU 0 (capture)	56	38	ICR40	31CH	000FFF1CH	—
ICU 1 (capture)	57	39	ICR41	318H	000FFF18H	—
ICU 2/3 (capture)	58	3A	ICR42	314H	000FFF14H	—
OCU 0 (match)	59	3B	ICR43	310H	000FFF10H	—
OCU 2 (match)	60	3C	ICR44	30CH	000FFF0CH	—
System reserved	61	3D	ICR45	308H	000FFF08H	—
System reserved	62	3E	ICR46	304H	000FFF04H	—
Interrupt delay source bit	63	3F	ICR47	300H	000FFF00H	—
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH	—
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H	—
System reserved	66	42	—	2F4H	000FFEF4H	—
System reserved	67	43	—	2F0H	000FFEF0H	—
System reserved	68	44	—	2ECH	000FFEECH	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address	Resource number
	10	16				
System reserved	69	45	—	2E8H	000FFEE8H	—
System reserved	70	46	—	2E4H	000FFEE4H	—
System reserved	71	47	—	2E0H	000FFEE0H	—
System reserved	72	48	—	2DCH	000FFEDCH	—
System reserved	73	49	—	2D8H	000FFED8H	—
System reserved	74	4A	—	2D4H	000FFED4H	—
System reserved	75	4B	—	2D0H	000FFED0H	—
System reserved	76	4C	—	2CCH	000FFECCH	—
System reserved	77	4D	—	2C8H	000FFEC8H	—
System reserved	78	4E	—	2C4H	000FFEC4H	—
System reserved	79	4F	—	2C0H	000FFEC0H	—
Used by INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H	—

■ PERIPHERAL RESOURCES

1. Interrupt Controller

(1) Description

The interrupt controller manages interrupt reception and arbitration.

Hardware configuration

This module consists of the following components :

- ICR register
- Interrupt priority determination circuit
- Interrupt level and interrupt number (vector) generator
- HOLD request removal request generator

• Main functions

This module has the following major functions :

- Detect NMI and interrupt requests
- Prioritize interrupts (according to level and number)
- Notify interrupt level of selected interrupt request (to CPU)
- Notify interrupt number of selected interrupt request (to CPU)
- Request (to the CPU) to return from stop mode in response to an NMI or interrupt request with interrupt level other than "11111_B"
- Issue requests to the bus master to cancel HOLD requests

(2) Register list

Interrupt Control Register (ICR)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ICR00	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR01	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR02	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR03	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR04	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR05	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR06	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR07	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR08	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR09	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR10	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR11	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR12	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR13	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR14	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR15	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR16	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR17	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR18	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR19	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR20	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR21	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR22	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR23	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR24	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR25	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR26	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR27	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR28	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR29	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR30	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR31	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0

(Continued)

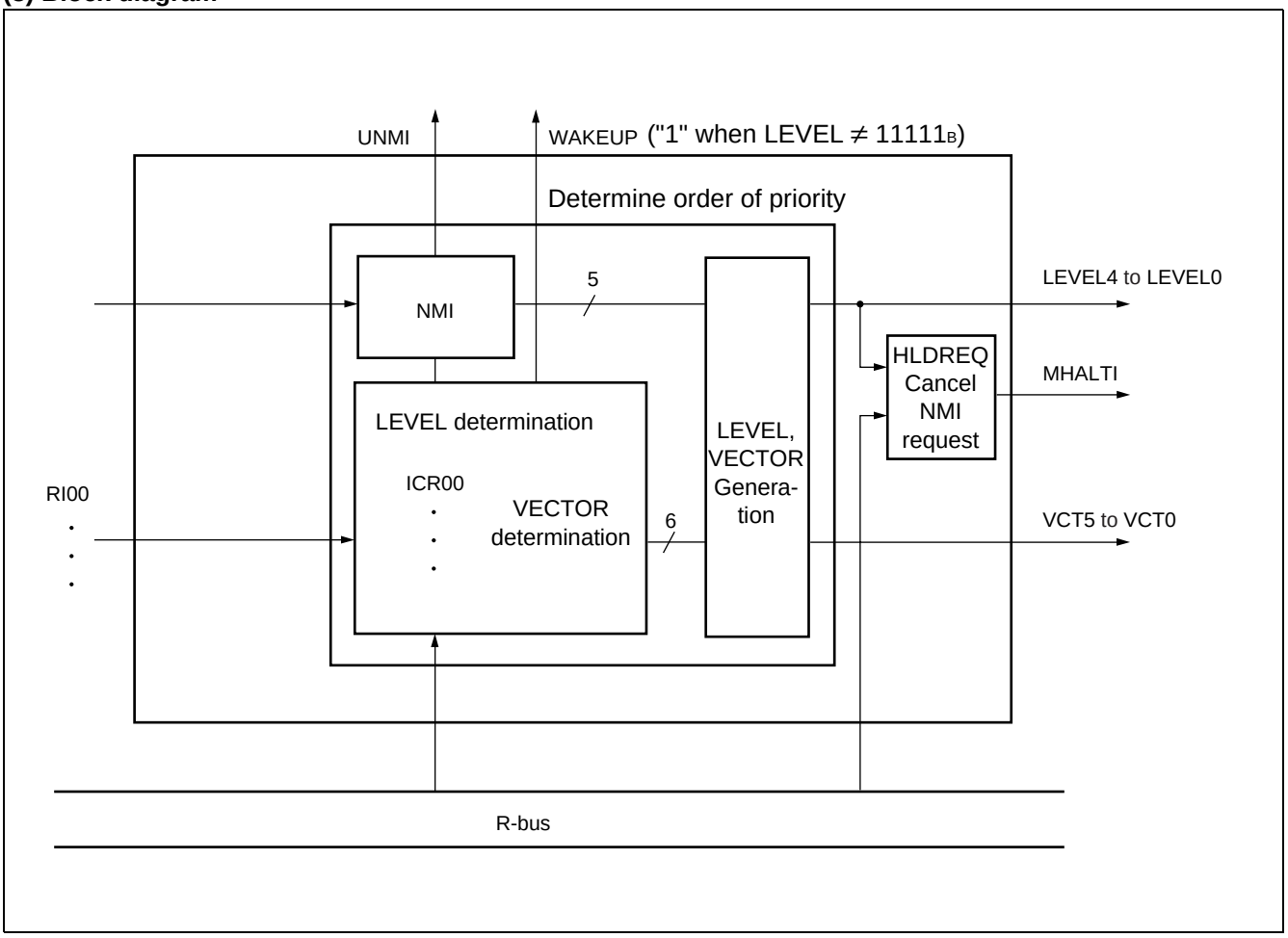
(Continued)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ICR32	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR33	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR34	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR35	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR36	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR37	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR38	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR39	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR40	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR41	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR42	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR43	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR44	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR45	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR46	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0
ICR47	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0

Hold request cancel request register (HRCL)

HRCL	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0

(3) Block diagram



2. External Interrupt/NMI Control

(1) Description

The external interrupt control unit is the block that controls external interrupt requests input to $\overline{\text{NMI}}$ and INT0 to INT15. The level that is detected as a request can be selected from “H”, “L”, rising edge, or falling edge (except for NMI).

Note : The MB91F353A/353A/352A/351A does not have INT8 to INT15.

(2) Register list

External interrupt enable register (ENIR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interrupt request register (EIRR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

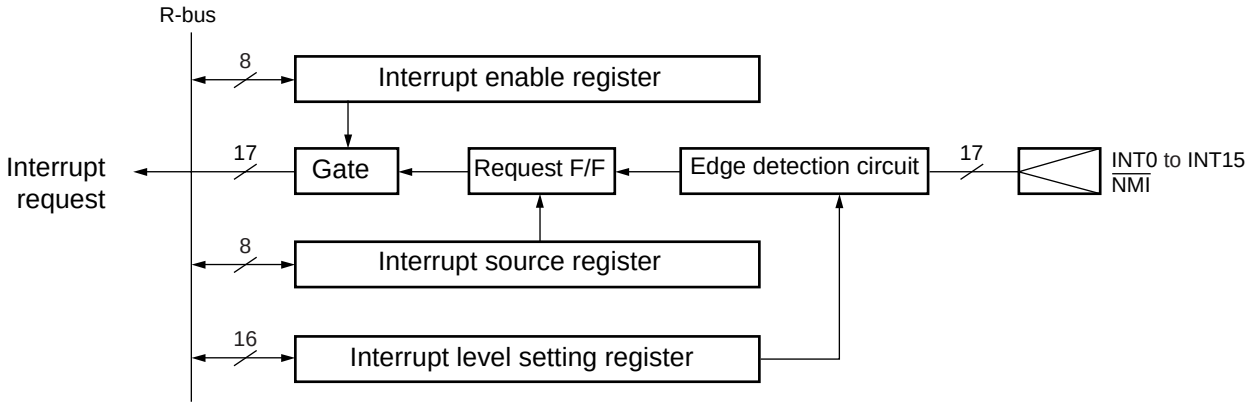
Request level setting register (ELVR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

The above registers (for 8 channels) are available in 2 sets; there are a total of 16 channels.

(3) Block diagram



3. REALOS-related Hardware

REALOS-related hardware is used by the real-time OS. Therefore, it cannot be used by user programs when REALOS is used.

• Delay interrupt module

(1) Description

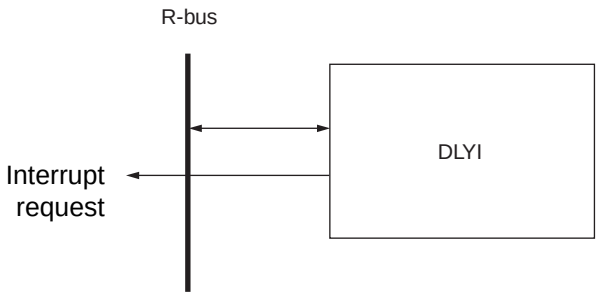
The delayed interrupt module generates a task switching interrupt.
This module enables software to issue or cancel an interrupt request to the CPU.

(2) Register list

Delayed Interrupt Control Register (DICR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	—	—	DLYI

(3) Block diagram

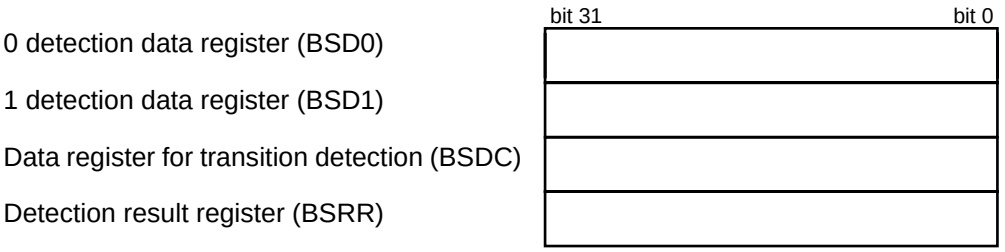


• **Bit Search Module**

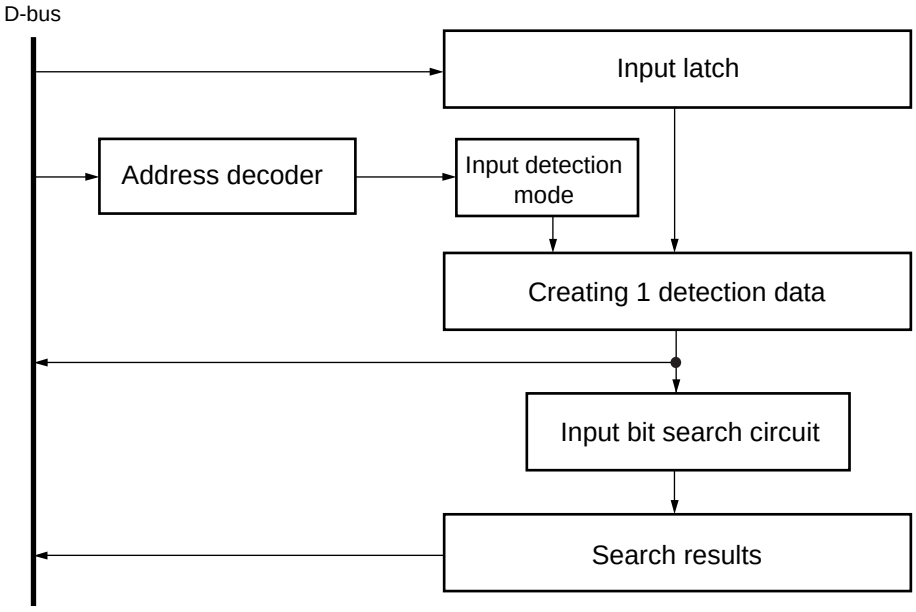
(1) Description

The bit search module searches data written to an input register for “0”, “1”, or a change point and returns the detected bit position.

(2) Register list



(3) Block diagram



4. 8/16-bit Up/Down Counter

(1) Description

This block is the up/down counter/timer consisting of six event input pins, two 8-bit up/down counter, two 8-bit reload/compare registers, and their control circuit.
The MB91F355A/F356B/F357B/355A/354A/V350A contains 2 channels of 8-bit up/down counter in this block.
The MB91F353A/353A/352A/351A contains 1 channel of 8-bit up/down counter in this block. It is not possible to use in 16-bit mode.
This module has the following features.

- 8-bit count register enabling counting from (0)d to (255)d
  (enabling counting from (0)d to (65535)d in 16 bits × 1 operation mode)
- Four different count modes available with selectable count clocks

  Count mode
  - Timer mode
  - Up/down count mode
  - Phase difference count mode (2 Multiplication)
  - Phase difference count mode (4 Multiplication)

- In timer mode, the ability to select the count clock input to use from among two internal clock circuits

  Count clock (When operating at 25 MHz)
  - 80 ns (12.5 MHz : Frequency division by 2)
  - 320 ns (3.125 MHz : Frequency division by 8)

- In up/down count mode, the ability to select the edge detection of the external pin input signals

  Detection edge
  - Falling edge detection
  - Rising edge detection
  - Detection at rising edge, falling edge, or both edges
  - Edge detection disabled

- The phase difference count mode is suitable for counting encoders such as motor encoders, and facilitates to count the angle of revolution and number of revolutions to a high precision by inputting the A phase, B phase, and Z phase outputs from the encoder
- ZIN pin has two selectable functions (valid in all modes)

  ZIN pin
  - Counter clear function
  - Gate function

- Compare and reload functions that can be used separately or in combination. When both functions are used in combination, up/down counting can be performed at an arbitrary width.

  Compare/reload function
  - Compare function (output interrupt request on compare match)
  - Compare function (output interrupt request and clear counter on compare match)
  - Reload function (output interrupt request and reload on underflow)
  - Compare/reload function (output interrupt request and clear counter on compare match; output interrupt request and reload on underflow)
  - Compare/reload disabled

- Count direction flag used to identify the preceding count direction
- Capable of independently controlling the generation of interrupts for compare match, reload (underflow), overflow, or on count direction change

(2) Register list

- **Up/down count register (UDCR)**

Up/down count register ch.0 (UDCR0)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D07	D06	D05	D04	D03	D02	D01	D00

Up/down count register ch.1 (UDCR1)*

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
D15	D14	D13	D12	D11	D10	D09	D08

- **Reload compare register (RCR)**

Reload compare register ch.0 (RCR0)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D07	D06	D05	D04	D03	D02	D01	D00

Reload compare register ch.1 (RCR1)*

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
D15	D14	D13	D12	D11	D10	D09	D08

- **Counter status register (CSR)**

Counter status register ch.0, ch.1 (CSR0, CSR1*)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0

- **Counter control register (CCRL)**

Counter control register ch.0, ch.1 (CCRL0, CCRL1*)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0

- **Counter control register (CCRH)**

Counter control register ch.0 (CCRH0)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

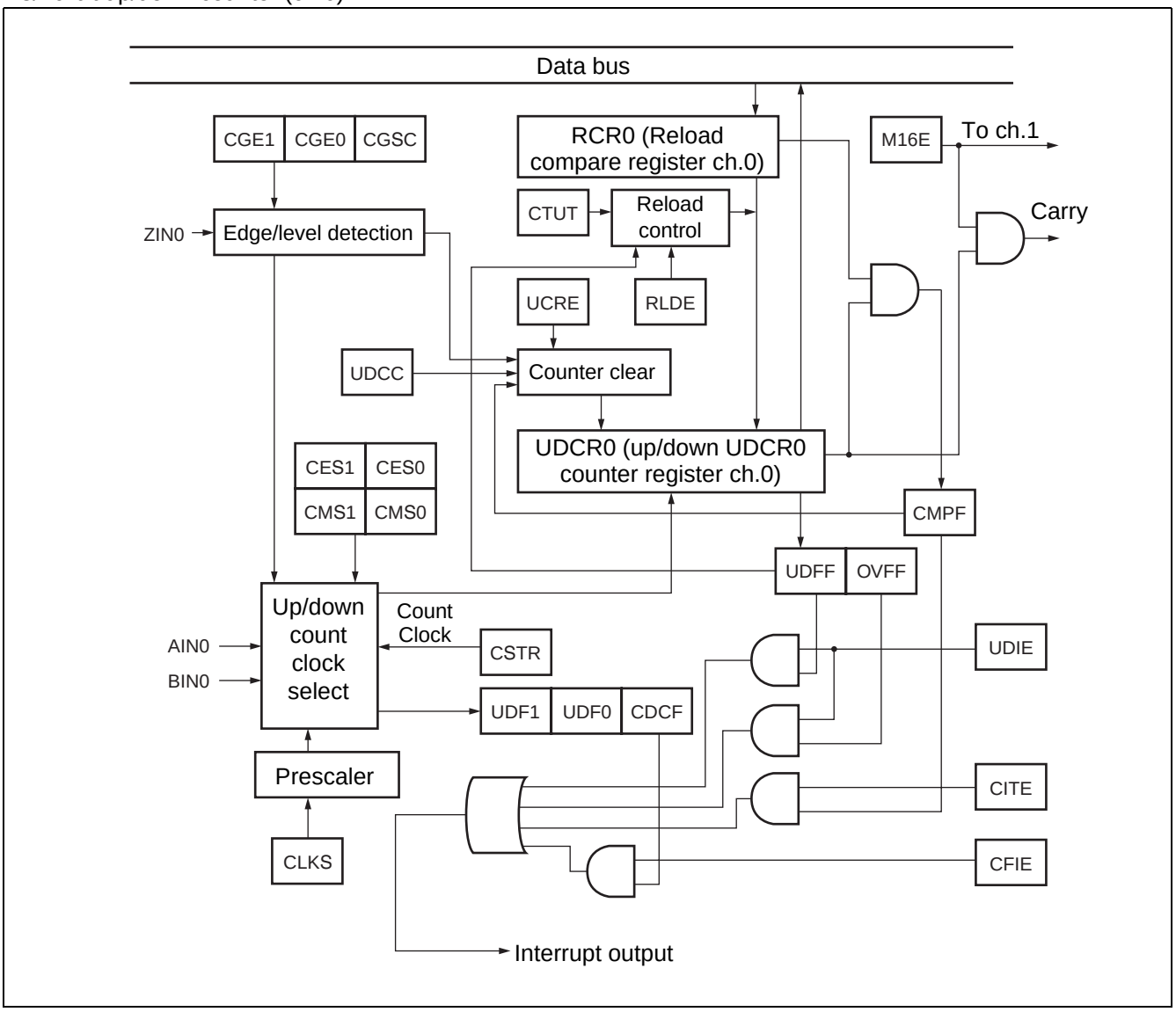
- **Counter control register ch.1 (CCRH1)***

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
Reserved	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

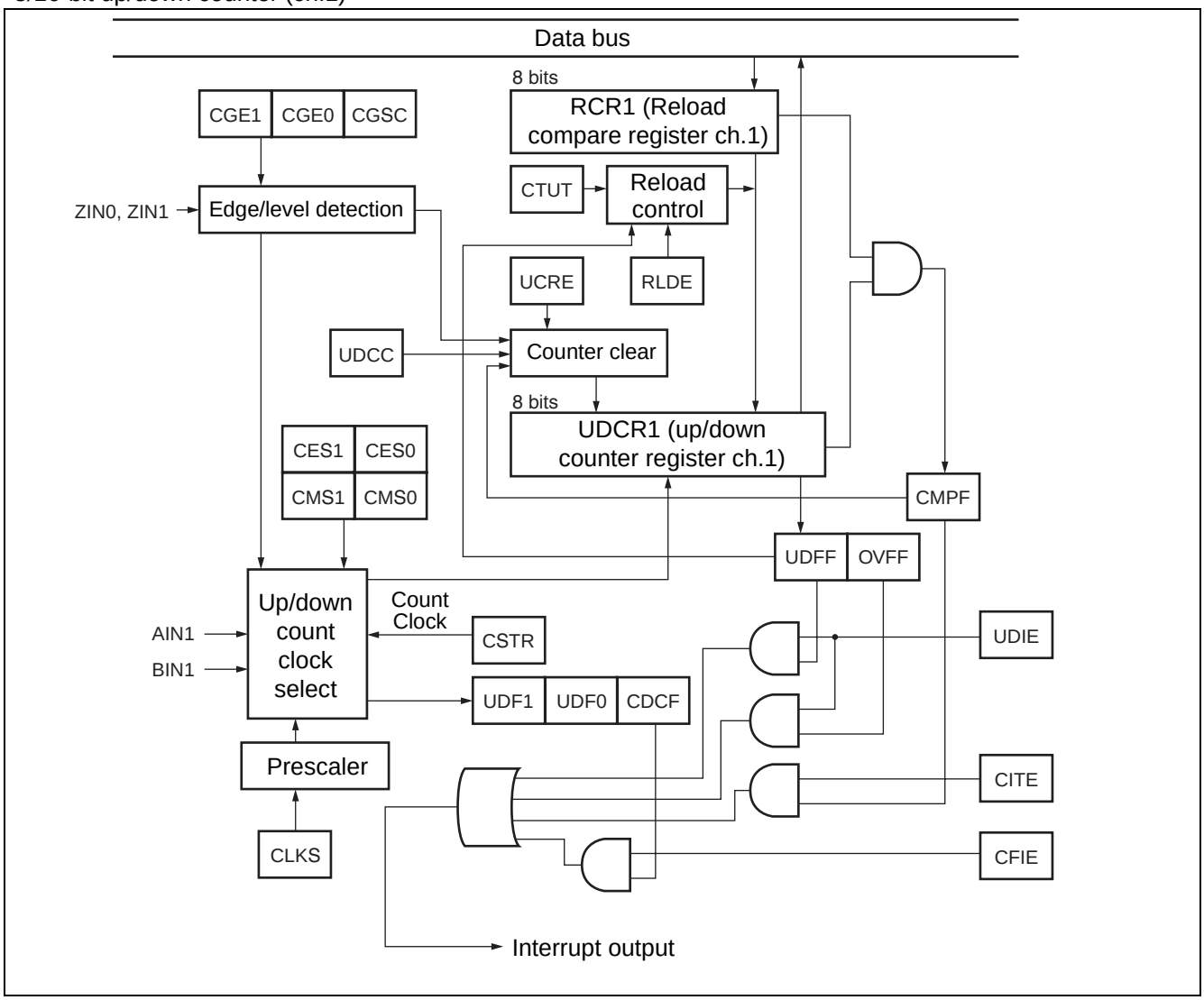
* : Access to the UDCR1, RCR1, CSR1, CCRL1, CCRH1 registers is prohibited on the MB91F353A/353A/352A/351A.

(3) Block diagram

• 8/16-bit up/down counter (ch.0)



•8/16-bit up/down counter (ch.1)



5. 16-bit Reload Timer

(1) Description

The 16-bit timer consists of a 16-bit down counter, 16-bit reload register, internal clock, clock generation prescaler, and control register.
The clock source can be selected from among three internal clocks (prepared by frequency dividing the machine clock by 2/8/32, and also by 64/128 only for ch.3) and an external event.
The interrupt can be used to initiate a DMA transfer.
The MB91F353A/353A/352A/351A does not have timer outputs (TOT0 to TOT3).
This timer has 4 built-in channels.

(2) Register list

Control status register (TMCSR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
—	—	Reserved	CSL2	CSL1	CSL0	Reserved	Reserved
	(ch.3 only)						

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	—	OUTL	RELD	INTE	UF	CNTE	TRG

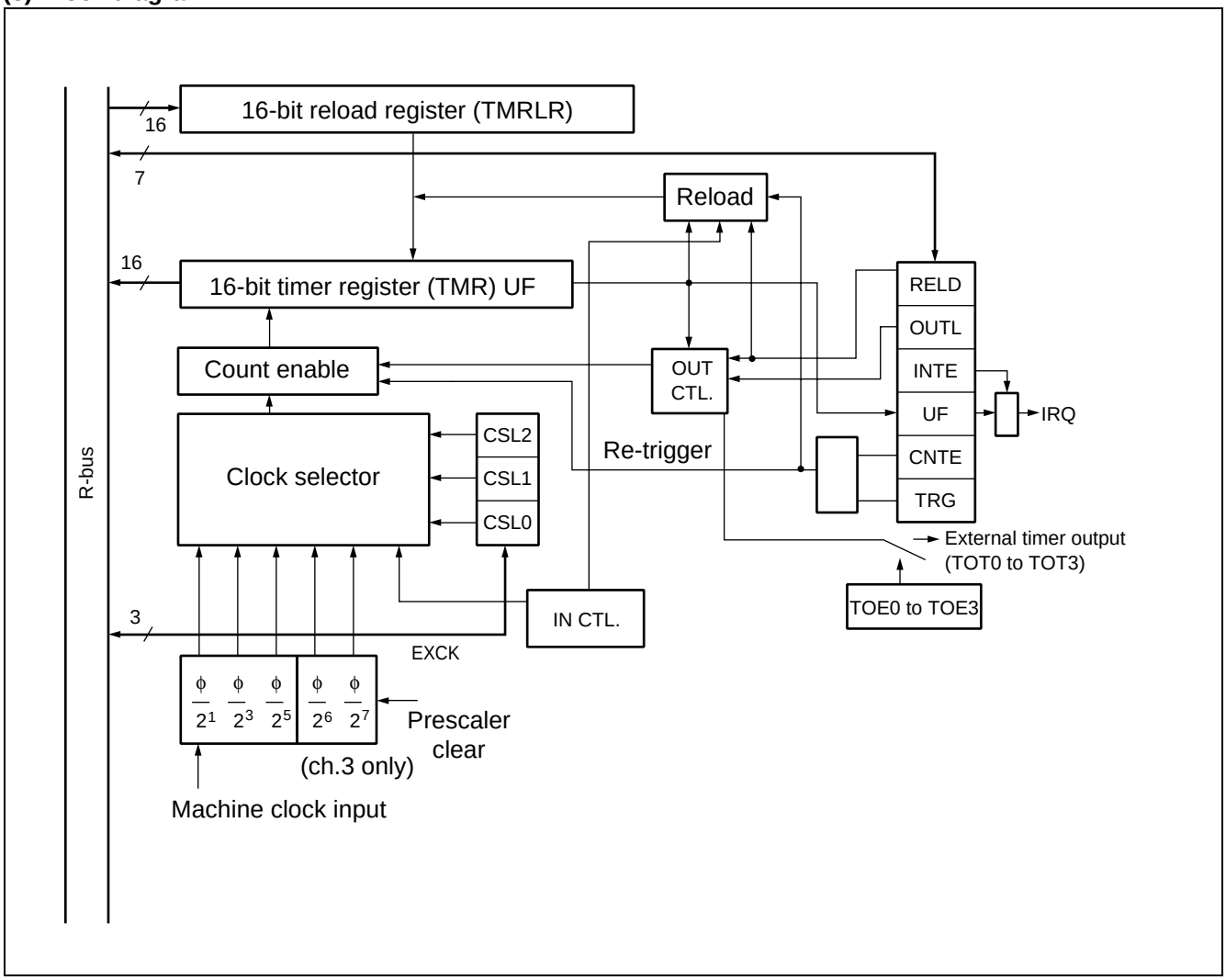
16-bit timer register (TMR)

bit 15							bit 0

16-bit reload register (TMRLR)

bit 15							bit 0

(3) Block diagram



Note : The MB91F353A/353A/352A/351A does not have external timer outputs (TOT0 to TOT3).

6. PPG (Programmable Pulse Generator)

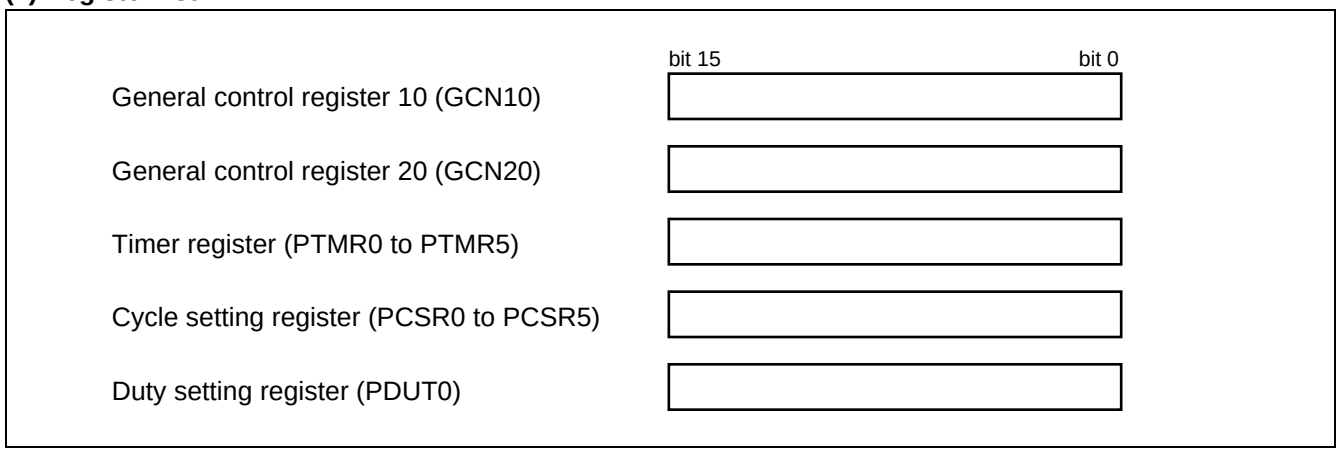
The PPG can efficiently output highly precise PWM wave forms.
The MB91F353A/353A/352A/351A contains 3 channels of PPG timer.
The MB91F355A/F356B/F357B/355A/354A/V350A contains 6 channels of PPG timer.

(1) Description

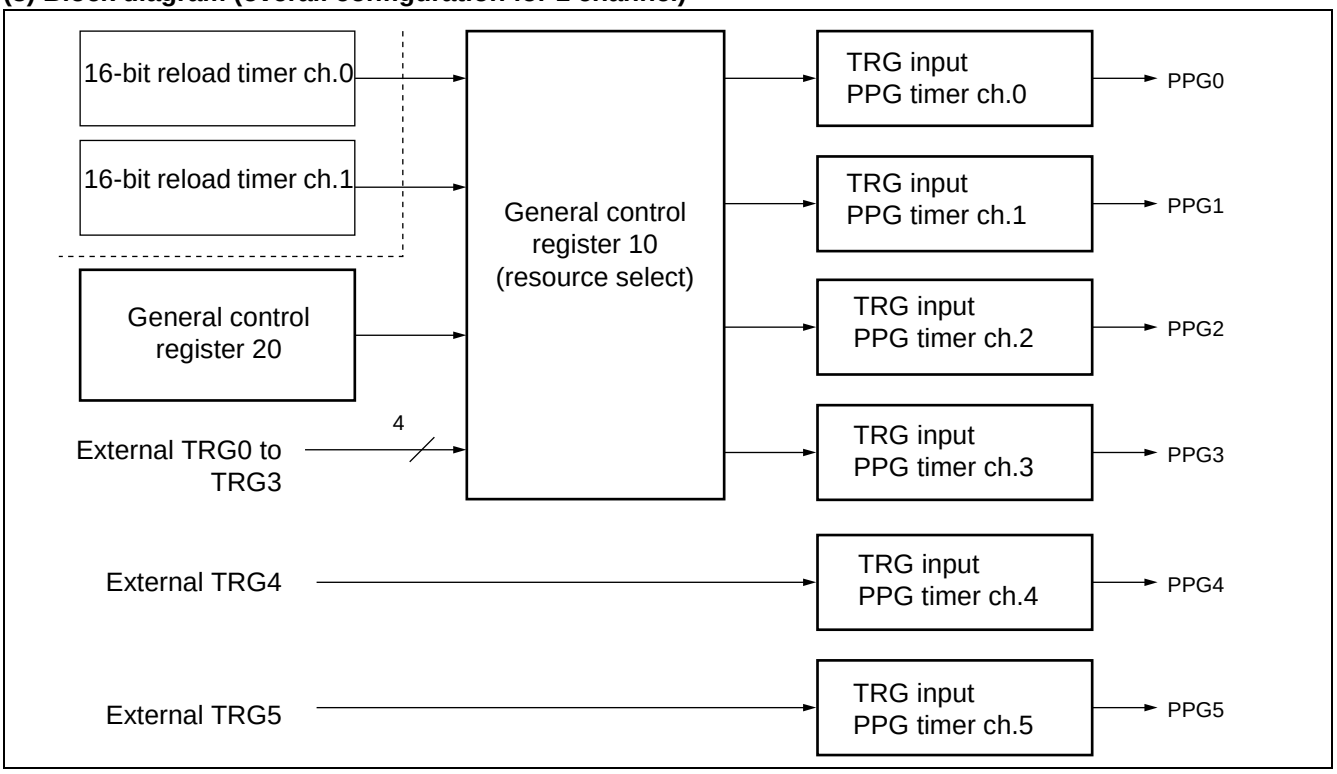
Each channel consists of a 16-bit down counter, 16-bit data register with cycle setting buffer, 16-bit compare register with duty ratio setting buffer, and pin control unit.
The count clocks for the 16-bit down counter can be selected from the following 4 types : (peripheral clock ϕ, ϕ/4, ϕ/16, ϕ/64)
The counter is initialized to "FFFF$_H$" at a reset or counter borrow.
PPG outputs (PPG0 to PPG5) are provided for each channel.

Note : The MB91F353A/353A/352A/351A contains 3 channels of PPG outputs PPG (0, 2, 4). There is no PPG (1, 3, 5).

(2) Register list



(3) Block diagram (overall configuration for 1 channel)



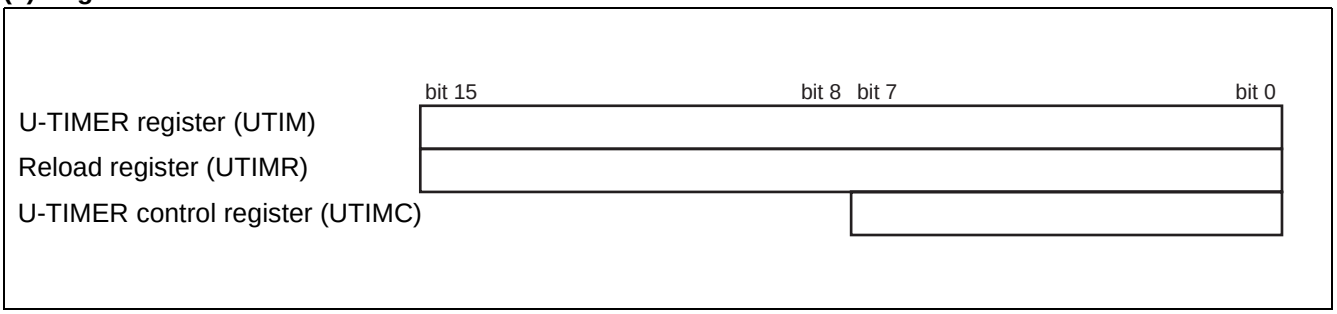
Note : The MB91F353A/353A/352A/351A does not have PPG1, PPG3, PPG5 and external TRG5.

7. U-TIMER (16-bit timer for UART baud rate generation)

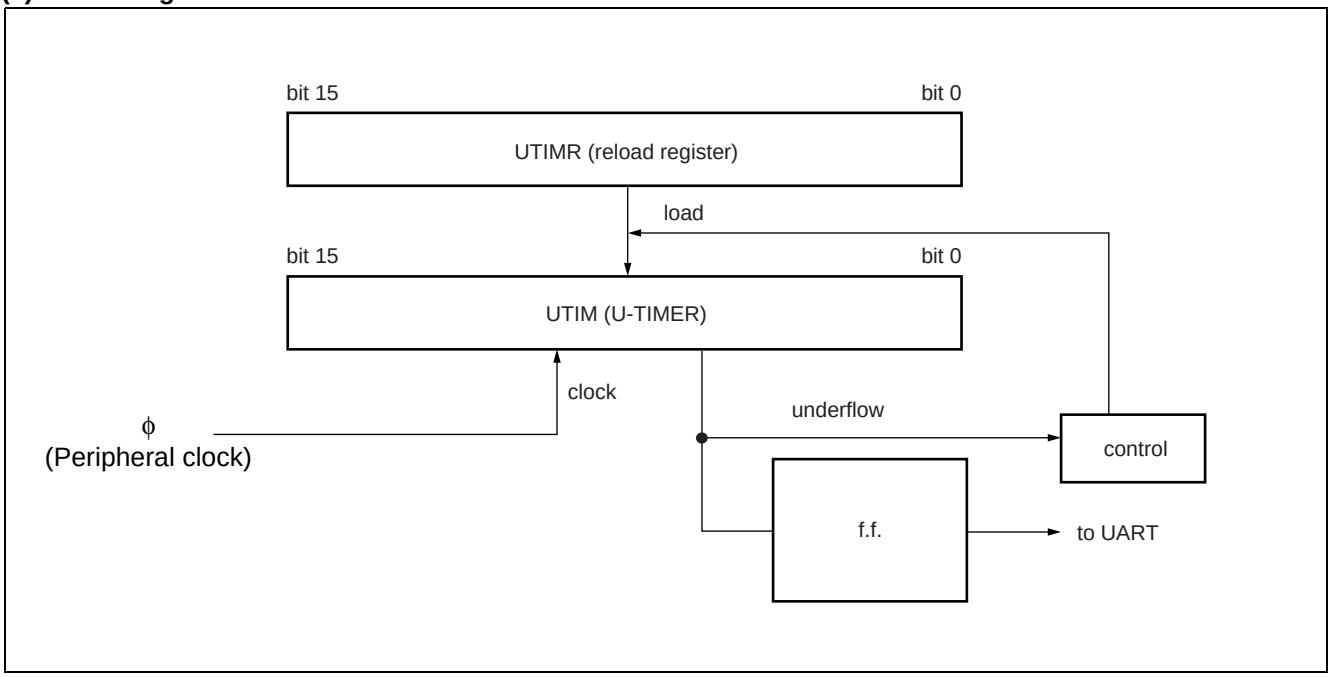
(1) Description

The U-TIMER is a 16-bit timer for generating the baud rate for the UART. An arbitrary baud rate can be set depending on the combination of the chip operating frequency and U-TIMER reload value.
The MB91F353A/353A/352A/351A contains 4 channels of this timer.
The MB91F355A/F356B/F357B/355A/354A/V350A contains 5 channels of this timer.

(2) Register list



(3) Block diagram



8. UART

(1) Description

The UART is a serial I/O port for asynchronous (start-stop) or CLK synchronous communication. This module has the features listed below.
The MB91F353A/353A/352A/351A contains 4 channels of UART.
The MB91F355A/F356B/F357B/355A/354A/V350A contains 5 channels of UART.

- Full duplex double buffer
- Asynchronous (start-stop synchronized) or CLK synchronized transmission
- Supports multi-processor mode
- Completely programmable baud rate.
  Arbitrary baud rate set by built-in timer (Refer to the section for "U-timer".)
- Variable baud rate can be input from an external clock.
- Error detection functions(parity, framing, overrun)
- Transmission signal format is NRZ
- UART (ch.0 to ch.2) can start DMA transfers using interrupts (ch.3 and ch.4 cannot start DMA transfers).
- Capable of clearing DMAC interrupt source by writing to DRCL register

(2) Register list

Serial input register/serial output register (SIDR/SODR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D7	D6	D5	D4	D3	D2	D1	D0

Serial status register (SSR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE

Serial mode register (SMR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MD1	MD0	—	—	CS0	—	—	—

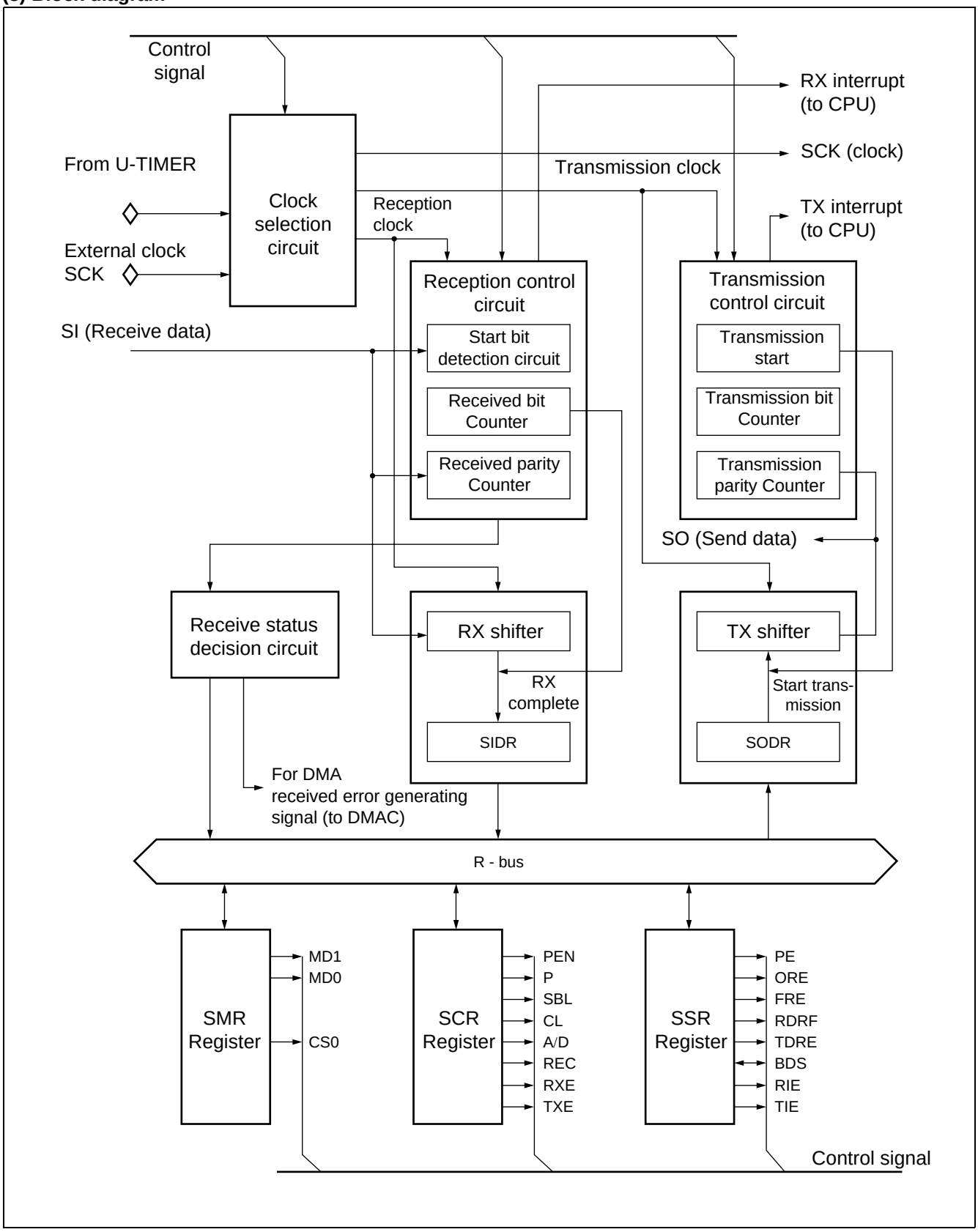
Serial control register (SCR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

DRCL register (DRCL)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	—	—	—

(3) Block diagram



9. Extended I/O serial interface (SIO)

(1) Description

This block is an 8-bit × 1 channel serial I/O interface that allows data transfer using clock synchronization.
LSB-first or MSB-first transfer mode can be selected for data transfer.
The MB91F353A/353A/352A/351A contains 2 channels of this SIO.
The MB91F355A/F356B/F357B/355A/354A/V350A contains 3 channels of this SIO.

The serial I/O interface operates in 2 modes :

- Internal shift clock mode : Data is transferred synchronized with the internal clock.
- External shift clock mode : Data is transferred synchronized with a clock supplied via the external pin (SCK). In this mode, data can also be transferred using CPU instructions by operating the general-purpose port that shares the external pin (SCK) .

(2) Register list

Serial mode control status register (SMCS)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	MODE	BDS	—	—

SIO test register (SES)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
—	—	—	—	—	—	TST1	TST0

SDR (Serial Data Register) (SDR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D7	D6	D5	D4	D3	D2	D1	D0

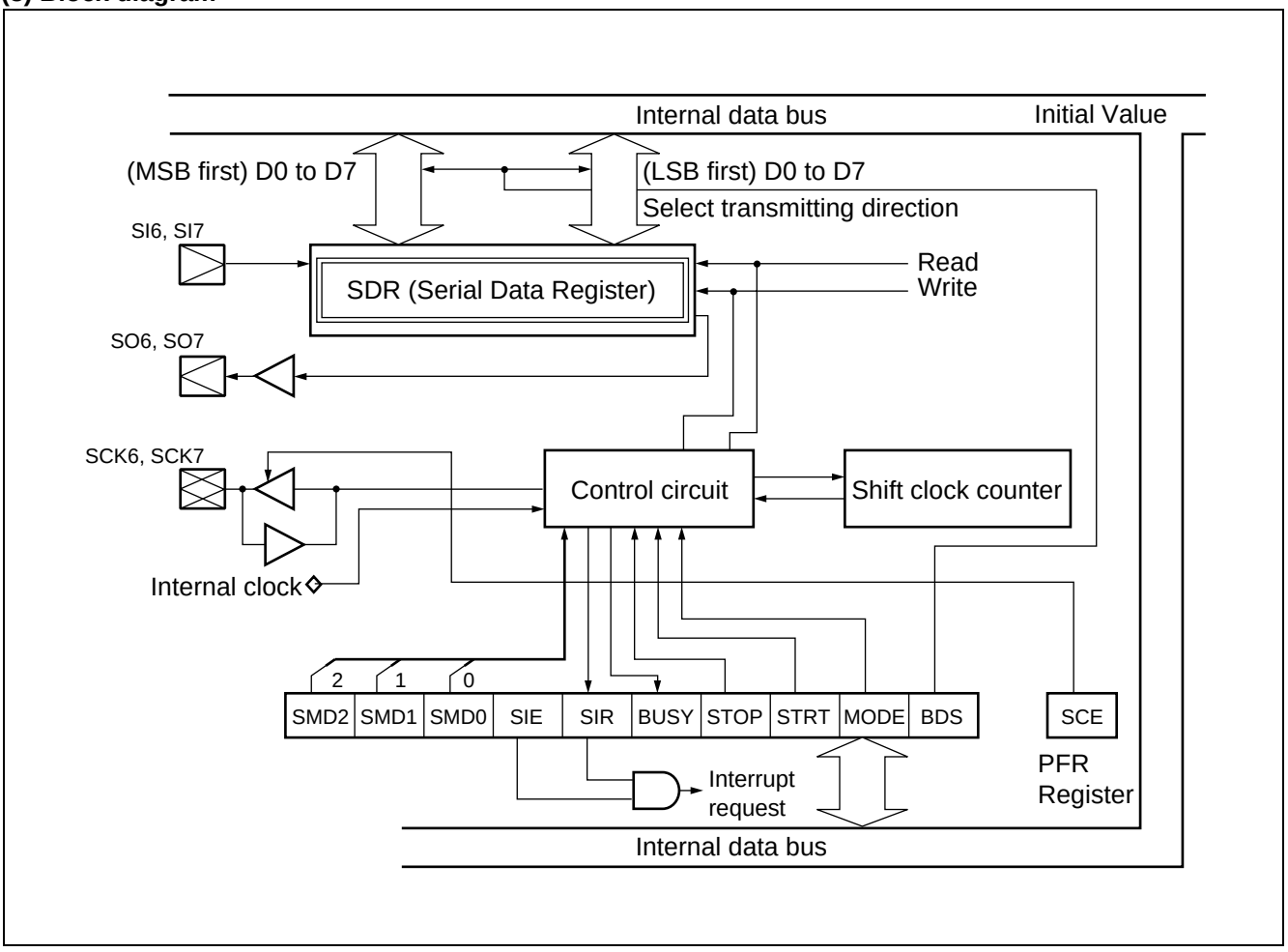
SIO prescaler control register (CDCR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
MD	—	—	—	DIV3	DIV2	DIV1	DIV0

DMAC interrupt source clear register (SRCL)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	—	—	—

(3) Block diagram



10. 16-bit free-run timer

(1) Description

The 16-bit free-run timer consists of a 16-bit up counter, control register, and status register. The count values of this timer are used as the base timer for the output compare and input capture modules.

- Four count clock frequencies are available.
- An interrupt can be generated on counter overflow.
- The counter can be initialized upon a match with compare register 0 of the output compare unit, depending on the mode.

(2) Register list

Timer data register (upper) (TCDT)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
T15	T14	T13	T12	T11	T10	T09	T08

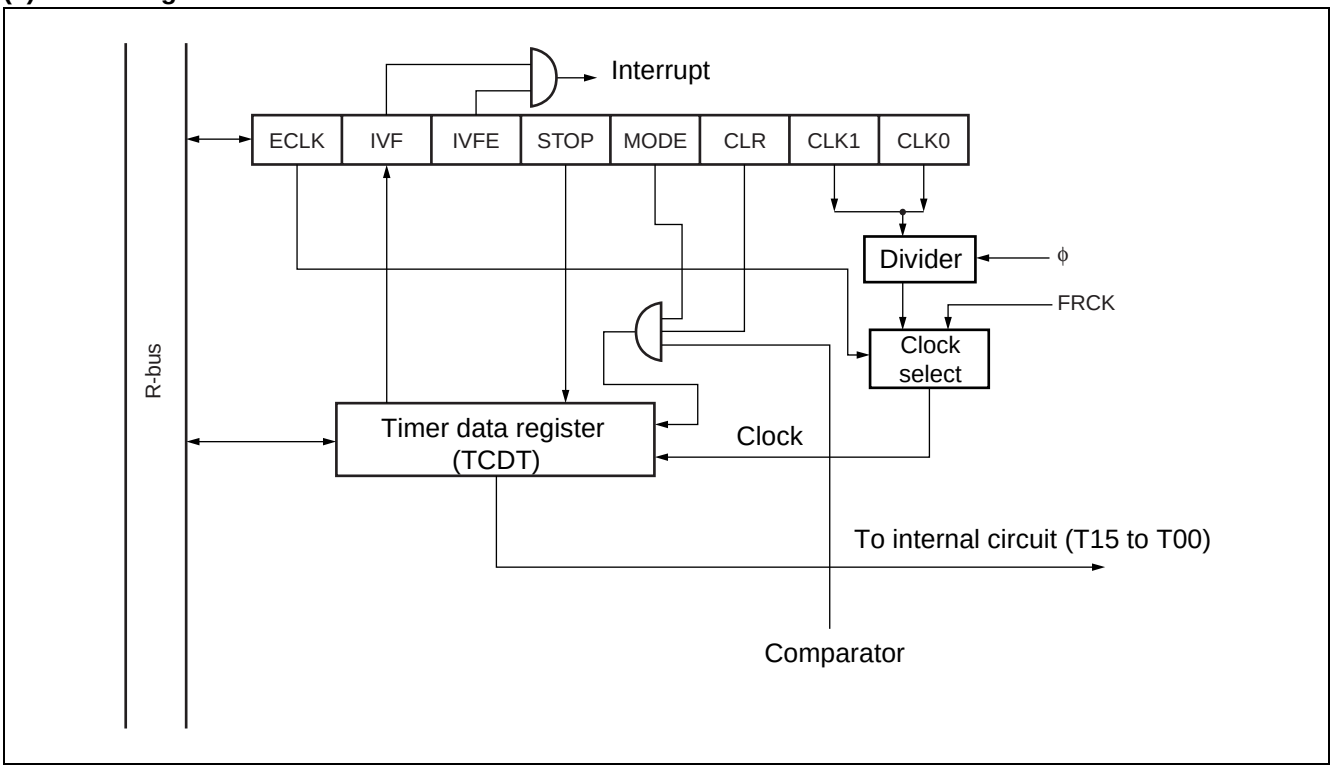
Timer data register (lower) (TCDT)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
T07	T06	T05	T04	T03	T02	T01	T00

Timer control status register (lower) (TCCS)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ECLK	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0

(3) Block diagram



11. Input Capture

(1) Description

This module detects the rising or falling edge or both edges of an external input signal and then, stores the value of the 16-bit free-run timer in a register. In addition, the module can generate an interrupt upon detection of an edge.
The input capture module consists of input capture data registers and a control register.
Each input capture unit has a corresponding external input pin.

- The detection edge of the external input can be selected from among 3 types.
  Rising edge
  Falling edge
  Both edges
- An interrupt can be generated upon detection of a valid edge in the external input.

(2) Register list

Input capture data register (upper) (IPCP)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08

Input capture data register (lower) (IPCP)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00

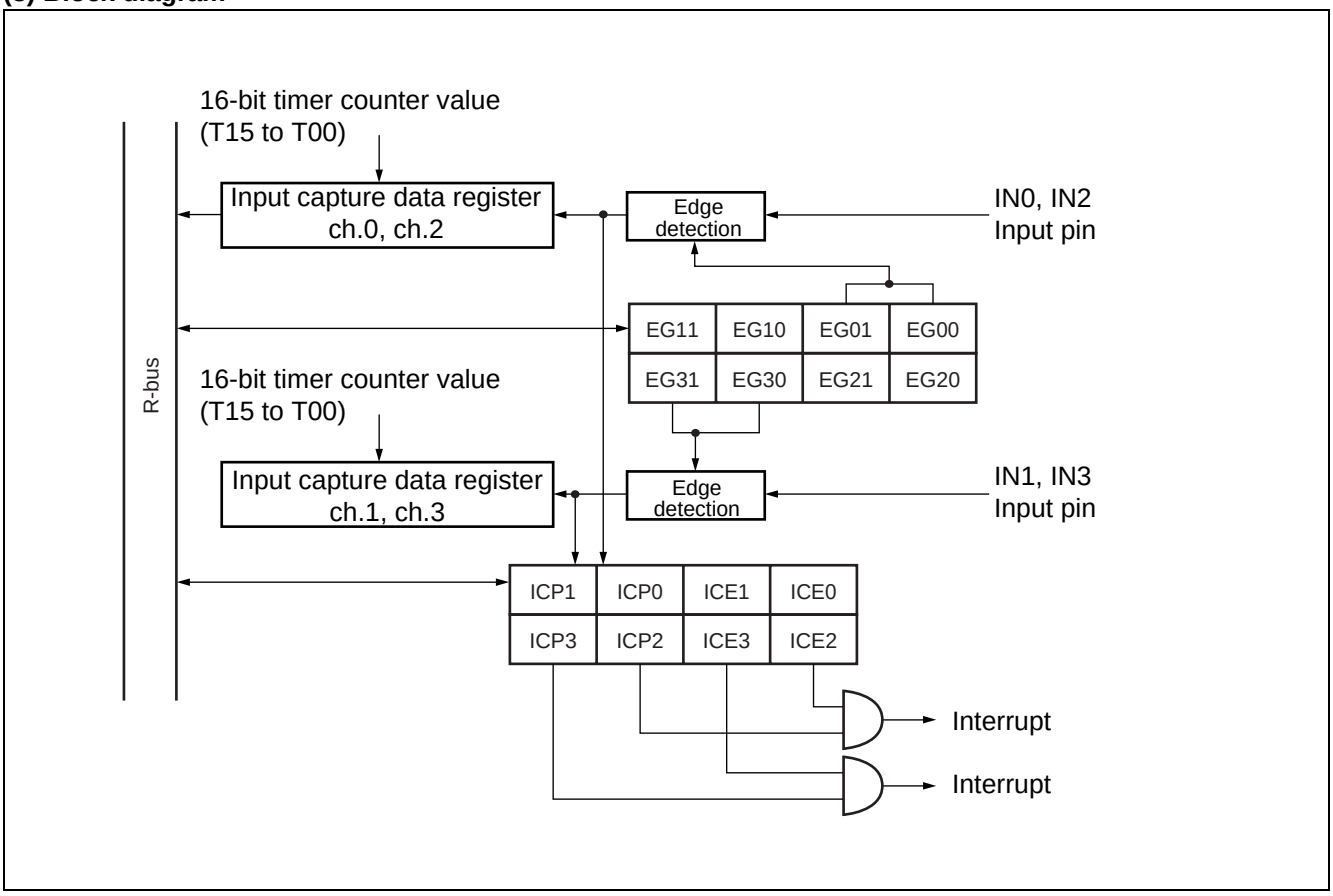
Input capture control register (ICS23)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20

Input capture control register (ICS01)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00

(3) Block diagram



12. Output Compare

(1) Description

The output compare module consists of a 16-bit compare register, compare output latch, and control register. When the 16-bit free-run timer value matches the compare register value, the output level is inverted and an interrupt is issued.

The MB91F353A/353A/352A/351A contains 2 channels of this block.

The MB91F355A/F356B/F357B/355A/354A/V350A contains 8 channels of this block.

This module has the following features.

- The output compare is able to operate independent of each of 8 compare register. There are output pins and interrupt flags corresponding to each of the compare registers.
- A pair of compare registers can be used to control the output terminal.
  The output terminal is reversed by using two compare registers.
- Capable of setting the initial value for each output pin.
- Interrupts can be generated upon a compare match.
- The ch.0 compare register is used as the compare clear register for the 16-bit free-run timer.

(2) Register list

Compare register (OCCP)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
C15	C14	C13	C12	C11	C10	C09	C08

Compare register (OCCP)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C07	C06	C05	C04	C03	C02	C01	C00

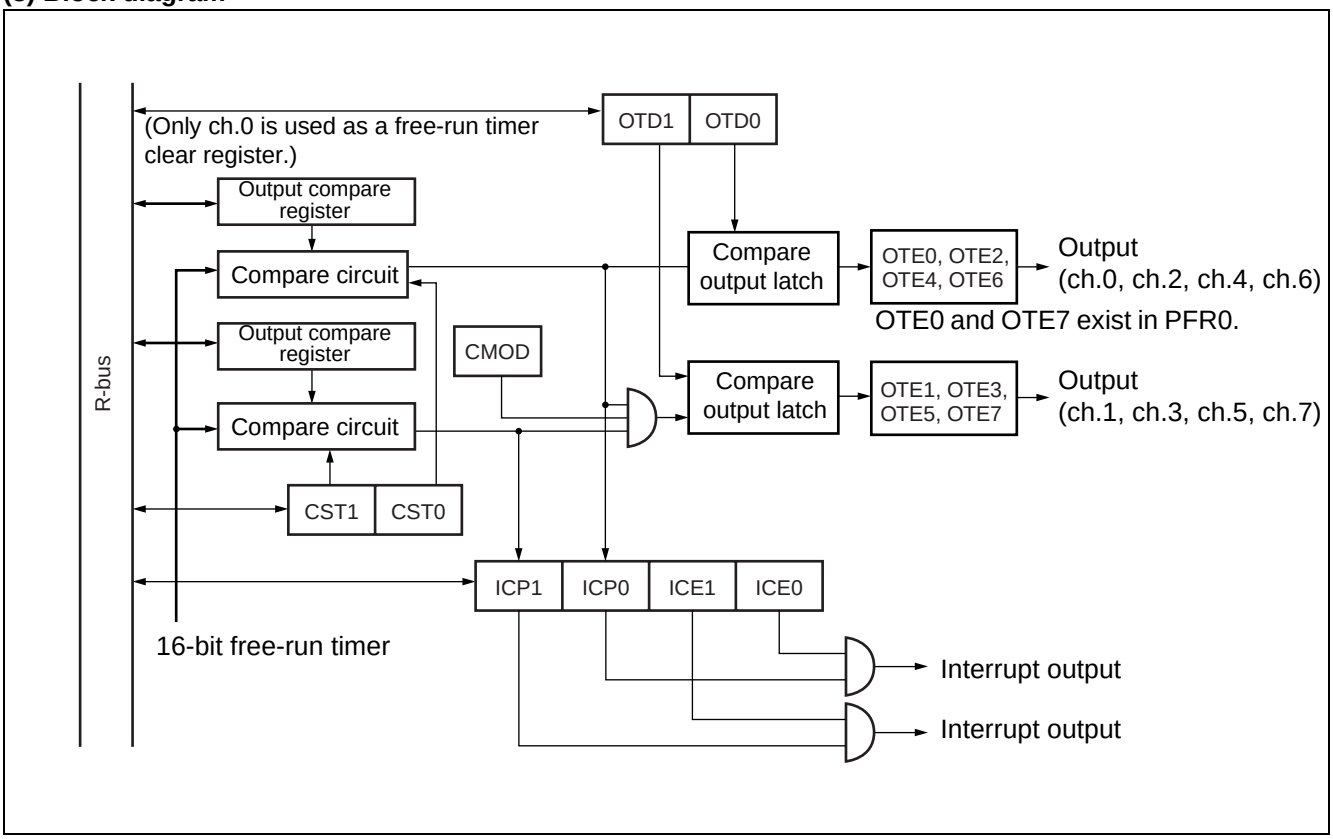
Output control register (OCS01)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
—	—	—	CMOD	—	—	OTD1	OTD0

Output control register (OCS23)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0

(3) Block diagram



13. I²C Interface

(1) Description

The I²C interface is a serial I/O port supporting the Inter-IC bus, operating as a master/slave device on the I²C bus. It has the following features :

- Master/slave transmission and reception
- Arbitration function
- Clock sync function
- Slave address and general call address detection function
- Transmission direction detection function
- Repeated start condition generation and detection function
- Bus error detection function
- 10-bit/7-bit slave address
- Slave address receive acknowledge control when in master mode
- Support for composite slave addresses
- Capable of interrupt when a transmission or bus error occurs
- Standard mode (Max 100 kbps)/High speed mode (Max 400 kbps) supported

(2) Register list

Bus control register (IBCR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT

Bus status register (IBSR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BB	RSC	AL	LRB	TRX	AAS	GCA	ADT

10-bit slave address resister (ITBA)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
—	—	—	—	—	—	TA9	TA8

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0

10-bit slave address mask resister (ITMK)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
ENTB	RAL	—	—	—	—	TM9	TM8

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

7-bit slave address resister (ISBA)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	SA6	SA5	SA4	SA3	SA2	SA1	SA0

7-bit slave address mask resister (ISMK)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0

D/A data register (IDAR)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
D7	D6	D5	D4	D3	D2	D1	D0

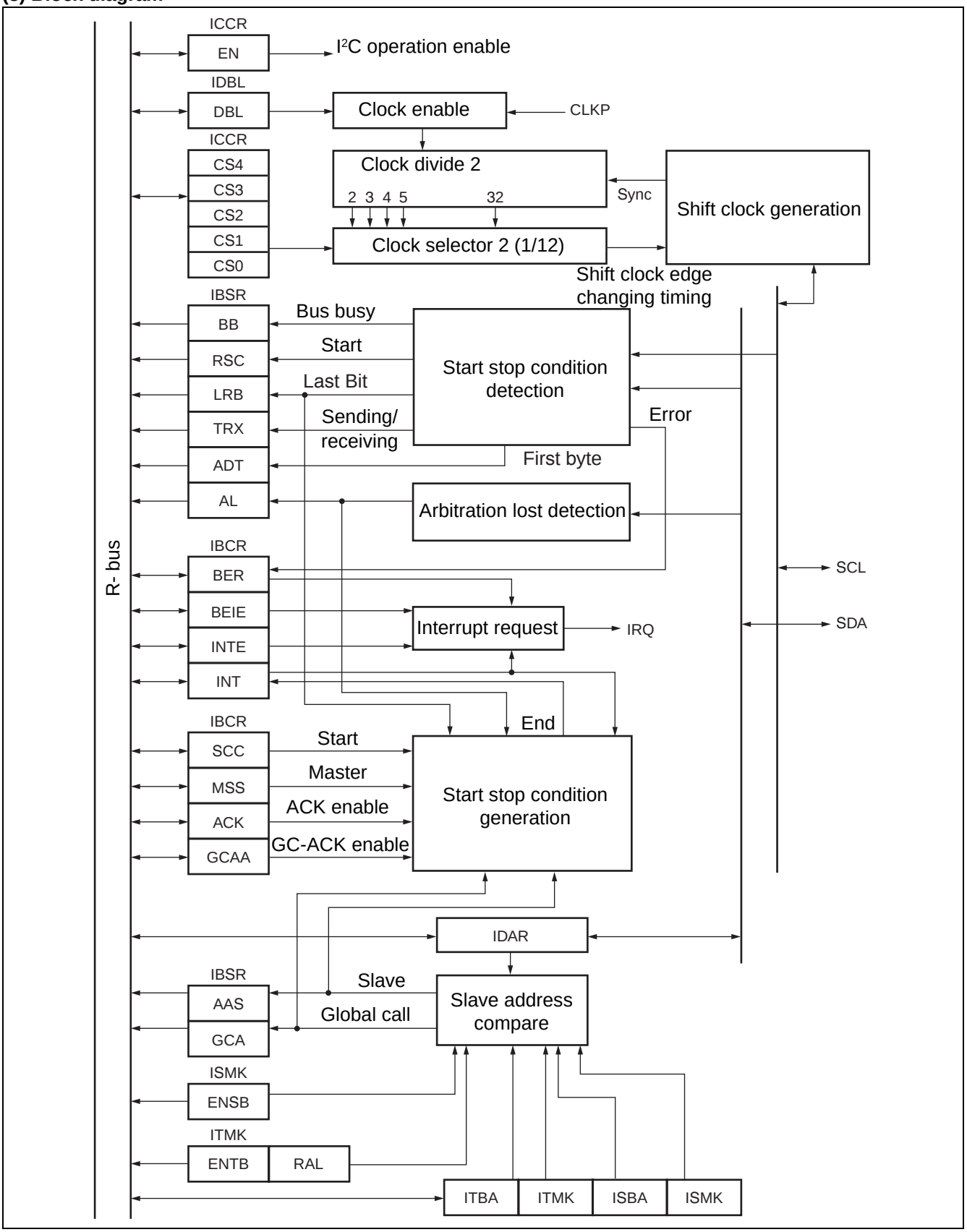
Clock control register (ICCR)

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
TEST	—	EN	CS4	CS3	CS2	CS1	CS0

Clock disable register (IDBL)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	—	—	DBL

(3) Block diagram



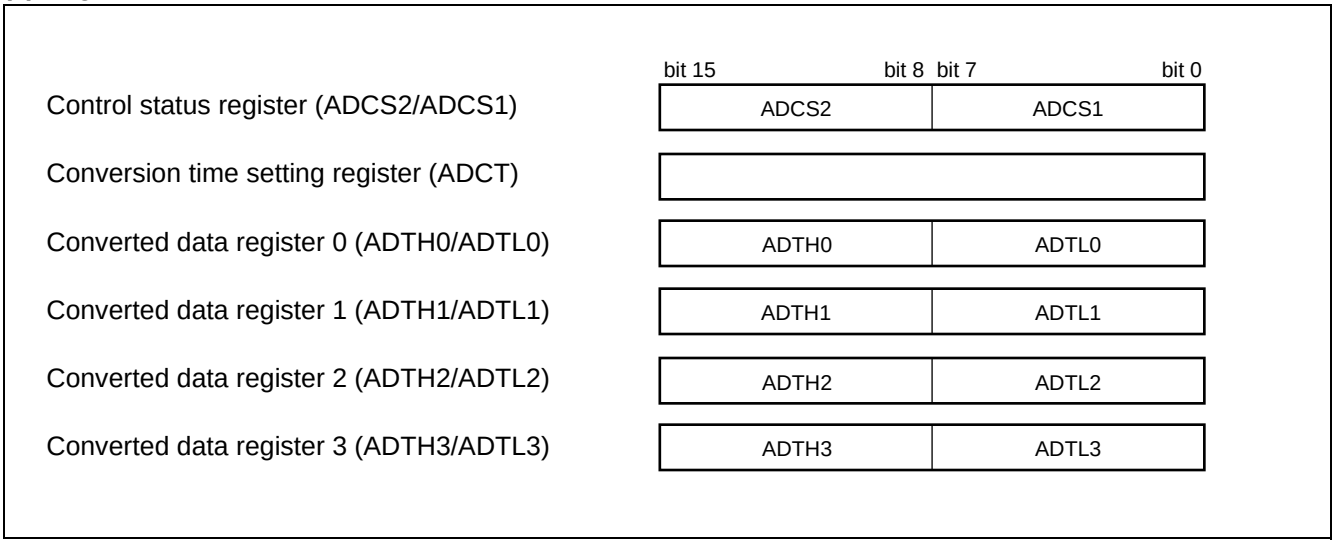
14. A/D converter

(1) Description

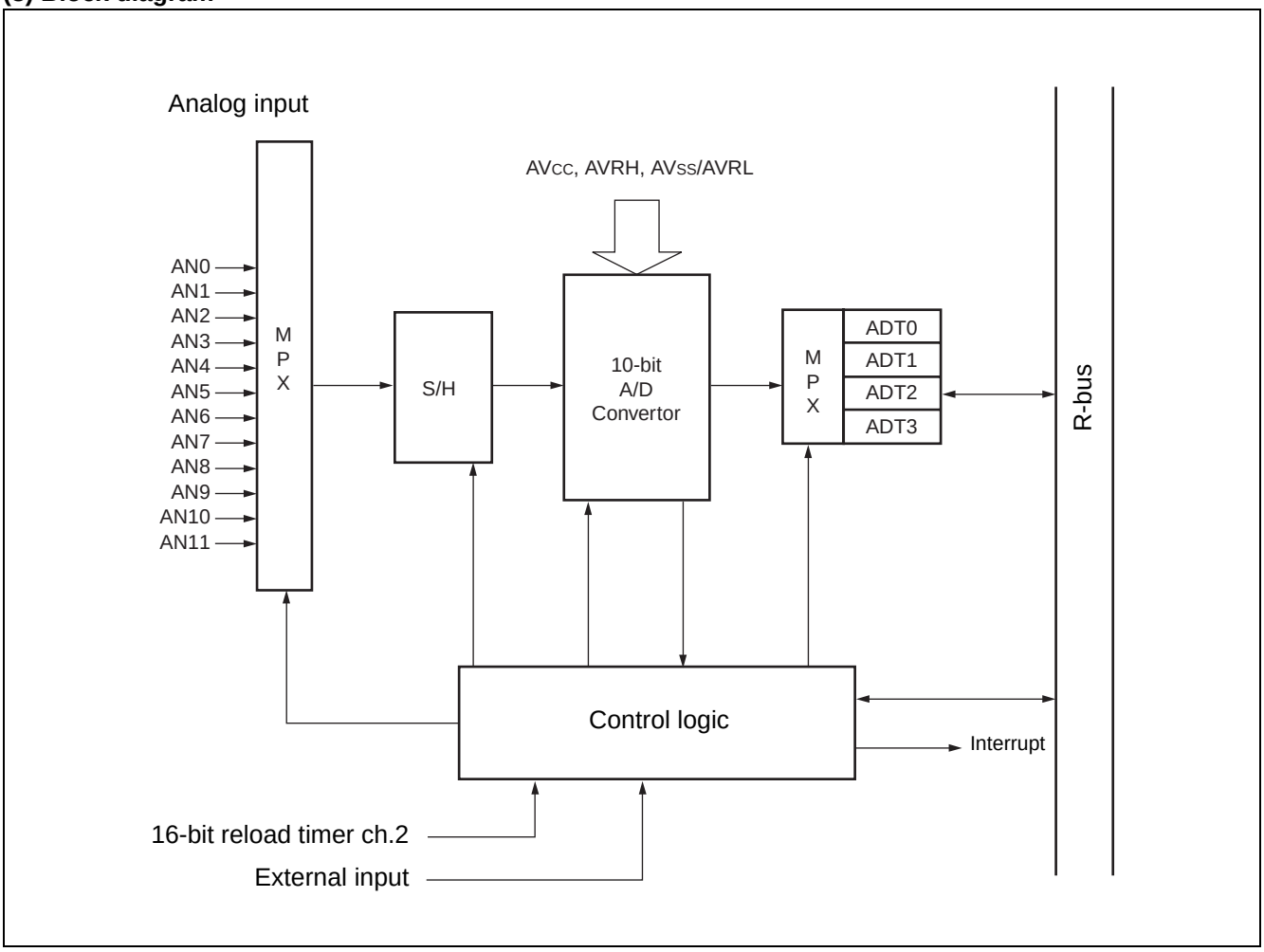
The A/D converter converts the analog input voltage into a digital value. It has the following features :

- Conversion time : 1.48 µs minimum per channel
- Employing serial / parallel conversion type for sample and hold circuit.
- 10-bit resolution (switchable between 8 and 10 bits)
- Programmatic selection of the analog input from among 12 channels
  (The MB91F353A/353A/352A/351A are input 8 channels.)
- Conversion mode
  Single conversion mode : Converts 1 selected channel a single time.
  Scan conversion mode : Scanning conversion of up to 4 channels.
- Converted data is stored in a data buffer (a total of 4 data buffers) .
- An interrupt request to the CPU can be generated upon completion of A/D conversion. The interrupt can be used to start a DMA transfer.
- The startup source can be selected from among software, external trigger (falling edge), and reload timer ch.2 (rising edge).

(2) Register list



(3) Block diagram



Note : The MB91F353A/353A/352A/351A does not have inputs AN8 to AN11.

15. 8-bit D/A converter

(1) Description

This block contains 3 channels of 8-bit D/A converters and D/A converter registers that can be used to control the independent output of each channel. The block has the following features.

- Power saving function
- 3.3 V interface

Note : The MB91F353A/353A/352A/351A contains 2 channels of D/A converter.

(2) Register list

D/A data register 0 to 2 (DADR0 to DADR2)

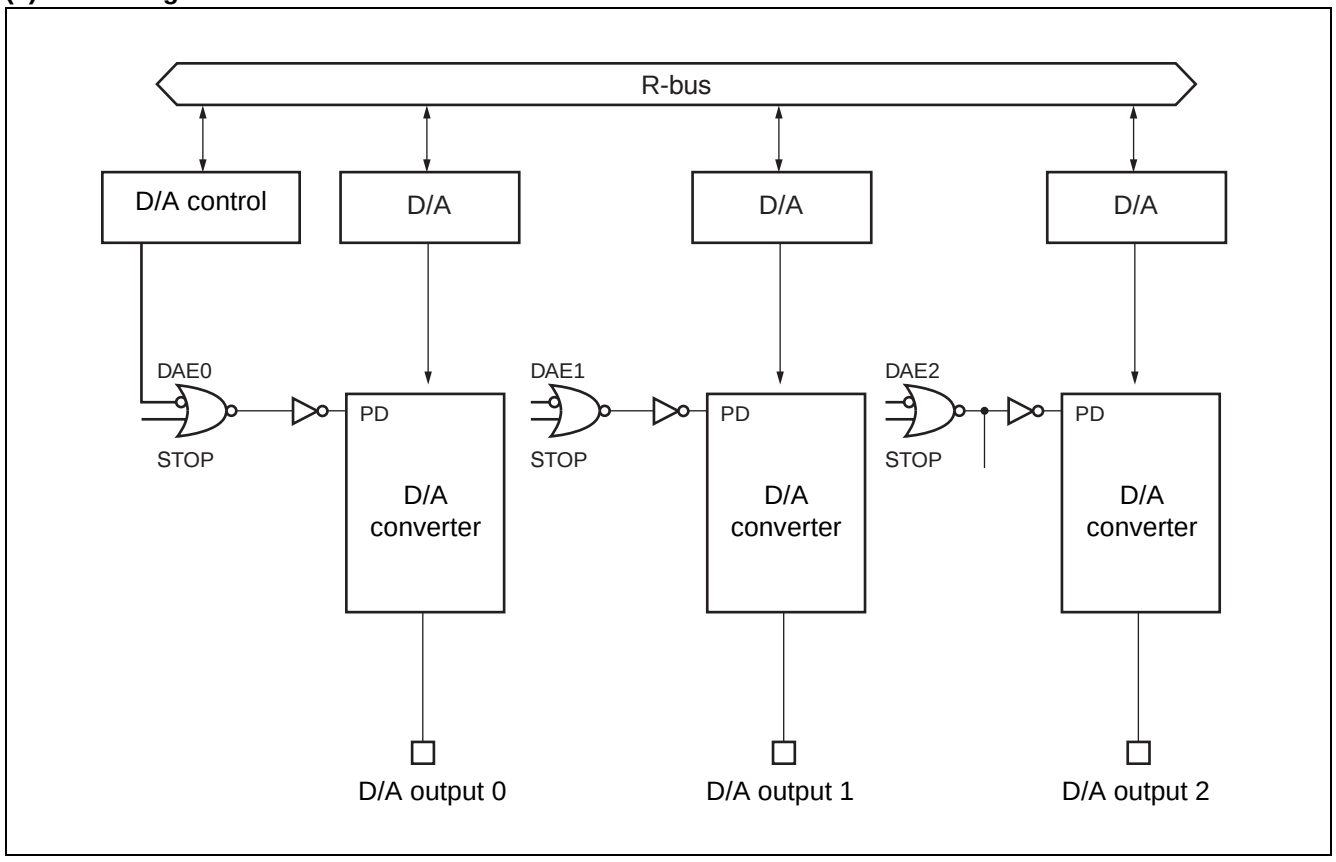
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

D/A control register 0 to 2 (DACR0 to DACR2)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	—	—	DAE

Note : The MB91F353A/353A/352A/351A does not have DADR2, DACR2.

(3) Block diagram



16. DMAC (DMA Controller)

(1) Description

This module provides direct memory access (DMA) transfers in the FR family devices.
The DMAC enables high speed transfers for various data without CPU intervention, thereby improving system performance.

- Hardware configuration

The main components of this module are as follows :

- Independent DMA channels × 5 channels
- 5 channels independent access control circuits
- 32-bit address registers (Supports reloading : 2 per channel)
- 16-bit transfer count registers (Supports reloading : 1 per channel)
- 4-bit block count registers (1 per channel)
- External transfer request input pins : DREQ0, DREQ1, and DREQ2. For ch.0 to ch.2 only
  Note : The MB91F353A/353A/352A/351A do not have an external interface.
- External transfer request acceptance output pins : DACK0, DACK1, and DACK2. For ch.0 to ch.2 only
  Note : The MB91F353A/353A/352A/351A do not have an external interface.
- DMA end output pins : DEOP0, DEOP1, and DEOP2. For ch.0 to ch.2 only
  Note : The MB91F353A/353A/352A/351A do not have an external interface.
- Fly-by transfer (memory to I/O and I/O to memory). For ch.0 to ch.2 only
  Note : The MB91F353A/353A/352A/351A do not support fly-by transfer.
- 2-cycle transfer

- Main functions

This module has the following major functions for data transfer :

- Supports data transfer over multiple independent channels (5 channels)

(1) Priority order (ch.0 > ch.1 > ch.2 > ch.3 > ch.4)

(2) Order can be reversed for ch.0 and ch.1

(3) DMAC activation triggers

- External dedicated pin input (edge detection/level detection for ch.0 to ch.2 only)

  Note : The MB91F353A/353A/352A/351A do not have an external interface.

- Internal peripheral request (Interrupt request sharing, including external interrupts)
- Software request (register write)

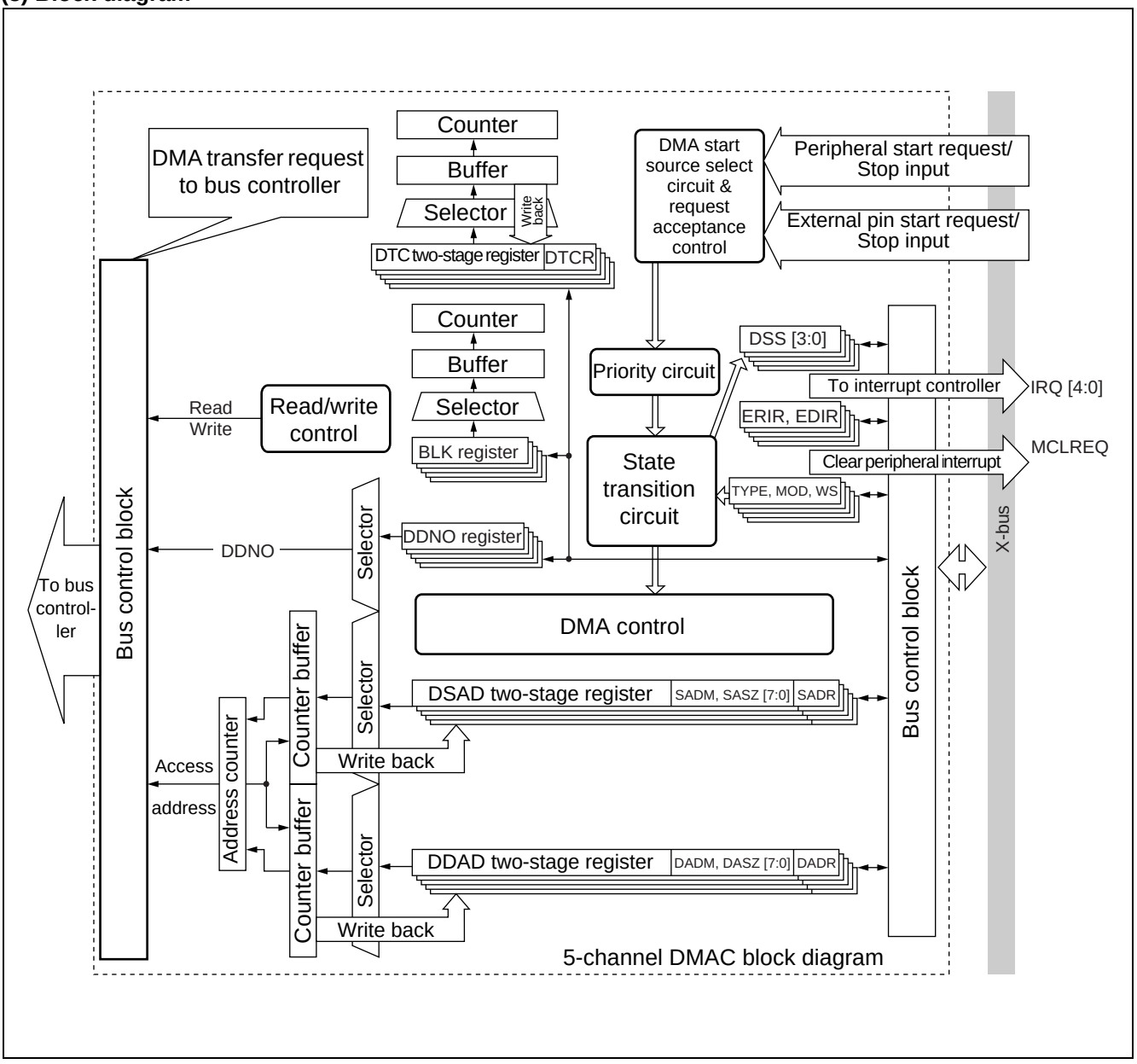
(4)Transmission mode

- Demand transfer, burst transfer, step transfer, or block transfer
- Addressing mode : 32-bit full addressing (increment, decrement, or fixed)
  (address increment can be in the range - 255 to + 255)
- Data length : Byte, halfword, or word
- Single-shot or reload operation selectable

(2) Register Description

			bit 31 ... bit 0
ch.0 Control/status	Register A	(DMACA0)	
	Register B	(DMACB0)	
ch.1 Control/status	Register A	(DMACA1)	
	Register B	(DMACB1)	
ch.2 Control/status	Register A	(DMACA2)	
	Register B	(DMACB2)	
ch.3 Control/status	Register A	(DMACA3)	
	Register B	(DMACB3)	
ch.4 Control/status	Register A	(DMACA4)	
	Register B	(DMACB4)	
Overall control register		(DMACR)	
ch.0 Transfer source address register		(DMASA0)	
		(DMADA0)	
ch.1 Transfer source address register		(DMASA1)	
		(DMADA1)	
ch.2 Transfer source address register		(DMASA2)	
		(DMADA2)	
ch.3 Transfer source address register		(DMASA3)	
		(DMADA3)	
ch.4 Transfer source address register		(DMASA4)	
		(DMADA4)	

(3) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog power supply voltage*1	DAVC	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Analog power supply voltage*1	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Analog reference voltage*1	AVRH	V_{SS} – 0.5	V_{SS} + 4.0	V	*3
Input voltage*1	V_I	V_{SS} – 0.5	V_{CC} + 0.5	V	*8
Input voltage (N-ch open-drain) *1	V_{IND}	V_{SS} – 0.5	V_{SS} + 5.5	V	
Analog pin input voltage*1	V_{IA}	V_{SS} – 0.5	AV_{CC} + 0.5	V	*8
Output voltage*1	V_O	V_{SS} – 0.5	V_{CC} + 0.5	V	
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	—	20	mA	*7
“L” level maximum output current	I_{OL}	—	10	mA	*4
“L” level maximum output current (N-ch open-drain)	I_{OLND}	—	20	mA	
“L” level average output current	I_{OLAV}	—	8	mA	*5
“L” level average output current (N-ch open-drain)	I_{OLAVND}	—	15	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*6
“H” level maximum output current	I_{OH}	—	– 10	mA	*4
“H” level average output current	I_{OHAV}	—	– 4	mA	*5
“H” level total maximum output current	ΣI_{OH}	—	– 50	mA	
“H” level total average output current	ΣI_{OHAV}	—	– 20	mA	*6
Power consumption	P_D	—	850	mW	
Operating temperature	Ta	– 40	+ 85	°C	
Storage temperature	T_{STG}	—	+ 125	°C	

*1 : The parameter is based on V_{SS} = DAVS = AV_{SS} = 0 V.

*2 : V_{CC} must not be lower than V_{SS} – 0.3 V.

*3 : Be careful not to exceed "V_{CC} + 0.3 V" , for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output current is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

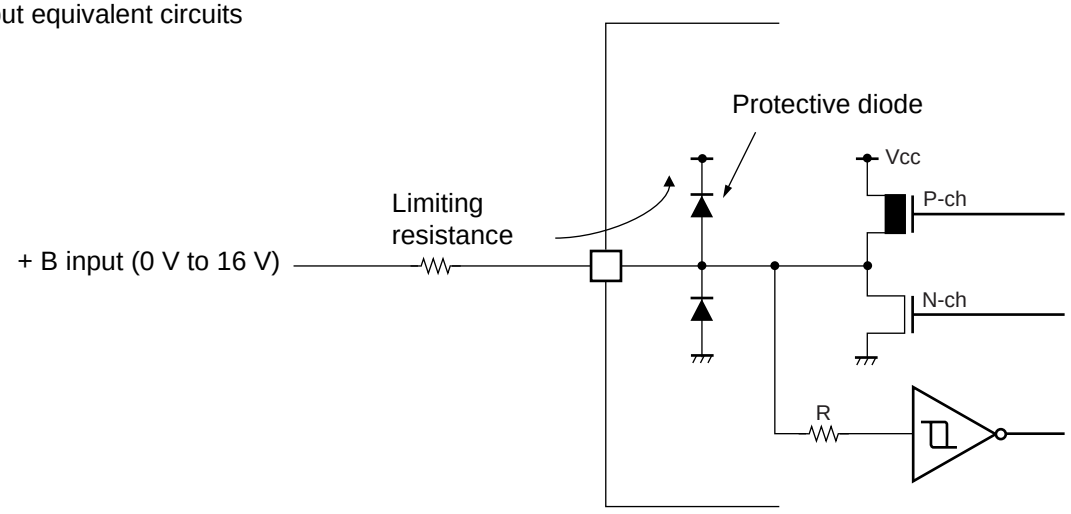
(Continued)

(Continued)

*7 : • Relevant pins : Ports 2, 3, 4, 5, 6, 8, 9, A, H, I, K, M, N, O and AN (A/D input) : MB91F353A/353A/352A/351A
Ports 2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P and AN (A/D input) : MB91F355A/F356B/F357B/355A/354A

- Use within recommended operating conditions.
- Use at DC voltage (current).
- + B signals are input signals that exceed the V_{CC} voltage.
- A limiting resistance should always be applied to +B signals by connecting the resistance between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in low power consumption mode, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if a + B input is applied when the microcontroller is off (not fixed at 0 V), power is supplied through the pin, possibly causing the microcontroller to partially operate.
- Note that if a + B input is applied when the power supply is turned on, power is supplied through the pin, possibly resulting in a power-supply voltage at which power-on reset does not work.
- Ensure that a + B input pin does not form an open circuit.
- Note that analog I/O pins other than the A/D input pins (such as the LCD drive and comparator input pins) cannot input + B.
- Sample recommended circuits :

• Input/output equivalent circuits



*8 : V_I must not exceed the rated voltage. However, If the maximum current to/from an input is limited by some means using external components, the I_{CLAMP} rating supersedes the V_I rating.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Other than MB91F356B/F357B)

(V_{SS} = DAVS = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	During normal operation
	V_{CC}	3.0	3.6	V	Hold RAM status at stop
Analog power supply voltage	DAVC	V_{SS} – 0.3	V_{SS} + 3.6	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6		
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	– 40	+ 85	°C	

(MB91F356B/F357B only)

(V_{SS} = DAVS = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	During normal operation
	V_{CC}	2.7	3.6	V	Hold RAM status at stop
	V_{CC}	3.0	3.6	V	When writing or erasing Flash memory
Analog power supply voltage	DAVC	V_{SS} – 0.3	V_{SS} + 3.6	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6		
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	– 40	+ 85	°C	
		0	+70	°C	When writing or erasing Flash memory*

* : Including the F355A/F353A

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port 2, 3, 4, 5, 6, 9, A	—	V_{CC} × 0.65	—	V_{CC} + 0.3	V	MB91F353A/353A/352A/351A
		Port 2, 3, 4, 5, 6, 9, A, B, C						MB91F355A/F356B/F357B/355A/354A
	V_{IHS}	Port 8, H, I, M, N, O, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$		V_{CC} × 0.8				Hysteresis input MB91F353A/353A/352A/351A
		Port 8, G, H, I, M, N, O, P, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$						Hysteresis input MB91F355A/F356B/F357B/355A/354A
	V_{IHST}	Port K, L				5.25		Hysteresis input withstand voltage of 5 V MB91F353A/353A/352A/351A
		Port J, K, L						Hysteresis input withstand voltage of 5 V MB91F355A/F356B/F357B/355A/354A
"L" level input voltage	V_{IL}	Port 2, 3, 4, 5, 6, 9, A	—	V_{SS}	—	V_{CC} × 0.25	V	MB91F353A/353A/352A/351A
		Port 2, 3, 4, 5, 6, 9, A, B, C						MB91F355A/F356B/F357B/355A/354A
	V_{ILS}	Port 8, H, I, M, N, O, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$				V_{CC} × 0.2		Hysteresis input MB91F353A/353A/352A/351A
		Port 8, G, H, I, M, N, O, P, MD0, MD1, MD2, $\overline{INIT}$, $\overline{NMI}$						Hysteresis input MB91F355A/F356B/F357B/355A/354A
	V_{ILST}	Port K, L						Hysteresis input withstand voltage of 5 V MB91F353A/353A/352A/351A
		Port J, K, L						Hysteresis input withstand voltage of 5 V MB91F355A/F356B/F357B/355A/354A

(Continued)

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
"H" level output voltage	V_{OH}	Port 2, 3, 4, 5, 6, 8, 9, A, H, I, J, K, M, N, O	V_{CC} = 3.0 V, I_{OH} = –4.0 mA		V_{CC} – 0.5	—	V_{CC}	V	MB91F353A/ 353A/352A/351A
		Port 2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P							MB91F355A/ F356B/F357B/ 355A/354A
"L" level output voltage	V_{OL1}	Port 2, 3, 4, 5, 6, 8, 9, A, H, I, K, M, N, O	V_{CC} = 3.0 V, I_{OL} = 4.0 mA		V_{SS}	—	0.4	V	MB91F353A/ 353A/352A/351A
		Port 2, 3, 4, 5, 6, 8, 9, A, B, C, G, H, I, J, K, M, N, O, P							MB91F355A/ F356B/F357B/ 355A/354A
	V_{OL2}	Port L	V_{CC} = 3.0 V, I_{OL} = 15.0 mA						N-ch open-drain
Input leak current (High-Z Output Leakage Current)	I_{LI}	All input pin	V_{CC} = 3.6 V, 0<V_I <V_{CC}		− 5	—	+ 5	µA	
Pull-up resistance	R_{UP}	Setting pin $\overline{INIT}$, Pull Up	V_{CC} = 3.6 V, V_I = 0.45 V		25	50	200	kΩ	
Power supply current	I_{CC}	V_{CC}	f_C = 12.5 MHz, V_{CC} = 3.3 V	Flash	—	160	220	mA	MB91F353A/ 353A/352A/351A Multiply by 4RUN When operating at CLKB : 50 MHz CLKT : 25 MHz CLKP : 25 MHz
				MASK		125	150		
				Flash		85	100		MB91F353A/ 353A/352A/351A Multiply by 2RUN When operating at CLKB : 25 MHz CLKT : 25 MHz CLKP : 12.5 MHz
				MASK		75	90		

(Continued)

(Continued)
(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	V_{CC}	f_C = 12.5 MHz, V_{CC} = 3.3 V	—	160	220	mA	MB91F355A/ F356B/F357B/ 355A/354A Multiply by 4RUN When operating at CLKB : 50 MHz CLKT : 25 MHz CLKP : 25 MHz
	I_{CCS}				100	140		MB91F353A/ 353A/352A/351A Multiply by 4RUN When operating at CLKB : 50 MHz CLKT : 25 MHz CLKP : 25 MHz MB91F355A/ F356B/F357B/ 355A/354A Sleep CLKP : When operating at 25 MHz
	I_{CCH}		Ta = +25 °C, V_{CC} = 3.3 V		1	100	µA	At stop
	I_{CCL}		Ta = +25 °C, f_C = 32.768 kHz, V_{CC} = 3.3 V		0.3	3.0	mA	Sub RUN When operating at CLKB : 32.768 kHz CLKT : 32.768 kHz CLKP : 32.768 kHz
	I_{CCLS}				0.2	2.0		Sub-sleep When operating at CLKP : 32.768 kHz
	I_{CCT}				5	120	µA	When operating in watch mode (Main Off, STOP)
Input capacitance	C_{IH}	Other than V_{CC}, V_{SS}, AV_{CC}, AV_{SS}, DAVC, DAVS	—	—	5	15	pF	

4. AC Characteristics

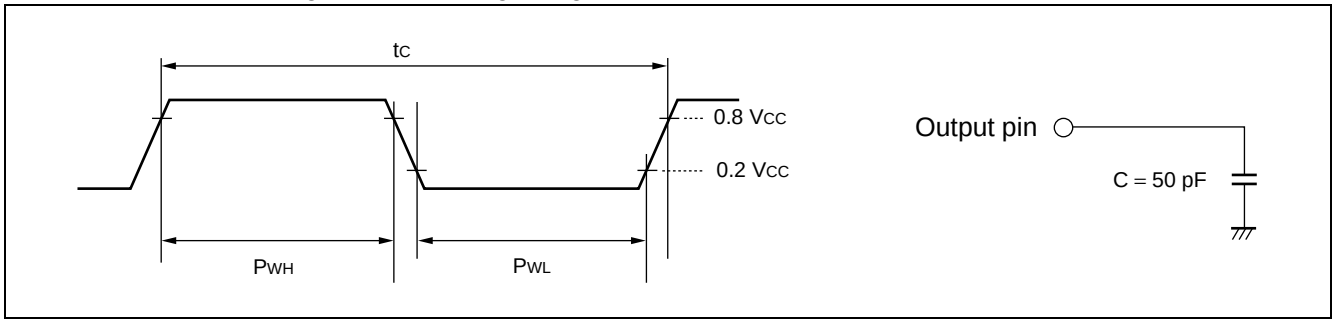
(1) Clock Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

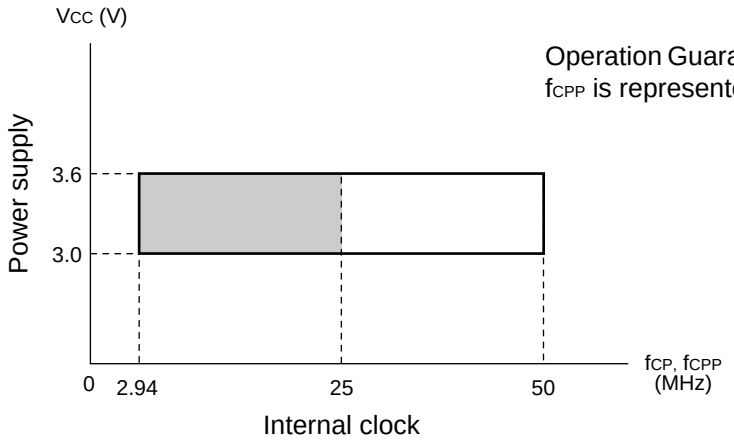
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	10	—	12.5	MHz	MAIN PLL (When operating at max internal frequency (50 MHz) = 12.5 MHz self-oscillation with × 4 PLL)
Clock cycle time	t_C			80		100	ns	
Clock frequency	f_C			10		25	MHz	MAIN self-oscillation (frequency-halved input)
Internal operating clock frequency	f_{CP}	—	When a minimum value of 12.5 MHz is input as the X0 clock frequency and x4 multiplication is set for the PLL of the oscillator circuit	3.13*		50	MHz	CPU
	f_{CPP}					25		Peripheral
	f_{CPT}							External bus
Internal operating clock cycle time	t_{CP}			20		320*	ns	CPU
	t_{CPP}			40				Peripheral
	t_{CPT}							External bus
Clock frequency	f_C	X0A, X1A	—	30	32.768	35	kHz	SUB self-oscillation
Clock cycle time	t_C			28.6	30.51	33.3	µs	
Input clock pulse width	—	X0, X1	P_{WH}/t_C P_{WL}/t_C	40	—	60	%	
Internal operating clock frequency	f_{CP}, f_{CPP}, f_{CPT}	—	When a standard value of 32.768 kHz is input as the X0A clock frequency	2*		32.768	kHz	
Internal operating clock cycle time	t_{CP}, t_{CPP}, t_{CPT}			30.51		500*	µs	

* : The values assume a gear cycle of 1/16.

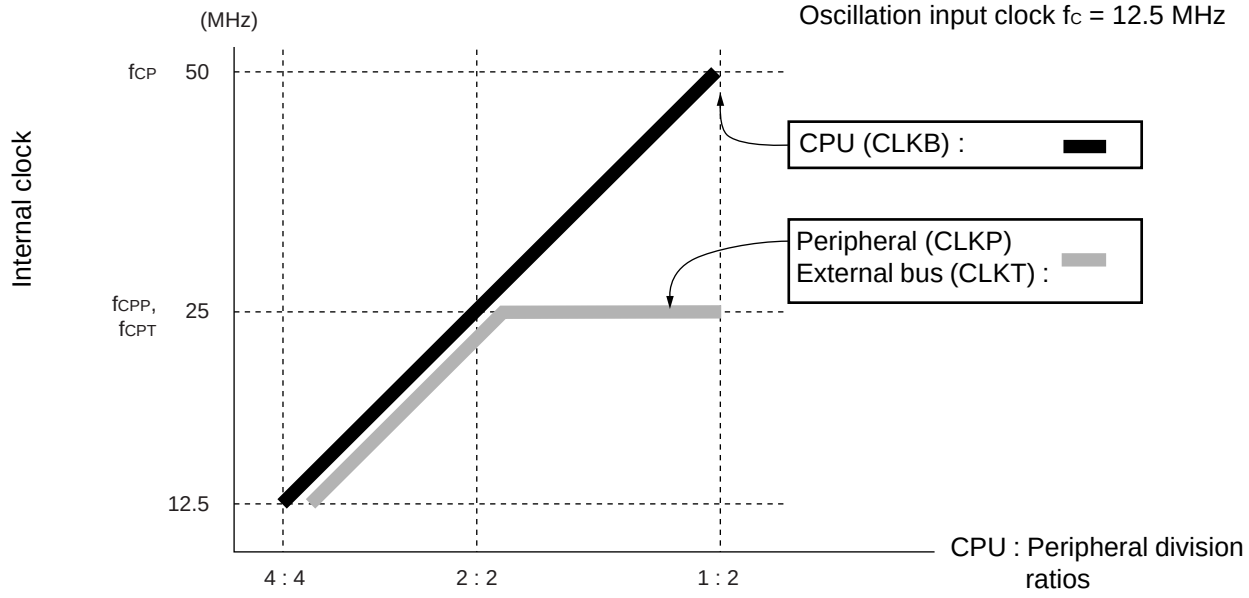
• Conditions for measuring the clock timing ratings



• Operation Guaranteed Range (Other than MB91F356B/F357B)



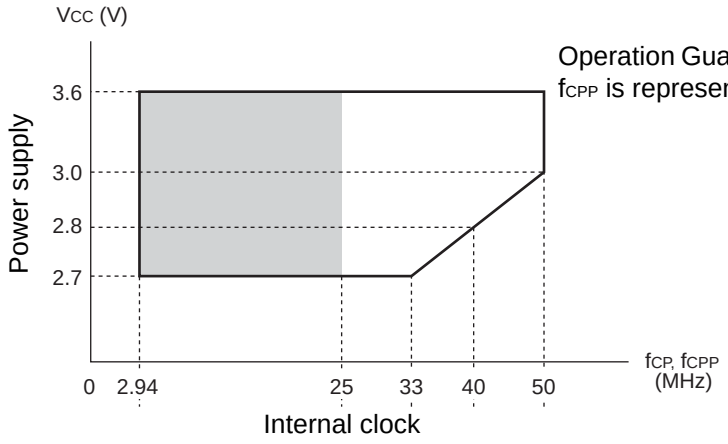
• External/internal clock setting range



Notes :
- When the PLL is used, the external clock input must fall between 10.0 MHz and 12.5 MHz.
- Set the PLL oscillation stabilization wait time longer than 454.5 µs.
- The internal clock gear setting should not exceed the relevant value in the table in “(1) Clock timing ratings”.

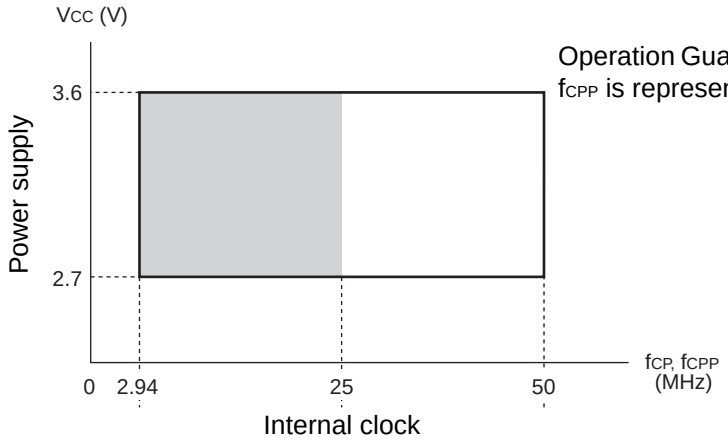
• Operation Guaranteed Range (MB91F356B/F357B only)

For Flash memory wait of 2 (FLWC register : WTC[2 : 0] = 010)



Operation Guaranteed Range (Ta = −40 °C to +85 °C)
f_{CPP} is represented by the shaded area.

For Flash memory wait of 3 (FLWC register : WTC[2 : 0] = 011)



Operation Guaranteed Range (Ta = −40 °C to +85 °C)
f_{CPP} is represented by the shaded area.

(2) Clock Output Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	MCLK*4 SYSCLK	—	t_{CPT}	—	ns	*1
SYSCLK ↑ → SYSCLK ↓	t_{CHCL}	MCLK*4 SYSCLK		t_{CYC} − 5	t_{CYC} + 5	ns	*2
SYSCLK ↓ → SYSCLK ↑	t_{CLCH}	MCLK*4 SYSCLK		t_{CYC} − 5	t_{CYC} + 5	ns	*3

*1 : t_{CYC} is the frequency of one clock cycle after gearing.

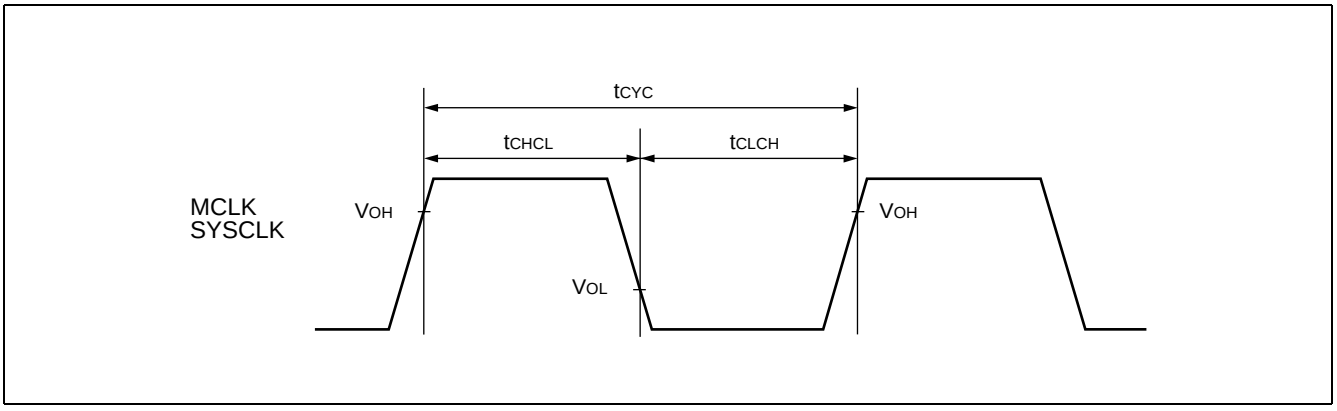
*2 : This value is the rating when the gear ratio is set to × 1. For the ratings when the gear ratio is set to 1/2, 1/4 or 1/8, substitute 1/2, 1/4 or 1/8 for n in the following equation.

$(1 / 2 \times 1 / n) \times t_{CYC} - 10$

*3 : This value is the rating when the gear ratio is set to × 1.

*4 : The MB91F353A/353A/352A/351A does not have MCLK pin.
In the following AC characteristics, MCLK is equal to SYSCLK.

Note : t_{CPT} represents the internal operating clock cycle time. Refer to “(1) Clock Timing”.

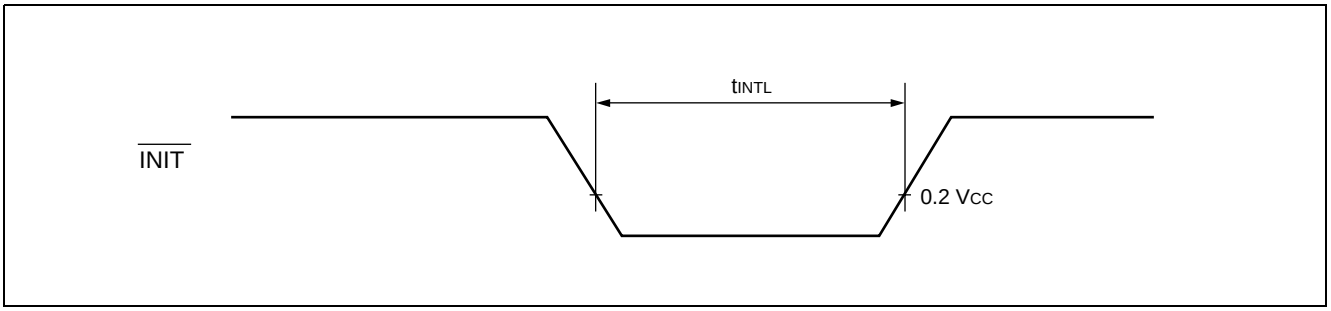


(3) Reset Ratings

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
$\overline{INIT}$ input time (at power-on)	t_{INTL}	$\overline{INIT}$	—	$t_C \times 10$	—	ns
$\overline{INIT}$ input time (other than at power-on)				$t_C \times 10$		ns

Note : t_C represents the clock cycle time. Refer to “(1) Clock Timing”.



(4) Normal Bus Access Read/Write Operation

• MB91F353A/353A/352A/351A

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS3}$ setup	t_{CSLCH}	SYSCLK, $\overline{CS0}$ to $\overline{CS3}$	AWRxL : W02 = 0	3	—	ns	*3
	t_{CSDLCH}		AWR0L : W02 = 1	− 3			
$\overline{CS0}$ to $\overline{CS3}$ hold	t_{CHCSH}		—	3	t_{CYC} / 2 + 6		
Address setup	t_{ASCH}	SYSCLK, A20 to A00*4			—		
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$, A20 to A00*4					
	t_{ASRL}	$\overline{RD}$, A20 to A00*4					
Address hold	t_{CHAX}	SYSCLK, A20 to A00*4			t_{CYC} / 2 + 6		
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$, A20 to A00*4			—		
	t_{RHAX}	$\overline{RD}$, A20 to A00*4					
Valid address → Valid data input time	t_{AVDV}	A20 to A00*4, D31 to D16		—	3 / 2 × t_{CYC} − 15		*1 *2
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	SYSCLK, $\overline{WR0}$, $\overline{WR1}$			6		
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWH}						
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		t_{CYC} − 5	—		
Data setup → $\overline{WRx}$ ↑	t_{DSWH}	$\overline{WR0}$, $\overline{WR1}$, D31 to D16		t_{CYC}			
$\overline{WRx}$ ↑ → Data hold time	t_{WHDX}			3			
$\overline{RD}$ delay time	t_{CHRL}	SYSCLK, $\overline{RD}$		—	6		
$\overline{RD}$ delay time	t_{CHRH}						
$\overline{RD}$ ↓ → Valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16			t_{CYC} − 10		*1
Data setup → $\overline{RD}$ ↑ Time	t_{DSRH}			10	—		
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}			0			
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		t_{CYC} − 5			
$\overline{AS}$ setup	t_{ASLCH}	SYSCLK, $\overline{AS}$		3			
$\overline{AS}$ hold	t_{CHASH}				t_{CYC} / 2 + 6		

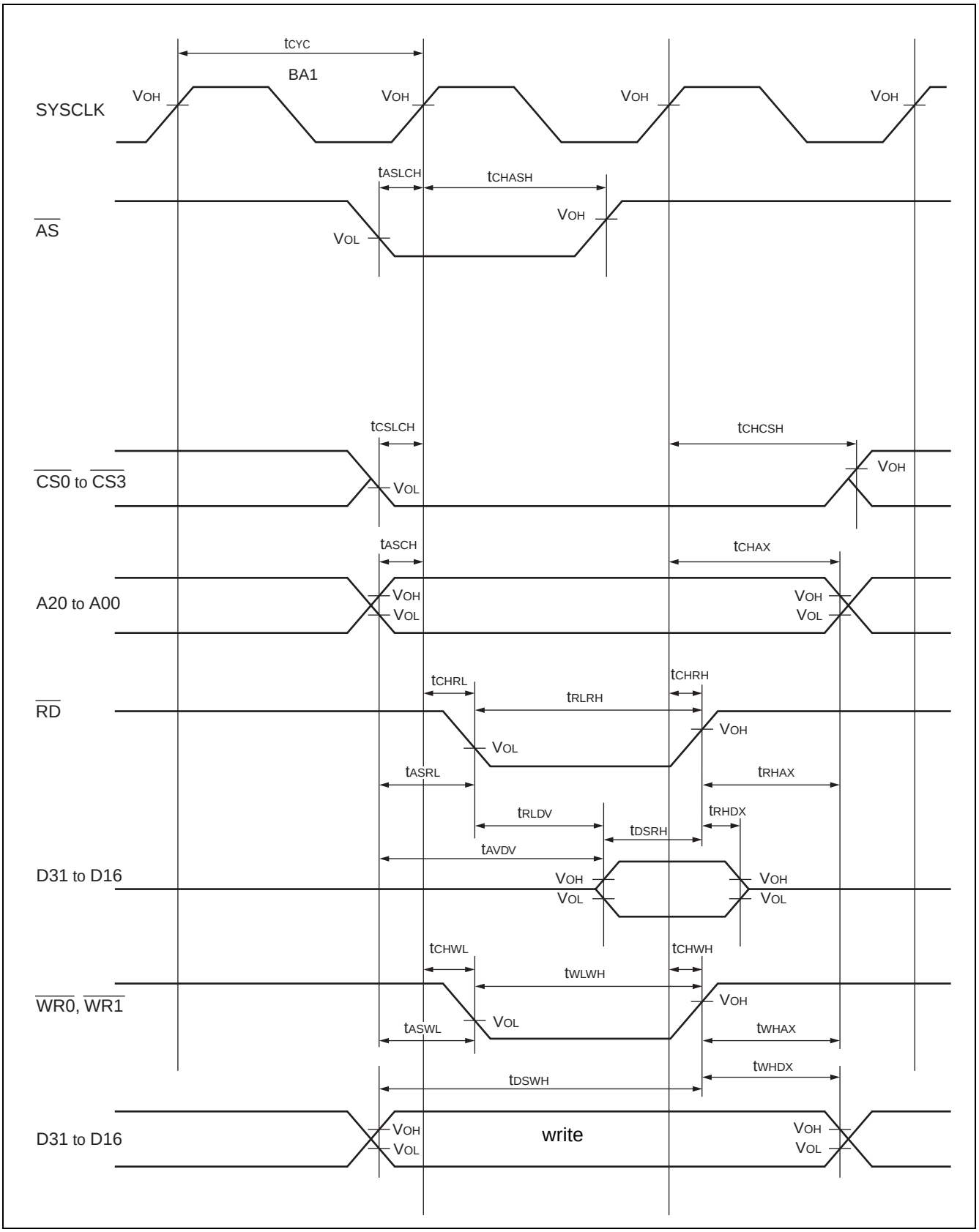
*1 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.

*2 : This value is the rating when the gear ratio is set to × 1. For the ratings when the gear ratio is set to between 1/2 to 1/16, substitute 1/2 to 1/16 for n in the following equation.
Calculation expression : 3/(2n) × t_{CYC} − 15

*3 : AWRxL : Area Wait Register

*4 : The MB91F353A/353A/352A/351A does not have A23 to A21.

Note : t_{CYC} represents the cycle time. Refer to “(2) Clock Output Timing”.


tCYC
BA1
SYSCLK
VOH
tASLCH
tCHASH
AS
VOL
tCSLCH
tCHCSH
CS0 to CS3
tASCH
tCHAX
A20 to A00
tCHRL
tCHRH
tRLRH
RD
tASRL
tRHAX
tRLDV
tRHDX
tDSRH
tAVDV
D31 to D16
tCHWL
tCHWH
tWLWH
WR0, WR1
tASWL
tWHAX
tWHDX
tDSWH
write

• MB91F355A/F356B/F357B/355A/354A

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS3}$ setup	t_{CSLCH}	MCLK, $\overline{CS0}$ to $\overline{CS3}$	AWRxL*3 : W02 = 0	3	—	ns	
	t_{CSDLCH}		AWR0L : W02 = 1	− 3	—	ns	
$\overline{CS0}$ to $\overline{CS3}$ hold	t_{CHCSH}		—	3	$t_{CYC}/2 + 6$	ns	
Address setup	t_{ASCH}	MCLK, A23 to A00*4		3	—	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$, A23 to A00*4		3	—	ns	
	t_{ASRL}	$\overline{RD}$, A23 to A00*4		3	—	ns	
Address hold	t_{CHAX}	MCLK, A23 to A00*4		3	$t_{CYC}/2 + 6$	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$, A23 to A00*4		3	—	ns	
	t_{RHAX}	$\overline{RD}$, A23 to A00*4		3	—	ns	
Valid address → Valid data input time	t_{AVDV}	A23 to A00*4, D31 to D16		—	$3 / 2 \times t_{CYC} - 15$	ns	*1 *2
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWL}	MCLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CHWH}			—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$		$t_{CYC} - 5$	—	ns	
Data setup → $\overline{WRx}$ ↑	t_{DSWH}	$\overline{WR0}$, $\overline{WR1}$, D31 to D16		t_{CYC}	—	ns	
$\overline{WRx}$ ↑ → Data hold time	t_{WHDX}			3	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	MCLK, $\overline{RD}$		—	6	ns	
$\overline{RD}$ delay time	t_{CHRH}			—	6	ns	
$\overline{RD}$ ↓ → Valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	$t_{CYC} - 10$	ns	*1
Data setup → $\overline{RD}$ ↑ time	t_{DSRH}		3.0 V ≤ V_{CC} ≤ 3.6 V	10	—	ns	
			2.7 V ≤ V_{CC} < 3.0 V	15	—	ns	MB91F356B/ F357B only
$\overline{RD}$ ↓ → Data hold time	t_{RHDX}		—	0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		$t_{CYC} - 5$	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	MCLK, $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	$t_{CYC}/2 + 6$	ns	

*1 : When the bus timing is delayed by automatic wait insertion or RDY input, add the time (t_{CYC} × the number of cycles added for the delay) to this rating.

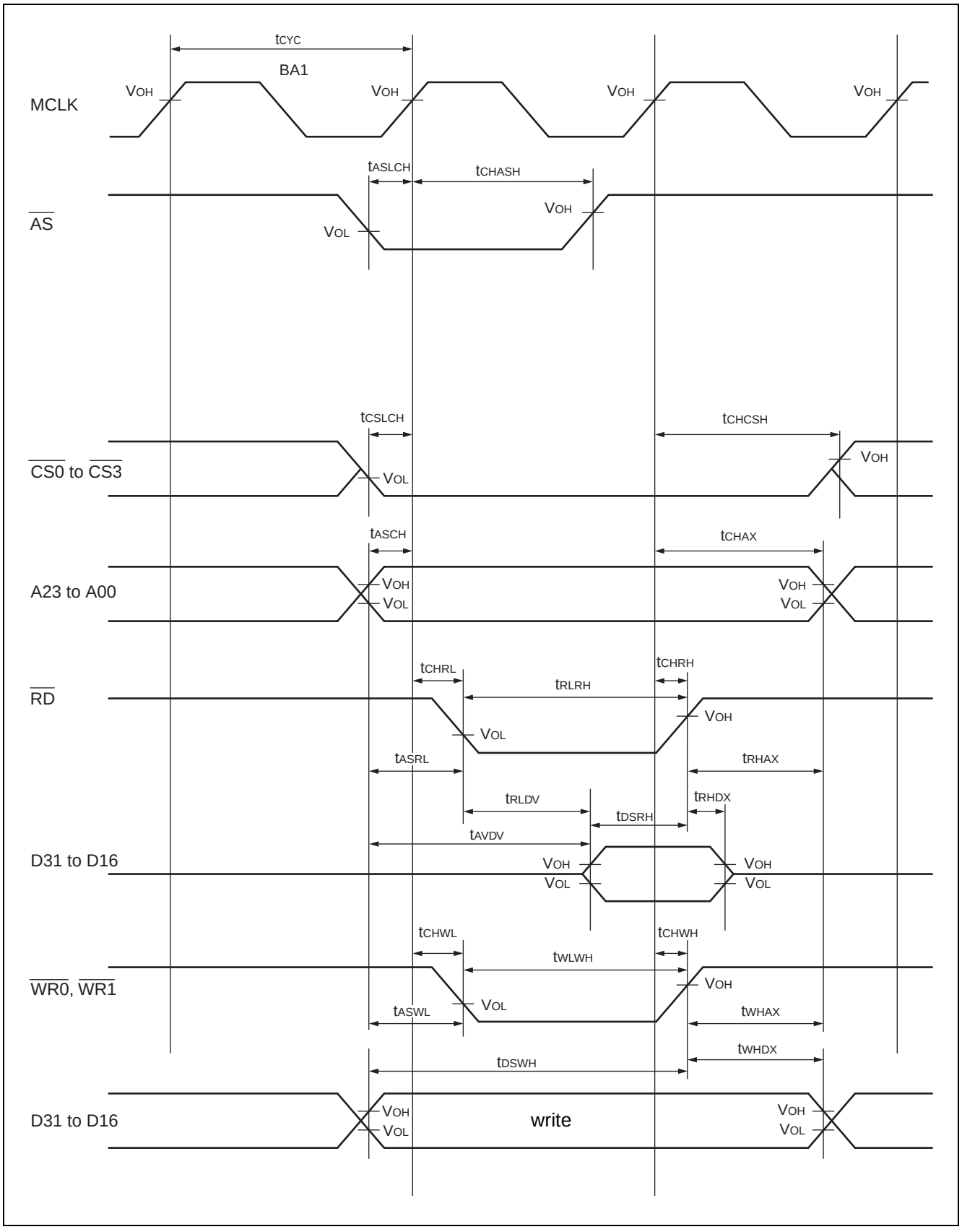
*2 : This value is the rating when the gear ratio is set to × 1. For the ratings when the gear ratio is set to between 1/2 to 1/16, substitute 1/2 to 1/16 for n in the following equation.

Calculation expression : $3/(2n) \times t_{CYC} - 15$

*3 : AWRxL : Area Wait Register

*4 : The MB91F353A/353A/352A/351A does not have A23 to A21.

Note : t_{CYC} represents the cycle time. Refer to “(2) Clock output timing”.

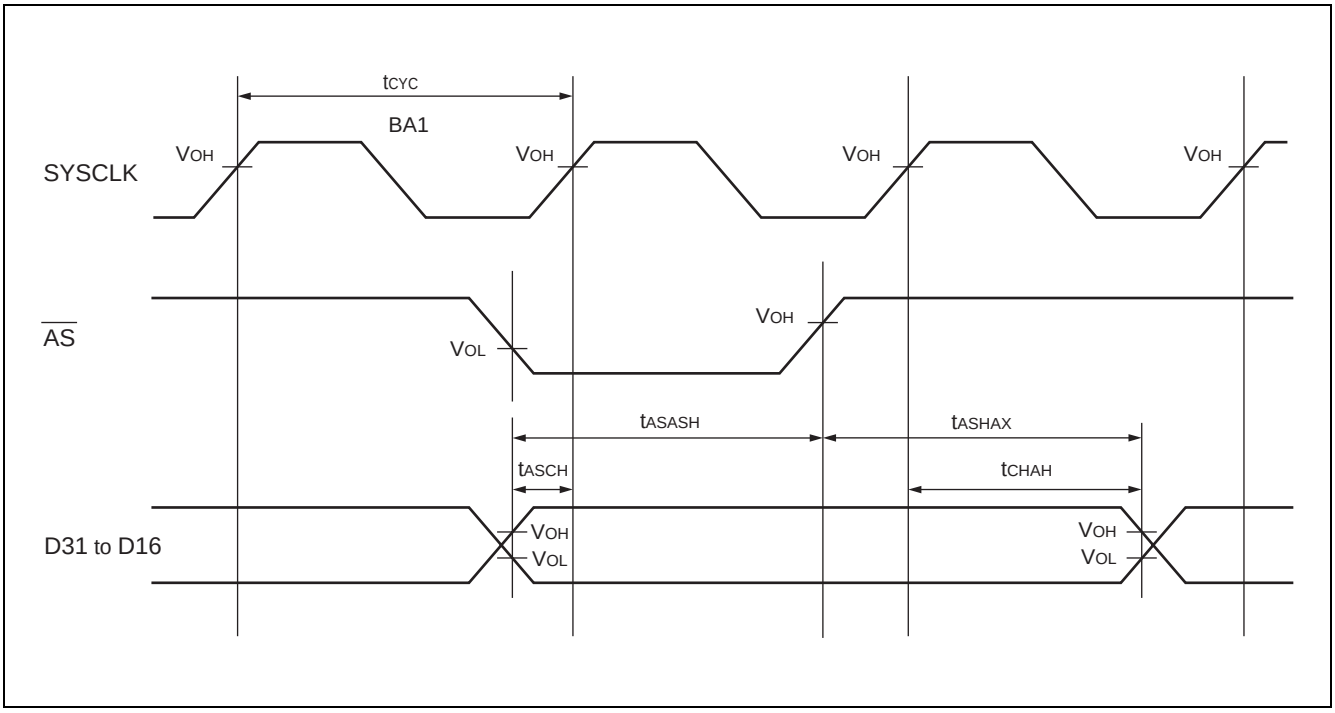

tCYC
BA1
MCLK
VOH
AS
tASLCH
tCHASH
VOL
CS0 to CS3
tCSLCH
tCHCSH
A23 to A00
tASCH
tCHAX
RD
tCHRL
tRLRH
tCHRH
tASRL
tRHAX
tRLDV
tRHDX
tDSRH
tAVDV
D31 to D16
WR0, WR1
tCHWL
tWLWH
tCHWH
tASWL
tWHAX
tWHDX
tDSWH
write

(5) Multiplex Bus Access Read/Write Operation

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
A15 to A00 Address AUDI setup time → SYSCLK ↑	t_{ASCH}	SYSCLK, D31 to D16	—	3	—	ns
SYSCLK ↑ → A15 to A00 Address AUDI hold time	t_{CHAX}			3	$t_{CYC}/2 + 6$	ns
A15 to A00 Address AUDI setup time → $\overline{AS}$ ↑	t_{ASASH}	SYSCLK, D31 to D16		12	—	ns
$\overline{AS}$ ↑ → A15 to A00 Address AUDI hold time	t_{ASHAX}			$t_{CYC} - 3$	$t_{CYC} + 3$	ns

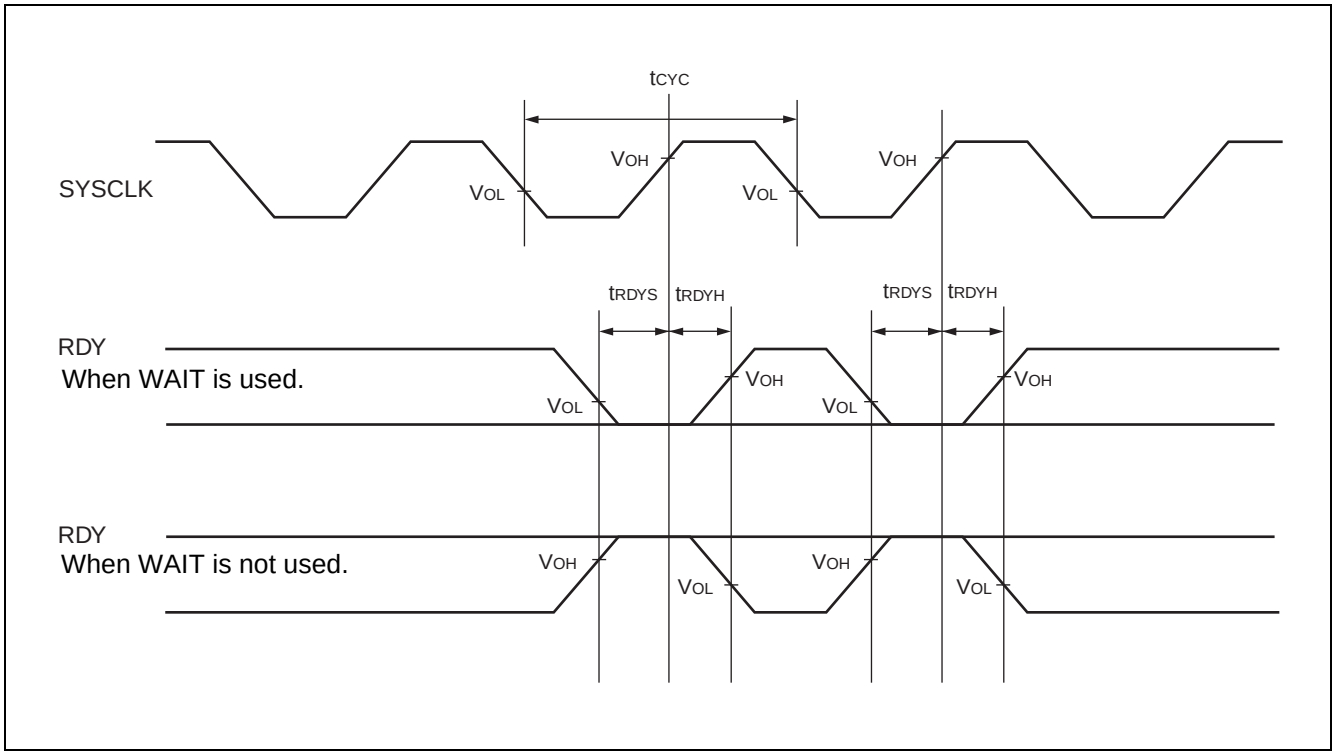
Notes : • This rating is not guaranteed when the CS → $\overline{RD}$/$\overline{WR}$ Setup Delay setting by AWR : bit1 is “0”.
• Beside this rating, normal bus interface ratings are applicable.
• t_{CYC} represents the cycle time. Refer to “(2) Clock Output Timing”.



(6) Ready Input Timings

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
RDY setup time → SYSCLK	t_{RDYS}	SYSCLK, RDY	—	15	—	ns
SYSCLK ↑ → RDY hold time	t_{RDYH}	SYSCLK, RDY	—	0	—	ns



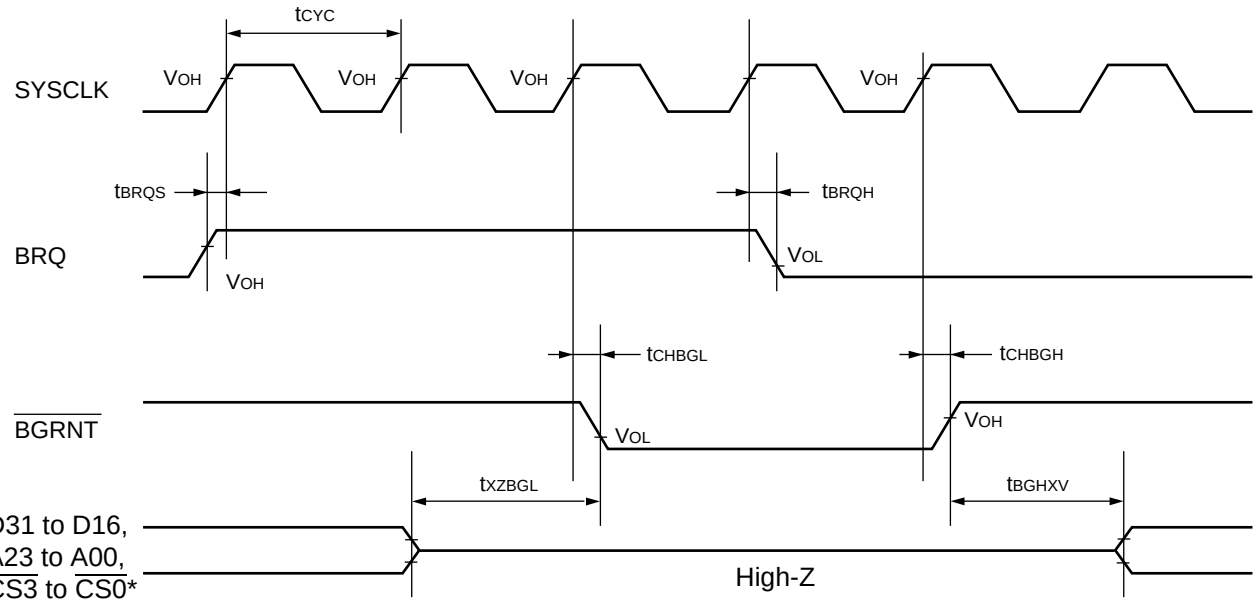
(7) Hold Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
BRQ setup time → SYSCLK ↑	t_{BRQS}	SYSCLK, BRQ	—	15	—	ns
SYSCLK ↑ → BRQ hold time	t_{BRQH}			0	—	ns
$\overline{BGRNT}$ delay time	t_{CHBGL}	SYSCLK, $\overline{BGRNT}$	—	t_{CYC} / 2 – 6	t_{CYC} / 2 + 6	ns
$\overline{BGRNT}$ delay time	t_{CHBGH}			t_{CYC} / 2 – 6	t_{CYC} / 2 + 6	ns
Pin floating → $\overline{BGRNT}$ fall time	t_{XZBGL}	$\overline{BGRNT}$, D31 to D16, A23 to A00, $\overline{CS3}$ to $\overline{CS0}$*		t_{CYC} – 10	t_{CYC} + 10	ns
$\overline{BGRNT}$ ↑ → Pin valid time	t_{BGHXV}			t_{CYC} – 10	t_{CYC} + 10	ns

* : These only apply in the case where the SREN bit of the area select register (ACR) is set to “1”.

Notes : • It takes 1 cycle or more from when BRQ is captured until $\overline{GBRNT}$ changes.
• t_{CYC} represents the cycle time. Refer to “(2) Clock Output Timing”.



* : These only apply in the case where the SREN bit of the area select register (ACR) is set to “1”.

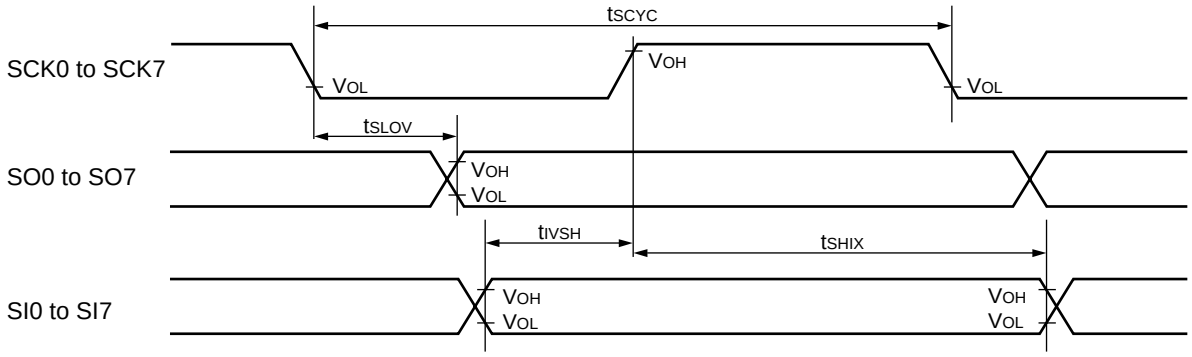
(8) UART, SIO Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

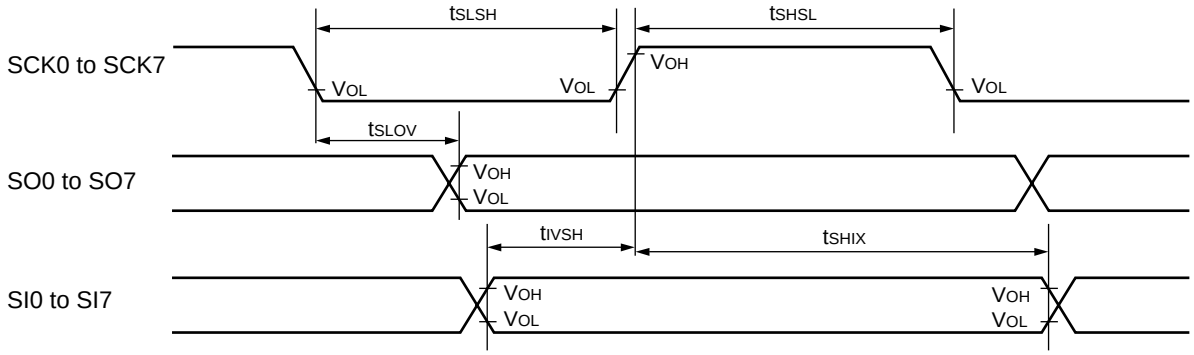
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock Cycle time	t_{SCYC}	SCK0 to SCK3, SCK6, SCK7	Internal shift lock mode	8 t_{CPP}	—	ns	MB91F353A/353A/352A/351A
		SCK0 to SCK7					MB91F355A/F356B/F357B/355A/354A
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK3, SCK6, SCK7, SO0 to SO3, SO6, SO7		− 80	+ 80		MB91F353A/353A/352A/351A
		SCK0 to SCK7, SO0 to SO7					MB91F355A/F356B/F357B/355A/354A
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK3, SCK6, SCK7, SI0 to SI3, SI6, SI7		100	—		MB91F353A/353A/352A/351A
		SCK0 to SCK7, SI0 to SI7					MB91F355A/F356B/F357B/355A/354A
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SCK6, SCK7, SI0 to SI3, SI6, SI7		60			MB91F353A/353A/352A/351A
		SCK0 to SCK7, SI4, SI5					MB91F355A/F356B/F357B/355A/354A
serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3, SCK6, SCK7	External shift clock mode	4 t_{CPP}			MB91F353A/353A/352A/351A
		SCK0 to SCK7					MB91F355A/F356B/F357B/355A/354A
serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3, SCK6, SCK7					MB91F353A/353A/352A/351A
		SCK0 to SCK7					MB91F355A/F356B/F357B/355A/354A
SCK ↓ → SO delay time	t_{SLOV}	SCK0 to SCK3, SCK6, SCK7, SO0 to SO3, SO6, SO7		—	150		MB91F353A/353A/352A/351A
		SCK0 to SCK7, SO0 to SO7					MB91F355A/F356B/F357B/355A/354A
Valid SI → SCK ↑	t_{IVSH}	SCK0 to SCK3, SCK6, SCK7, SI0 to SI3, SI6, SI7		60	—		MB91F353A/353A/352A/351A
		SCK0 to SCK7, SI0 to SI7					MB91F355A/F356B/F357B/355A/354A
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SCK6, SCK7, SI0 to SI3, SI6, SI7					MB91F353A/353A/352A/351A
		SCK0 to SCK7, SI0 to SI7					MB91F355A/F356B/F357B/355A/354A

Notes : • Above rating is for CLK synchronous mode.
• t_{CPP} represents the peripheral clock cycle time. Refer to “(1) Clock Timing”.

• Internal shift clock mode



• External shift clock mode

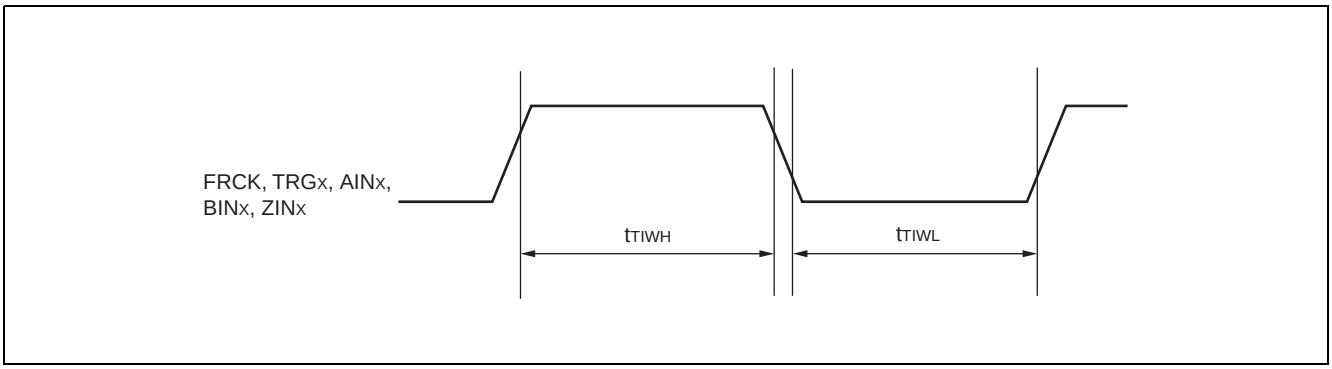


(9) Free-run timer Clock, PPG Timer Input Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCK, TRG0 to TRG4, AIN0, BIN0, ZIN0	—	2 t_{CPP}	—	ns	MB91F353A/353A/ 352A/351A
		FRCK, TRG0 to TRG5, AIN0, AIN1, BIN0, BIN1, ZIN0, ZIN1					MB91F355A/F356B/ F357B/355A/354A

Note : t_{CPP} represents the peripheral clock cycle time. Refer to “(1) Clock Timing”.

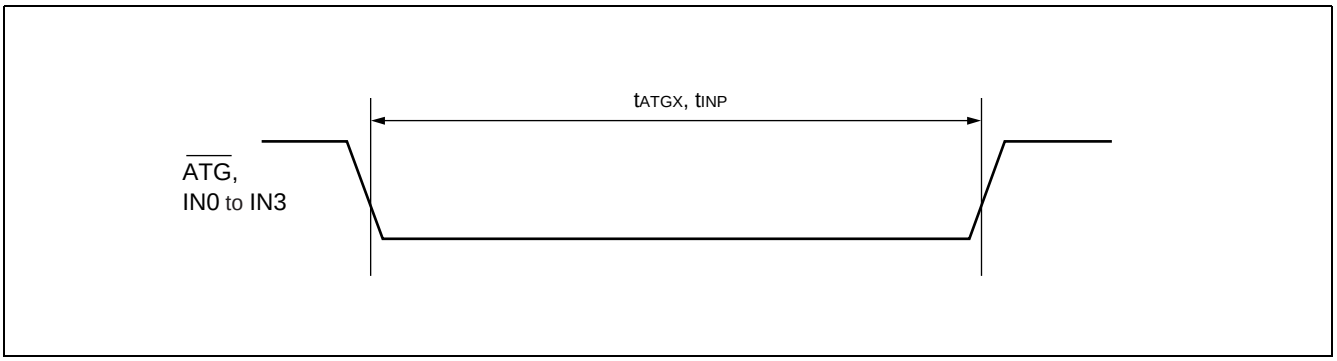


(10) Trigger Input Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
A/D activation trigger input time	t_{ATGX}	$\overline{ATG}$	—	5 t_{CPP}	—	ns
Input capture input trigger	t_{INP}	IN0 to IN3	—	5 t_{CPP}	—	ns

Note : t_{CPP} represents the peripheral clock cycle time. Refer to “(1) Clock Timing”.



(11)DMA controller timing*1

• For edge detection (block/step transfer mode, burst transfer mode)

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
DREQ Input pulse width	t_{DRWL}	DREQ0 to DREQ2	—	2 t_{CYC}*2	—	ns
DREQ Input pulse width	t_{DSWH}	DSTP0 to DSTP2		2 t_{CYC}*2	—	ns

*1 : The MB91F353A/353A/352A/351A does not have this standard.

*2 : t_{CYC} becomes t_{CP} when f_{CPT} is greater than f_{CP}.

• For level detection (demand transfer mode)

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
DREQ setup time	t_{DRS}	MCLK, DREQ0 to DREQ2	—	15	—	ns
DREQ hold time	t_{DRH}	MCLK, DREQ0 to DREQ2		0.0	—	ns
DSTP setup time	t_{DSTPS}	MCLK, DSTP0 to DSTP2		15	—	ns
DSTP hold time	t_{DSTPH}	MCLK, DSTP0 to DSTP2		0.0	—	ns

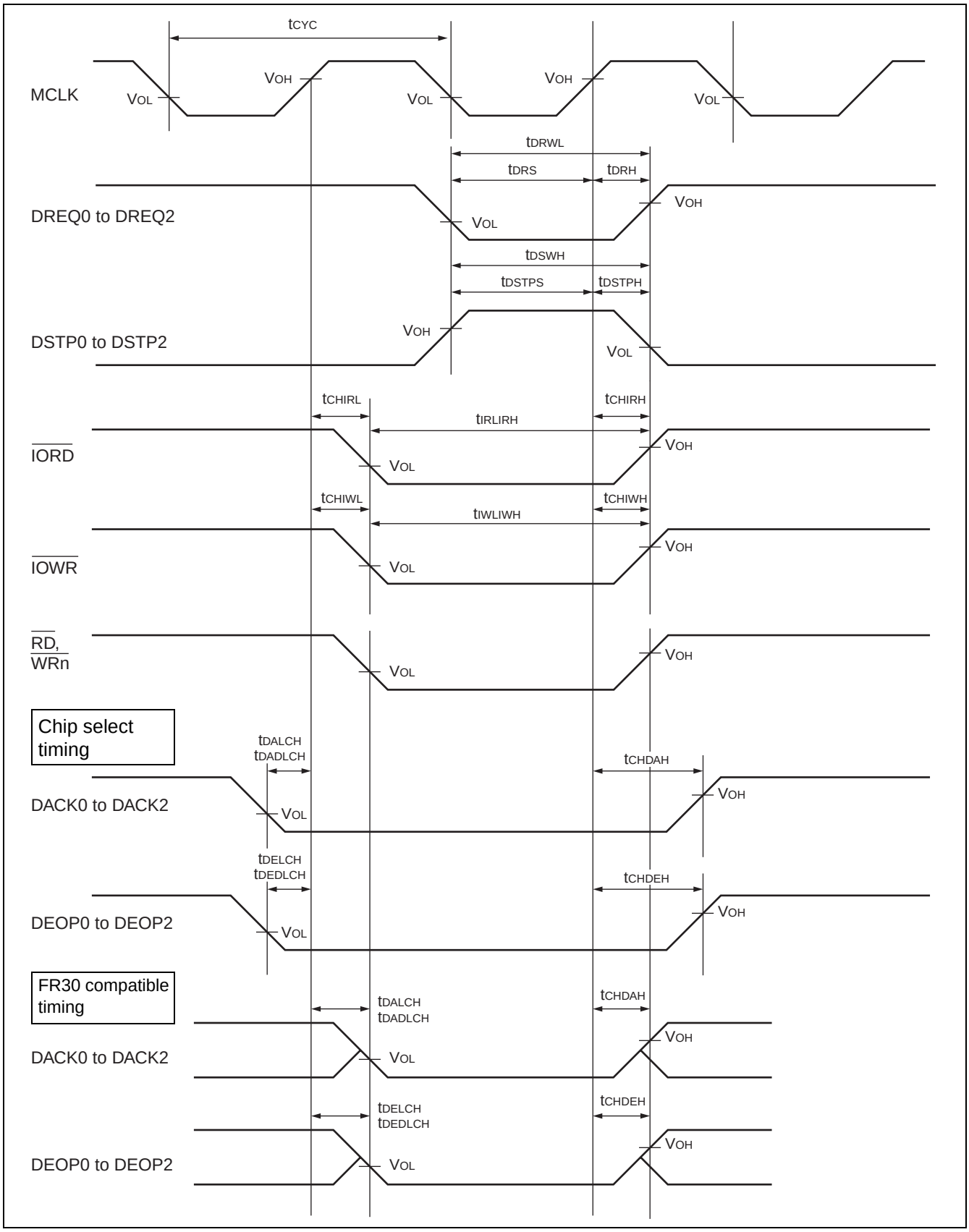
• Common operation mode

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
DACK delay time	t_{DALCH}	MCLK, DACK0 to DACK2	AWRxL* : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DADLCH}		AWR0L : W02 = 1	− 3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDAH}		—	—	$t_{CYC}/2 + 6$	ns	CS timing
				—	6	ns	FR30 compatible
DEOP delay time	t_{DELCH}	MCLK, DEOP0 to DEOP2	AWR0L : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DEDLCH}		AWRxL* : W02 = 1	− 3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDEH}		—	—	$t_{CYC}/2 + 6$	ns	CS timing
				—	6	ns	FR30 compatible
$\overline{IORD}$ delay time	t_{CHIRL}	MCLK, $\overline{IORD}$	—	—	6	ns	
	t_{CHIRH}			—	6	ns	
$\overline{IOWR}$ delay time	t_{CHIWL}	MCLK, $\overline{IOWR}$		—	6	ns	
	t_{CHIWH}			—	6	ns	
$\overline{IORD}$ minimum pulse width	t_{IRLIRH}	$\overline{IORD}$		12	—	ns	
$\overline{IOWR}$ minimum pulse width	t_{IWLIWH}	$\overline{IOWR}$		12	—	ns	

* : AWRxL : Area Wait Register.

Note : t_{CYC} represents the cycle time. Refer to “(2) Clock output timing”.


tCYC
MCLK
VOH
VOL
tDRWL
tDRS
tDRH
DREQ0 to DREQ2
tDSWH
tDSTPS
tDSTPH
DSTP0 to DSTP2
tCHIRL
tCHIRH
tIRLIRH
IORD
tCHIWL
tCHIWH
tIWLIWH
IOWR
RD, WRn
Chip select timing
tDALCH
tDADLCH
tCHDAH
DACK0 to DACK2
tDELCH
tDEDLCH
tCHDEH
DEOP0 to DEOP2
FR30 compatible timing

(12) I²C Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

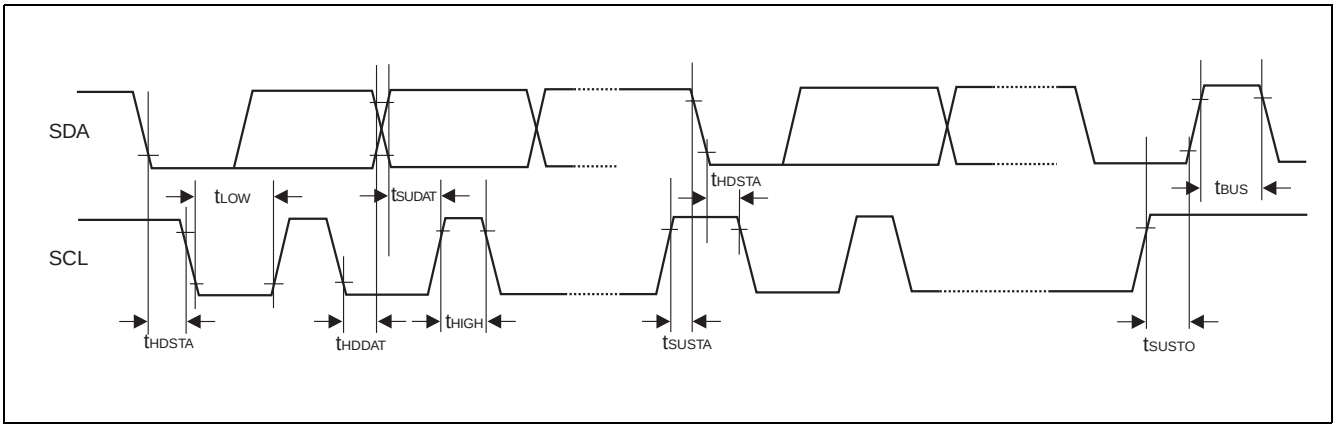
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.0 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
“L” width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
“H” width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistance and load capacitance of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} only has to be met if the device does not extend the “L” width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



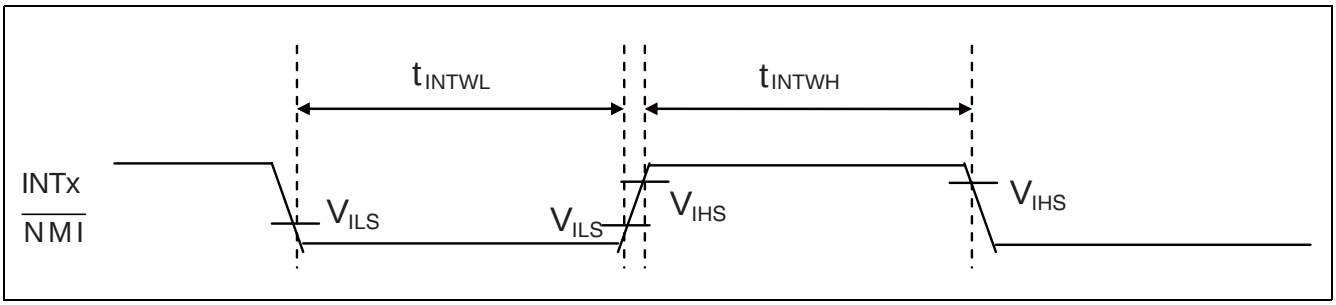
(13) External Interrupt Input Timing

(V_{CC} = 3.0 V to 3.6 V, V_{CC} = 2.7 V to 3.6 V (MB91F356B/F357B only) ,
V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Standard-mode		Unit	Remark
				Min	Max		
Input pulse width	t_{INTWH} t_{INTWL}	INT0 to INT7 $\overline{NMI}$	—	3 t_{CYCP}	—	ns	*1 MB91F353A/353A/352A/351A
				1.0	—	µs	*2 MB91F353A/353A/352A/351A
		INT0 to INT15 $\overline{NMI}$	—	3 t_{CYCP}	—	ns	*1 MB91F355A/F356B/F357B/355A/354A
				1.0	—	µs	*2 MB91F355A/F356B/F357B/355A/354A

*1 : t_{CYCP} : The cycle time of peripheral clock (except STOP mode)

*2 : At STOP mode



5. Electrical Characteristics for the A/D Converter

• **MB91F353A/353A/352A/351A**

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, AVRH = 3.0 V to 3.6 V, V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error *1	—	—	− 5.0	—	+ 5.0	LSB	At AV_{CC} = 3.3 V, AVRH = 3.3 V
Nonlinear error *1			− 3.5		+ 3.5		
Differential linear error *1			− 2.5		+ 2.5		
Zero transition voltage *1		AN7 to AN0	AVRL − 2.0	AVRL + 1.0	AVRL + 6.0		
Full-transition voltage *1			AVRH − 5.5	AVRH + 1.5	AVRH + 3.0		
Conversion time		—	1.48*2	—	300	µs	
Analog power supply current (analog + digital)	I_A	AV_{CC}	—	7	—	mA	
	I_{AH}			—	5	µA	At STOP
Reference power supply current (between AVRH and AVRL)	I_R	AVRH		470	—		At AVRH = 3.0 V, AVRL = 0.0 V
	I_{RH}			—	10		At STOP
Analog input capacitance	—	AN7 to AN0		40	—	pF	
Interchannel disparity				—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : When the peripheral resource clock frequency is 25.0 MHz, set the Conversion Time Setting Register (ADCT) to a value equal to or greater than 5334_H.
Set each bit as follows :
Sampling time : SAMP3 to SAMP0 ≥ 5_H
Conversion time a : CV03 to CV0 ≥ 3_H
Conversion time b : CV13 to CV0 ≥ 3_H
Conversion time c : CV23 to CV0 ≥ 4_H

• **MB91F355A/F356B/F357B/355A/354A/V350A**

(V_{CC} = AV_{CC} = 3.0 V to 3.6 V, AVRH = 3.0 V to 3.6 V, V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40°C to + 85°C)

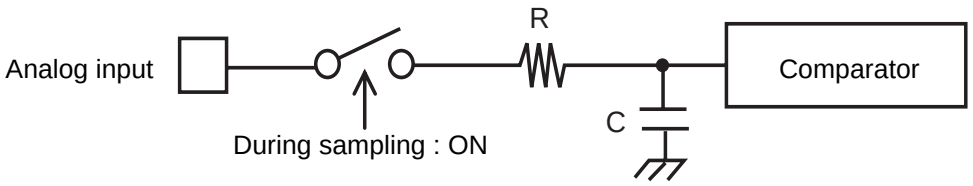
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error*1			− 5.0		+ 5.0	LSB	AV_{CC} = 3.3 V, AVRH = 3.3 V
Nonlinear error*1			− 3.5		+ 3.5		
Differential linear error*1			− 2.5		+ 2.5		
Zero transition voltage*1		AN11 to AN0	AVRL − 2.0	AVRL + 1.0	AVRL + 6.0		
Full-transition voltage*1			AVRH − 5.5	AVRH + 1.5	AVRH + 3.0		
Conversion time		—	1.48*2	—	300	µs	
Analog power supply current (analog + digital)	I_A	AV_{CC}	—	8	—	mA	
	I_{AH}			—	5	µA	At stop
Reference power supply current (between AVRH and AVRL)	I_R	AVRH		470	—		AVRH = 3.0 V, AVRL = 0.0 V
	I_{RH}			—	10		At stop
Analog input capacitance	—	AN11 to AN0		40	—	pF	
Interchannel disparity				—	4	LSB	

*1 : Measured in the CPU sleep state

*2 : When the peripheral resource clock frequency is 25.0 MHz, set the Conversion Time Setting Register (ADCT) to a value equal to or greater than 5334_H.
Set each bit as follows :
Sampling time : SAMP3 to SAMP0 ≥ 5_H
Conversion time a : CV03 to CV0 ≥ 3_H
Conversion time b : CV13 to CV0 ≥ 3_H
Conversion time c : CV23 to CV0 ≥ 4_H

- **About the external impedance and sampling time of the analog input**
  - A/D converter with sample and hold circuit. If the external impedance is too high to ensure sufficient sampling time, the analog voltage of the internal sample and hold capacitor will not be sufficiently charged, adversely affecting the A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Moreover, if sufficient sampling time cannot be ensured, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit schematic

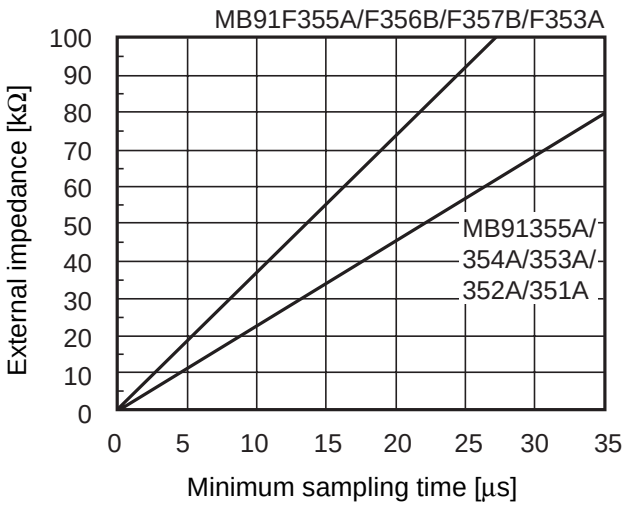


	R	C
MB91355A/354A/353A/352A/351A	0.18 kΩ (Max)	63.0 pF (Max)
MB91F355A/F353A/F356B/F357B	0.18 kΩ (Max)	39.0 pF (Max)

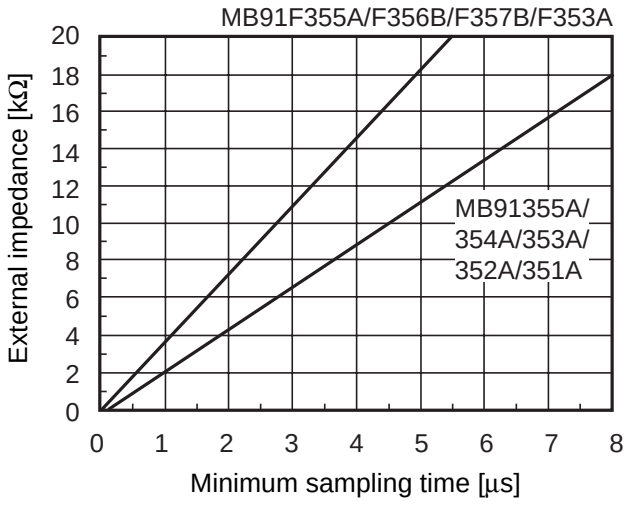
Note : The values are reference values.

- The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

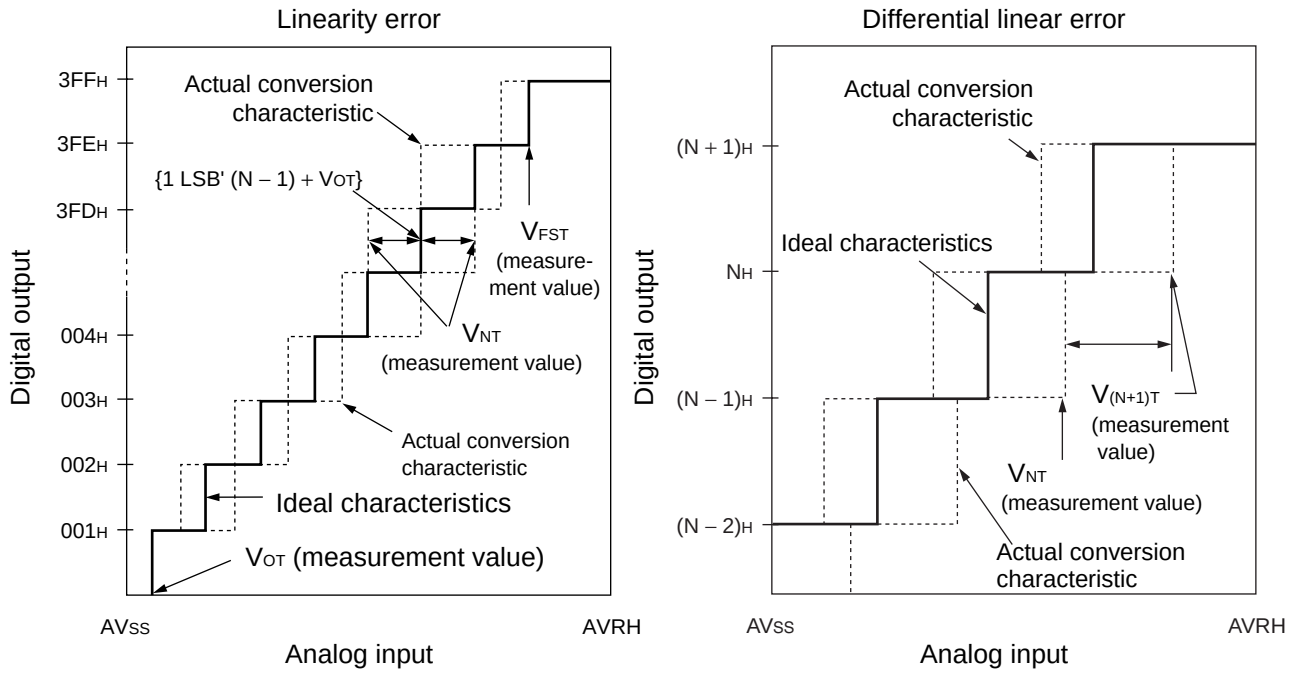


- **About errors**

The smaller the value of | AVRH−AVSS | , the greater the relative error.

Definition of A/D Converter Terms

- Resolution
  Analog variation that is recognized by an A/D converter.
- Linearity error
  The difference between the line connecting the zero transition point ("00 0000 0000"←→"00 0000 0001") and the full-scale transition point ("11 1111 1110" ←→ "11 1111 1111") and the actual conversion characteristics.
- Differential linear error
  Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1\ LSB' \times (N-1) + V_{OT}\}}{1\ LSB'}\ [LSB]$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB'} - 1\ [LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

N : A/D converter digital output value

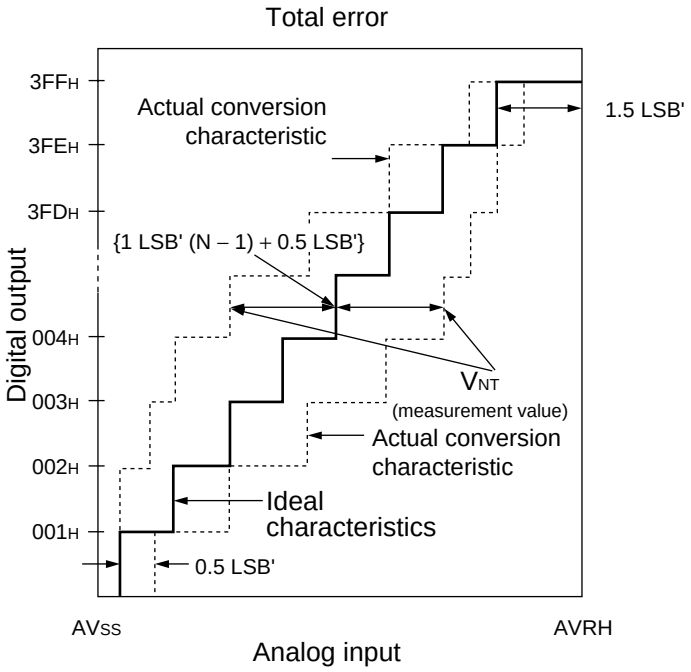
V_{OT} : The voltage at which the digital output transitions from $(000)_H$ to $(001)_H$

V_{FST} : The voltage at which the digital output transitions from $(3FE)_H$ to $(3FF)_H$

V_{NT} : The voltage at which the digital output transitions from $(N-1)_H$ to N_H

• Total error

This error indicates the difference between the actual and ideal values, including the zero transition error/full-scale transition error/linearity error.



$$1LSB' \text{ (Ideal value)} = \frac{AVRH - AV_{SS}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value

V_{NT} : The voltage at which the digital output transitions from $(N + 1)_H$ to N_H

V_{OT}' (Ideal value) = AV_{SS} + 0.5 LSB' [V]

V_{FST}' (Ideal value) = AVRH – 1.5 LSB' [V]

6. Electrical Characteristics for the D/A Converter

(V_{CC} = DAVC = 3.0 V to 3.6 V, V_{SS} = DAVS = AV_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	8	bit	
Nonlinear error			− 2.0	—	+ 2.0	LSB	When the output is unloaded
Differential linear error			− 1.0	—	+ 1.0		When the output is unloaded
Conversion speed			—	0.6	—	µs	When load capacitance (C_L) = 20 pF
				3.0			When load capacitance (C_L) = 100 pF
Output high impedance		DA0, DA1	2.0	2.9	3.8	kΩ	MB91F353A/353A/352A/351A
		DA0 to DA2					MB91F355A/F356B/F357B/355A/354A
Analog current	—	DAVC	—	40	—	µA	10 µs conversion when the output is unloaded
	I_{ADA}			—	460*		Input digital code, when fixed at $7A_H$ or 85_H
	I_{ADAH}			0.1	—		At power-down

* : This D/A converter varies in current consumption depending on each input digital code.

This rating indicates the current consumption when the digital code that maximizes current consumption is input.

■ FLASH MEMORY ERASE and PROGRAM PERFORMANCE

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Ta = +25 °C V_{CC} = 3.3 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time		—	8	—	s	Excludes 00_H programming prior erasure
Half word (16-bit width) programming time		—	16	3600	µs	Excludes system-level overhead
Erase/program cycle	—	10000	—	—	cycle	
Flash data retention time	Average Ta = +85 °C	20	—	—	year	*

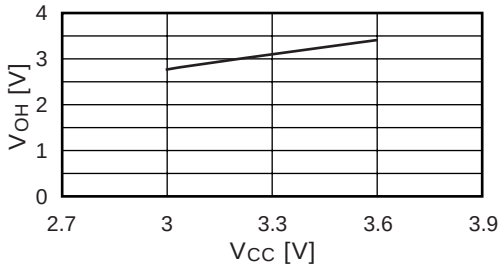
* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C).

■ EXAMPLE CHARACTERISTICS

• MB91F353A

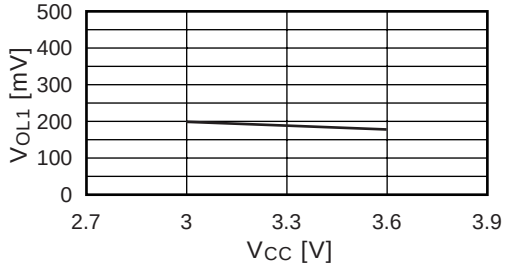
"H" level output voltage

V_{OH} vs. V_{CC}
Ta = + 25 °C



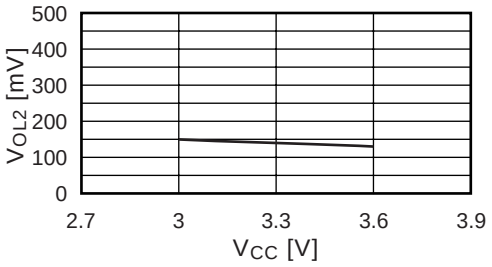
"L" level output voltage

V_{OL1} vs. V_{CC}
Ta = + 25 °C



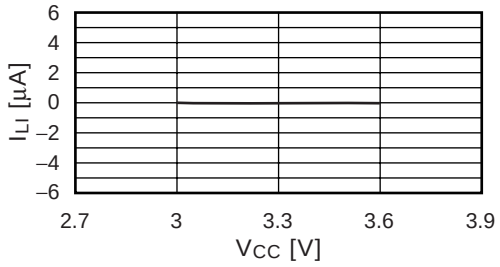
"L"level output voltage (N-ch open-drain)

V_{OL2} vs. V_{CC}
Ta = + 25 °C



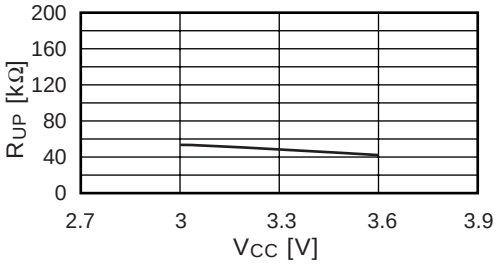
Input leak current

I_{LI} vs. V_{CC}
Ta = + 25 °C



Pull-up resistance

R_{UP} vs. V_{CC}
Ta = + 25 °C



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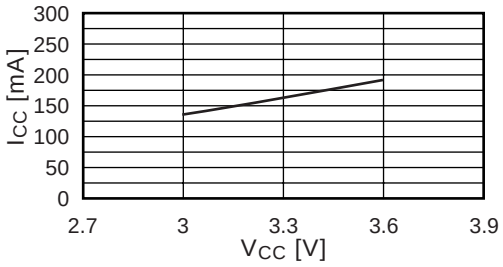
Power supply current

I_{CC} vs. V_{CC}

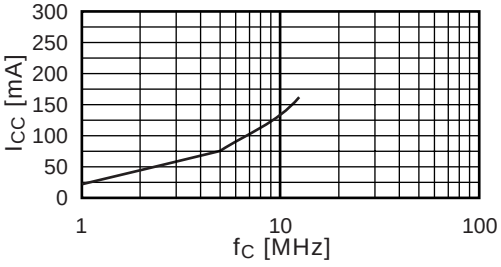
Ta = + 25 °C, f_{CP} = 50 MHz, f_{CPP} = 25 MHz



Power supply current

I_{CC} vs. f_C

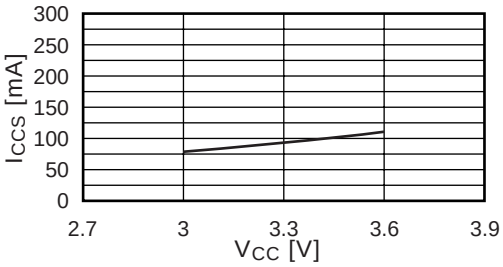
Ta = + 25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × fc (multiplied by4)



Power supply current at sleep

I_{CCS} vs. V_{CC}

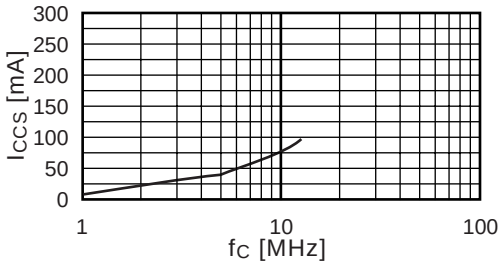
Ta = + 25 °C, f_{CP} = 50 MHz, f_{CPP} = 25 MHz



Power supply current at sleep

I_{CCS} vs. f_C

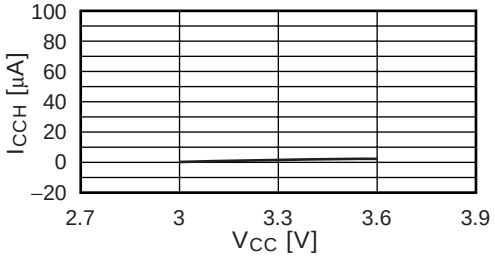
Ta = + 25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × fc (multiplied by 4)



Power supply current at stop

I_{CCH} vs. V_{CC}

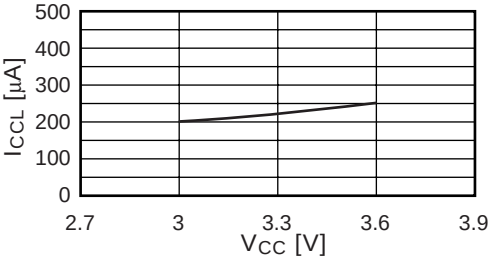
Ta = + 25 °C



Sub-RUN power supply current

I_{CCL} vs. V_{CC}

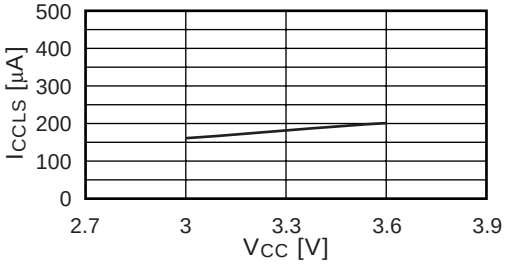
Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = 25 MHz



Sub sleep power supply current

I_{CCLS} vs. V_{CC}

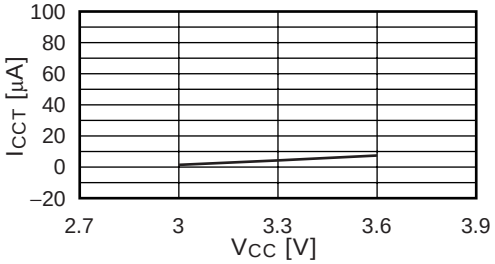
Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = f_{CPT} = 32 kHz



Watch mode power supply current

I_{CCT} vs. V_{CC}

Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = f_{CPT} = 32 kHz



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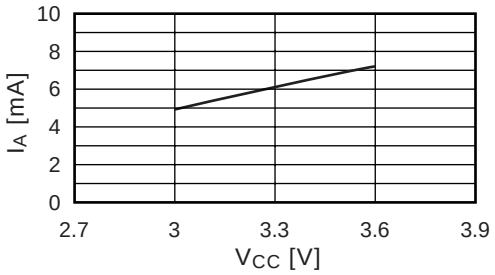
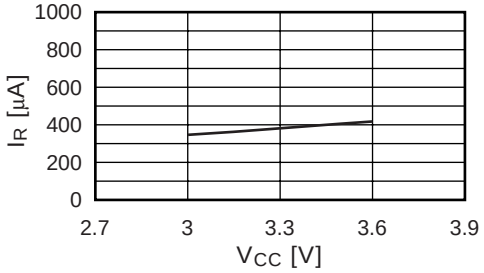
A/D converter power supply current

I_A vs. V_{CC}
Ta = + 25 °C



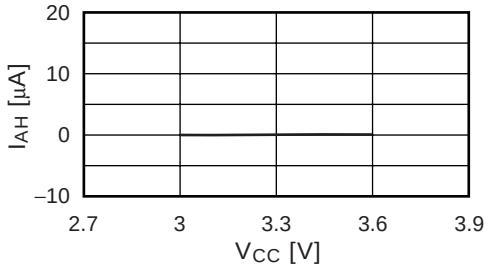
A/D converter reference power supply current

I_R vs. V_{CC}
Ta = + 25 °C



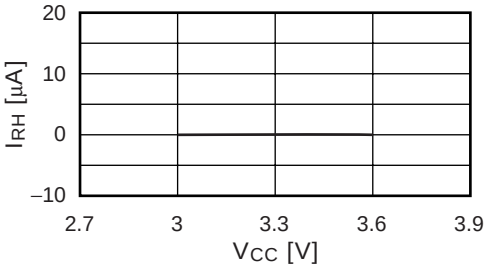
A/D converter power supply current at stop

I_{AH} vs. V_{CC}
Ta = + 25 °C



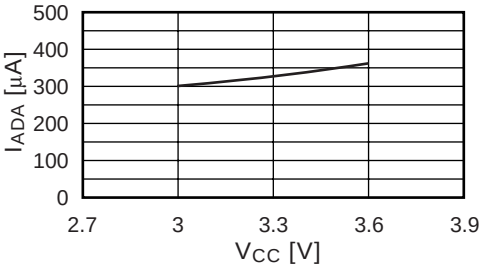
A/D converter reference power supply current at stop

I_{RH} vs. V_{CC}
Ta = + 25 °C



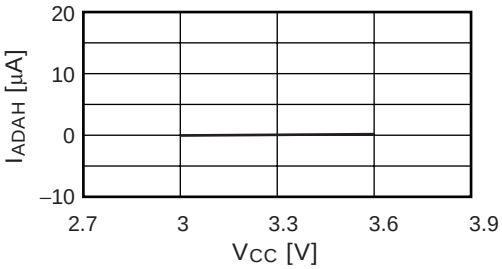
D/A converter power supply current <per 1 channel>

I_{ADA} vs. V_{CC}
Ta = + 25 °C



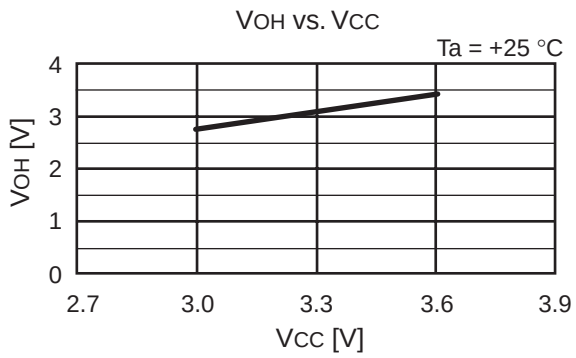
D/A converter power supply current at power down

I_{ADAH} vs. V_{CC}
Ta = + 25 °C

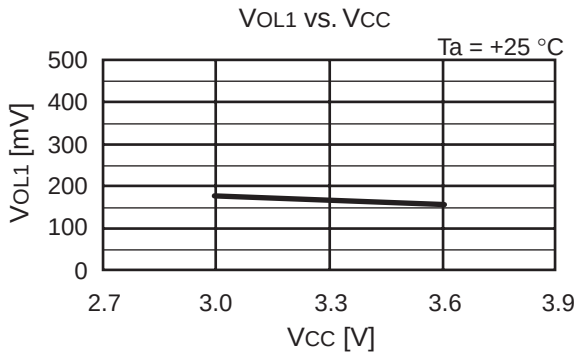


• MB91355A

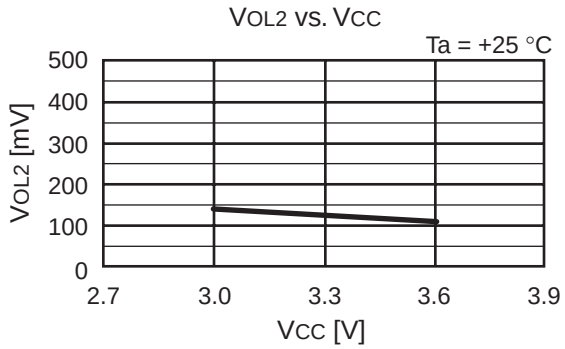
"H" level output voltage



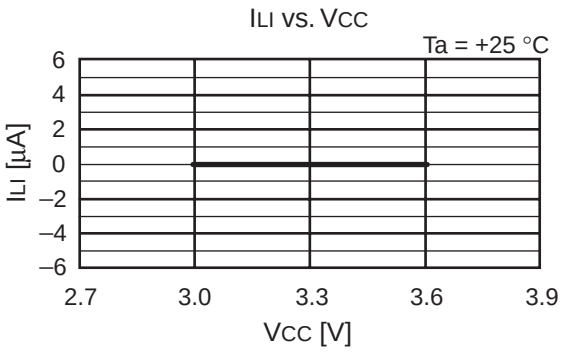
"L" level output voltage



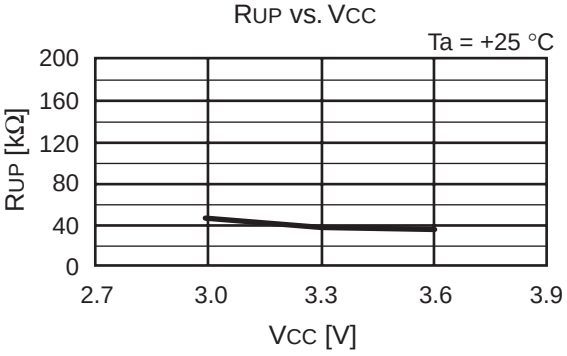
"L" level output voltage (N-ch open-drain)



Input leak current



Pull-up resistance



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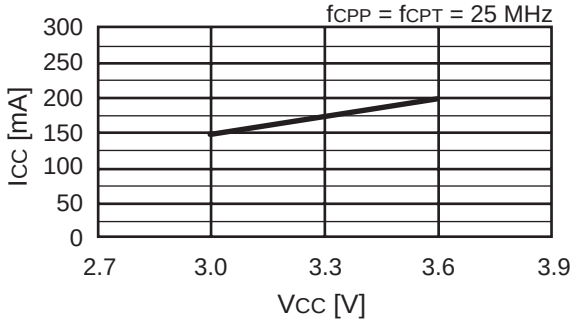
Power supply current

I_{CC} vs. V_{CC}

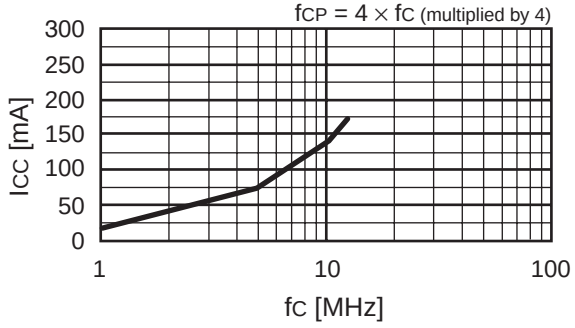
Ta = +25 °C, f_{CP} = 50 MHz, f_{CPP} = f_{CPT} = 25 MHz



Power supply current

I_{CC} vs. f_C

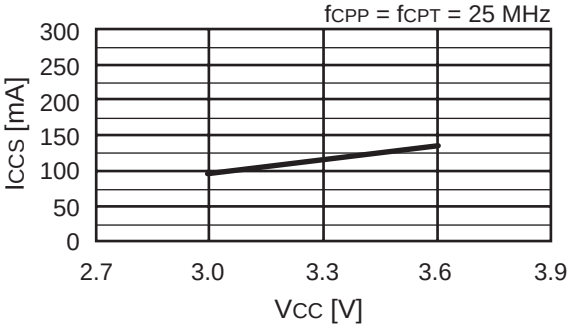
Ta = +25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × f_C (multiplied by 4)



Power supply current at sleep

I_{CCS} vs. V_{CC}

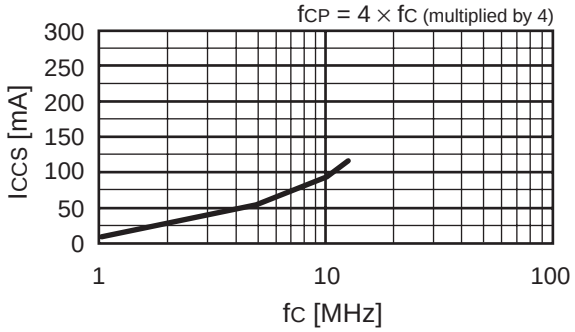
Ta = +25 °C, f_{CP} = 50 MHz, f_{CPP} = f_{CPT} = 25 MHz



Power supply current at sleep

I_{CCS} vs. f_C

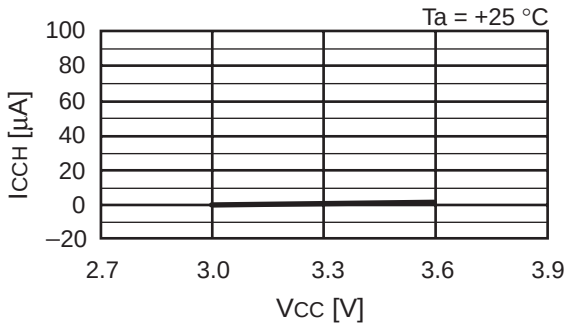
Ta = +25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × f_C (multiplied by 4)



Power supply current at stop

I_{CCH} vs. V_{CC}

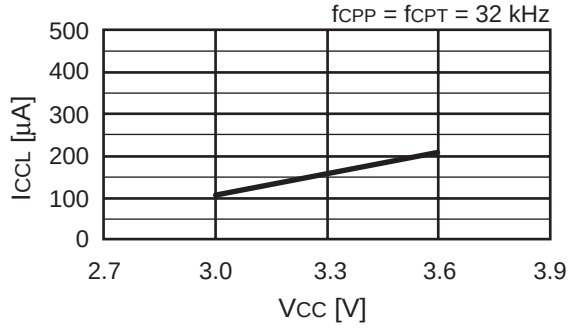
Ta = +25 °C



Sub RUN power supply current

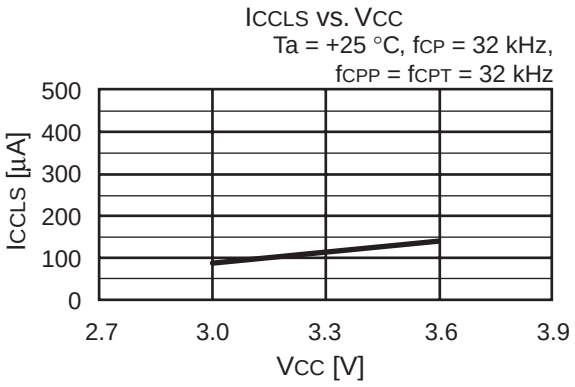
I_{CCL} vs. V_{CC}

Ta = +25 °C, f_{CP} = 32 kHz, f_{CPP} = f_{CPT} = 32 kHz

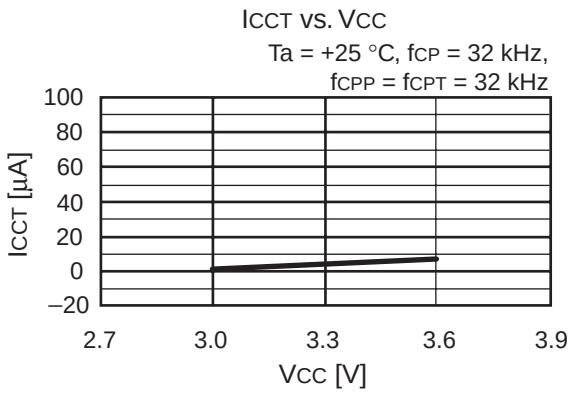


(Continued)

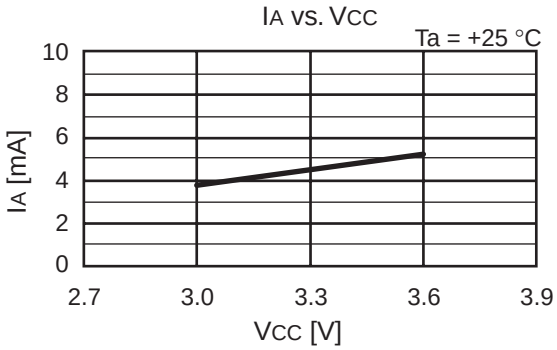
Sub sleep power supply current



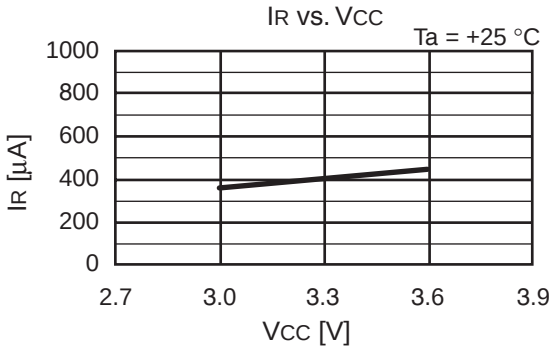
Watch mode power supply current



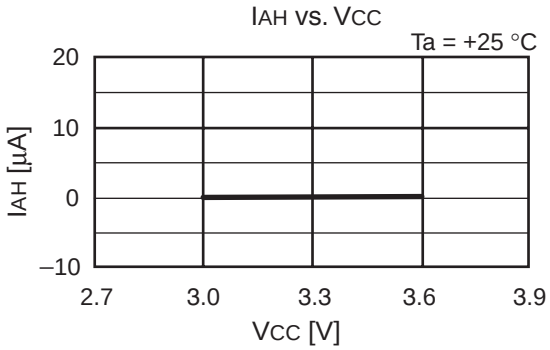
A/D converter power supply current



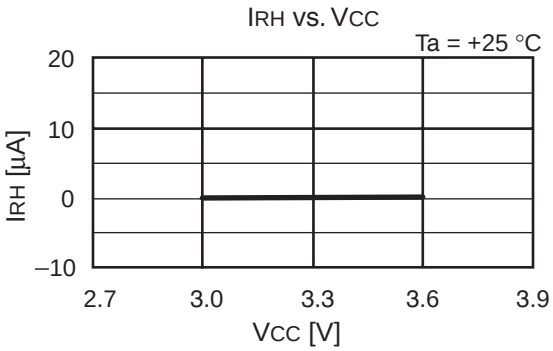
A/D converter reference power supply voltage



A/D converter power supply current at stop



A/D converter reference power supply current at stop



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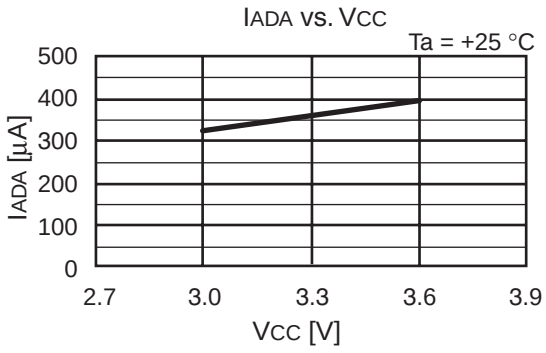
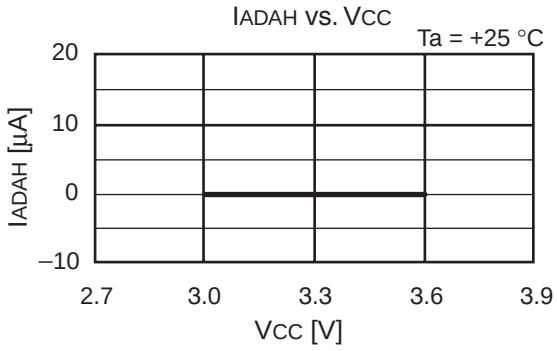
D/A converter power supply current
< per 1 channel >



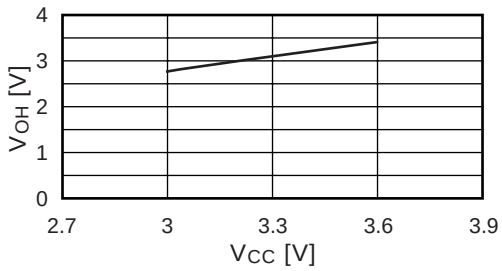
D/A converter power supply current at power down



• MB91353A/352A/351A

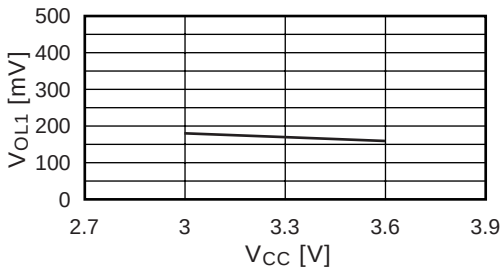
"H" level output voltage

V_{OH} vs. V_{CC}
Ta = + 25 °C



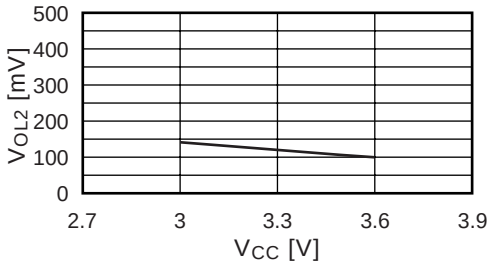
"L" level output voltage

V_{OL1} vs. V_{CC}
Ta = + 25 °C



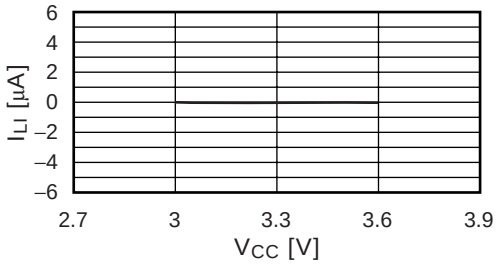
"L"level output voltage (N-ch open-drain)

V_{OL2} vs. V_{CC}
Ta = + 25 °C



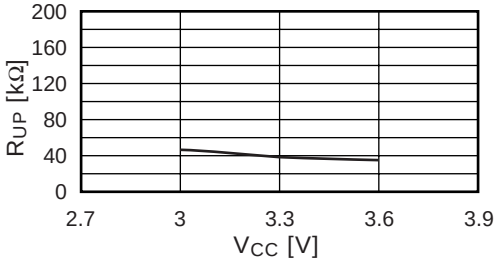
Input leak current

I_{LI} vs. V_{CC}
Ta = + 25 °C



Pull-up resistance

R_{UP} vs. V_{CC}
Ta = + 25 °C

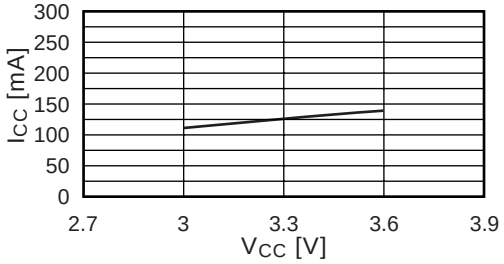


(Continued)

Power supply current

I_{CC} vs. V_{CC}

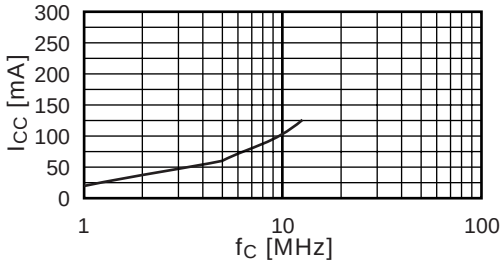
Ta = + 25 °C, f_{CP} = 50 MHz, f_{CPP} = 25 MHz



Power supply current

I_{CC} vs. f_C

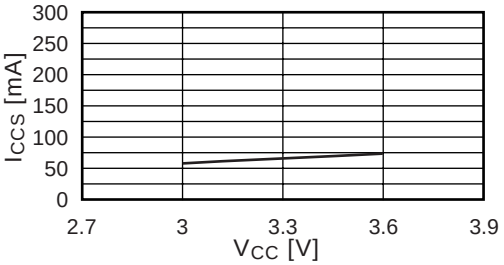
Ta = + 25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × fc (multiplied by4)



Power supply current at sleep

I_{CCS} vs. V_{CC}

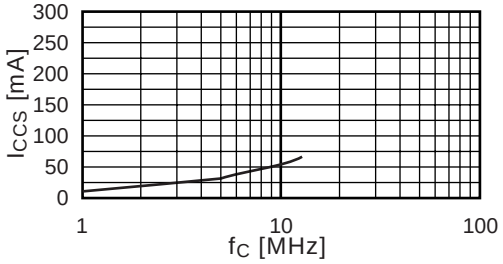
Ta = + 25 °C, f_{CP} = 50 MHz, f_{CPP} = 25 MHz



Power supply current at sleep

I_{CCS} vs. f_C

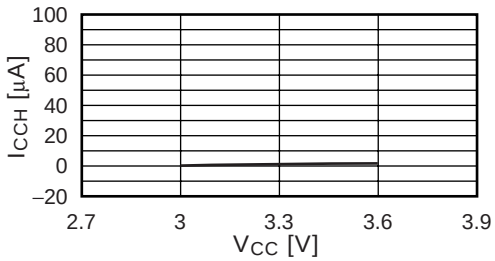
Ta = + 25 °C, V_{CC} = 3.3 V, f_{CP} = 4 × fc (multiplied by 4)



Power supply current at stop

I_{CCH} vs. V_{CC}

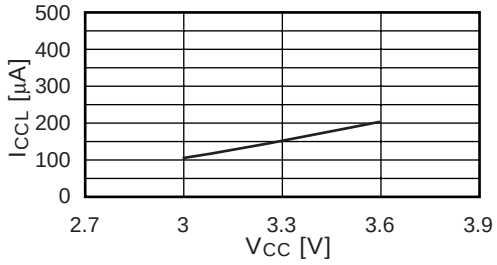
Ta = + 25 °C



Sub-RUN power supply current

I_{CCL} vs. V_{CC}

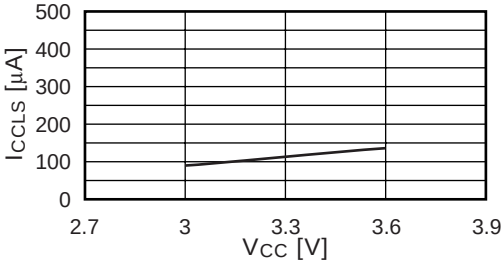
Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = 25 MHz



Sub sleep power supply current

I_{CCLS} vs. V_{CC}

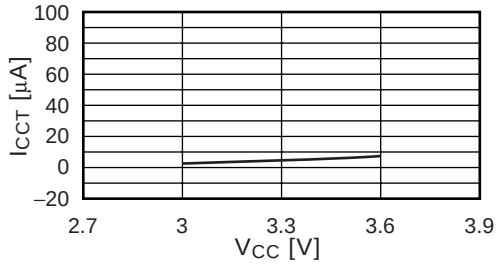
Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = f_{CPT} = 32 kHz



Watch mode power supply current

I_{CCT} vs. V_{CC}

Ta = + 25 °C, f_{CP} = 32 kHz, f_{CPP} = f_{CPT} = 32 kHz



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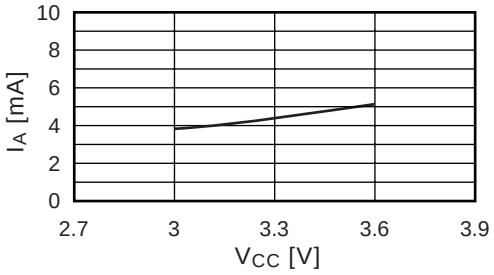
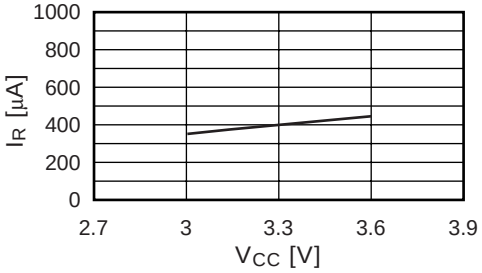
A/D converter power supply current

I_A vs. V_{CC}
Ta = + 25 °C



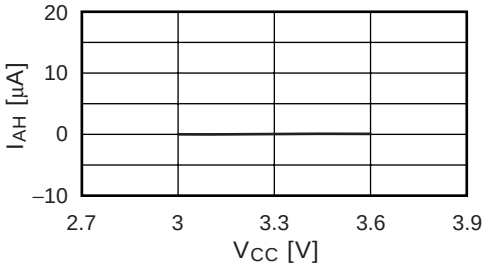
A/D converter reference power supply current

I_R vs. V_{CC}
Ta = + 25 °C



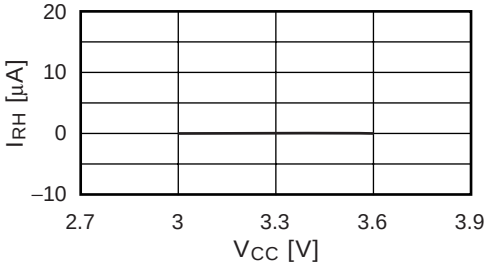
A/D converter power supply current at stop

I_{AH} vs. V_{CC}
Ta = + 25 °C



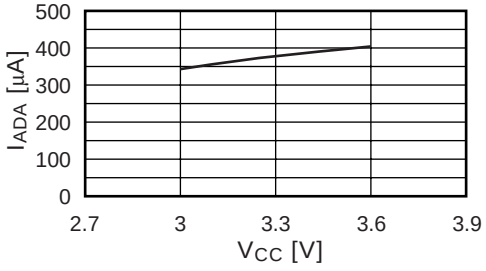
A/D converter reference power supply current at stop

I_{RH} vs. V_{CC}
Ta = + 25 °C



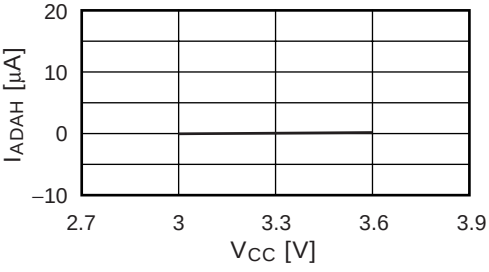
D/A converter power supply current <per 1 channel>

I_{ADA} vs. V_{CC}
Ta = + 25 °C



D/A converter power supply current at power down

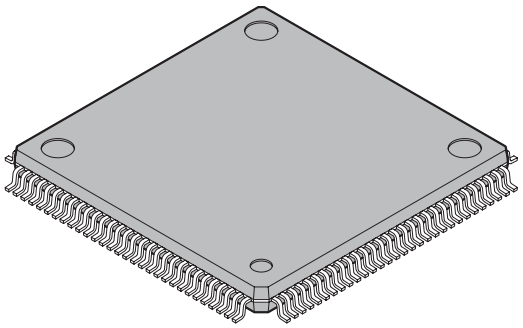
I_{ADAH} vs. V_{CC}
Ta = + 25 °C



■ ORDERING INFORMATION

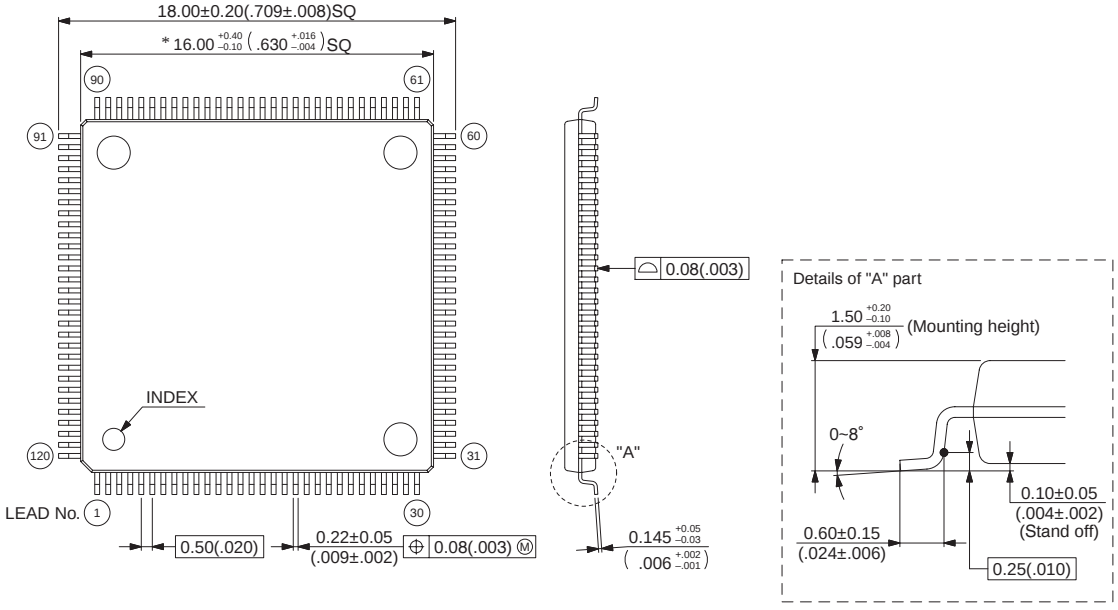
Part number	Package	Remarks
MB91F355APMT-002	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91F356BPMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91F357BPMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91355APMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91354APMT	176-pin plastic LQFP (FPT-176P-M02)	Lead-free Package
MB91F353APMT	120-pin plastic LQFP (FPT-120P-M21)	Lead-free Package
MB91351APMT	120-pin plastic LQFP (FPT-120P-M21)	Lead-free Package
MB91352APMT	120-pin plastic LQFP (FPT-120P-M21)	Lead-free Package
MB91353APMT	120-pin plastic LQFP (FPT-120P-M21)	Lead-free Package

■ PACKAGE DIMENSION

120-pin plastic LQFP  (FPT-120P-M21)	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

120-pin plastic LQFP
(FPT-120P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Resin protrusion is +0.25(.010) MAX(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

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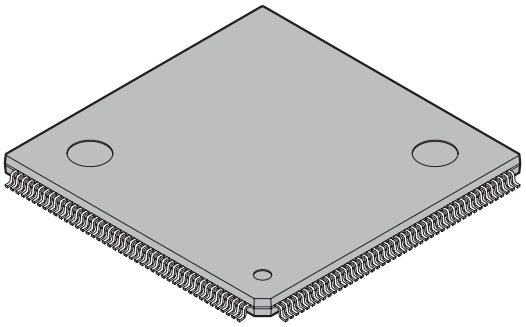
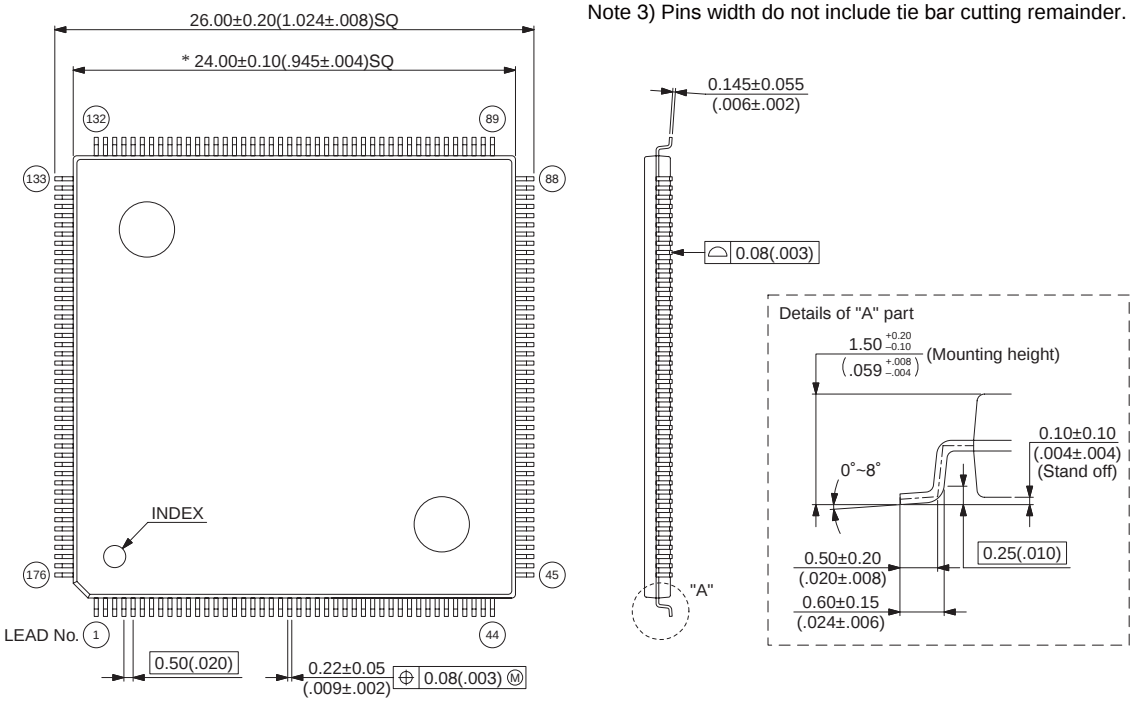
176-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	24.0 × 24.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.86g
(FPT-176P-M02)	Code (Reference)	P-LFQFP176-24×24-0.50

176-pin plastic LQFP
(FPT-176P-M02)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
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■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
98	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Changed the Internal operating clock frequency; Value (Min) : 2.94 → 3.13 Changed the Internal operating clock cycle time; Value (Max) : 340 → 320
118	■ ELECTRICAL CHARACTERISTICS (13) External Interrupt Input Timing	Added (13) External Interrupt Input Timing

The vertical lines marked in the left side of the page show the changes.

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