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NTE4013B & NTE4013BT
Integrated Circuit
CMOS, Dual D–Type Flip–Flop

Description:

The NTE4013B and NTE4013BT dual D–type flip–flops are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each flip–flop has independent Data (D), Direct Set (S), Direct Reset (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip–flops for counter and toggle applications.

Features:

- Supply Voltage Range: 3V to 15V
- High Noise Immunity: $0.45V_{DD}$ Typ
- Diode Protection on All Inputs
- Capable of Driving Two Low–Power TTL Loads of One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Available in Two Package Types:
  NTE4013B (14–Lead DIP)
  NTE4013BT (SOIC–14 Surface Mount)

Absolute Maximum Ratings: (V_{SS} = 0V, Note 1 unless otherwise specified)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18V
Input or Output Voltage (DC or Transient), V_{in}, V_{out} . . . . . –0.5 to V_{DD}+0.5V
Input or Output Current (DC or Transient), Per Pin, I_{in}, I_{out} . . . . . ±10mA
Power Dissipation, P_D 500mW
Derate Above 65°C . . . . . 7mW/°C
Operating Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed, they are meant to imply that the device should be operated at these limits. The tables of “Recommended Operating Conditions” and “Electrical Characteristics” provide conditions for actual device operation.

Recommended Operating Conditions: (V_{SS} = 0V unless otherwise specified)

DC Supply Voltage, V_{DD} . . . . . +3V_{DC} to +15V_{DC}
Input Voltage, V_{IN} . . . . . 0V_{DC} to V_{DD}
Operating Ambient Temperature Range, T_A . . . . . –40° to +85°C

Electrical Characteristics: (V_{SS} = 0V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	V_{DD}	Test Conditions		Min	Typ	Max	Unit
Output Voltage, "0" Level	V_{OL}	5	$\|I_O\|$ < 1.0µA		–	–	0.05	V
		10			–	–	0.05	V
		15			–	–	0.05	V
Output Voltage, "1" Level	V_{OH}	5	$\|I_O\|$ < 1.0µA		4.95	–	–	V
		10			9.95	–	–	V
		15			14.95	–	–	V
Input Voltage, "0" Level	V_{IL}	5	$\|I_O\|$ < 1.0µA	V_O = 4.5V or 0.5V	–	–	1.5	V
		10		V_O = 9V or 1V	–	–	3.0	V
		15		V_O = 13.5V or 1.5V	–	–	4.0	V
Input Voltage, "1" Level	V_{IH}	5	$\|I_O\|$ < 1.0µA	V_O = 0.5V or 4.5V	3.5	–	–	V
		10		V_O = 1V or 9V	7.0	–	–	V
		15		V_O = 1.5V or 13.5V	11.0	–	–	V
Output Drive Current, Source	I_{OH}	5	Note 2	V_{OH} = 4.6V	–0.44	–0.88	–	mA
		10		V_{OH} = 9.5V	–1.1	–2.25	–	mA
		15		V_{OH} = 13.5V	–3.0	–8.8	–	mA
Output Drive Current, Sink	I_{OL}	5	Note 2	V_{OL} = 0.4V	0.44	0.88	–	mA
		10		V_{OL} = 0.5V	1.1	2.25	–	mA
		15		V_{OL} = 1.5V	3.0	8.8	–	mA
Input Current	I_{in}	15	V_{IN} = 0V		–	-10^{-5}	–0.3	µA
		15	V_{IN} = 15V		–	10^{-5}	0.3	µA
Quiescent Current (Per Package)	I_{DD}	5	V_{IN} = V_{DD} or V_{SS}		–	–	4.0	µA
		10			–	–	8.0	µA
		15			–	–	16.0	µA

Note 2. I_{OH} and I_{OL} are measured one output at a time.

AC Electrical Characteristics: (C_L = 50pF, R_L = 200k, T_A = +25°C, Note 3 unless otherwise specified)

Parameter	Symbol	V_{DD}	Test Conditions	Min	Typ	Max	Unit
Clock Operation							
Propagation Delay Time	t_{PHL}, t_{PLH}	5		–	200	350	ns
		10		–	80	160	ns
		15		–	65	120	ns
Transition Time	t_{THL}, t_{TLH}	5		–	100	200	ns
		10		–	50	100	ns
		15		–	40	80	ns
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5		–	100	200	ns
		10		–	40	80	ns
		15		–	32	65	ns
Maximum Clock Rise and Fall Time	t_{RCL}, t_{FCL}	5		–	–	15	µs
		10		–	–	10	µs
		15		–	–	5	µs

Note 3. AC Paramters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (C_L = 50pF, R_L = 200k, T_A = +25°C, Note 3 unless otherwise specified)

Parameter	Symbol	V_{DD}	Test Conditions	Min	Typ	Max	Unit
Clock Operation (Cont'd)							
Minimum Setup Time	t_{SU}	5		–	20	40	ns
		10		–	15	30	ns
		15		–	12	25	ns
Maximum Clock Frequency	f_{CL}	5		2.5	5.0	–	MHz
		10		6.2	12.5	–	MHz
		15		7.6	15.5	–	MHz
Set and Reset Operation							
Propagation Delay Time	$t_{PHL(R)}$, $t_{PLH(S)}$	5		–	150	300	ns
		10		–	65	130	ns
		15		–	45	90	ns
Minimum Set and Reset Pulse Width	$t_{WH(R)}$, $t_{WH(S)}$	5		–	90	180	ns
		10		–	40	80	ns
		15		–	25	50	ns
Averag Input Capacitance	C_{IN}	Any		–	5.0	7.5	pF

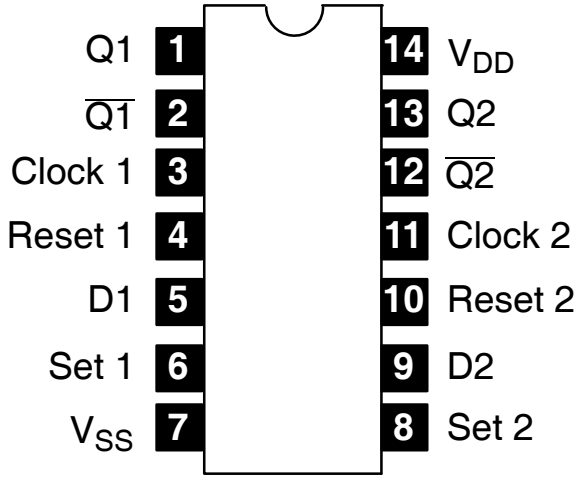
Note 3. AC Paramters are guaranteed by DC correlated testing.

Truth Table

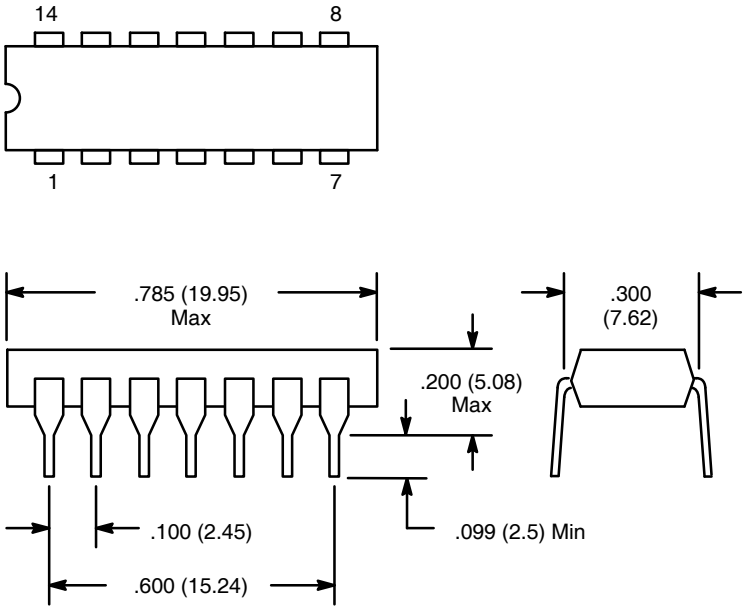
INPUTS				OUTPUTS	
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$
⎍	0	0	0	0	1
⎍	1	0	0	1	0
⎎	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = Don't Care
† = Level Change

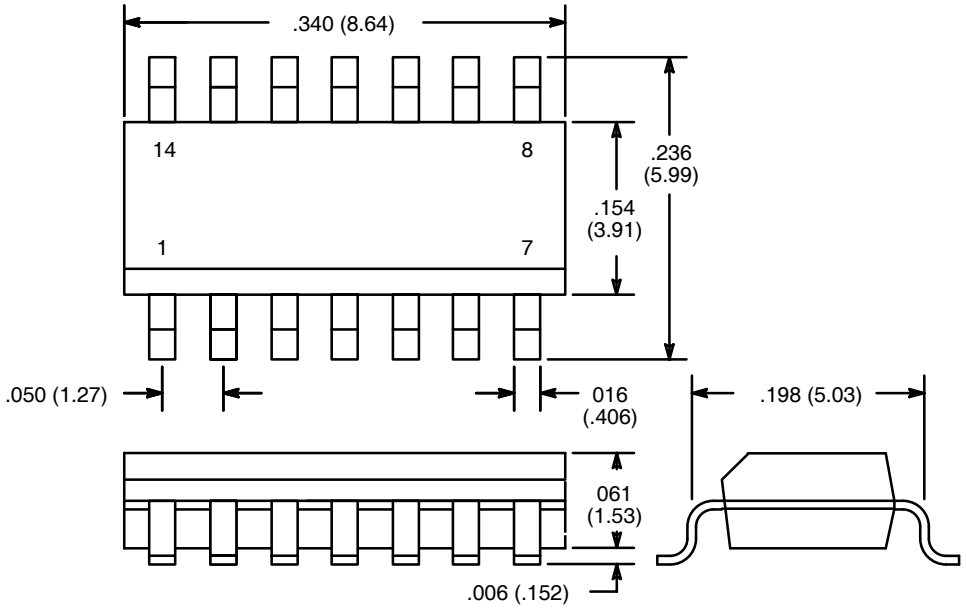
Pin Connection Diagram



NTE4013B (14−Lead DIP)



NTE4013BT (SOIC−14)



NOTE: Pin1 on Beveled Edge