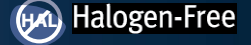


## EPC2054 – Enhancement Mode Power Transistor

 $V_{DS}$ , 200 V $R_{DS(on)}$ , 43 mΩ $I_D$ , 3 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

## Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	200	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	3	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	32	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

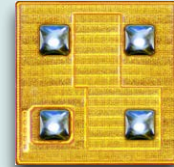
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.9	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	14	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	83	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details

Static Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 0.12 \text{ mA}$	200			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 160 \text{ V}$		0.001	0.1	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.003	0.5	
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5 \text{ V}$ , $T_J = 125^\circ\text{C}$		0.1	1	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.001	0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 1 \text{ mA}$	0.8	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 1 \text{ A}$		32	43	mΩ
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$		1.5		V

<sup>#</sup> Defined by design. Not subject to production test.



EPC2054 eGaN® FETs are supplied only in passivated die form with solder bumps  
Die Size: 1.3 mm x 1.3 mm

## Applications

- High Speed DC-DC conversion
- Wireless Power Transfer
- High Frequency Hard-Switching and Soft-Switching Circuits
- Lidar/Time of Flight (ToF)
- Automation
- Solar
- Class-D Audio

## Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra Low  $Q_G$
- Ultra Small Footprint



Dynamic Characteristics ( $T_j = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance <sup>#</sup>	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		358	573	pF
$C_{RSS}$	Reverse Transfer Capacitance			0.3		
$C_{OSS}$	Output Capacitance <sup>#</sup>			89	134	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }100\text{ V}, V_{GS} = 0\text{ V}$		120		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			152		
$R_G$	Gate Resistance			0.8		$\Omega$
$Q_G$	Total Gate Charge <sup>#</sup>	$V_{DS} = 100\text{ V}, V_{GS} = 5\text{ V}, I_D = 1\text{ A}$		2.9	4.3	nC
$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 100\text{ V}, I_D = 1\text{ A}$		0.9		
$Q_{GD}$	Gate-to-Drain Charge			0.3		
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
$Q_{OSS}$	Output Charge <sup>#</sup>	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		15	23	
$Q_{RR}$	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Figure 1: Typical Output Characteristics 25°C

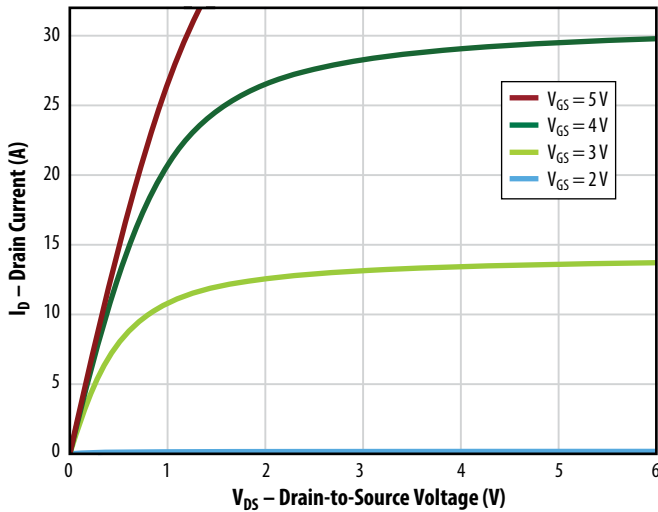


Figure 2: Transfer Characteristics

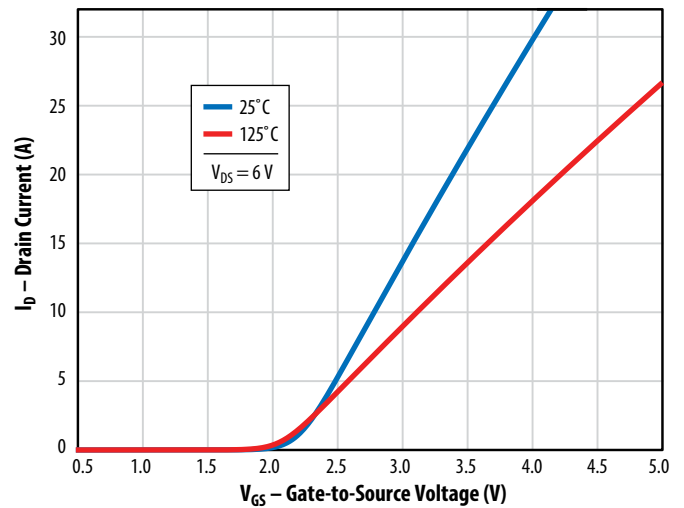


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

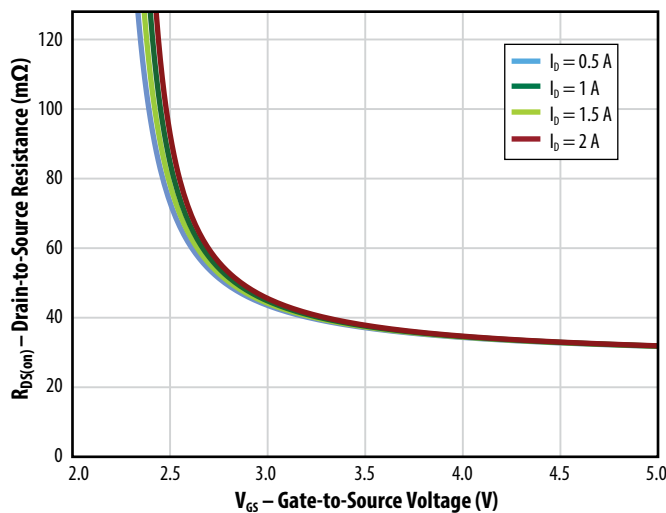


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

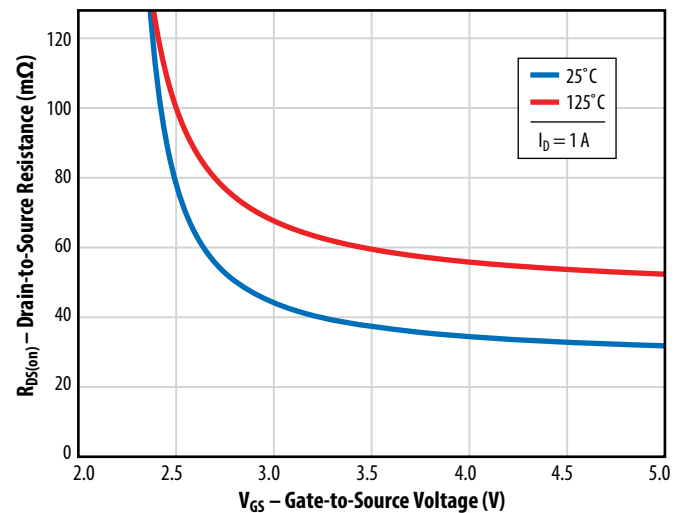


Figure 5a: Capacitance (Linear Scale)

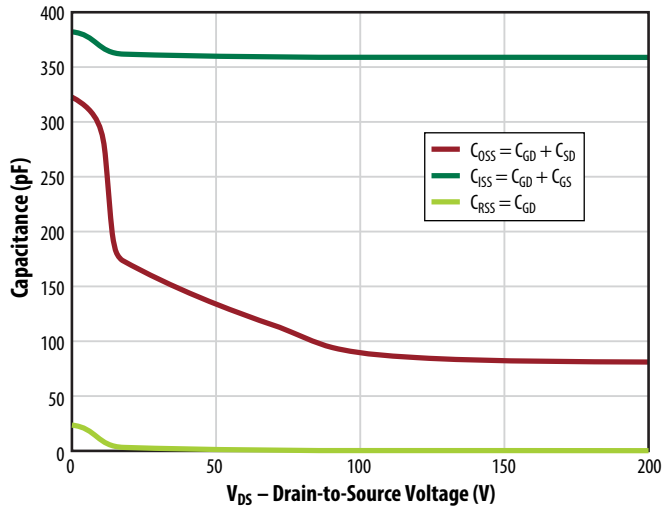


Figure 5b: Capacitance (Log Scale)

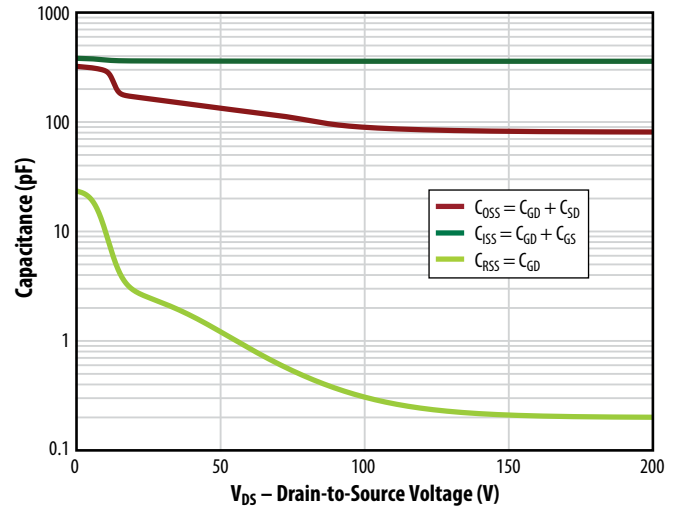


Figure 6: Output Charge and  $C_{OSS}$  Stored Energy

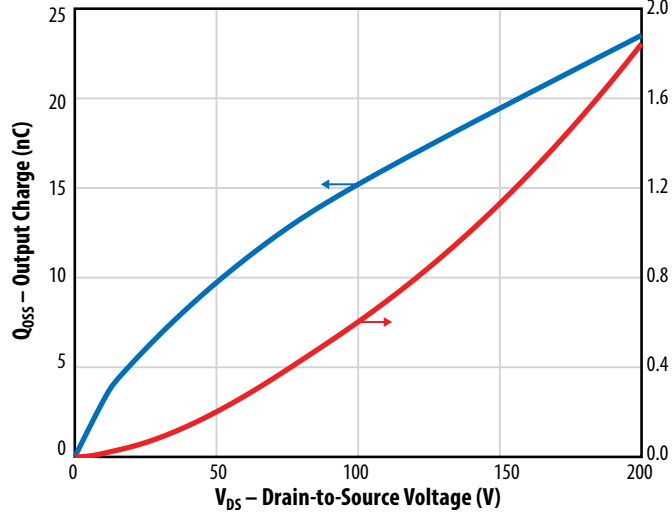


Figure 7: Gate Charge

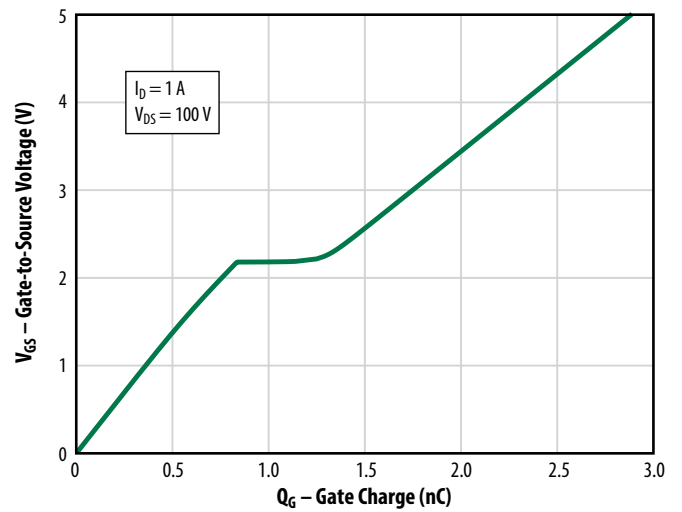


Figure 8: Reverse Drain-Source Characteristics

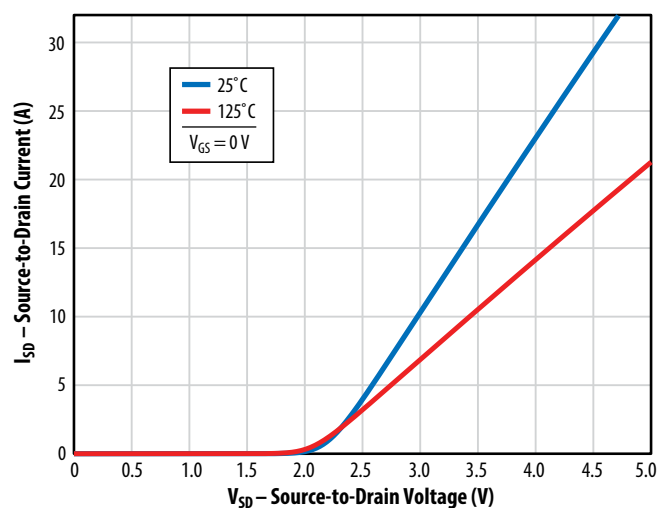
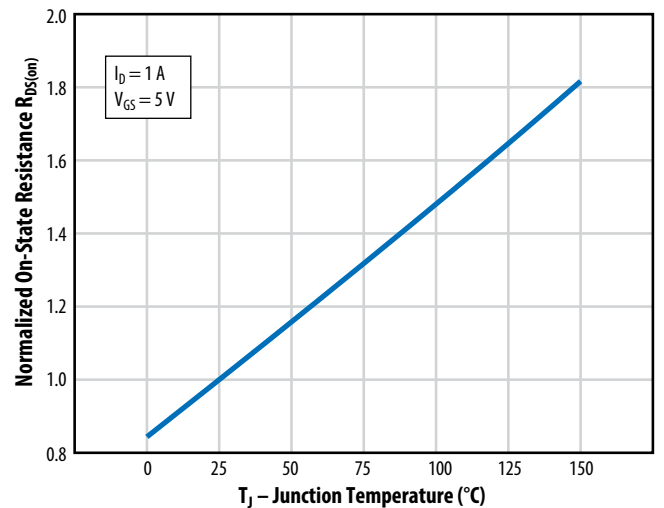


Figure 9: Normalized On Resistance vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Normalized Threshold Voltage vs. Temperature

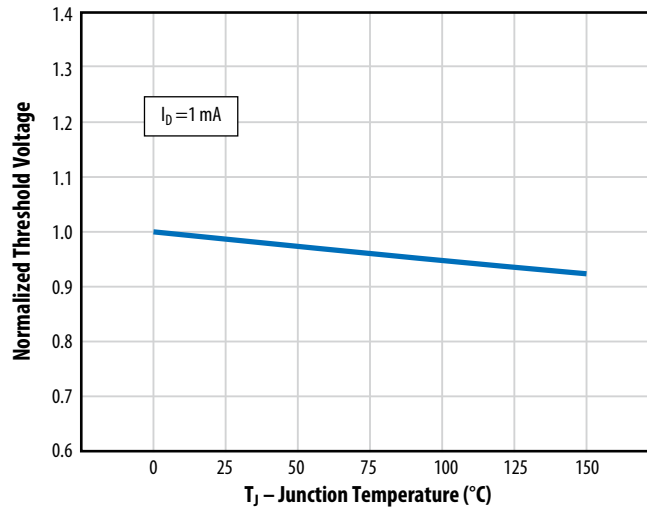


Figure 11: Transient Thermal Response Curves

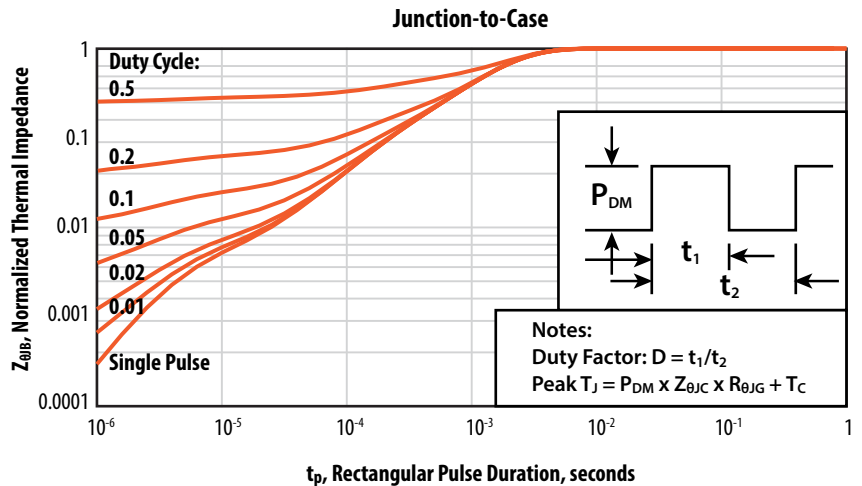
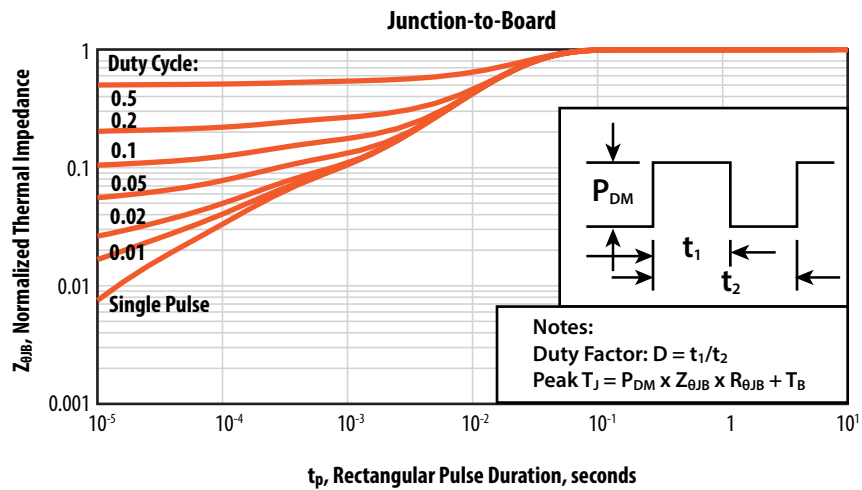
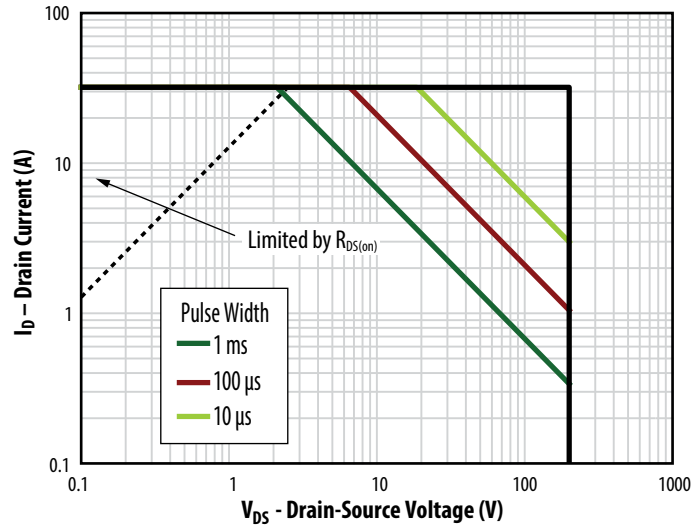
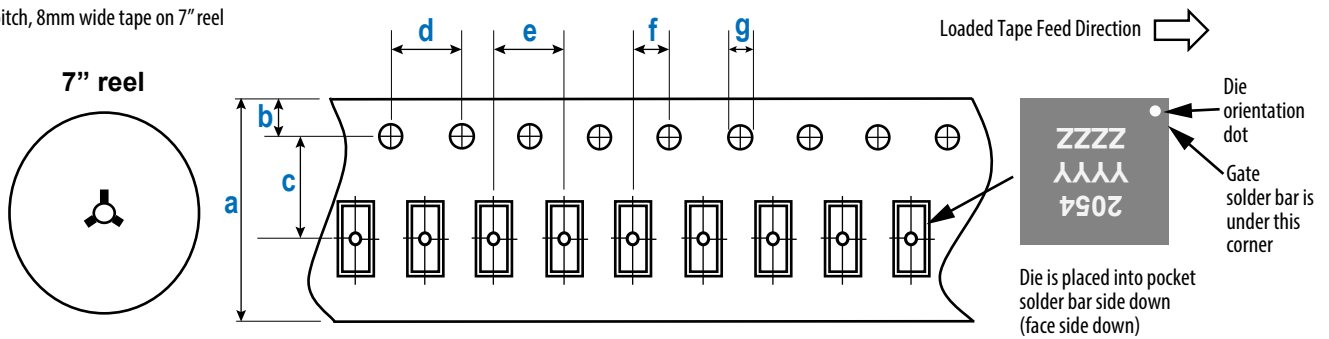


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

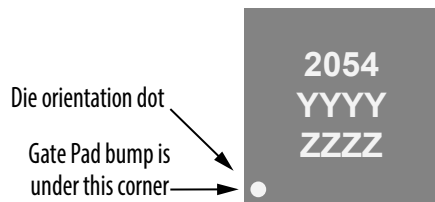


EPC2054 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

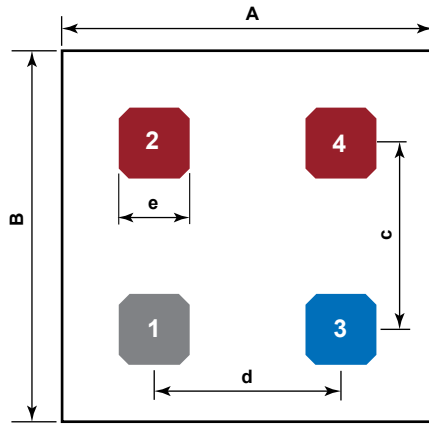
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2054	2054	YYYY	ZZZZ

**DIE OUTLINE**

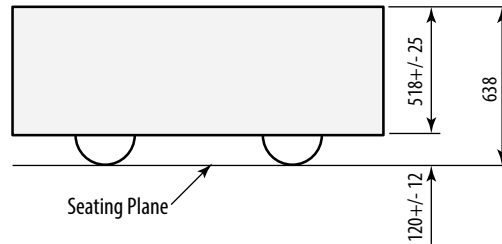
Solder Bump View



Pad 1 is Gate;  
Pad 3 is Drain;  
Pads 2, 4 are Source

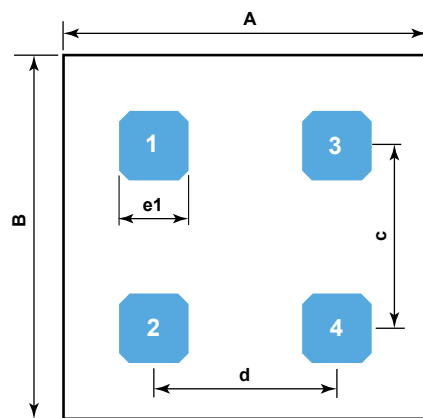
DIM	Micrometers		
	MIN	Nominal	MAX
A	1270	1300	1330
B	1270	1300	1330
c		650	
d		650	
e		250	

Side View



**RECOMMENDED LAND PATTERN**

(measurements in  $\mu\text{m}$ )



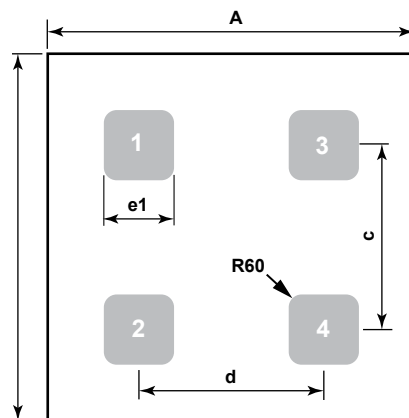
DIM	Micrometers
A	1300
B	1300
c	650
d	650
e1	230

The land pattern is solder mask defined  
Solder mask is 10  $\mu\text{m}$  smaller per side than bump

Pad 1 is Gate;  
Pad 3 is Drain;  
Pads 2, 4 are Source

**RECOMMENDED STENCIL DRAWING**

(measurements in  $\mu\text{m}$ )



DIM	Micrometers
A	1300
B	1300
c	650
d	650
e1	230

Recommended stencil should be 4mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at

<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Revised June, 2021