

CDMA Evaluation Board For PLL Frequency Synthesizer

FEATURES

Self-contained evaluation board that includes a synthesizer, VCO, and loop filter for generating CDMA frequencies (824 MHz to 849 MHz)

Designed for 3 kHz loop bandwidth

Accompanying software allows complete control of synthesizer functions from a PC

Battery operated: choice of 3 V or 5 V supply

Typical phase noise performance of -81 dBc/Hz at 300 Hz offset

Typical spurious performance of better than -81 dBc at 30 kHz offset from carrier

GENERAL DESCRIPTION

The EVAL-ADF4112EBZ1 evaluation board is designed to evaluate the performance of the [ADF4112](#) frequency synthesizer for phase locked loops (PLLs). Figure 1 is the functional block diagram of the board and shows the [ADF4112](#) frequency synthesizer, a PC connector, an SMA connector for the reference input, the power supplies, and an RF output. There is also a loop filter (3 kHz bandwidth) and a voltage controlled oscillator (VCO) incorporated on the board. A cable is included in the evaluation board package to connect the evaluation board to a PC printer port.

The evaluation board package contains Windows® based software to allow easy programming of the [ADF4112](#) frequency synthesizer.

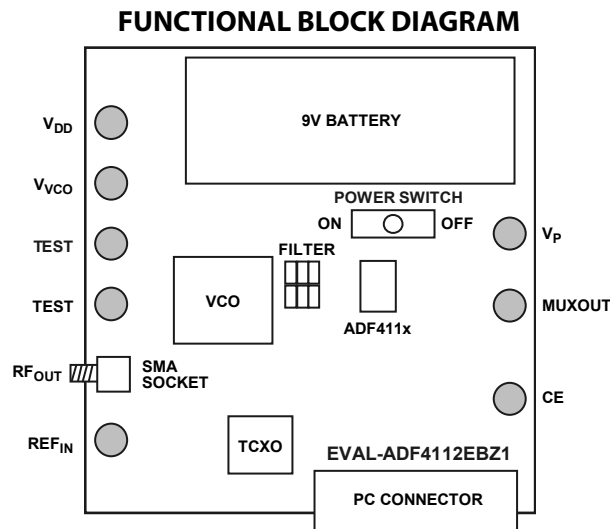


Figure 1.

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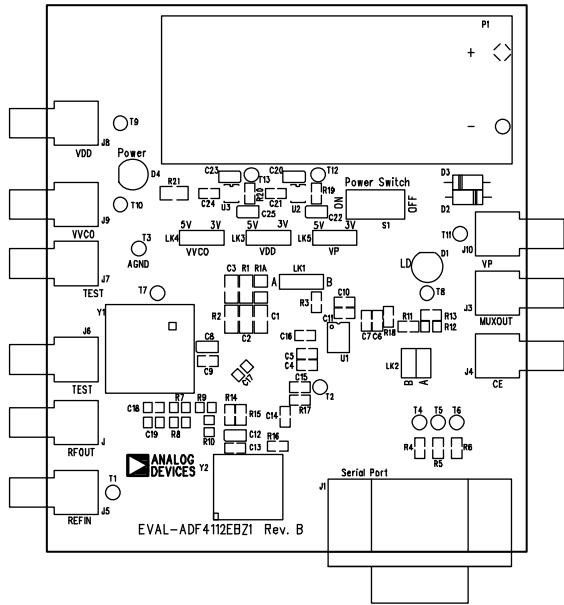
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REVISION HISTORY

7/11—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The evaluation board package includes a cable for connecting the EVAL-ADF4112EBZ1 to the printer port of a PC. The silkscreen and cable diagram for the evaluation board are shown in Figure 2 and Figure 3. The board schematics are shown in Figure 5 and Figure 6.



NOTES:
 1. THE VALUES FOR LOOP COMPONENTS ARE AS FOLLOWS:
 C1 = 4.7nF, C2 = 47nF, C3 = 620pF, R1 = 5.1kΩ, R2 = 22kΩ.

Figure 2. Evaluation Board Silkscreen

The evaluation board is powered from a single 9 V battery. The power supply circuitry allows the user to individually choose either 3 V or 5 V for the V_{DD} of the ADF4112, the V_P of the ADF4112, and the supply of the VCO. The default settings are 3 V for the

V_{DD} of the ADF4112 and 5 V for the V_P of the ADF4112 and for the supply of the VCO.

It is important to note that the V_{DD} of the ADF4112 should never exceed the V_P of the ADF4112 because damage to the device may result.

The EVAL-ADF4112EBZ1 includes all the components required for LO generation. A 13 MHz temperature compensated crystal oscillator (TCXO) from Vectron International, Inc., provides the necessary reference input. The PLL comprises the ADF4112 frequency synthesizer, the passive loop filter (20 kHz bandwidth), and the VCO (190-836T from Vari-L Company, Inc.). The output is available at RFOUT through a standard SMA connector. A different reference input and different power supplies can be used, if desired. In this case, insert SMA connectors as shown in the silkscreen (Figure 2) and cable diagram (Figure 3).

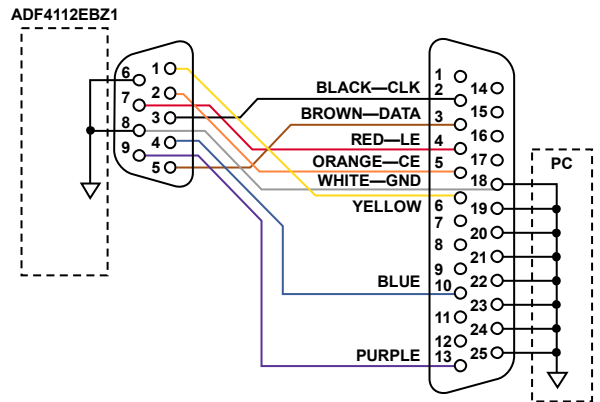


Figure 3. PC Cable Diagram

EVALUATION BOARD SOFTWARE

The evaluation board software is provided on the CD-ROM included in the evaluation board package.

INSTALLING THE SOFTWARE

To load the software, double-click **setup.exe**, and then follow the on-screen instructions from the installation wizard. The software is installed into the default directory **C:/Program Files/Analog Devices**.

USING THE SOFTWARE

To run the software,

1. From the **Start** menu, point to **Program** and **ADF4XXX**, and then click **ADF4XXX_revx**.
2. A dialog box appears, asking which device is to be evaluated. Select **ADF4112**, and click **OK**. The **Main Interface Page** window appears (see Figure 4).
3. Click **Evaluation Board**, and the **Evaluation Board** window appears. Select **ADF4112EBZ1** from the list, and click **OK**.

The **ADF4112** frequency synthesizer is then programmed with the correct settings for a CDMA system working at 836 MHz. In addition, a 30 kHz PFD frequency is set up, a 32/33 prescaler is chosen, and a charge pump current of 5 mA is programmed.

To change any of these settings, click the parameter to be modified (for example, click **RF VCO Output Frequency**). A dialog box appears in which you can either type in a new value or increment and decrement the set value by the channel spacing.

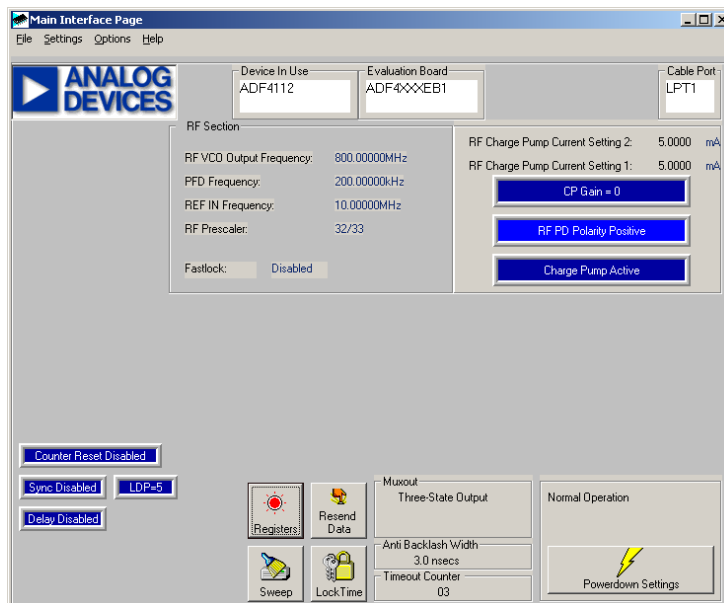
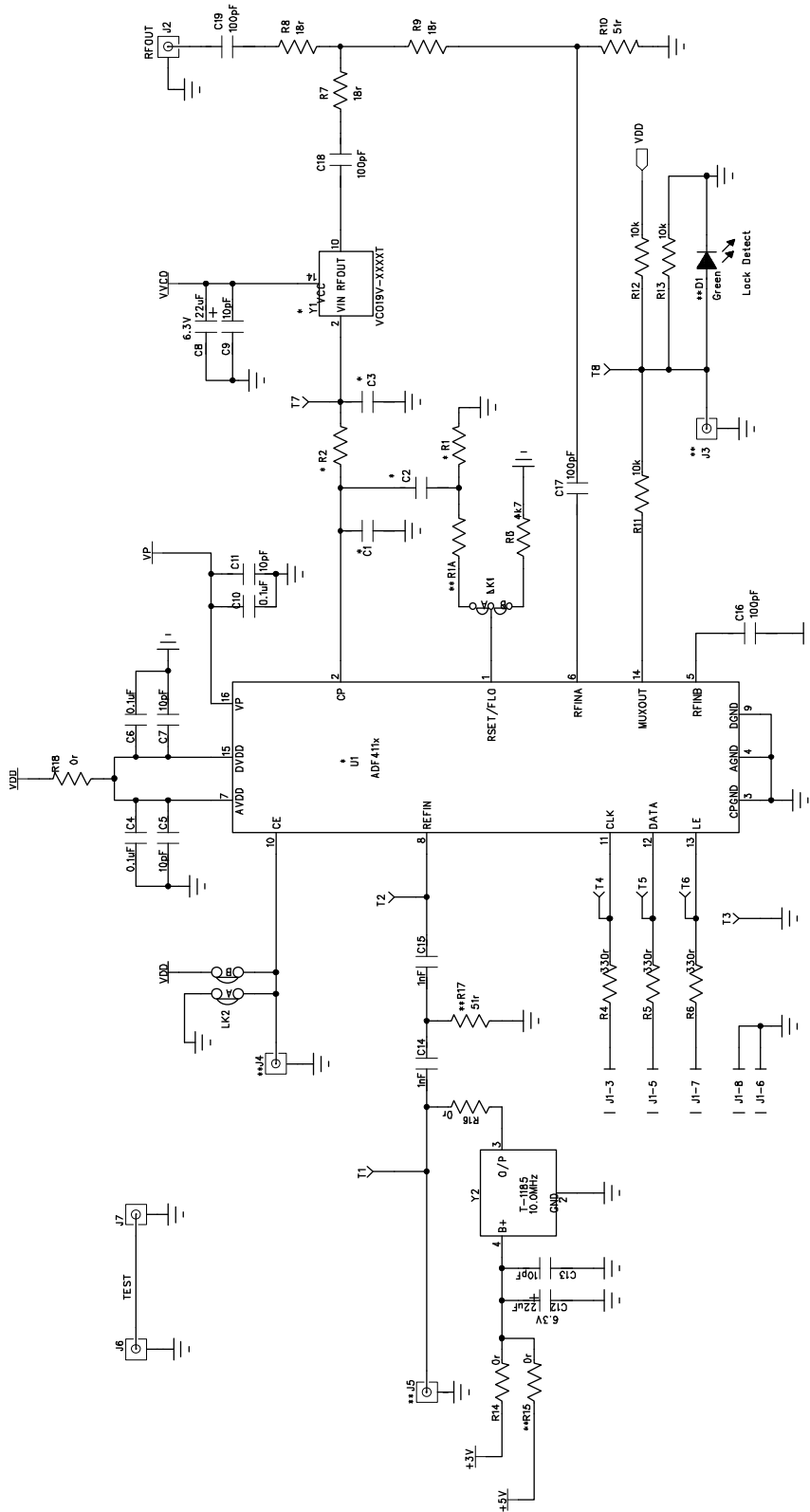


Figure 4. Main Interface Page Window

EVALUATION BOARD SCHEMATICS



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Note on non-inserted components.
 * - These components must be inserted by the user for correct operation of the board.
 ** - These components can be inserted by the user for expansion purposes.

Figure 5. Evaluation Board Circuit Diagram (Page 1)

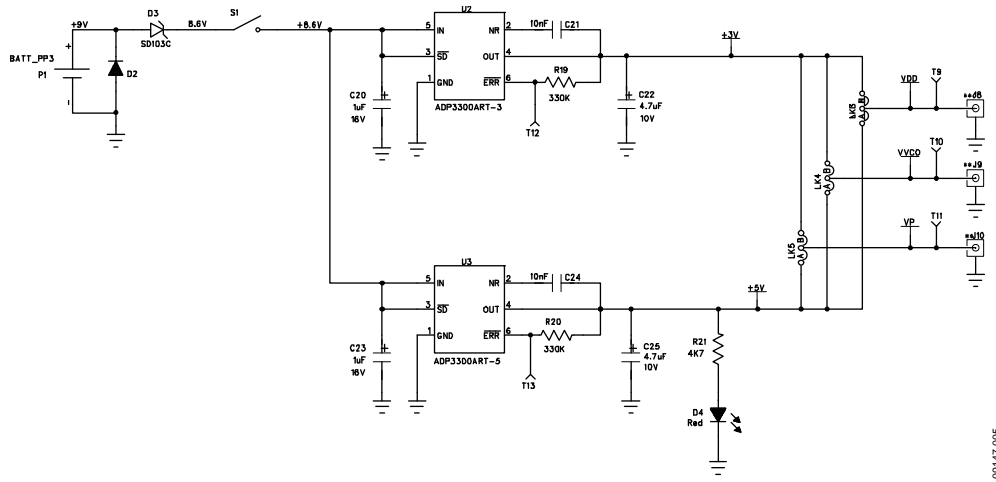


Figure 6. Evaluation Board Circuit Diagram (Page 2)

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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