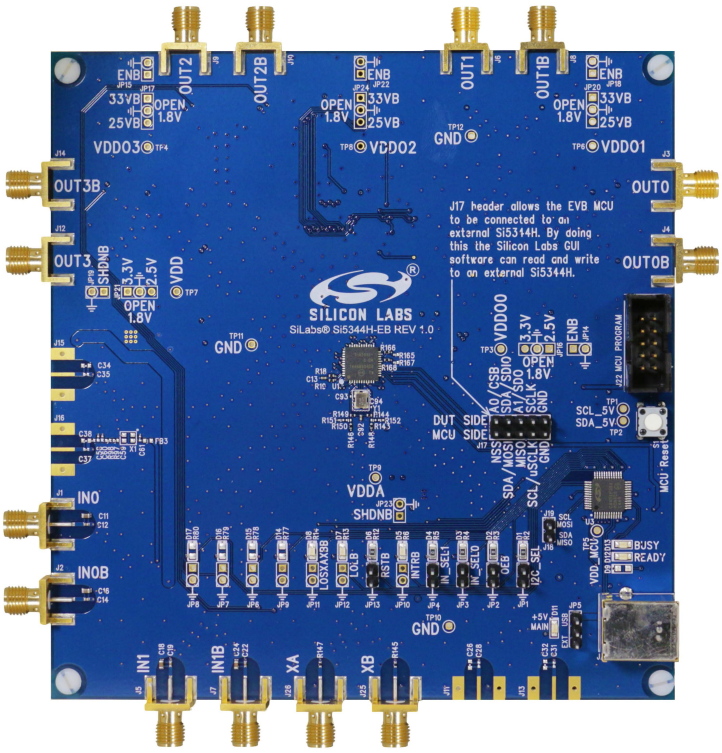
UG149: Si5344H Evaluation Board User's Guide

The Si5344H-EVB is used for evaluating the Si5344H Any-Frequency, Any-Output, Jitter Attenuating Clock Multiplier. The Si5344H combines 4th generation DSPLL and Multisynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. The Si5344H-EVB has two independent input clocks and four independent output clocks. The Si5344H-EVB can be controlled and configured using the ClockBuilder® Pro (CBPro) software tool.



Si5344H Evaluation Board

EVB FEATURES:

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5344H.
- CBPro GUI-programmable VDD supply allows the device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI-programmable VDDO supplies allow each of the ten outputs to have its own supply voltage, selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5344H.
- SMA connectors for input clocks, output clocks, and optional external timing reference clock.

1. Overview

1.1 Functional Block Diagram

A functional block diagram of the Si5344H-EVB is shown below. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section 1.2 Si5344H EVB Support Documentation or Section 1.3 Quick Start for more information.

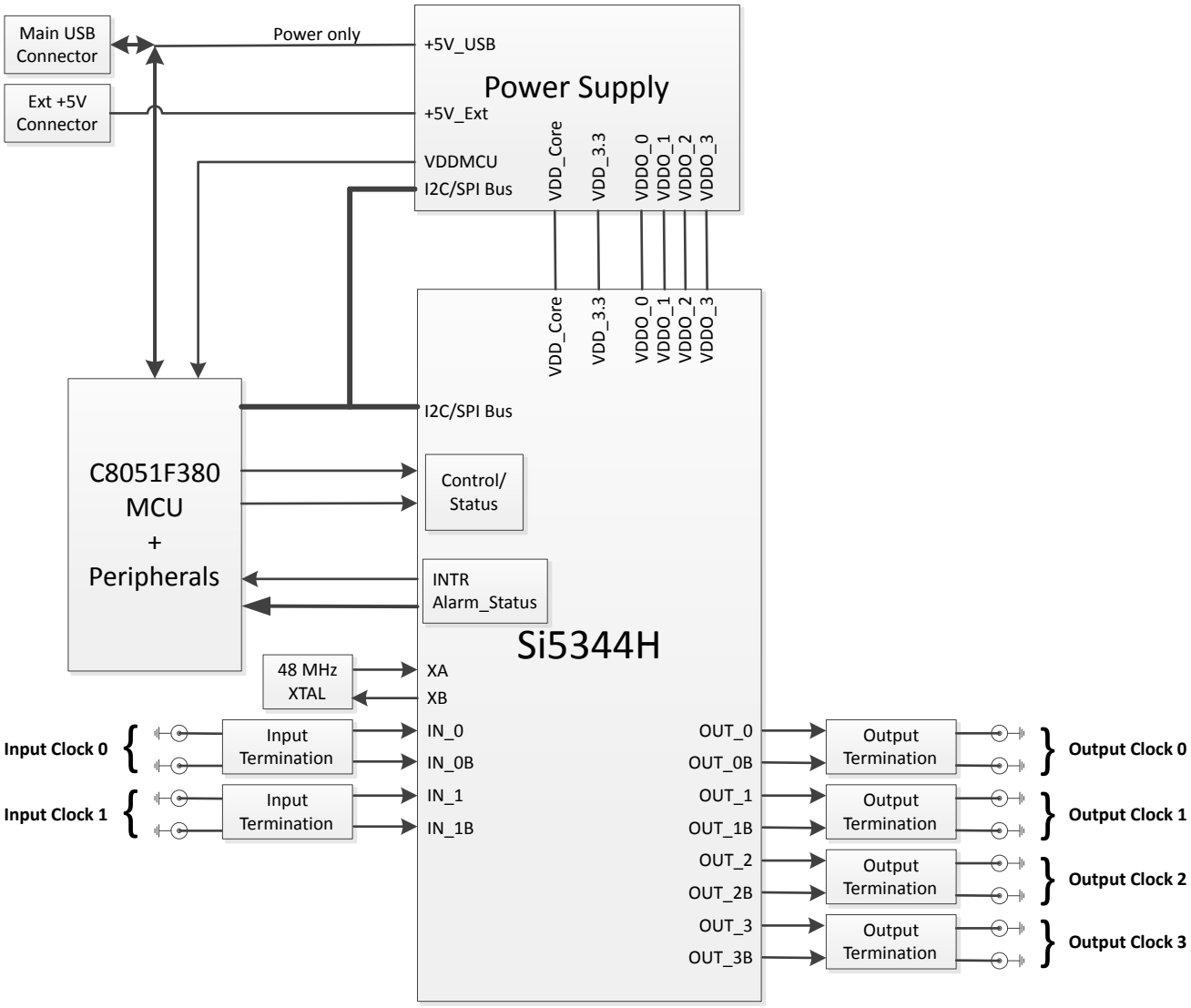


Figure 1.1. Si5344H-EVB Functional Block Diagram

1.2 Si5344H EVB Support Documentation

The Si5344H EVB Schematic and Bill of Materials (BOM) can be found online at: http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx. Contact Silicon labs for related user's guides, data sheets, and software.

Note: The Si5344H EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

1.3 Quick Start

1. Install ClockBuilder Pro desktop software: http://www.silabs.com/CBPro.
   - Installation instructions and the user's guide for ClockBuilder Pro can also be found at the download link shown above.
2. Connect a USB cable from the Si5344H-EVB to the PC where the software is installed.
3. Confirm jumpers are installed as shown in Table 1.1 Si5344H EVB Jumper Defaults on page 3.
4. Launch the ClockBuilder Pro software.
5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5344H-EVB.
6. Contact Silicon Labs for the Si5344H data sheet.

1.4 Jumper Defaults

Table 1.1. Si5344H EVB Jumper Defaults

Location	Type	I = Installed 0 = Open		Location	Type	I = Installed 0 = Open
JP1	2 pin	I		JP14	2 pin	O
JP2	2 pin	I		JP15	2 pin	O
JP3	2 pin	I		JP16	3 pin	all open
JP4	2 pin	I		JP17	3 pin	all open
JP5	3 pin	1 to 2		JP18	2 pin	O
JP6	2 pin	O		JP19	2 pin	O
JP7	2 pin	O		JP20	3 pin	all open
JP8	2 pin	O		JP21	3 pin	all open
JP9	2 pin	O		JP22	2 pin	O
JP10	2 pin	O		JP23	2 pin	O
JP11	2 pin	O		JP24	3 pin	all open
JP12	2 pin	O				
JP13	2 pin	O		JP17	5x2 Hdr	All 5 installed

Note:
1. Refer to the Si5344H EVB Schematics for the functionality associated with each jumper.

1.5 Status LEDs

Table 1.2. Si5344H EVB Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	INTRB	Blue	DUT Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB	Blue	DUT Loss of Reference
D11	+5V MAIN	Green	Main USB +5 V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

D11 is illuminated when USB +5 V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.

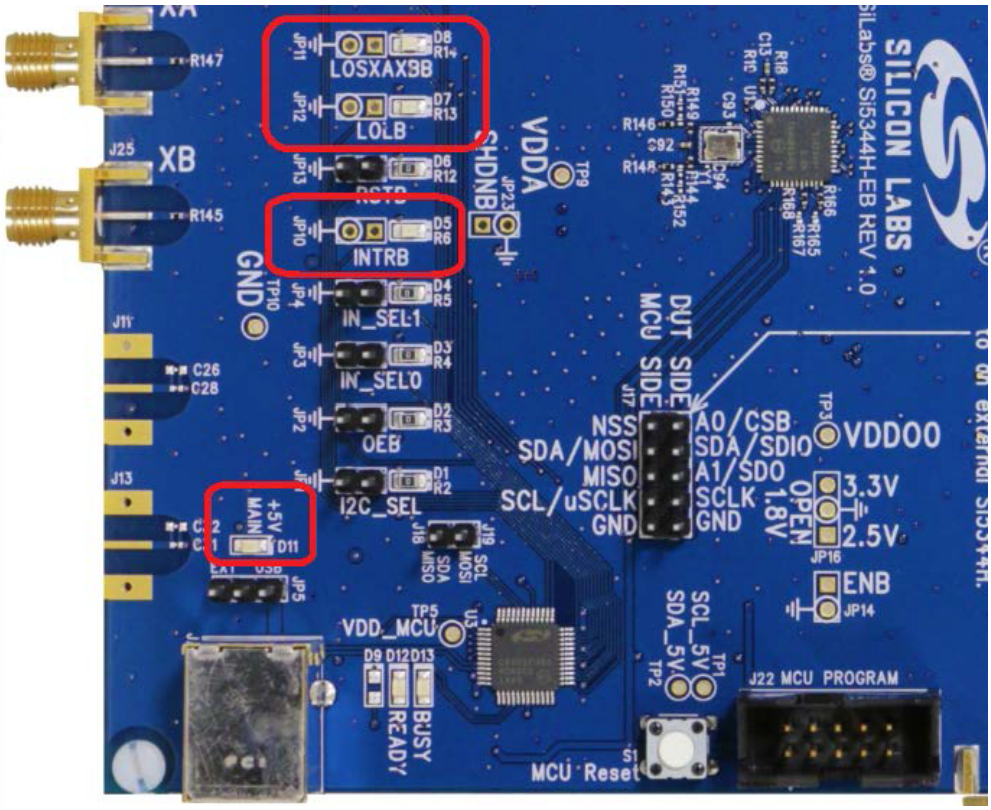


Figure 1.2. Status LEDs

1.6 External Reference Input (XA/XB)

An external reference (XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5344H-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with a REFCLK, C93 and C94 must be populated and the XTAL removed (see the figure below). The REFCLK can then be applied to J25 and J26.

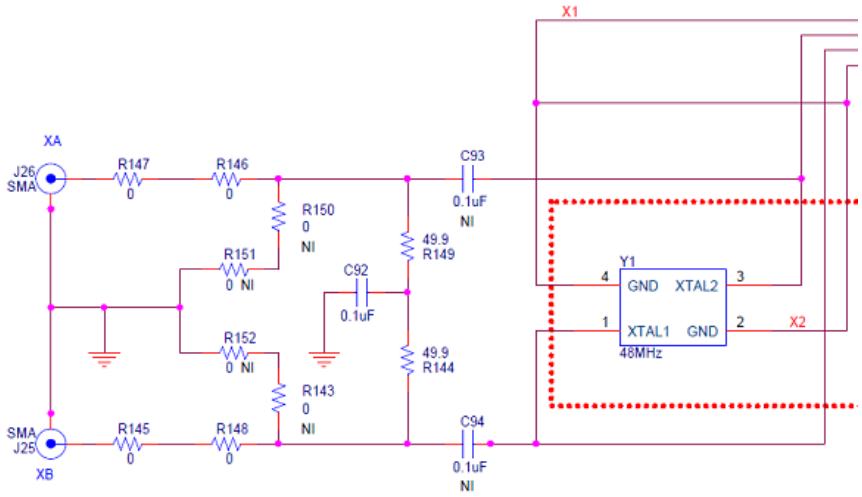


Figure 1.3. External Reference Input Circuit

1.7 Clock Input Circuits (INx/INxB and FB-IN/FB-INB)

The Si5344H-EVB has four SMA connectors (IN0/IN0B and IN1/IN1B) for receiving external clock signals. All input clocks are terminated, as shown in the figure below.

Input clocks are AC coupled and 50 W terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. See the Si5344H data sheet for details on how to configure inputs as single-ended.

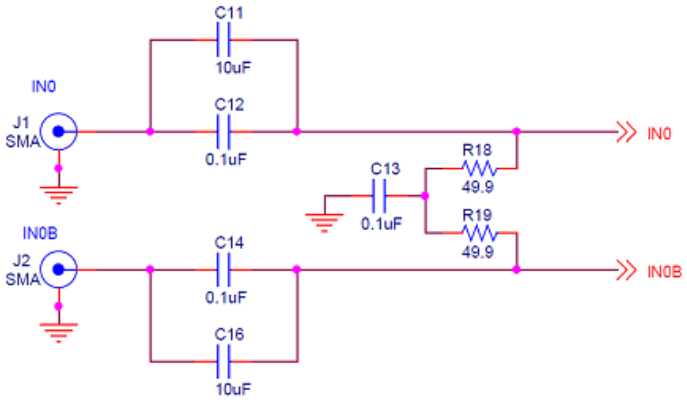


Figure 1.4. Input Clock Termination Circuit

1.8 Clock Output Circuits (OUTx/OUTxB)

Each of the eight outputs (four differential pairs) is AC coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal has no DC bias. If DC coupling is required, the AC coupling capacitors can be replaced with a resistor of appropriate value. The Si5344H-EVB provides pads for optional output termination resistors and/or low frequency capacitors.

Note: Components with schematic "NI" designation are not normally populated on the Si5344H-EVB and provide locations on the PCB for optional DC/AC terminations by the end user.

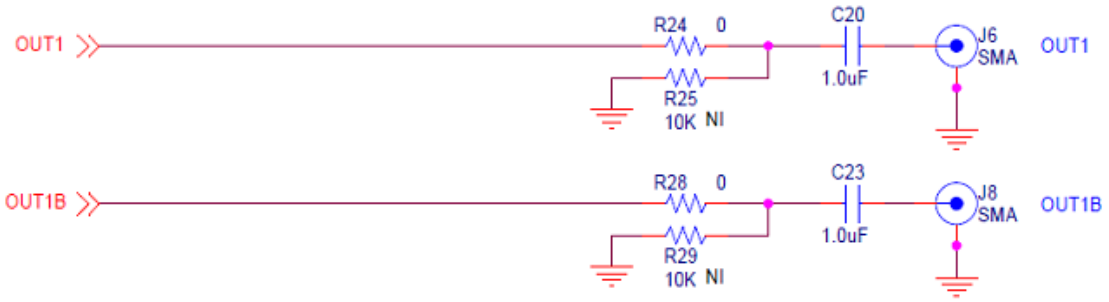


Figure 1.5. Output Clock Termination Circuit

2. Using Si5344H EVB

2.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect the software to the EVB with a USB cable, as shown in the figure below.

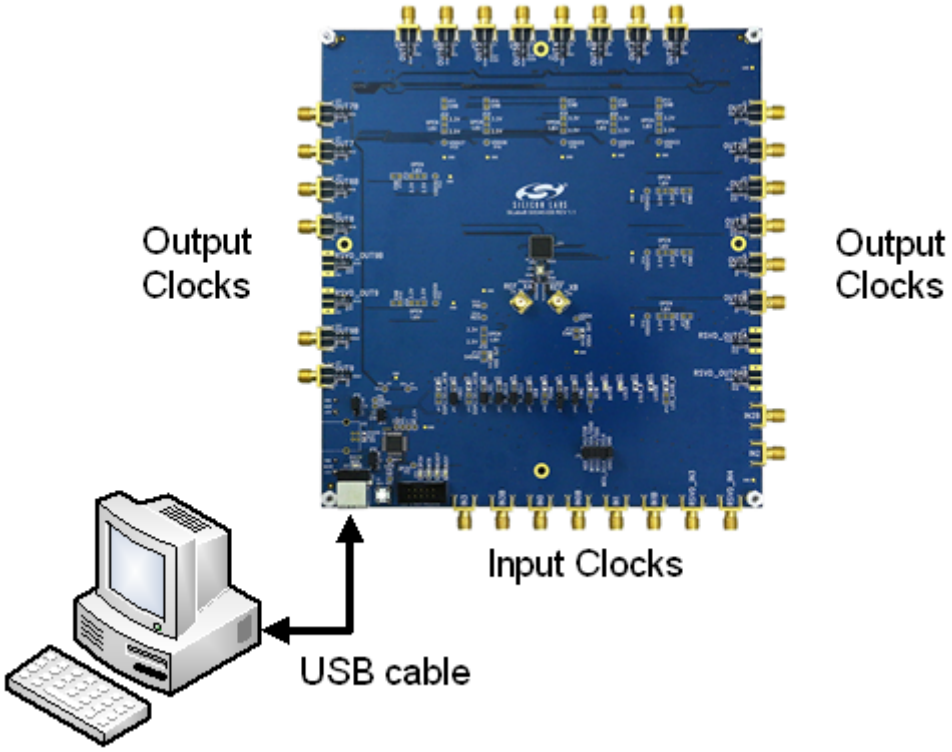


Figure 2.1. EVB Connection Diagram

2.2 Main Features of ClockBuilder Pro Applications

The ClockBuilder Pro installer installs two main applications: the ClockBuilder Pro Wizard and the EVB GUI.

Figure 2.2. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- Create a new design.
- Review or edit an existing design.
- Export: create in-system programming.

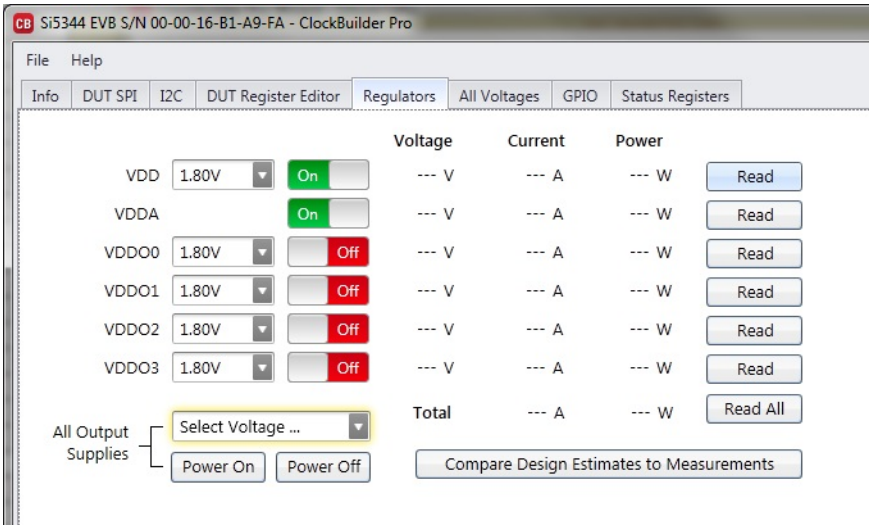


Figure 2.3. Application #2: EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5344H).
- Control the EVB's regulators.
- Monitor voltage, current, power on the EVB.

2.3 Common ClockBuilder Pro Workflow Scenarios

There are three common workflow scenarios when using CBPro and the Si5344H EVB. These workflow scenarios are as follows:

Workflow Scenario #1:	Testing a Silicon Labs-created Default Configuration
Workflow Scenario #2:	Modifying the Default Silicon Labs-created Device Configuration
Workflow Scenario #3:	Testing a User-created Device Configuration

Each scenario is described in more detail in the following sections.

2.3.1 Workflow Scenario #1: Testing a Silicon Labs Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

1. Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.

Figure 2.4. ClockBuilder Pro Desktop Icon

2. When the EVB is detected, select the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

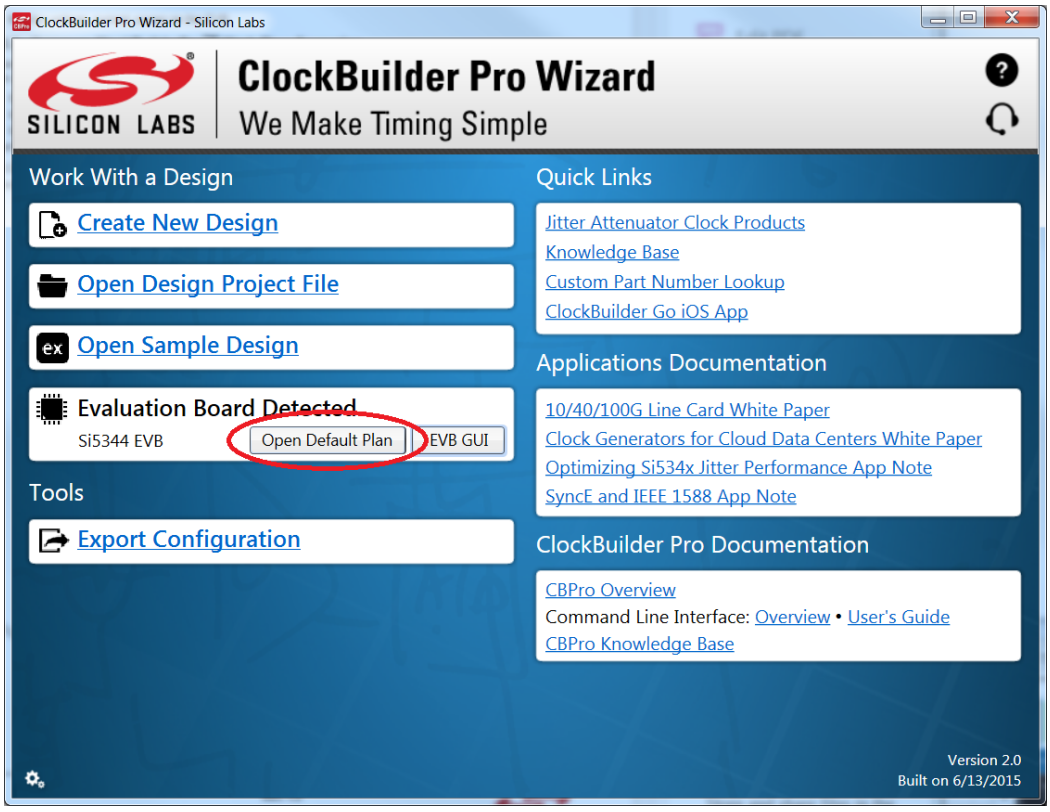


Figure 2.5. Open Default Plan

3. Once you open the default plan (based on your EVB model number), a popup window opens.

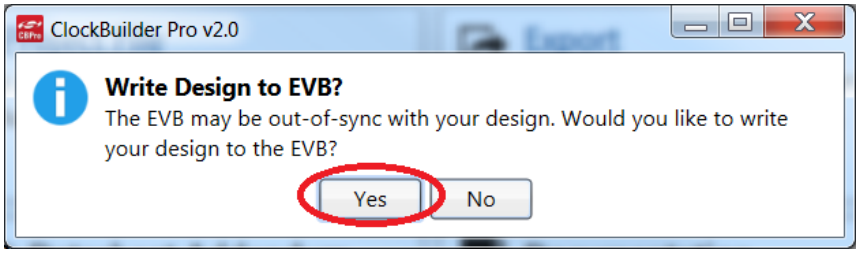


Figure 2.6. Write Design to EVB Dialog

4. Select "Yes" to write the default plan to the Si5344H device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

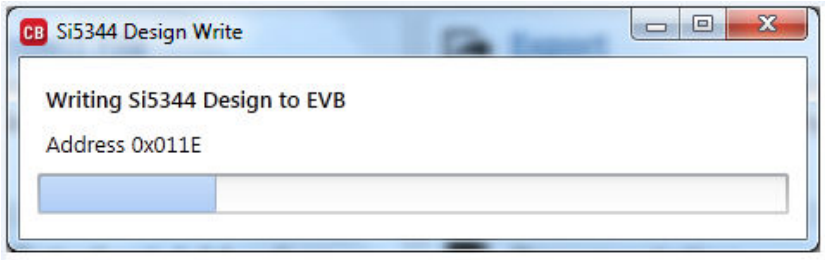


Figure 2.7. Writing Design Status

5. After CBPro writes the default plan to the EVB, select "Open EVB GUI".

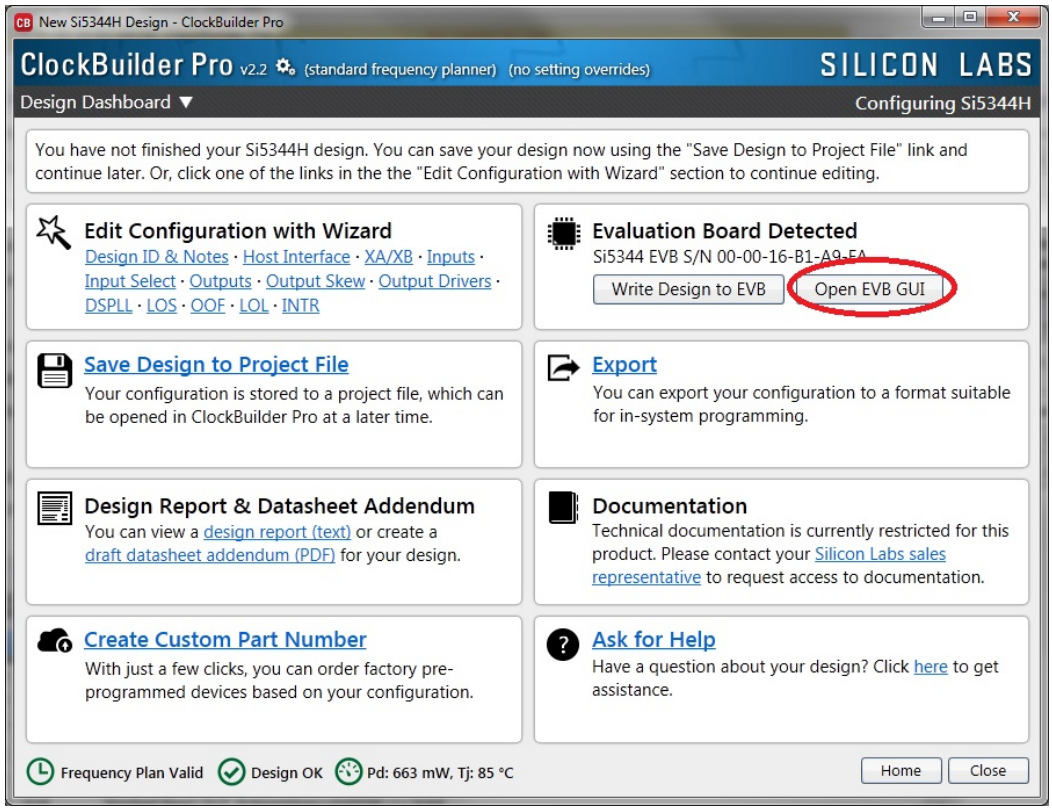


Figure 2.8. Open EVB GUI

6. The EVB GUI opens. All power supplies are set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown in the figure below.

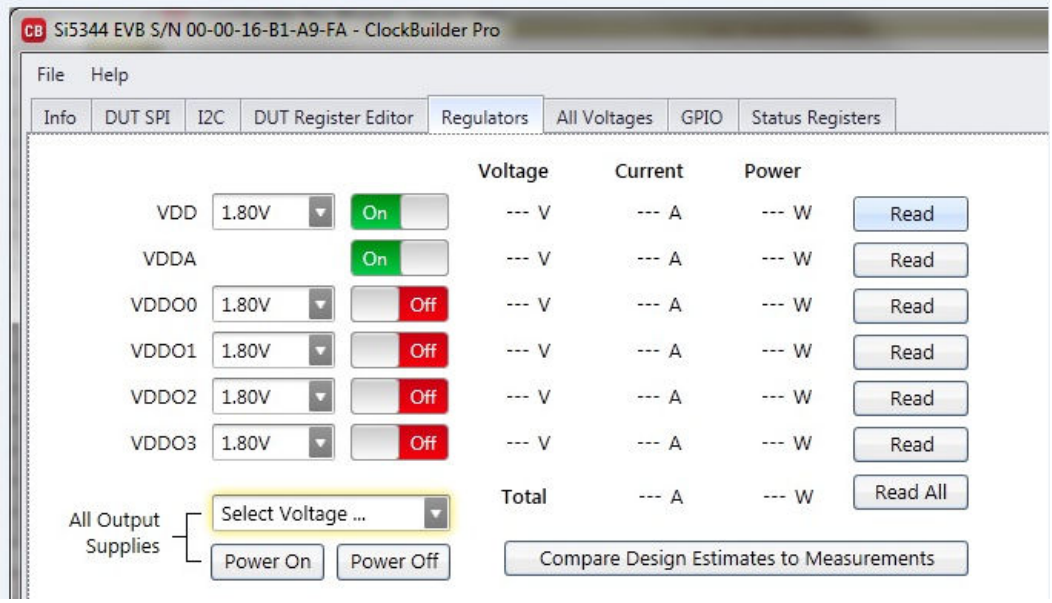


Figure 2.9. EVB GUI Window

Verify Free-run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the "Read All" button (bottom right-hand corner of Figure 2.9 EVB GUI Window on page 12) and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA power supplies "Off" and then "On" will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB".

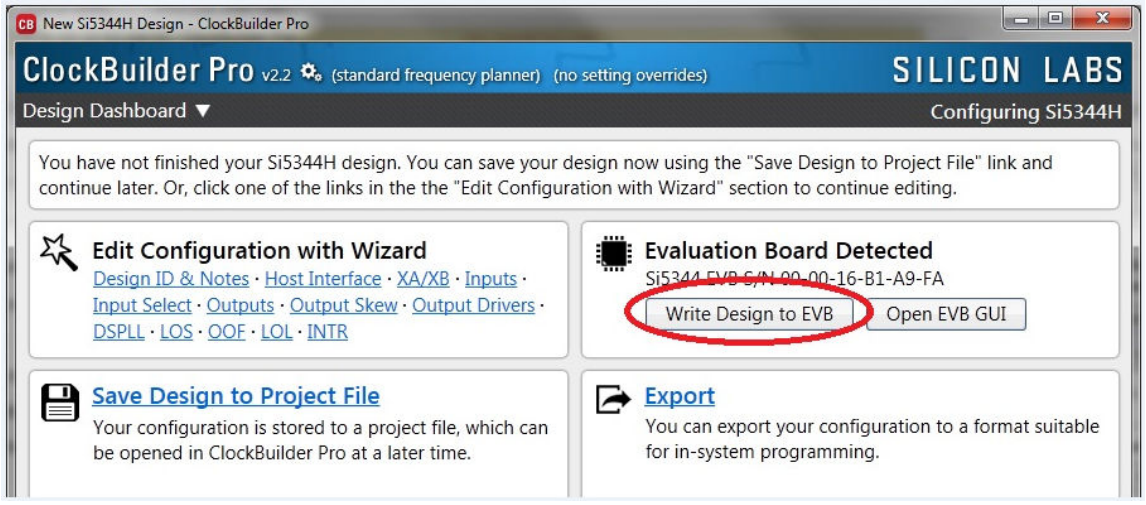


Figure 2.10. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running in free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on "View Design Report" as highlighted in the figure below.

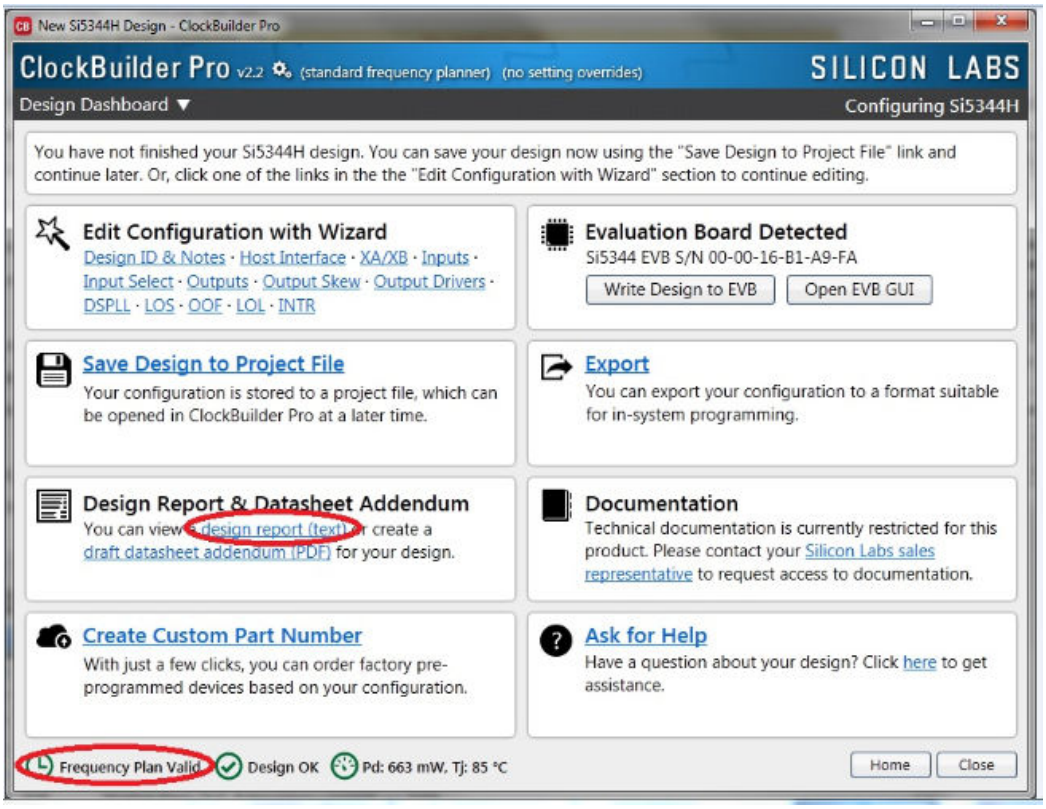


Figure 2.11. View Design Report

Your configuration's design report opens in a new window, as shown in the figure below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

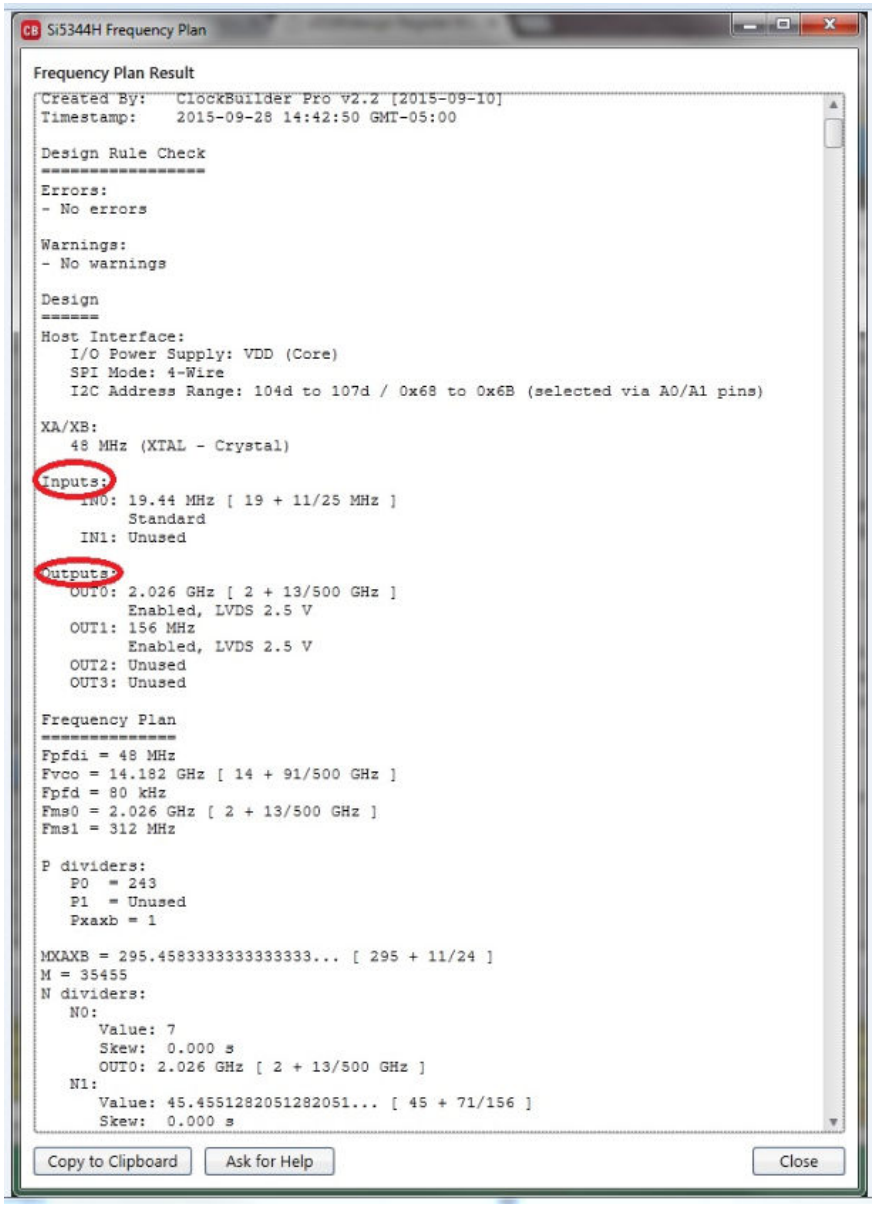


Figure 2.12. Design Report Window

Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

2.3.2 Workflow Scenario #2: Modifying the Default Silicon Labs Created Device Configuration

1. To modify the "default" configuration using the CBPro Wizard, select "Edit Configuration with Wizard".

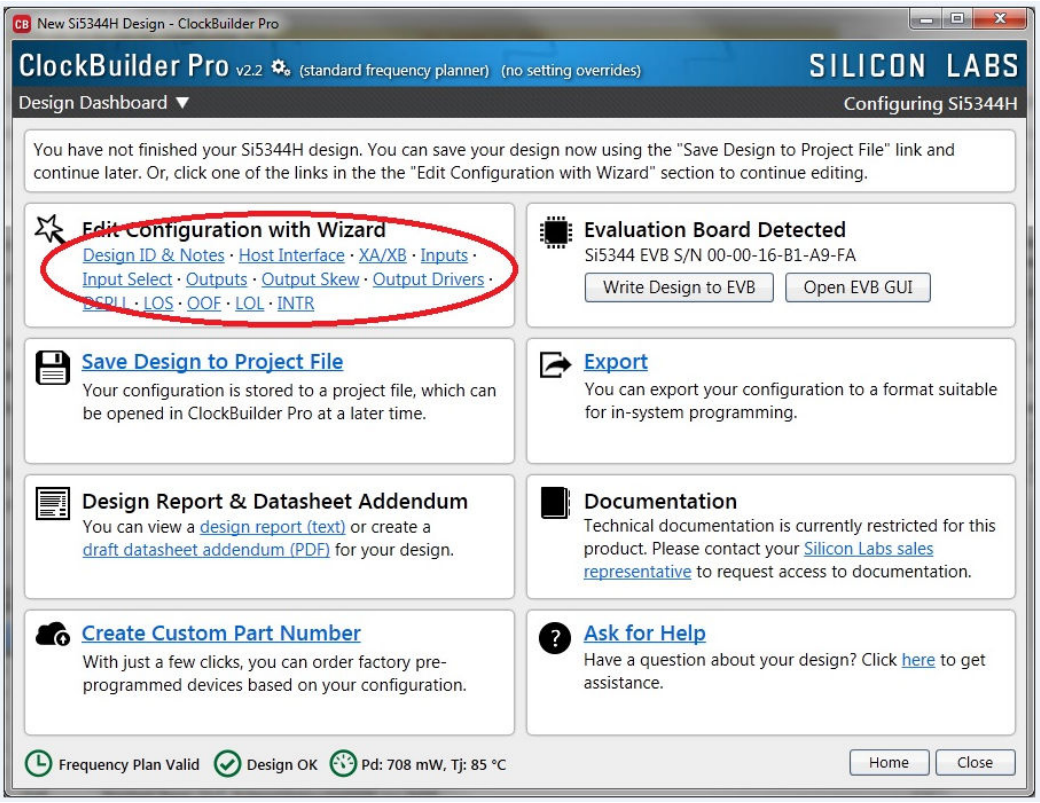


Figure 2.13. Edit Configuration with Wizard

2. You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

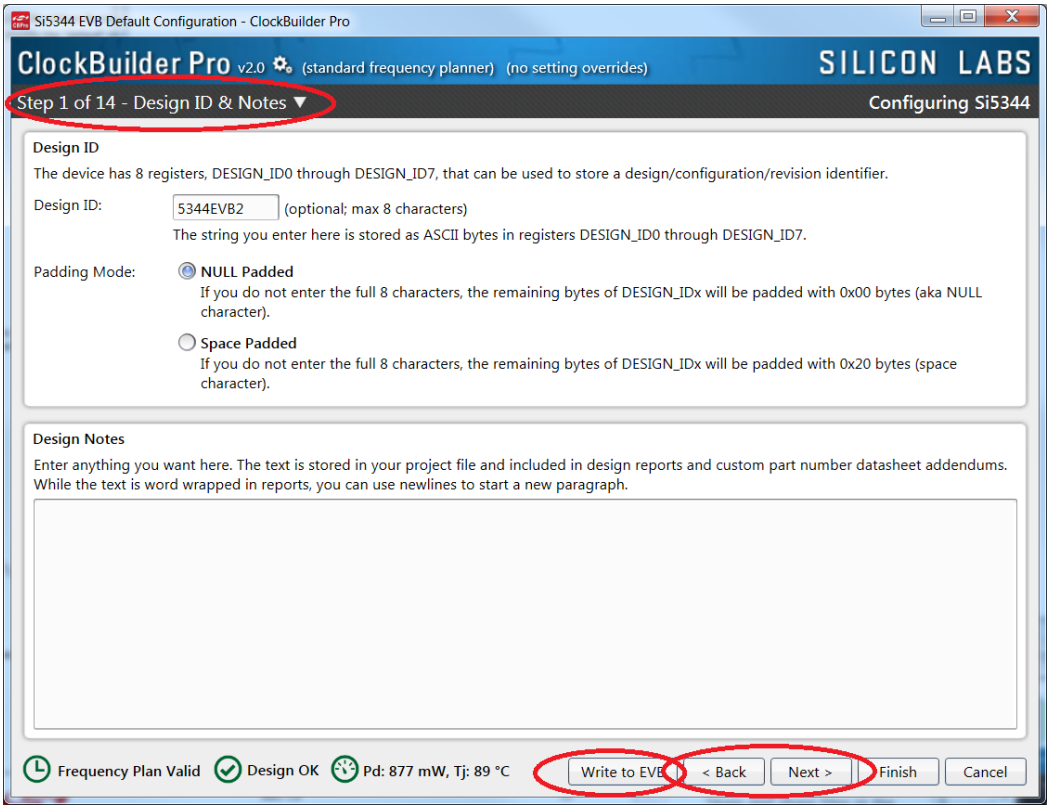


Figure 2.14. Design Wizard

Note: You can click on the icon on the lower left hand of the menu to confirm that your frequency plan is valid. After making your desired changes, you can click on "Write to EVB" to update the DUT to reconfigure your device in real-time. The Design Write status window opens each time you make a change.

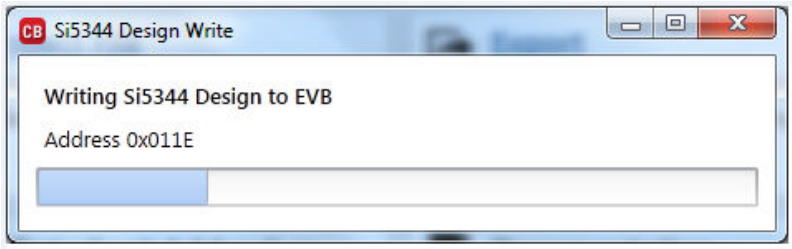


Figure 2.15. Writing Design Status

2.3.3 Workflow Scenario #3: Testing a User Created Device Configuration

1. To test a previously-created user configuration, open the CBPro Wizard by clicking the icon on your desktop and then selecting "Open Design Project File".

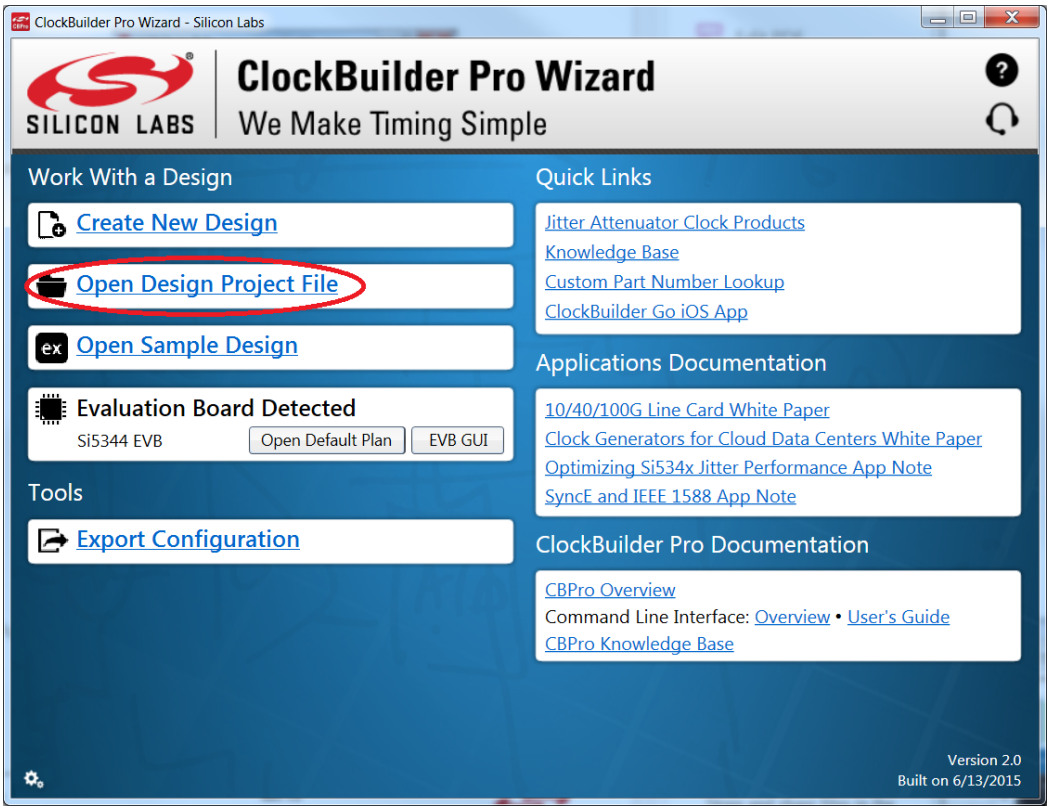


Figure 2.16. pen Design Project File

2. Locate your CBPro design file (*.slabtimeproj or *.sitproj file) design file in the Windows file browser.

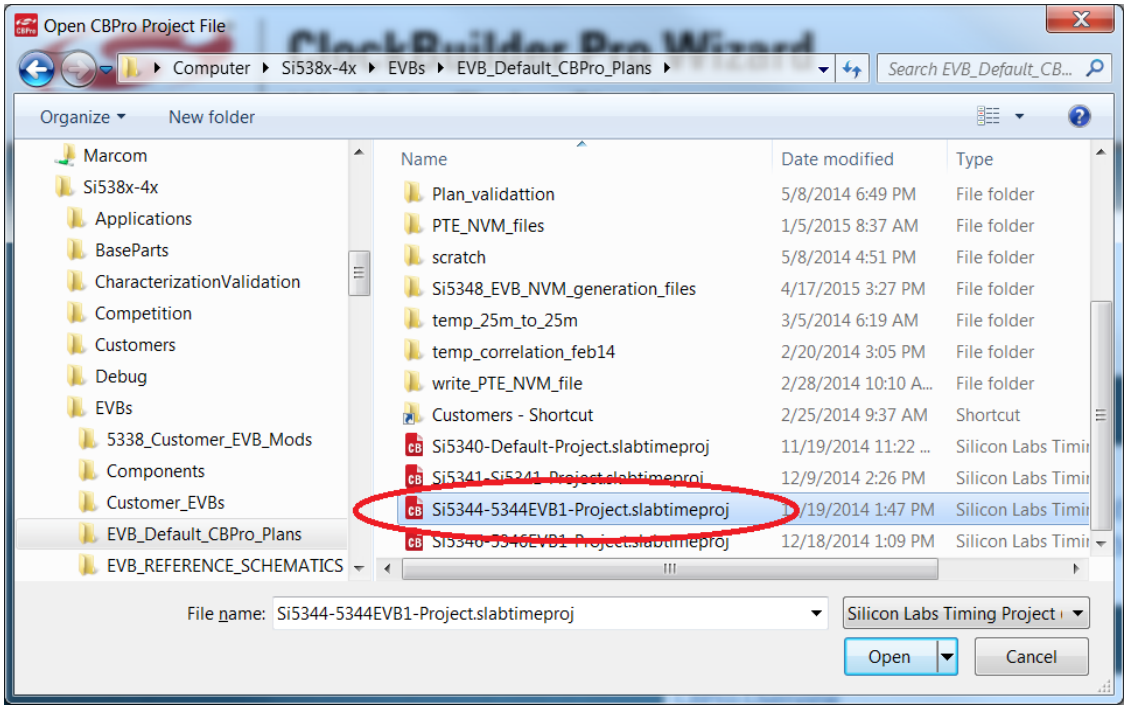


Figure 2.17. Browse to Project File

3. Select "Yes" when the WRITE DESIGN to EVB popup appears:

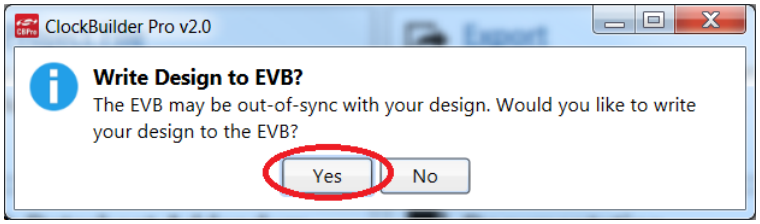


Figure 2.18. Write Design to EVB Dialog

4. The progress bar is launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

2.4 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export", as shown in the figure below.

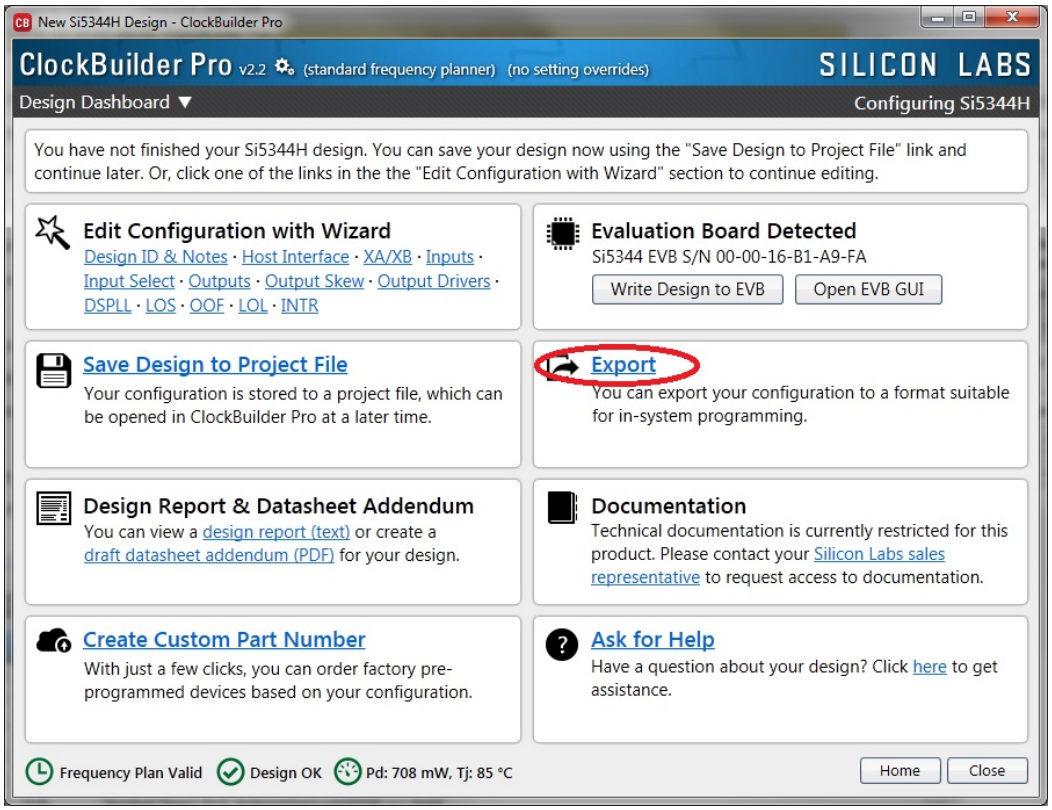


Figure 2.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

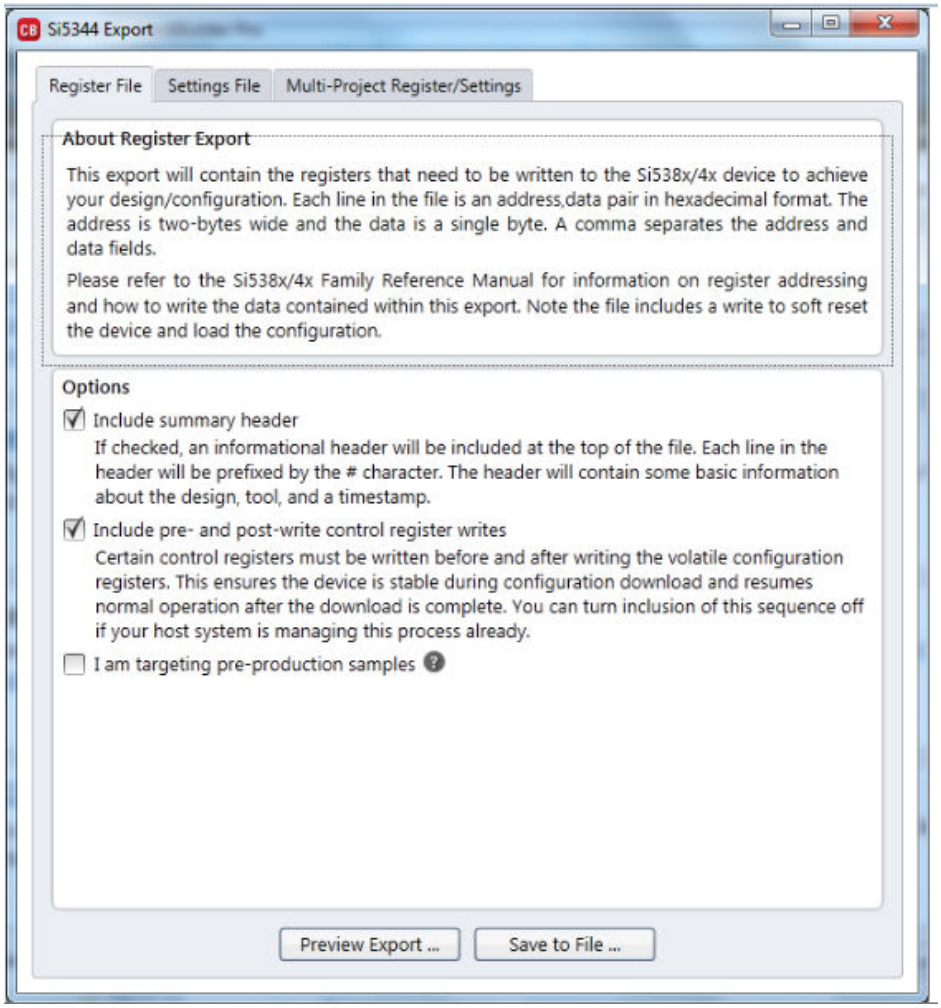


Figure 2.20. Export Settings

3. Writing A New Frequency Plan or Device Configuration to Non-volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5344H using ClockBuilder Pro on the Si5344H EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5344H RAM space and can be done virtually unlimited number of times. Writing to OTP is limited, as described below.

Refer to the Si534x/8x Family Reference Manuals and device datasheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can only be programmed a maximum of two times. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

4. Serial Device Communications (Si5344H ↔ MCU)

4.1 On-Board SPI Support

The MCU on-board the Si5344H-EVB communicates with the Si5344H device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5344H device is the SPI slave. The Si5344H device can also support a 2-wire I2C serial interface, although the Si5344H-EVB does NOT support the I2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I2C.

4.2 External I2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5344H pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5344H device. The shunt at JP1 (I2C_SEL) must also be removed to select I^2C as Si5344H interface type. An external I2C controller connected to the Si5344H side of J17 can then communicate to the Si5344H device. (For more information on I^2C signal protocol, please refer to the Si5344H data sheet.)

The figure below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5344H device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I2C operation should use J17 pin 4 (DUT_SDA_SDIO) as the I^2C SDA and J17 pin 8 (DUT_SCLK) as the I^2C SCLK. Please note the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

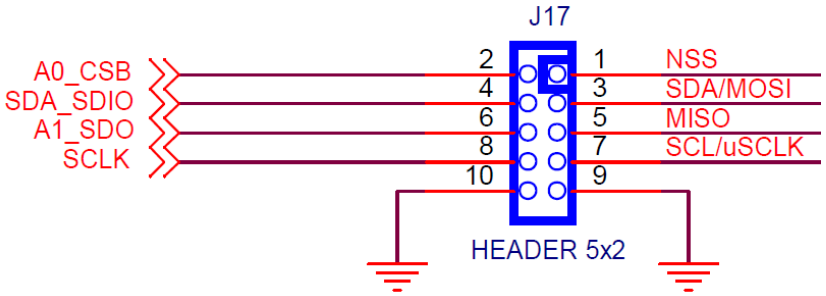
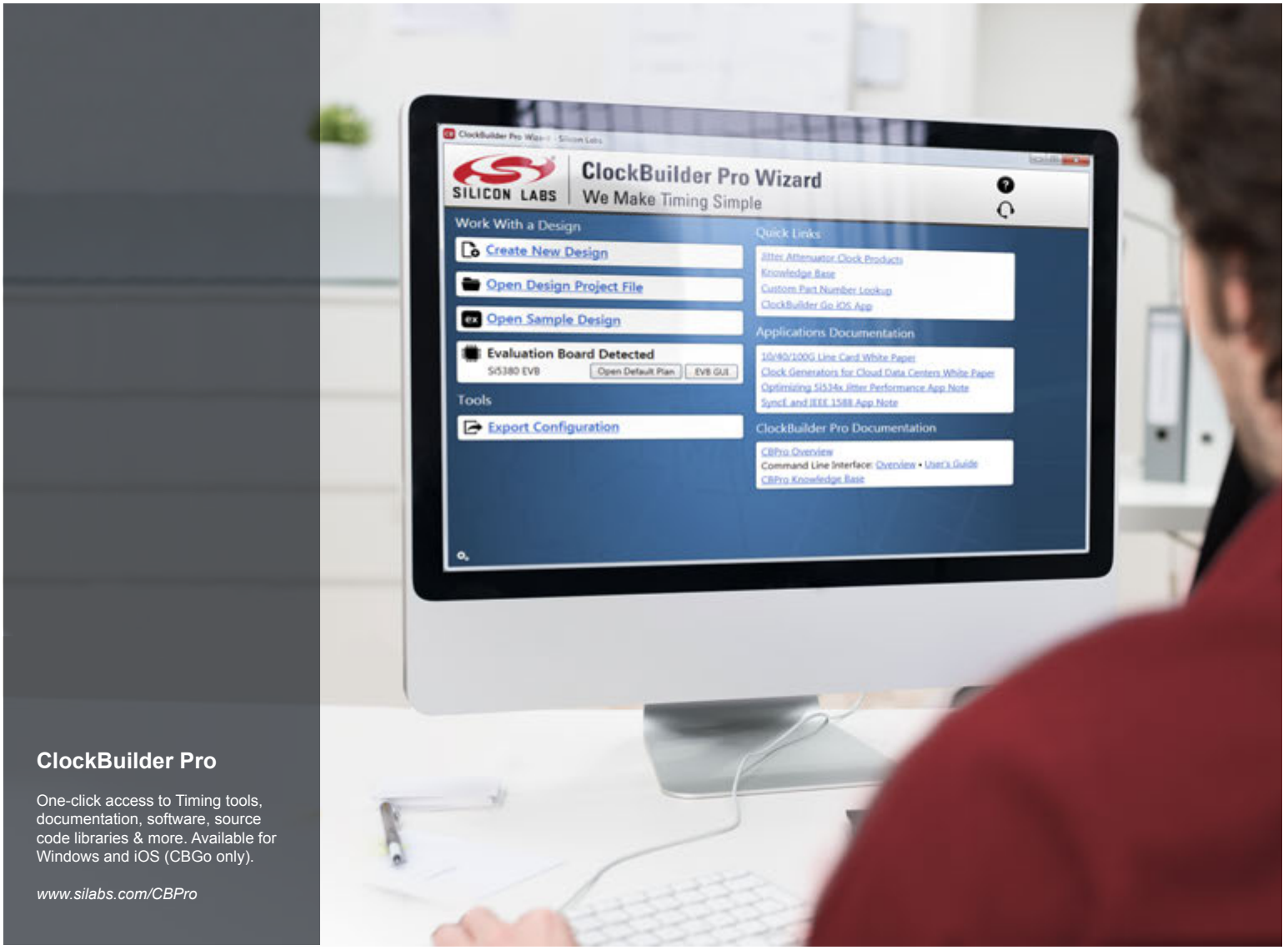


Figure 4.1. Serial Communications Header J17



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

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