International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

IRGC100B120KB②

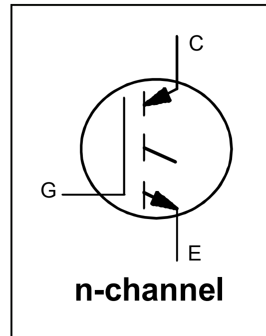
Die in Wafer Form

Features

- GEN5 Non Punch Through (NPT) Technology
- Low $V_{CE(on}$
- 10µs Short Circuit Capability
- Square RBSOA
- Positive $V_{CE(on)}$ Temperature Coefficient

Benefits

- Benchmark Efficiency for Motor Control Applications
- Rugged Transient Performance
- Excellent Current Sharing in Parallel Operation



n-channel

V_{CES} = 1200V
$I_{C(Noml)}$ = 100A
$V_{CE(on)}$ typ = 2.3V①
@ $I_{C(nom)}$ @ 25°C
Motor Control IGBT
Short Circuit Rated
150mm Wafer

Electrical Characteristics (Wafer Form)①

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	——	2.3	2.6	V	V_{GE} = 15V, I_C = 100A, T_J = 25°C
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	——	——		V_{GE} = 0V, I_{CES} = 1mA , T_J = 25°C
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	4.5	——	6.0		V_{GE} = $V_{CE,}$ I_C = 1mA, T_J = 25°C
I_{CES}	Zero Gate Voltage Collector Current	——	——	40	µA	V_{CE} = 1200V, V_{GE} = 0V, T_J = 25°C
I_{GES}	Gate Emitter Leakage Current	——	——	± 400	nA	V_{CE} = 0V, V_{GE} = ±20V, T_J = 25°C

Mechanical Parameter

Nominal Backside Metal Composition, (Thickness)	Al - Ti - Ni/V - Ag (1kA -1kA - 4kA - 6kA)
Nominal Front Metal Composition, (Thickness)	99% Al 1% Si (4µm)
Dimensions	0.488" x 0.488"
Wafer Diameter	150mm, with std. < 100> flat
Wafer Thickness, Tolerance	185µm, +/-15µm
Relevant Die Mechanical Dwg. Number	01-5318
Minimum Street Width	100µm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	Consistent throughout same wafer lot
Recommended Storage Environment	Store in original container, in desiccate nitrogen, with no contamination
Recommended Die Attach Conditions	For optimum electrical results, die attach temperature should not exceed 300ºC.

Note:

① This IR product is100% tested at wafer level and is manufactured using established, mature and well characterized processes. Due to restrictions in die level processing, die may not be equivalent to standard package products and are therefore offered with a conditional performance guarantee. The above data sheet is based on IR sample testing under certain predetermined and assumed conditions, and are provided for illustration purposes only. Customers are encouraged to perform testing in actual proposed packaged and use conditions. IR die products are tested using IR-based quality assurance procedures and are manufactured using IR's established processes. Programs for customer-specified testing are available upon request. IR has experienced assembly yields of generally 95% or greater for individual die; however, customer's results will vary. Estimates such as those described and set forth in this data sheet for semiconductor die will vary depending on a number of packaging, handling, use and other factors. Sold die may not perform on an equivalent basis to standard package products and are therefore offered with a limited warranty as described in IR's applicable standard terms and conditions of sale. All IR die sales are subject to IR's applicable standard terms and conditions of sale, which are available upon request. For customers requiring a particular parameter to be guaranteed, special testing can be carried out or product can be purchased as known good die.

② Part number shown is for die in wafer. Contact factory for these other options.

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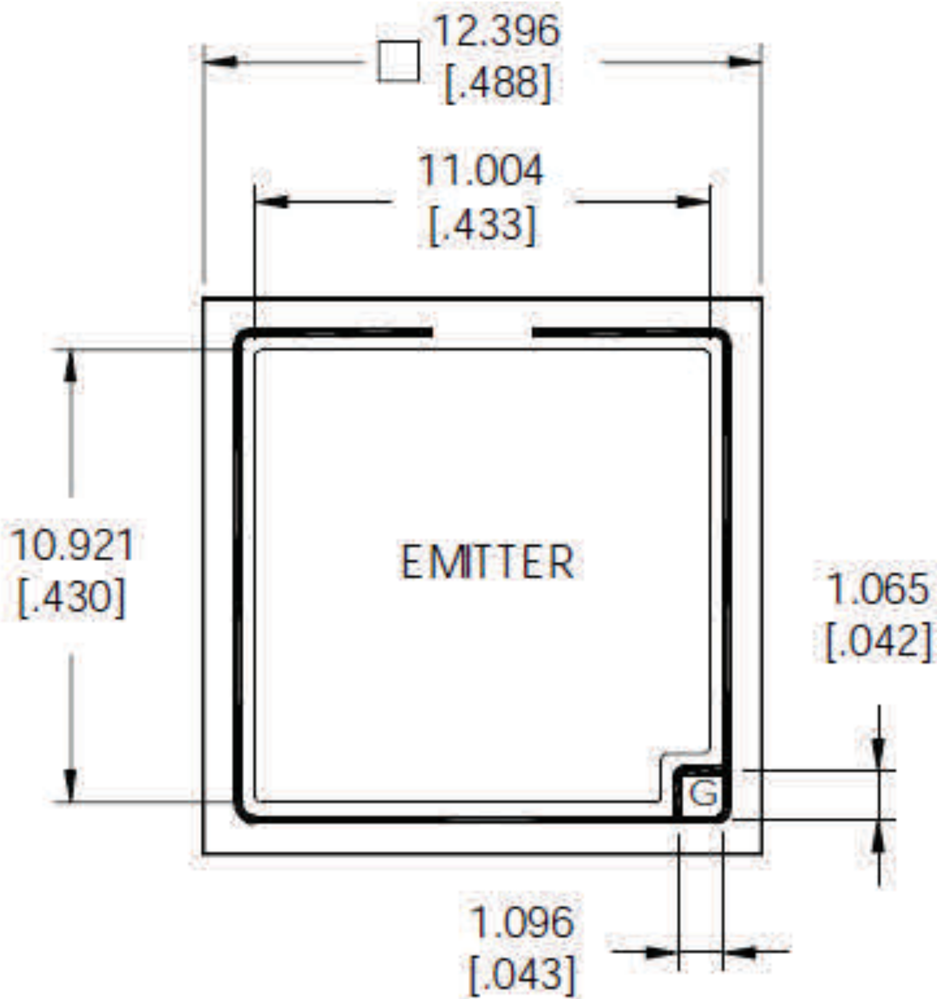
Die Outline



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: [INCH].
3. LETTER DESIGNATION:

S = SOURCE	SK = SOURCE KELVIN	E = EMITTER
G = GATE	IS = CURRENTSENSE	

4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635 TOLERANCE	= +/- 0.013
WIDTH	< [.0250] TOLERANCE	= +/- [.0005]
&	> 0.635 TOLERANCE	= +/- 0.025
LENGTH	> [.0250] TOLERANCE	= +/- [.0010]
OVERALL DIE:	< 1.270 TOLERANCE	= +/- 0.102
WIDTH	< [.050] TOLERANCE	= +/- [.004]
&	> 1.270 TOLERANCE	= +/- 0.203
LENGTH	> [.050] TOLERANCE	= +/- [.008]

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Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non-standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Further Information

For further information please contact your local IR Sales office.

Revision History

Date	Comments
07/06/2015	• Updated IFX logo on all pages • Removed Vceon @ I_C =10A, V_{GE} = 15V on page1. • Added Vceon @ I_C =100A, V_{GE} = 15V on page1. • Corrected Vgeth min from 4.4V to 4.5V on page1. • Corrected Iges from +/-3uA to +/-400nA on page1.

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