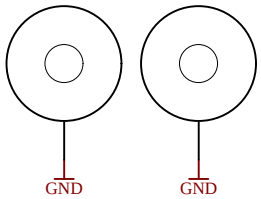
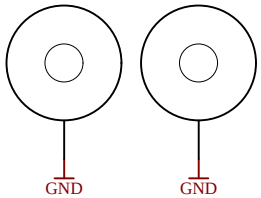
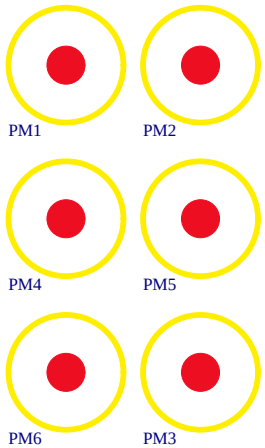
01.SchDoc
02.SchDoc
03.SchDoc
04.SchDoc
05.SchDoc
06.SchDoc
07.SchDoc
08.SchDoc
09.SchDoc
10.SchDoc

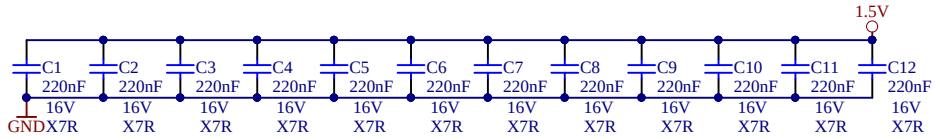
Mount.Hole 3.2mm Mount.Hole 3.2mm

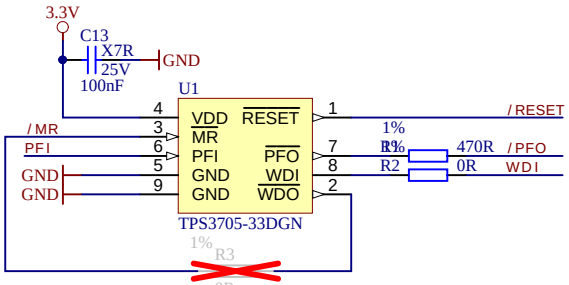


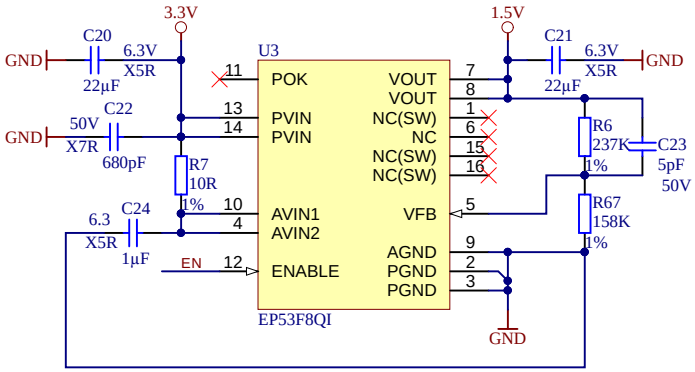
Mount.Hole 3.2mm Mount.Hole 3.2mm

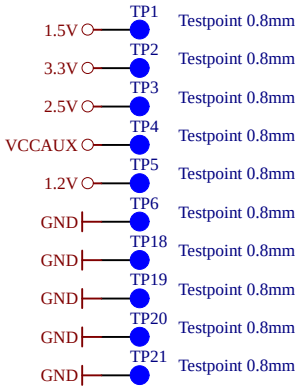


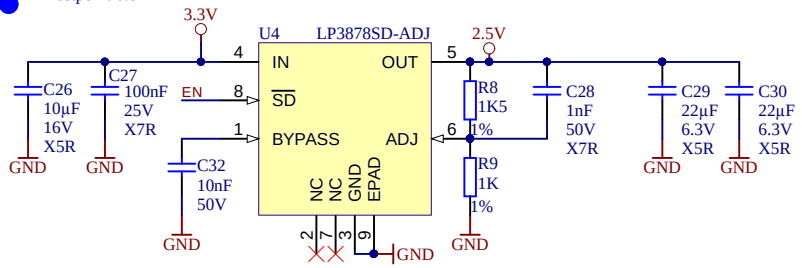


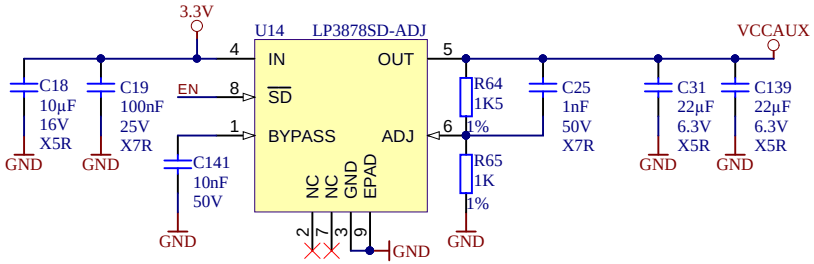




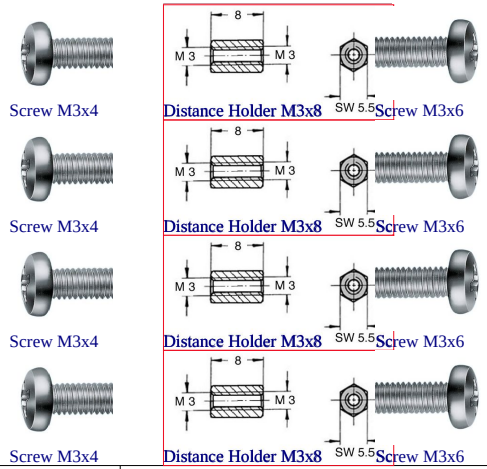




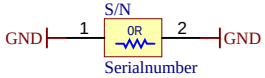




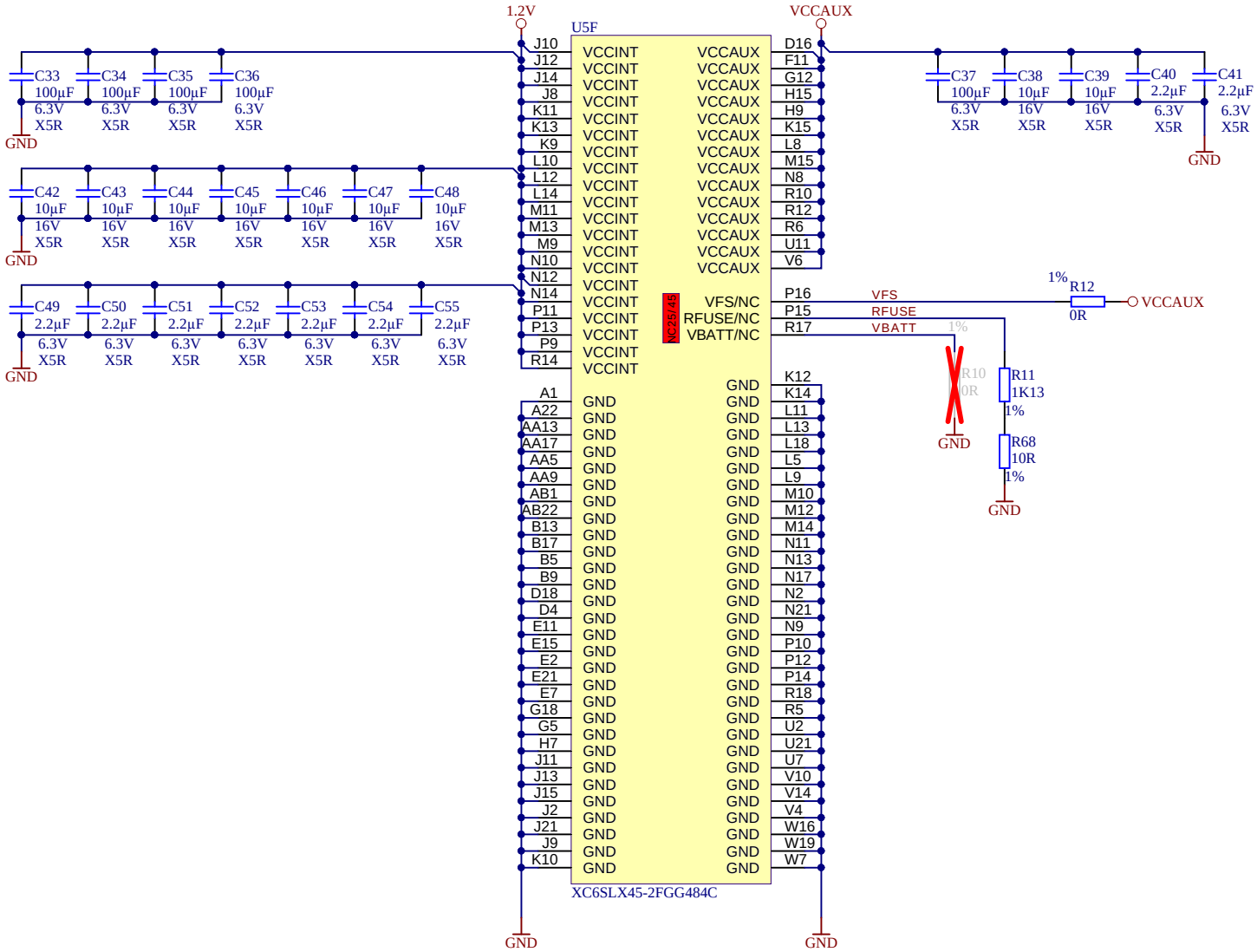
Top of Board



Serial
Serial
Serialnumber 6,3 x 6.3mm



Title: TE0600			
A4	Number: GigaBee FPGA Module TE0600-03		Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page1 of 12
Filename: 00.SchDoc			



Title: TE0600 - FPGA_PWR			
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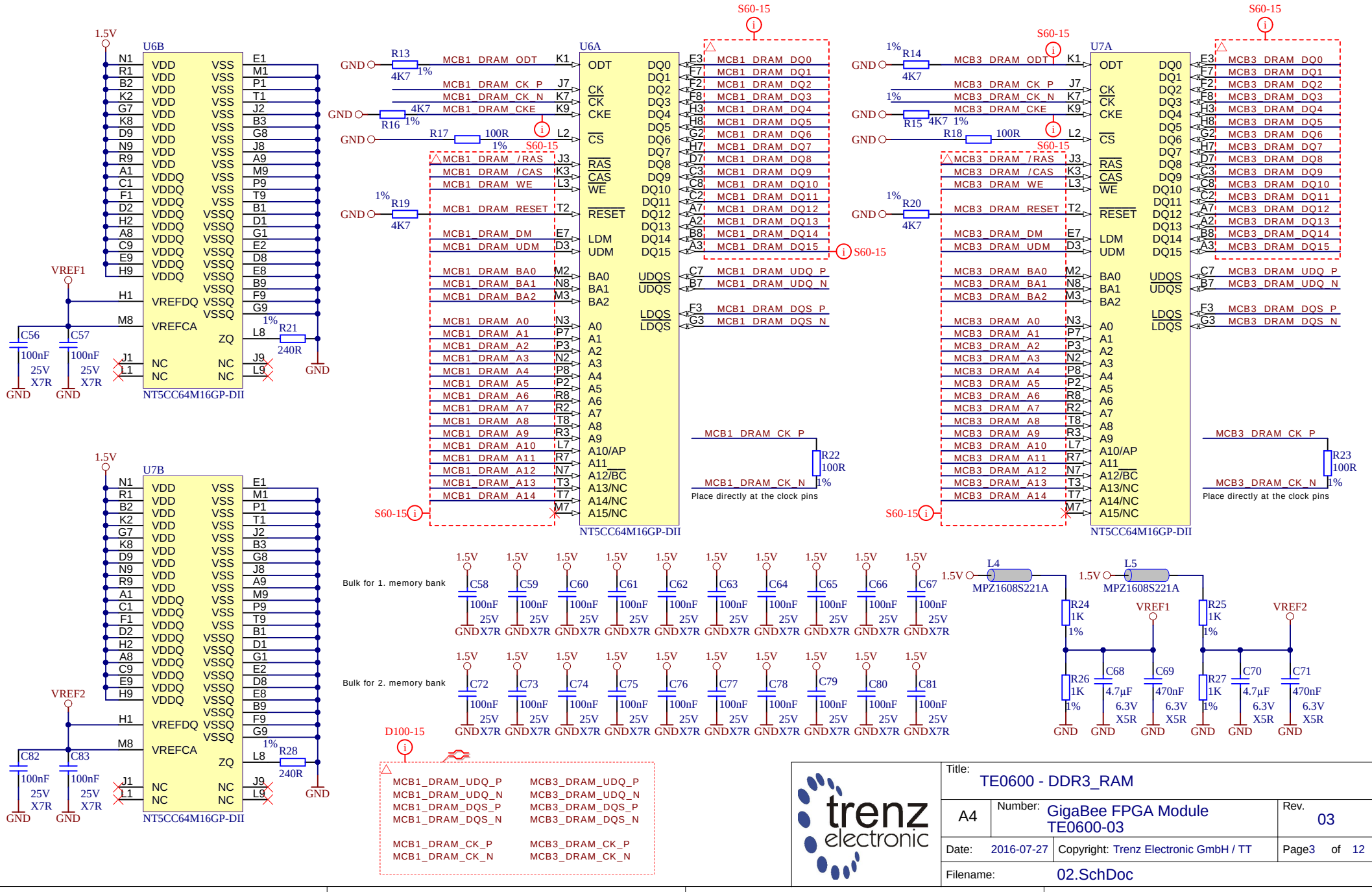
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page2 of 12
Filename: 01.SchDoc			



Title: TE0600 - DDR3_RAM			
A4	Number: GigaBee FPGA Module TE0600-03		Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page3 of 12
Filename: 02.SchDoc			

Trace widths should be 3 to 5 mils.
• Trace spacing should be three times the trace width.
• Signals must not be routed over splits or voids.
• Routing of differential pairs adjacent to noisy signal lines or high-speed switching
devices such as clock chips should be avoided.
• The spacing between differential clocks/strobes and other signals on the same PCB
layer should be 20 mil. The 20 mil spacing should be maintained when using serpentine routing for length matching.
Differential clocks/strobes are to be routed as 100O differential signals. The clock
pairs must be routed on the same PCB layer with no layer changes or hops after the
initial pad to via breakout.
The Data (DQ), Data Mask (DM), and Data Strobe (DQS) signals should receive the highest
priority (that is, routed first), because they are the highest speed DDR signals.
• DQ, DM, and DQS signals should be routed in a data group (per byte). Each group should have similar loading and routing to maintain timing and signal integrity.
• The provided spacing should be 20 mil between a data group and any other signals.
• DQS signals should be isolated from other signals by 20 mil to avoid crosstalk.
• There should be a maximum of ±25 ps electrical delay (±150 mil) between any DQ/DM and its associated DQS strobe.
• A data group should be referenced to a GROUND plane.
• DQ bit swapping at the memory interface is permitted to facilitate layout. Swapping
should only be done within a data group.
• DQS to DQS_N trace lengths should be matched (±10 mil).
• Memory terminations (if external terminations are used) should be placed after the
associated memory component in a fly-by fashion.
• For 16-bit DDR devices, the LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±25 ps of the electrical delay (±150 mil).
When the data groups have been routed, the next highest priority is the differential clock
(CK / CK_N). The clock should be routed first because all address and control trace length
matching must be referenced to the differential clock PCB trace length, which might need
to be adjusted as the layout task proceeds.
• CK to CK_N trace lengths must be matched (±10 mil).
• CK and DQS trace lengths must be matched (±250 mil) to maximize setup and hold margins.
• There must be a maximum ±50 ps electrical delay (±300 mil) between any address/control signals and the associated CK and CK_N differential clock FPGA output.
• Address and control signals can be referenced to a POWER plane if a GROUND plane
is not next to this group of signals in the PCB stack-up.
To avoid crosstalk, address and command signals should be kept on a different routing layer from DQ, DQS, and DM.
• Differential clock terminations (if external terminations are used) must be located as
close as possible to the load, after the clock pads of the PCB. PCB trace lengths used in
trace length matching must exclude the CLINE length of the PCB trace from memory ball to terminating resistor.

Classnames:
S60-15 uses 1.5V or GND plane as reference
D100-15 uses 1.5V or GND plane as reference

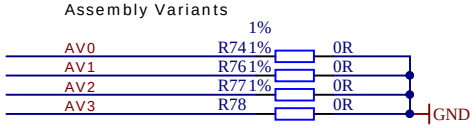
S60-25 uses 2.5V or GND plane as reference
D100-25 uses 2.5V or GND plane as reference

S60-IO uses VCCIO0 or GND plane as reference
D100-IO uses VCCIO0 or GND plane as reference

S60-33 uses 3.3V or GND plane as reference
D100-33 uses 3.3V or GND plane as reference

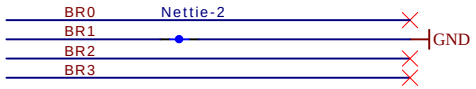
AV0 = 0 -> commercial AV0 = 1 -> Industrial
AV1 = 0 -> speedgrade 2 AV1 = 1 -> speedgrade 3
AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte
AV3 = Open -> Customized variants

Assembly Variants



BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02
1	1	0	1	-03

Board Revisions



Enable pullups in FPGA

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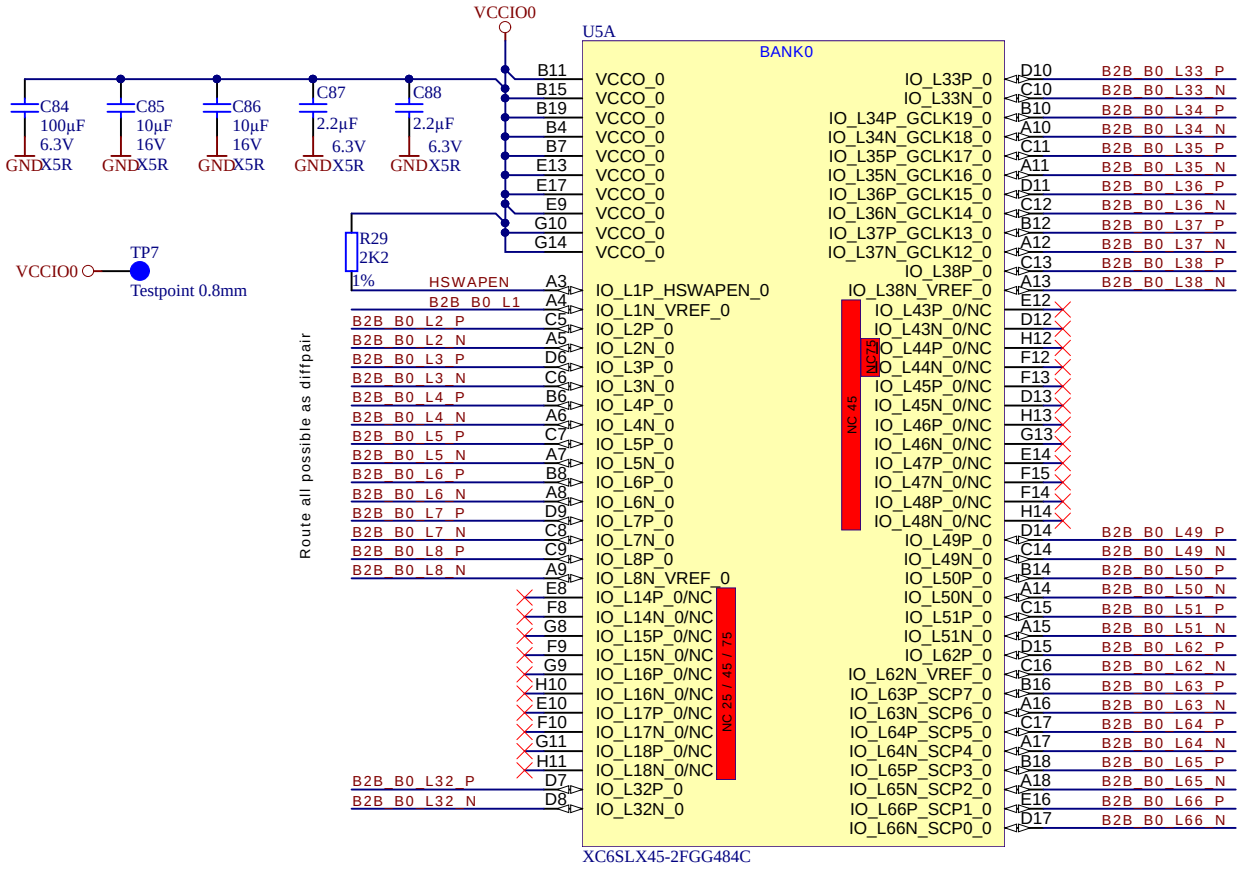
Title: TE0600 - Configuration		
A4	Number: GigaBee FPGA Module TE0600-03	Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT	Page4 of 12
Filename: 03.SchDoc		



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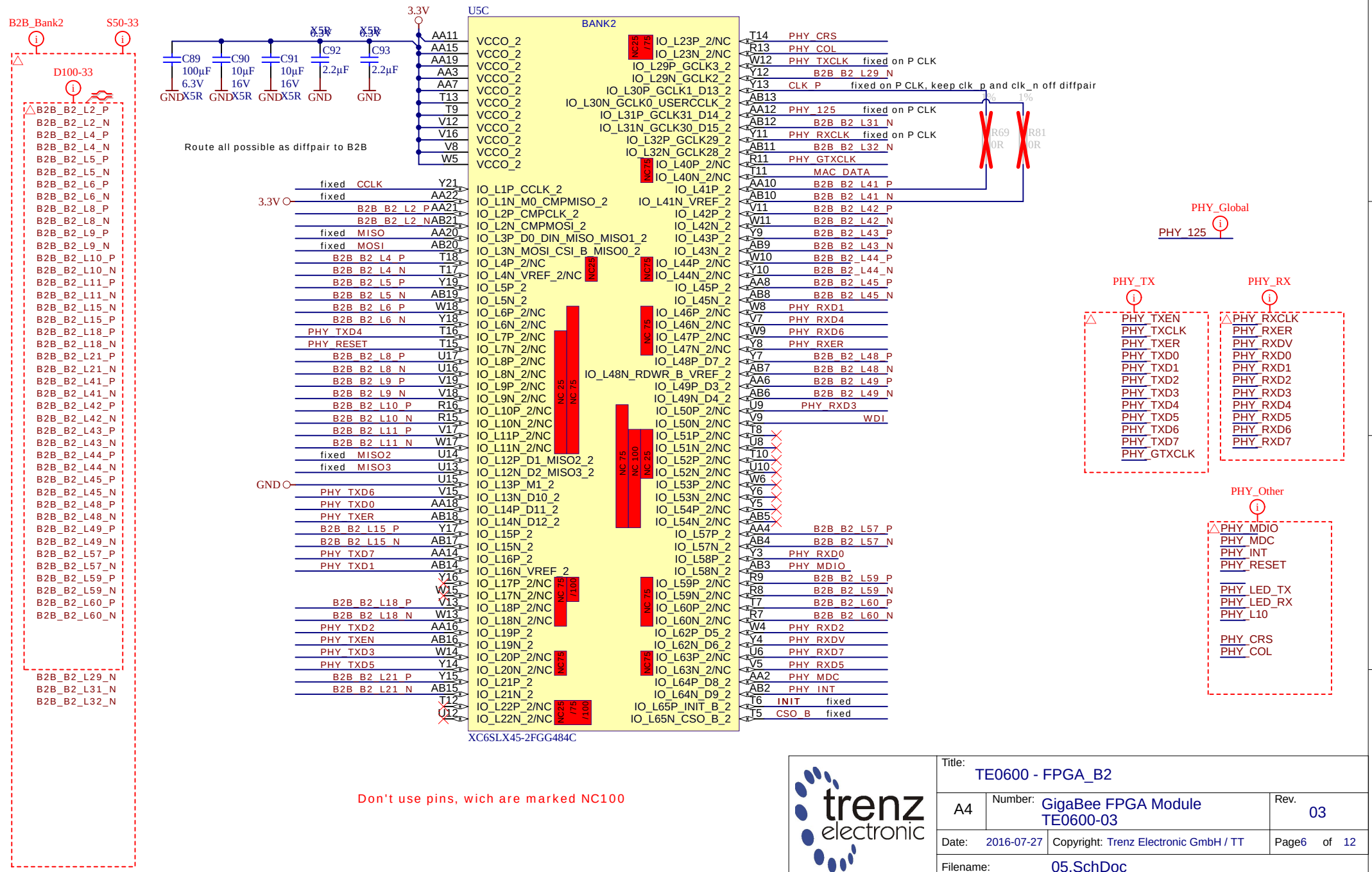
Title: TE0600 - FPGA_B0			
A4	Number: GigaBee FPGA Module TE0600-03		Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page5 of 12
Filename: 04.SchDoc			


B2B_Bank2
S50-33
D100-33
B2B_B2_L2_P
B2B_B2_L2_N
B2B_B2_L4_P
B2B_B2_L4_N
B2B_B2_L5_P
B2B_B2_L5_N
B2B_B2_L6_P
B2B_B2_L6_N
B2B_B2_L8_P
B2B_B2_L8_N
B2B_B2_L9_P
B2B_B2_L9_N
B2B_B2_L10_P
B2B_B2_L10_N
B2B_B2_L11_P
B2B_B2_L11_N
B2B_B2_L15_P
B2B_B2_L15_N
B2B_B2_L18_P
B2B_B2_L18_N
B2B_B2_L21_P
B2B_B2_L21_N
B2B_B2_L29_N
B2B_B2_L31_N
B2B_B2_L32_N
3.3V
C89 100µF 6.3V X5R
C90 10µF 16V X5R
C91 10µF 16V X5R
C92 2.2µF
C93 2.2µF
GND
Route all possible as diffpair to B2B
U5C
BANK2
XC6SLX45-2FGG484C
Don't use pins, wich are marked NC100
PHY_Global
PHY_125
PHY_TX
PHY_TXEN
PHY_TXCLK
PHY_TXER
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_GTXCLK
PHY_RX
PHY_RXCLK
PHY_RXER
PHY_RXDV
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_Other
PHY_MDIO
PHY_MDC
PHY_INT
PHY_RESET
PHY_LED_TX
PHY_LED_RX
PHY_L10
PHY_CRS
PHY_COL
R69 0R
R81 0R
1%
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Title: TE0600 - FPGA_B2
A4
Number: GigaBee FPGA Module TE0600-03
Rev. 03
Date: 2016-07-27
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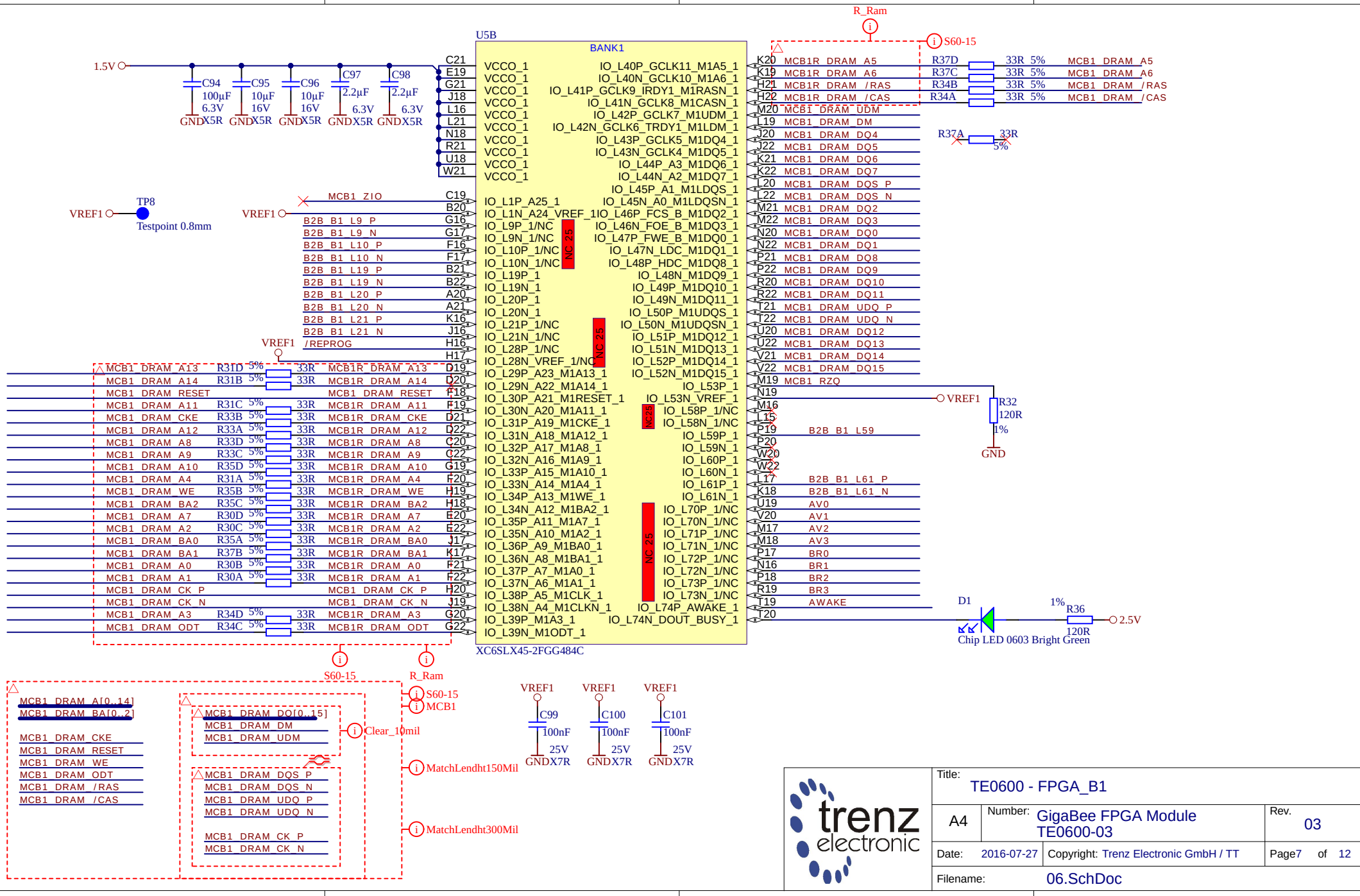
Filename: 05.SchDoc



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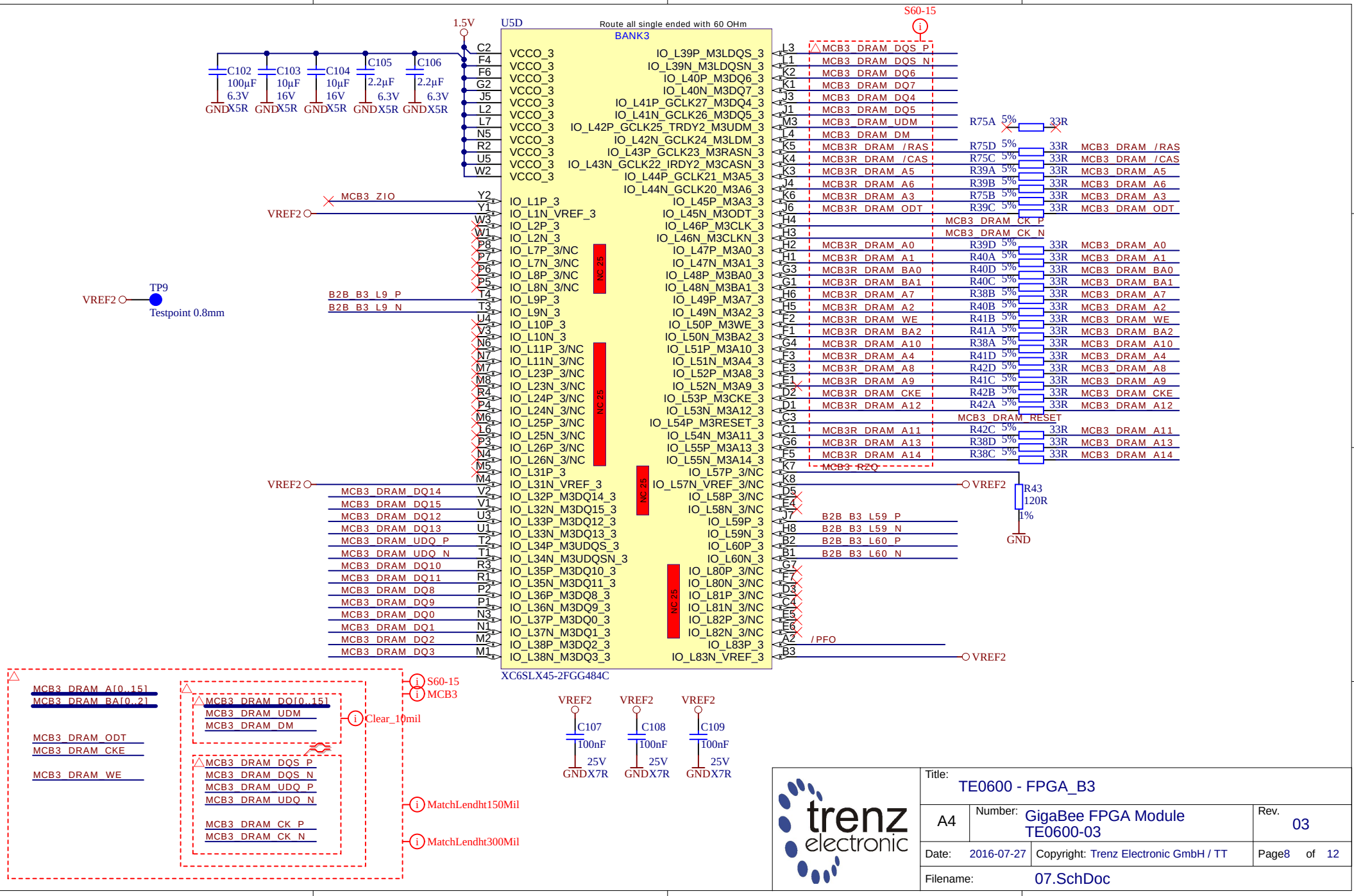
Title: TE0600 - FPGA_B1			
A4	Number: GigaBee FPGA Module TE0600-03		Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page7 of 12
Filename: 06.SchDoc			


1.5V
U5D
Route all single ended with 60 OHm
BANK3
S60-15
C102 100µF 6.3V X5R
C103 10µF 16V X5R
C104 10µF 16V X5R
C105 2.2µF 6.3V X5R
C106 2.2µF 6.3V X5R
GND
VCCO_3
IO_L1P_3
IO_L1N_VREF_3
IO_L2P_3
IO_L2N_3
IO_L7P_3/NC
IO_L7N_3/NC
IO_L8P_3/NC
IO_L8N_3/NC
IO_L9P_3
IO_L9N_3
IO_L10P_3
IO_L10N_3
IO_L11P_3/NC
IO_L11N_3/NC
IO_L23P_3/NC
IO_L23N_3/NC
IO_L24P_3/NC
IO_L24N_3/NC
IO_L25P_3/NC
IO_L25N_3/NC
IO_L26P_3/NC
IO_L26N_3/NC
IO_L31P_3
IO_L31N_VREF_3
IO_L32P_M3DQ14_3
IO_L32N_M3DQ15_3
IO_L33P_M3DQ12_3
IO_L33N_M3DQ13_3
IO_L34P_M3UDQS_3
IO_L34N_M3UDQSN_3
IO_L35P_M3DQ10_3
IO_L35N_M3DQ11_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L45P_M3A3_3
IO_L45N_M3ODT_3
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L49P_M3A7_3
IO_L49N_M3A2_3
IO_L50P_M3WE_3
IO_L50N_M3BA2_3
IO_L51P_M3A10_3
IO_L51N_M3A4_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L53P_M3CKE_3
IO_L53N_M3A12_3
IO_L54P_M3RESET_3
IO_L54N_M3A11_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L57P_3/NC
IO_L57N_VREF_3/NC
IO_L58P_3/NC
IO_L58N_3/NC
IO_L59P_3
IO_L59N_3
IO_L60P_3
IO_L60N_3
IO_L80P_3/NC
IO_L80N_3/NC
IO_L81P_3/NC
IO_L81N_3/NC
IO_L82P_3/NC
IO_L82N_3/NC
IO_L83P_3
IO_L83N_VREF_3
NC 25
MCB3_ZIO
VREF2
TP9
Testpoint 0.8mm
B2B_B3_L9_P
B2B_B3_L9_N
MCB3_DRAM_DQ14
MCB3_DRAM_DQ15
MCB3_DRAM_DQ12
MCB3_DRAM_DQ13
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_DQ10
MCB3_DRAM_DQ11
MCB3_DRAM_DQ8
MCB3_DRAM_DQ9
MCB3_DRAM_DQ0
MCB3_DRAM_DQ1
MCB3_DRAM_DQ2
MCB3_DRAM_DQ3
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_DQ6
MCB3_DRAM_DQ7
MCB3_DRAM_DQ4
MCB3_DRAM_DQ5
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3R_DRAM_/RAS
MCB3R_DRAM_/CAS
MCB3R_DRAM_A5
MCB3R_DRAM_A6
MCB3R_DRAM_A3
MCB3R_DRAM_ODT
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3R_DRAM_A0
MCB3R_DRAM_A1
MCB3R_DRAM_BA0
MCB3R_DRAM_BA1
MCB3R_DRAM_A7
MCB3R_DRAM_A2
MCB3R_DRAM_WE
MCB3R_DRAM_BA2
MCB3R_DRAM_A10
MCB3R_DRAM_A4
MCB3R_DRAM_A8
MCB3R_DRAM_A9
MCB3R_DRAM_CKE
MCB3R_DRAM_A12
MCB3_DRAM_RESET
MCB3R_DRAM_A11
MCB3R_DRAM_A13
MCB3R_DRAM_A14
MCB3_RZQ
R75A 5% 33R
R75D 5% 33R MCB3_DRAM_/RAS
R75C 5% 33R MCB3_DRAM_/CAS
R39A 5% 33R MCB3_DRAM_A5
R39B 5% 33R MCB3_DRAM_A6
R75B 5% 33R MCB3_DRAM_A3
R39C 5% 33R MCB3_DRAM_ODT
R39D 5% 33R MCB3_DRAM_A0
R40A 5% 33R MCB3_DRAM_A1
R40D 5% 33R MCB3_DRAM_BA0
R40C 5% 33R MCB3_DRAM_BA1
R38B 5% 33R MCB3_DRAM_A7
R40B 5% 33R MCB3_DRAM_A2
R41B 5% 33R MCB3_DRAM_WE
R41A 5% 33R MCB3_DRAM_BA2
R38A 5% 33R MCB3_DRAM_A10
R41D 5% 33R MCB3_DRAM_A4
R42D 5% 33R MCB3_DRAM_A8
R41C 5% 33R MCB3_DRAM_A9
R42B 5% 33R MCB3_DRAM_CKE
R42A 5% 33R MCB3_DRAM_A12
R42C 5% 33R MCB3_DRAM_A11
R38D 5% 33R MCB3_DRAM_A13
R38C 5% 33R MCB3_DRAM_A14
R43 120R 1%
B2B_B3_L59_P
B2B_B3_L59_N
B2B_B3_L60_P
B2B_B3_L60_N
/PFO
C107 100nF 25V X7R
C108 100nF 25V X7R
C109 100nF 25V X7R
MCB3_DRAM_A[0..15]
MCB3_DRAM_BA[0..2]
MCB3_DRAM_ODT
MCB3_DRAM_CKE
MCB3_DRAM_WE
MCB3_DRAM_DQ[0..15]
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
S60-15
MCB3
Clear_10mil
MatchLendht150Mil
MatchLendht300Mil
XC6SLX45-2FGG484C
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Title: TE0600 - FPGA_B3
A4
Number: GigaBee FPGA Module TE0600-03
Rev. 03
Date: 2016-07-27
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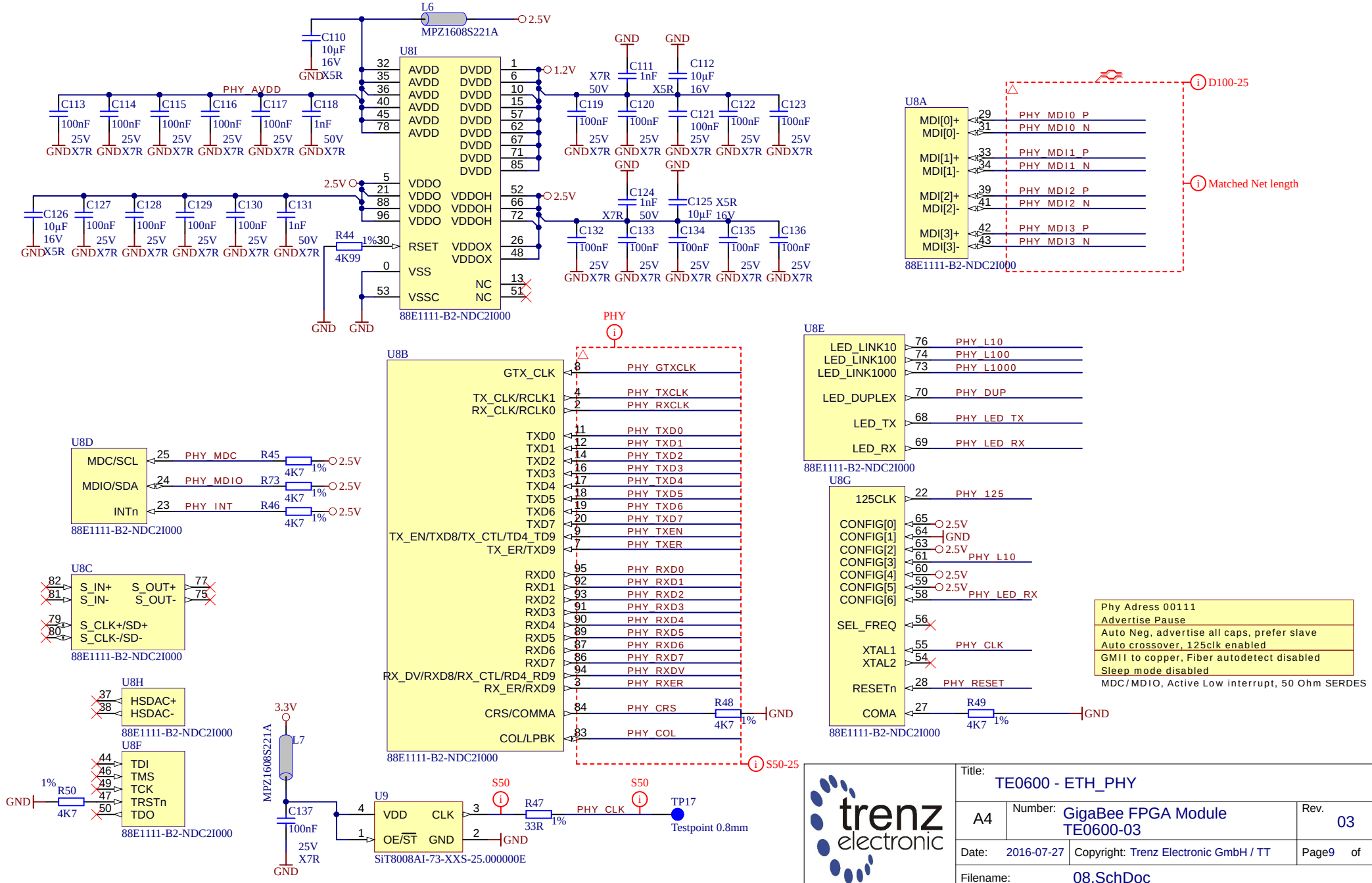
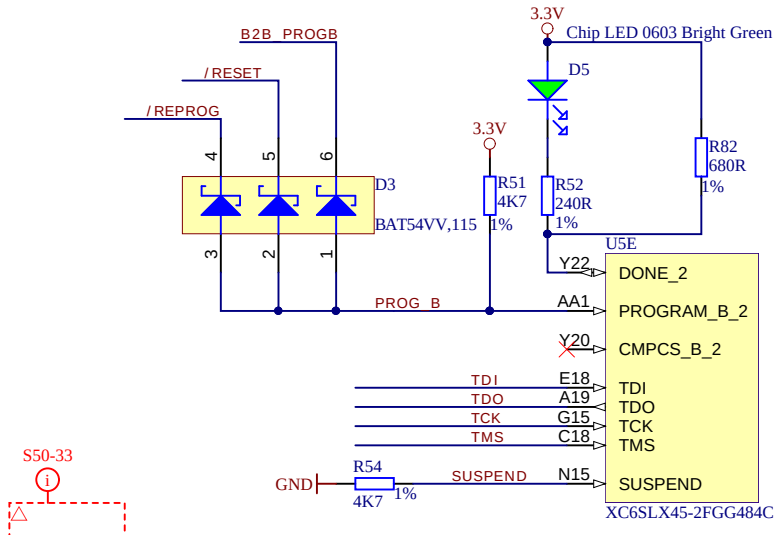
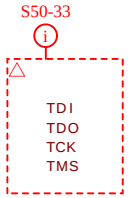
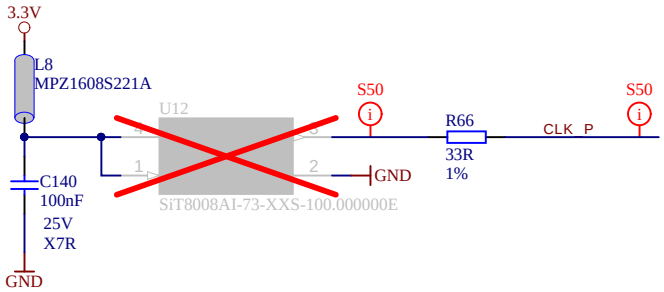
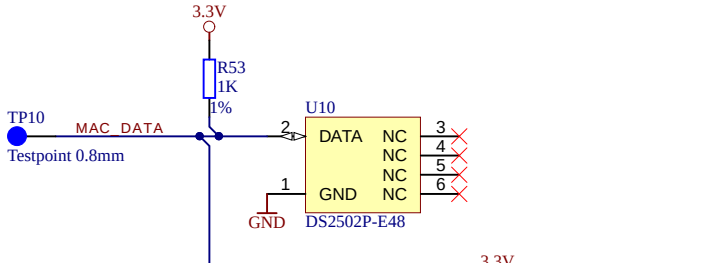
Page8 of 12
Filename: 07.SchDoc

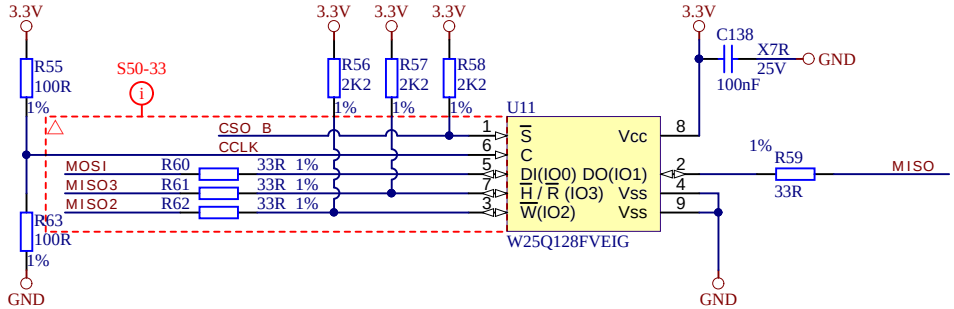

L6
MPZ1608S221A
2.5V
C110
10µF
16V
X5R
U8I
AVDD
DVDD
VDDO
VDDOH
VDDOX
RSET
VSS
VSSC
NC
1.2V
2.5V
PHY_AVDD
C113 C114 C115 C116 C117 C118
100nF 100nF 100nF 100nF 100nF 1nF
25V X7R
50V
C119 C120 C121 C122 C123
C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136
R44
4K99
1%
88E1111-B2-NDC2I000
GND
U8A
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-25
Matched Net length
PHY
U8B
GTX_CLK
TX_CLK/RCLK1
RX_CLK/RCLK0
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TX_EN/TXD8/TX_CTL/TD4_TD9
TX_ER/TXD9
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RX_DV/RXD8/RX_CTL/RD4_RD9
RX_ER/RXD9
CRS/COMMA
COL/LPBK
PHY_GTXCLK
PHY_TXCLK
PHY_RXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_CRS
PHY_COL
R48
4K7
S50-25
U8E
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_TX
LED_RX
PHY_L10
PHY_L100
PHY_L1000
PHY_DUP
PHY_LED_TX
PHY_LED_RX
U8G
125CLK
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
CONFIG[6]
SEL_FREQ
XTAL1
XTAL2
RESETn
COMA
PHY_125
PHY_CLK
PHY_RESET
R49
U8D
MDC/SCL
MDIO/SDA
INTn
PHY_MDC
PHY_MDIO
PHY_INT
R45
R73
R46
U8C
S_IN+
S_IN-
S_OUT+
S_OUT-
S_CLK+/SD+
S_CLK-/SD-
U8H
HSDAC+
HSDAC-
U8F
TDI
TMS
TCK
TRSTn
TDO
R50
3.3V
MPZ1608S221A
L7
C137
U9
VDD
CLK
OE/ST
GND
SiT8008AI-73-XXS-25.000000E
S50
R47
33R
PHY_CLK
TP17
Testpoint 0.8mm
Phy Adress 00111
Advertise Pause
Auto Neg, advertise all caps, prefer slave
Auto crossover, 125clk enabled
GMII to copper, Fiber autodetect disabled
Sleep mode disabled
MDC/MDIO, Active Low interrupt, 50 Ohm SERDES
trenz electronic
Title: TE0600 - ETH_PHY
A4
Number: GigaBee FPGA Module TE0600-03
Rev. 03
Date: 2016-07-27
Copyright: Trenz Electronic GmbH / TT
Page9 of 12
Filename: 08.SchDoc









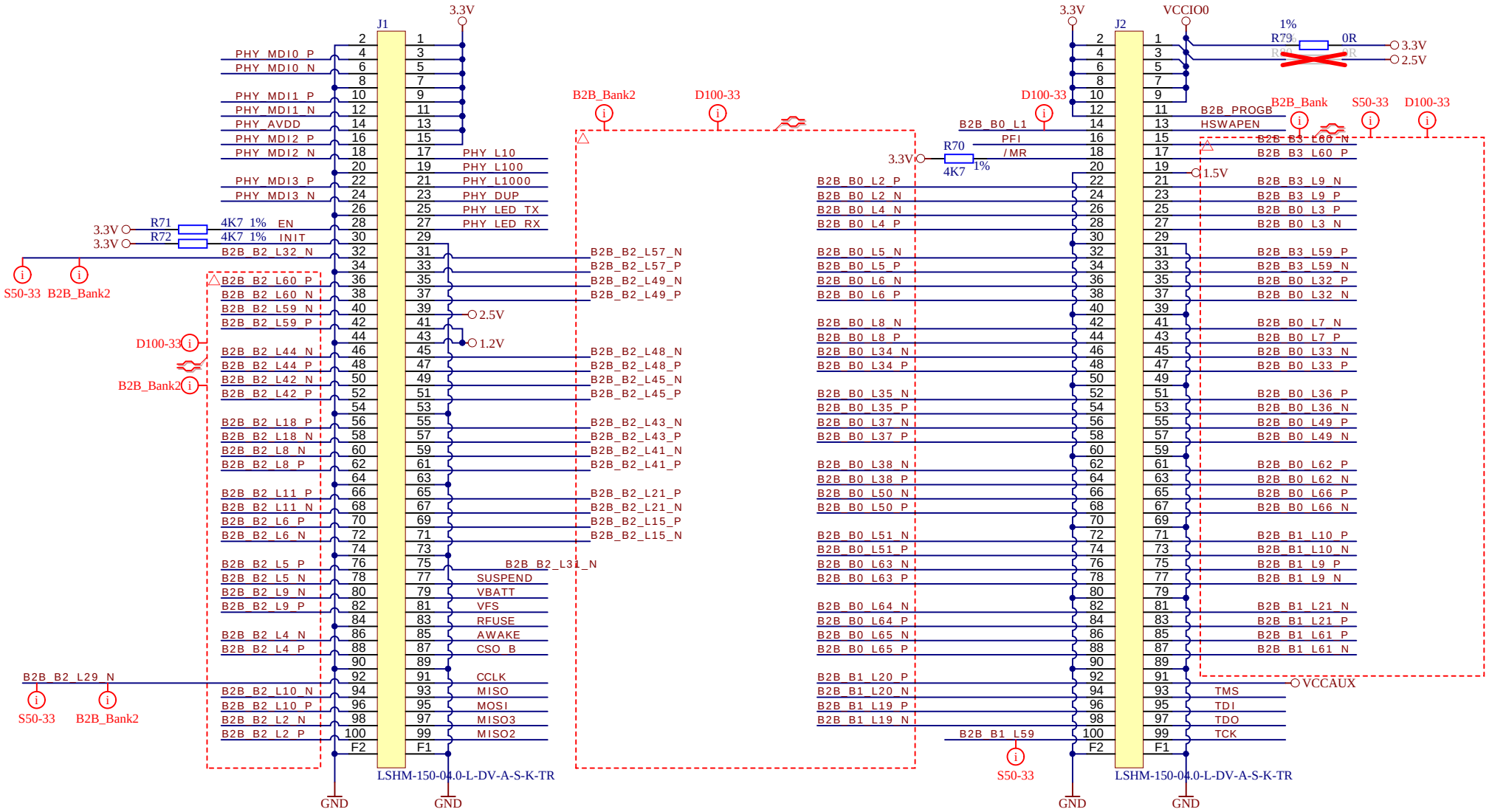


Put cclk termination close to the input pin

Testpoint 0.8mm TP16 CLK_P

Testpoint 0.8mm TP22 PROG_B

trenz electronic	Title: TE0600 - FPGA_CFG		
	A4	Nummer: GigaBee FPGA Module TE0600-03	Rev. 03
	Datum: 2016-07-27	Zeichner: Trenz Electronic GmbH / TT	Blatt 10 von 12
	Filename: 09.SchDoc		



trenz electronic	Title: TE0600 - B2B Connectors		
A4	Number: GigaBee FPGA Module TE0600-03		Rev. 03
Date: 2016-07-27	Copyright: Trenz Electronic GmbH / TT		Page11 of 12
Filename: 10.SchDoc			

CHANGES REV02 to REV03

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1) added NetTie (board revision 03)
2) optimized placement and routing pwr DCDC
3) added tespoints
4) changed OSC U9 (AN25008, SiT8008AI-73-XXS-25.000000E)
5) update Razorbeam Connectors, full update lib
6) added serial number (tracebility pad)
7) added thermal vias to mounting holes
8) changed SPI flash (AN26012,W25Q128FVEIG 3V 128MBit Serial Flash)
9) changed DDR3 (AN27202, AN27039)
10) U13 (DS2432P+) is not populated

trenz electronic	Title: TE0600 - Changes list		
	A4	Number: GigaBee FPGA Module TE0600-03	Rev. 03
	Date: 2016-07-27	Copyright: Trenz Electronic GmbH	Page12 of 12
	Filename: Revision_Changes.SchDoc		