Click here to ask an associate for production status of specific part numbers.

MAX25606

6-Switch Matrix Manager for Automotive Lighting

General Description

The MAX25606 6-switch matrix manager IC for automotive lighting applications includes a 6-switch array for bypassing individual LEDs in a single- or dual-string application. It features six individually controlled n-channel MOSFET switches with each switch having an on-resistance of 0.2Ω and rated to withstand 16V. A single current source can be used to power all the LEDs connected in series. Individual LEDs can be dimmed by turning on and off the bypass switches across each LED. The device can also be configured in two string applications with three switches in series per string. Each switch can be connected across one, two, or three LEDs in series. It also allows for parallel connection of two switches to bypass high-current LEDs. The IC also includes an internal charge pump that powers the gate drive for the switches.

The IC features a universal asynchronous receiver-transmitter (UART) communication interface. Each switch can be turned on, turned off, or PWM modulated with 12 bits of PWM duty cycle adjustment. Transitions between two different PWM settings can either happen instantly or a logarithmic fade transition can be applied. The logarithmic fade algorithm is built into the device and only requires a single software command. The IC features open-LED protection as well as open and short LED fault reporting through the serial interface. The device is available in a 20-pin 4x4mm side wettable TQFN and a 20-pin thin shrink small-outline package (TSSOP) with exposed pad. The device is AEC-Q100 grade 1 qualified and designed to operate over the full -40ºC to +125ºC temperature range.

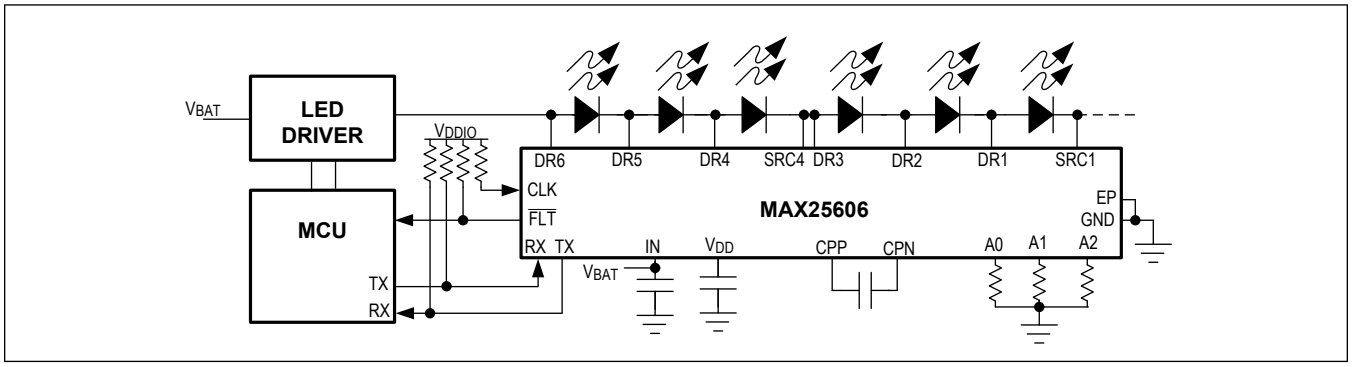
Applications

- Automotive Matrix LED Systems and Adaptive Drive Beam Lights

Benefits and Features

- Automotive Ready: AEC-Q100 Qualified
- Six-Switch Matrix Manager Allows for Flexible Configuration
  - Single and Dual-String Configurations
  - Up to 6 Switches in Series for Single String
  - Up to 3 Switches in Series in Dual-String
  - Up to 3 LEDs per Switch
- Robust Serial Interface
  - Multidrop UART Communication Interface
  - Up to 64 Addressable Devices
- Optimal PWM Dimming Arrangement Provides Excellent Dimming Performance
  - Programmable 12-Bit PWM Dimming
  - Fade Transition Between PWM Dimming States
  - Internal Clock Generator or External Clock for PWM Dimming
- EMI Mitigation
  - Programmable Slew Rate for EMI Control
  - Integrated Spread Spectrum Frequency Dithering
- Protection Features and Package Improve Reliability
  - Open-LED Protection
  - Programmable Open and Short-LED Threshold
  - Open and Shorted-LED Fault Reporting
  - Open Trace Fault Reporting
  - Thermally Enhanced 20-Pin Side Wettable TQFN and 20-Pin TSSOP with Exposed Pad

Simplified Block Diagram



Ordering Information appears at end of datasheet.

19-100947; Rev 1; 4/22

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Absolute Maximum Ratings

IN to GND ..... -0.3V to +65V
V_{DD} to GND ..... -0.3V to +2.5V
CPN to GND ..... -0.3V to +65V
CPP to GND ..... -0.3V to +70V
CPP to CPN ..... -0.3V to +6V
CPP to DR6 ..... -0.3V to +70V
DR6 to GND ..... -0.3V to +65V
DRx to DR(x-1) (Note 1) ..... -0.3V to +16V
SRCx to GND ..... -0.3V to +65V
DR6 to SRC4 ..... -0.3V to +48V
DR4 to SRC4 ..... -0.3V to +16V
DR3 to SRC1 ..... -0.3V to +48V
DR1 to SRC1 ..... -0.3V to +16V

Continuous Current on DRx, SRCx 750mA
$\overline{FLT}$, CLK to GND ..... -0.3V to +6V
RX, TX to GND ..... -0.3V to +6V
A0, A1, A2 to GND ..... -0.3V to V_{DD} + 0.3V
Continuous Power Dissipation (20-Pin TQFN SW) (T_A = +70ºC, derate 25.6mW/ºC above +70ºC) 2050mW
Continuous Power Dissipation (20-Pin TSSOP) (T_A = +70ºC, derate 26mW/ºC above +70ºC) 2122mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Does not apply to DR4 to DR3.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20 TQFN-EP* (SW)

Package Code	T2044Y+3C
Outline Number	21-100068
Land Pattern Number	90-0037
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	59ºC/W
Junction to Case (θ_{JC})	6ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	39ºC/W
Junction to Case (θ_{JC})	6ºC/W

20 TSSOP-EP*

Package Code	U20E+3C
Outline Number	21-100132
Land Pattern Number	90-100049
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	46ºC/W
Junction to Case (θ_{JC})	2ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	37ºC/W
Junction to Case (θ_{JC})	2ºC/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(Input Voltage = IN = 5V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltages						
Supply Voltage	V_{IN}	Operating Voltage Range	4.0		60	V
Input Current	I_{IN}			2	5	mA
Input Power-On Reset (POR) Threshold	V_{IN-POR}	V_{IN} Rising	3.6		3.9	V
Charge-Pump Operating Voltage	V_{CPP}				65	V
V_{DD} Regulator						
V_{DD} Output	V_{DD}	2.2µF Capacitor Placed between V_{DD} and GND Pins. I_{VDD} = 10mA	1.71	1.8	1.89	V
VDD undervoltage lockout (UVLO) Rising Threshold	UVLO_R_TH		1.61		1.69	V
VDD UVLO Falling Threshold	UVLO_F_TH		1.54		1.63	V
LED Dimming						
Internal Oscillator Frequency	F_{OSC}	Used for Charge Pump and PWM Dimming of LEDs		16.384		MHz
LED Switches						
Single-Switch On-Resistance	R_{DSON}			0.2		Ω
On-Resistance with Series Switches 3-1 On				0.6	1.2	Ω
On-Resistance with Series Switches 6-4 On				0.6	1.2	Ω
Open LED Threshold	V_{OTH}		12.5	13.75	15	V
Open Trace Threshold	I_{LED_MIN}	Minimum Current Required to Detect Open Trace		45	100	mA
Short LED Threshold	V_{STH}	VSTH[2:0] = 0b000, Rising V_{DS}	1.26	1.40	1.54	V
		VSTH[2:0] = 0b001, Rising V_{DS}	3.24	3.6	3.96	
		VSTH[2:0] = 0b010, Rising V_{DS}	3.6	4.00	4.4	
		VSTH[2:0] = 0b011, Rising V_{DS}	4.95	5.5	6.05	
		VSTH[2:0] = 0b100, Rising V_{DS}	5.4	6.0	6.6	
		VSTH[2:0] = 0b101, Rising V_{DS}	5.94	6.6	7.26	
		VSTH[2:0] = 0b110, Rising V_{DS}	6.48	7.2	7.92	
		VSTH[2:0] = 0b111, Rising V_{DS}	6.93	7.70	8.47	
$\overline{FLT}$ Flag						
$\overline{FLT}$ Output Low Voltage		I_{SINK} = 2 mA		0.06	0.4	V
$\overline{FLT}$ Output High Leakage Current		$\overline{FLT}$ = 5V			1	µA
Clock External Sync Input, Clock Frequency	f_{CLK}		0.3		18	MHz

Electrical Characteristics (continued)

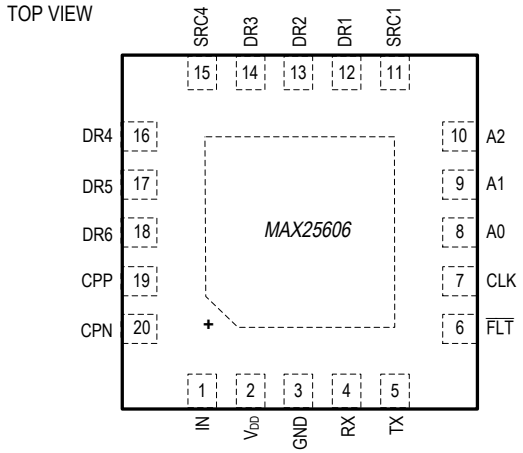
(Input Voltage = IN = 5V, T_A = T_J = -40ºC to +125ºC, unless otherwise noted. Typical values are at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, RX)						
Input High Voltage	V_{IH}		1.4			V
Input Low Voltage	V_{IL}				0.4	V
DIGITAL OUTPUTS (CLK, TX)						
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V
THERMAL SHUTDOWN						
Thermal-Warning Threshold	TH_WARN	Rising Temperature		140		ºC
Thermal-Warning Hysteresis	HYS_WARN			15		°C
Thermal-Shutdown Threshold	TH_SHDN	Rising Temperature		165		ºC
Thermal-Shutdown Hysteresis	HYS_SHDN			15		ºC
CHARGE PUMP						
Charge-Pump Output Voltage	V_o	V_{CPP} - V_{CPN}, I_{CPP} = 190µA	3.8		5.8	V
Charge-Pump Power-Good Threshold	V_{CPP_OK}	Rising Threshold		4.0		V
UART Timing						
UART Bit Rate	F_{UART}		10		500	kbps

Note 2: Limits are 100% production tested at TA = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

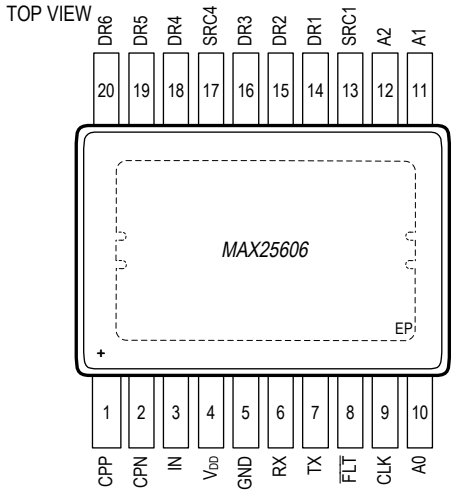
Pin Configurations

TQFN



TQFN
4mm × 4mm

TSSOP



TSSOP

Pin Description

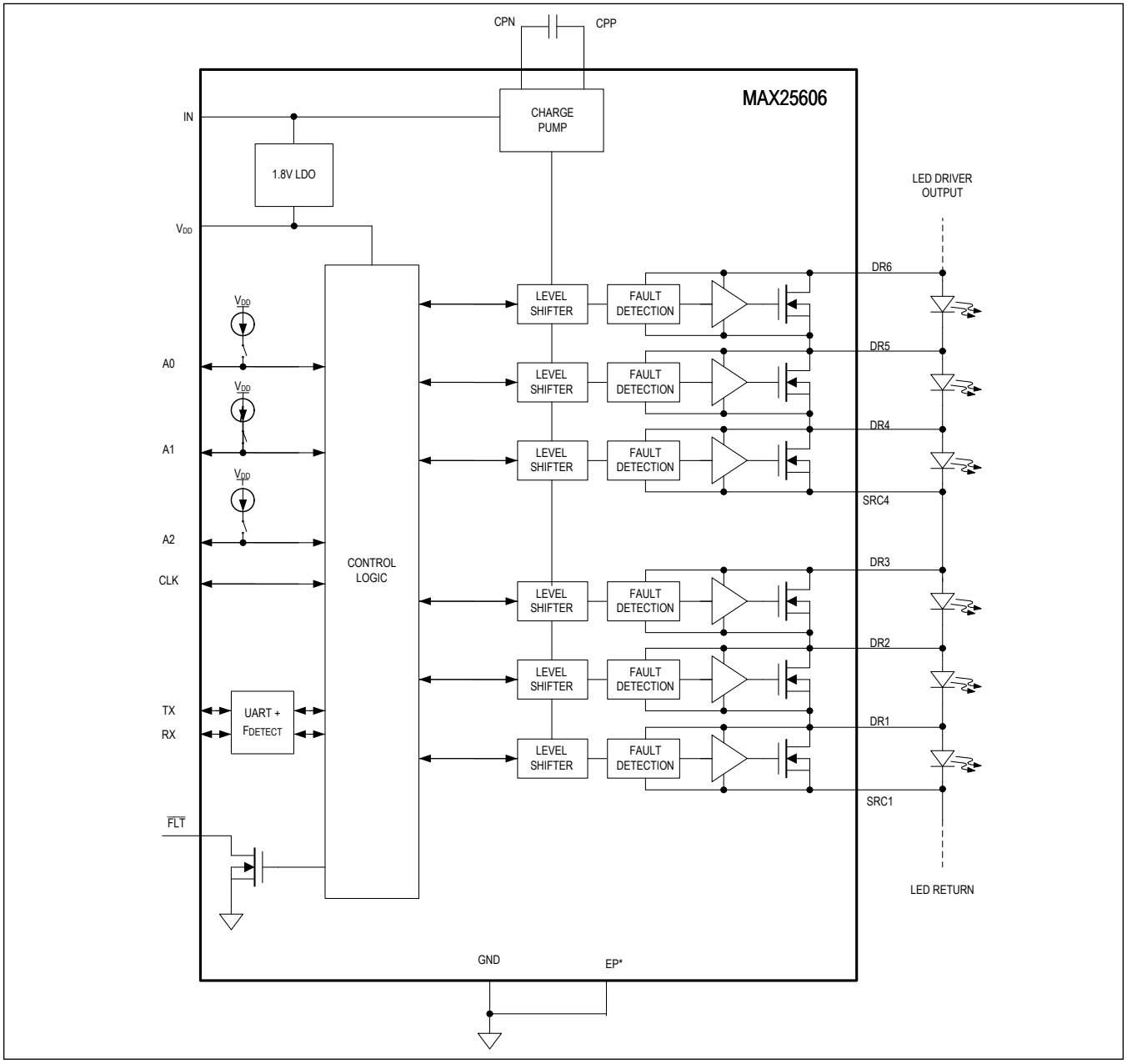
PIN		NAME	FUNCTION
TQFN	TSSOP		
1	3	IN	Input Supply. Connect to external power supply to provide power to the device. Connect a minimum 0.1µF ceramic capacitor between IN and GND.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
2	4	V_{DD}	LDO Output. Nominal voltage is 1.8V. Connect a minimum 2.2µF ceramic capacitor between V_{DD} and GND.
3	5	GND	Ground Connection
4	6	RX	UART Receive Input
5	7	TX	UART Transmit Output
6	8	$\overline{FLT}$	Open-Drain Fault Indicator. Goes low when a fault condition is present.
7	9	CLK	Sequence Period Programming Input. Connect a resistor from CLK to GND to set the sequence period.
8	10	A0	A0 programming input. Connect a resistor from A0 to GND to set the 4 least-significant bytes (LSBs) of the UART device ID.
9	11	A1	A1 programming input. Connect a resistor from A1 to GND to set the 2 most-significant bytes (MSBs) of the UART device ID.
10	12	A2	A2 programming input. Connect a resistor from A2 to GND to use as a general purpose decode, such as for a binning resistor. The corresponding A2 code can be read through the UART interface after powerup.
11	13	SRC1	Source of Internal Switch 1
12	14	DR1	Drain of Internal Switch 1
13	15	DR2	Drain of Internal Switch 2
14	16	DR3	Drain of Internal Switch 3
15	17	SRC4	Source of Internal Switch 4
16	18	DR4	Drain of Internal Switch 4
17	19	DR5	Drain of Internal Switch 5
18	20	DR6	Drain of Internal Switch 6
19	1	CPP	Charge Pump Capacitor Positive Connection. Connect a 0.1µF ceramic capacitor from CPP to CPN.
20	2	CPN	Charge Pump Capacitor Negative Connection. Connect a 0.1µF ceramic capacitor from CPP to CPN.
-	—	EP	Exposed Pad Connection. Connect this pad to a contiguous ground plane.

Functional Diagrams

MAX25606 Block Diagram



Detailed Description

The MAX25606 6-switch matrix manager IC for automotive lighting applications includes a 6-switch array for bypassing individual LEDs in single- or dual-string applications. It features six individually controlled n-channel MOSFET switches, each switch having an RD_{SON} of 0.2Ω and rated to withstand 16V. Each group of three cascoded switches can withstand up to 48V. The low on-resistance of the switches minimizes conduction loss and power dissipation.

For single-string applications a single current source can be used to power all the LEDs connected in series. Dual-string applications use a separate current source for each string, with three switches in series per string. For high-current applications, the two sets of three switches can be connected in parallel with a single current source. Each switch can be connected across one, two, or three LEDs in series.

The IC features a serial peripheral interface (UART) for serial communication. The MAX25606 is a slave device that uses the UART to communicate with an external micro-controller (µC), which acts as the master. Up to 64 separate devices can be connected using a star topology. Each of the six switches can be independently programmed to bypass the LEDs in the string. Each switch can be turned on, turned off, or PWM modulated with 12 bits of PWM duty cycle adjustment. Transitions between two different PWM settings can either happen instantly or a logarithmic fade transition can be applied. The logarithmic fade algorithm is built into the device and only requires a single software command. The µC can assign device Cluster IDs to allow for simultaneous programming of multiple devices. The serial interface allows the user to program the slew rate to minimize EMI. The PWM frequency can be set by an internal oscillator or synchronized to an external clock source. The IC features built-in open circuit protection, as well as detailed open- and short-LED fault reporting and open trace fault reporting through the serial interface. The short LED fault threshold is programmable to accommodate a wide variety of LED diodes. The IC also includes an internal charge pump that provides power for the gate drive of each of the LED bypass switches.

The device is available in a 20-pin 4x4mm side wettable TQFN and a 20-pin TSSOP package with exposed pad. The device is AEC-Q100 Grade 1 qualified and designed to operate over the -40ºC to +125ºC temperature range.

Power-On Reset and VDD UVLO

Once the IC is powered, an internal power-on reset (POR) signal sets all the registers to their default states. All six switches are in the on-state upon a POR (all LEDs are off). The LEDs remain off until a command is received by the UART. To ensure reliable operation, the IN supply voltage (V_{IN}) must be greater than V_{IN-POR}. If V_{IN} falls below V_{IN-POR} and the VDD regulator output falls below VDD_UVLO, the registers reset to their default state. The IN voltage must be greater than V_{IN-POR} and VDD must be above VDD_UVLO for proper operation. The bypass switches remain in their default on-state until the UART is used to enable LED dimming.

Internal Switches

Each switch connected between DRn and DRn-1 has a typical on-resistance of 0.2Ω. This measurement includes the on-resistance of the internal switch and the resistance of the bond wires to the DRn and DRn-1 pads. Each bypass switch, when driven to an off state, allows the string current to flow through the corresponding parallel-connected LED, turning the LEDs on. Driving the bypass switch to an on state shunts the current through the bypass switch and turns the LEDs off. Each bypass switch can have one, two or three LEDs in series across it.

All six switches are connected in a cascode configuration to allow for animation in applications where the LED string cathode does not connect to ground. The switches are divided into two groups of three to give the option of controlling two parallel LED strings with a single MAX25605 device. Alternatively, a single string can be controlled by connecting SRC4 and DR3 externally.

The slew rate of the switches can be programmed to minimize the current undershoot or overshoot during segment transitions.

Charge Pump

The MAX25606 integrates a charge pump that provides the voltage rails for each switch gate driver and level shifter. The charge pump requires a single 0.1µF capacitor connected between CPP and CPN for operation. The charge pump includes spread spectrum, which dithers the switching frequency by ±6% around the fundamental of 16.384MHz. The input power for the charge pump is taken from the higher voltage of IN, DR6, or DR3. Therefore, IN and DR6 should have

an external decoupling capacitor of at least 0.01µF as close as possible to the device, assuming DR6 is always a greater voltage than DR3. If the DR6 and DR3 segments are controlling two different LED strings, then DR3 should also have a close decoupling capacitor.

A status flag CP_NOT_RDY indicates that the charge pump is not yet powered up. When the charge pump is not powered up, the switches inside the IC are off, allowing any current from the LED driver to flow through the LEDs.

Register configurations for LED short detection threshold and switch slew rate in address 0x02 gets level shifted to each switch. Since the level-shift circuit uses the charge pump supply, these registers can only be updated if the charge pump is ready. If the charge pump loses power, these level-shifted registers are reset to 0. The level-shifted registers for each switch only get updated if the charge pump supply is good and a new value is written to the logic level register map. Therefore, if a nonzero value is used for the slew rate or short threshold setting, it is recommended to write 0 and rewrite the correct value to these registers any time the charge pump supply is interrupted. Make sure the SW_GO_EN bit is set to 0 whenever updating the register 0x02 configuration bits.

Programming Options

MAX25606 Pin Resistor Decode Table

Multiple MAX25606 devices can be used in a multidrop UART bus with an external uC acting as the master. The resistors on pins A0 and A1 are used to program the UART Device ID of the MAX25606. The first two LSBs of the A1 code are concatenated with the 4 bits of the A0 code to produce the device ID. For example, a value of 309Ω on A1 (code x2) and a value of 1050Ω on A0 (code x8) result in a Device ID of x28.

Table 1. Device ID and A0/A1 Inputs

{A1[1:0], A0[3:0]}	DEVICE ID
x00	x00
x01	x01
...	...
x3F	x3F

The remaining unused bits {A1[3:2], A2[3:0]} can be used for as general purpose indicators, for example, a binning resistor and/or a hardware revision identifier. The MAX25606 stores the coded value of the resistors on A0, A1, and A2 in the STAT_RES_CODE register, address 0x0C, and thus the information is available to the microcontroller through the UART bus.

Resistor Programming Table

The IC provides 16 levels of detection between 0 and 1.2V on the A0, A1, and A2 pins, which are used to configure the MAX25606 device ID. The pins source 400 µA, allowing the use of an external resistor between A0/A1/A2 and GND to set the voltage level. See Table 2 for recommended resistor values.

Table 2. A0/A1/A2 Recommended Values

A0/A1/A2[3:0] DECODE VALUE	A0/A1 RESISTOR VALUE (Ω, 1%)
0000	95.3
0001	200
0010	309
0011	422
0100	536
0101	649
0110	768
0111	909
1000	1050
1001	1210

1010	1400
1011	1620
1100	1870
1101	2150
1110	2490
1111	2870

A0 sets the four LSBs of the 6-bit device ID. A1 sets the two MSBs of the 6-bit device ID.

PWM Clock and Synchronous Operation with Multiple Devices

The PWM clock for the IC can be selected from the internal oscillator or from an external clock source driving the CLK pin. The CLK pin is bidirectional, allowing a single device to be the master clock, providing a common clock source to multiple devices. The PWM clock source and CLK pin direction are configured through PWM_CLK[1:0] in the CNFG_GEN (0x03) register. The default value is internal oscillator with the CLK pin disabled. For synchronous operation with multiple devices, use the PWM_CLK_SEL bits in the CNFG_GEN (0x03) register to set the master with internal oscillator and CLK pin output, and the slave devices with external oscillator and CLK pin input.
The PWM dimming frequency is programmable by setting the value of the DIV[1:0] bits in the CNFG_GEN (0x03) register, which sets the divide ratio for both the internal (16.384 MHz) and external clock sources.

The CLK output mode requires a pullup resistor from CLK to VDD because the CLK output is an open-drain output. The pullup strength depends on the desired UART frequency. A 10kΩ resistor pullup works for most frequencies. If 500k baud rate is needed, then a stronger pullup resistor, on the order of 1kΩ, is most likely required.

Parallel Operation for Higher Current Applications

The switches in the IC can handle current up to 0.75A (max); however, for applications that require higher currents, the switches can be configured in parallel. For example, if the current capability needs to be doubled with three LEDs, connect switch SW0 in parallel to SW3, SW1 in parallel to SW4, and SW2 in parallel to SW5. Make sure the switches connected in parallel have the same phase shift and PWM dimming duty cycles.

PWM Dimming

The IC provides 12-bit programmable dimming on each individual switch. An internal 12-bit counter (COUNT) is generated according to the clock settings. The switch turns off when COUNT is equal to the delay set by the corresponding PSFT register and stays off until the COUNT exceeds the sum of PSFT and PWM duty-control registers. In this way, the duty cycle and relative phase shift of the individual switches can be set independently.

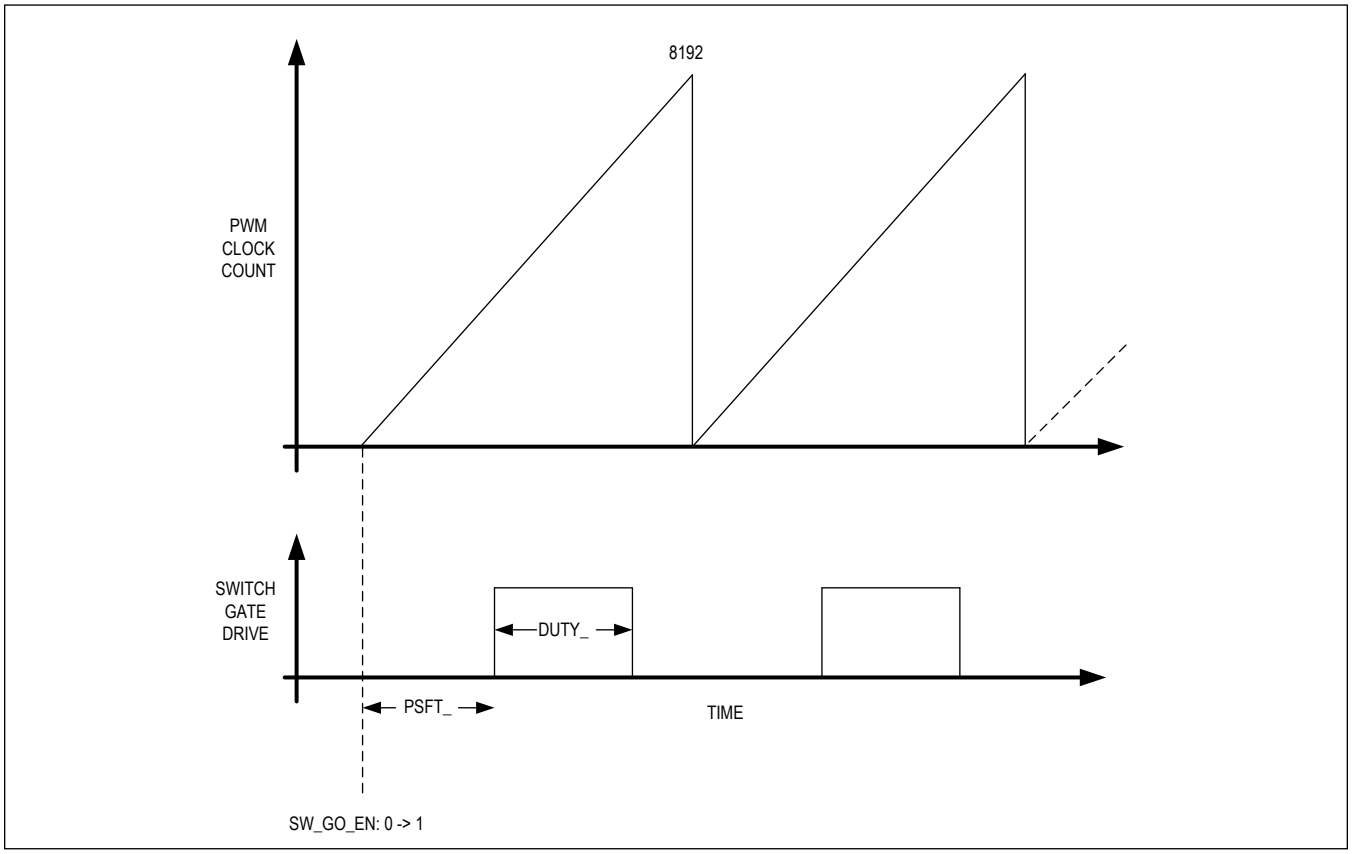


Figure 1. PWM Phase and Duty Cycle Definitions

Dimming With and Without Fade

Each switch of the IC can be independently programmed to perform dimming without fade transition, or dimming with fade transition. For dimming without fade transition, the dimming changes from the initial value to the target value in one dimming cycle. For dimming with fade transition, the dimming changes transitionally step by step, starting from the initial value to the target value in multiple dimming cycles, following a predetermined exponential curve.

To enable dimming with fade transition, set the FADE bit to 1 and the DUTY bits to the target value for the specific switches. Each transitional step value is calculated using 12 bits according to the following formula:

$$DUTYnext = DUTYnow \times CF$$

where DUTY is the duty cycle and CF is the constant factor

CF = 1.0625 and CF = 0.9375 for an up transition and down transition, respectively.

DUTYnext continues to be updated according to the formula until DUTYnext reaches the target value.

The transition period is defined by the TDIM_ register for the switch. The number of transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 1(/8191) to 8191(/8191) is 115 steps.
The number of transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from 8191(/8191) to 1(/8191) is 111 steps.

Duty-cycle steps smaller than CF update in one step.

Each step runs TDIM_ PWM dimming cycles, and each dimming cycle consists of 8192 clock cycles by default; therefore Tstep = TDIM_ x 8192. The 8192 clock cycles timer can also be changed to 16384, 32768, or 65536 clock cycles by

programming bits [3:2] in register address 0x02.

LED Fault Detection and Protection

The IC is able to detect a shorted LED, open LED, and open trace between the device and the LED. To detect and report a LED fault, several conditions must be met. First, the LED switch must be operating and LED-open and LED-short detection requires the switch to be open so the duty cycle must be greater than zero. Conversely, open-fault detection requires the switch to be closed so the PWM duty cycle must be less than 100%. In general, it takes up to one dimming cycle to make sure these conditions have been met after a fault condition is applied. This period depends on the PWM dimming frequency.

To ensure proper operation of the fault detection circuits, it is recommended to use a minimum PWM pulse width which is at least twice as long as the programmed slew rate.

LED Short Threshold

The LED short threshold is programmable to support single LED short detection for applications with 1, 2, or 3 LEDs per switch. The short threshold can be independently programmed for each group of three cascoded switches. The VSTH_123 programs the short threshold for the three switches between DR3 and SRC1. The VSTH_456 programs the short threshold for the three switches between DR6 and SRC4.

UART Serial Interface

Overview

The MAX25606 includes a full-duplex UART serial interface to enable fully programmable matrix manager functionality. The system ECU/MCU acts as the UART master, driving read/write packets on the RX line and receiving packets on the TX line. The RX and TX lines can connect up to 64 MAX25606 devices on a common bus using a star topology. The device address of each MAX25606 is pin-programmable using external resistors to ground on the A0 and A1 pins. Devices may be addressed individually using their Device ID[5:0]. They may also be simultaneously addressed using the General Call ID or by using the programmable Cluster Call ID value.

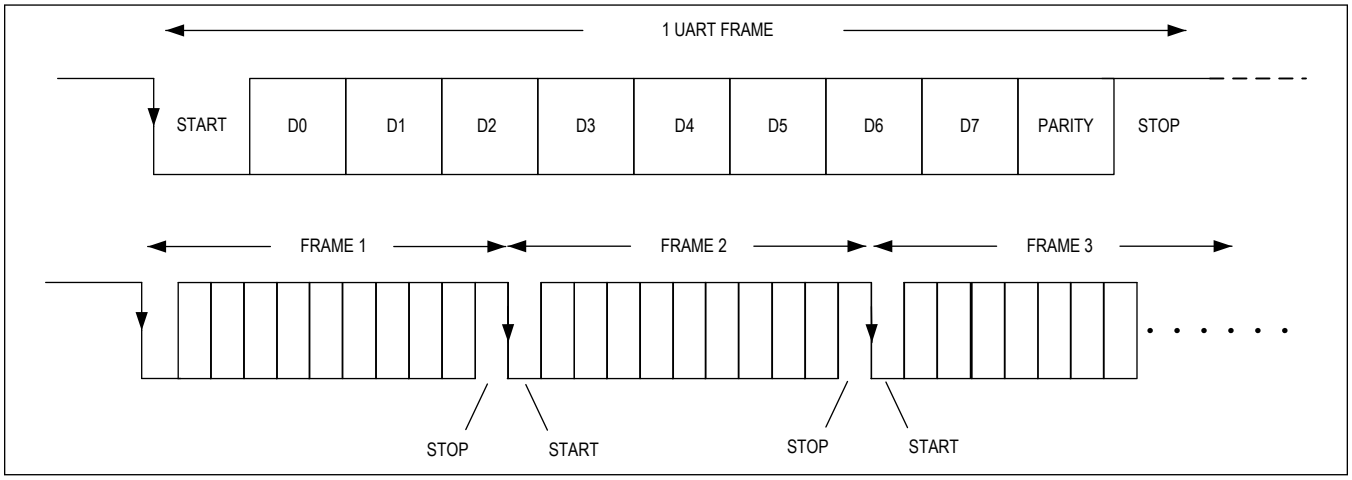
The baud rate of incoming UART packets on RX is automatically detected by the MAX25606, from a minimum of 10kbps up to a maximum of 500kbps. The MAX25606 then returns frames on the TX line at the same baud rate according to the packet format described below.

Device Connections

The UART interface ensures compatibility with standard microcontrollers from a variety of manufacturers. The RX line should be driven by the microcontroller master. It can be connected to an individual MAX25606 or to multiple devices in a star topology. The TX line is an open-drain output. Multiple devices can share the same TX connection as well. No external timing reference is required, the MAX25606 automatically detects the bit rate on each RX packet and adjusts the bit rate of the TX response accordingly.

UART Frame Format

Read/write packets are composed from multiple UART frames. Each frame consists of 1 start bit, 8 data bits, 1 parity bit (even), and 1 stop bit. The parity bit should be high if the number of ones in the data bits is odd, otherwise it should be low. If the next frame is in the same packet, there can be no more than 12-bit periods of idle (high) state between frames.



Synchronization and Acknowledge Frames

Each read/write packet must begin with a special Synchronization (SYNC) frame. This is a UART frame containing the data x79.

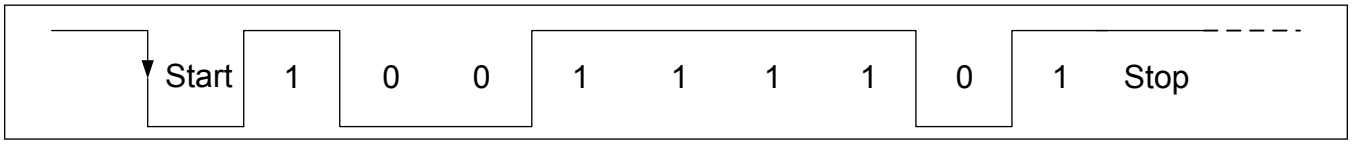


Figure 2. SYNC Frame

Each response packet always begins with a special Acknowledge (ACK) frame. This is a UART frame containing the data xC3.

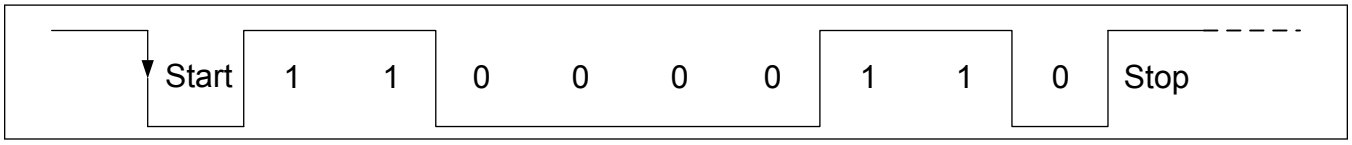


Figure 3. ACK Frame

Device ID and Address Frame Format

Each MAX25606 device in the star configuration should be assigned a unique device ID number using resistors connected to the ADDR0 and ADDR1 pins. There are 64 possible device IDs that can be assigned in this way, from x00 to x3F. See *MAX25606 Pin Resistor Decode Table*.

In addition to addressing devices individually, the MAX25606 also supports Global Call and Cluster Call write commands. A Global write command addresses all devices on the bus. A Cluster call addresses all devices with a matching cluster call ID in the CNFG_UART register. Read commands cannot use the Global/Cluster Call option and must be addressed to a specific device ID.

The address frame data bits are assigned as follows: the MSB is the Global/Cluster call bit. The next 6 bits are the device ID. The LSB is the Read/Write bit.

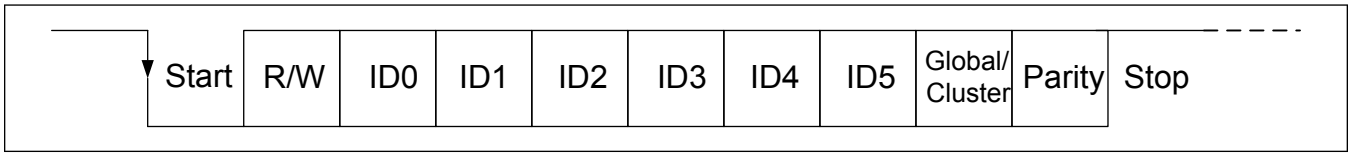


Figure 4. SYNC Frame

Write Transactions

Each write packet consists of five UART frames on the RX pin. The first frame shall be the SYNC packet. The second frame consists of the Global/Cluster call flag, then the 6-bit device ID, and then the R/W bit. The R/W bit shall be low for a write command. The third frame shall be the register address being written to. The fourth frame shall be the lower byte of the data being written. The fifth and final frame shall include the 3-bit cyclic redundancy check (CRC) code followed by the upper 5 bits of the data being written. Upon receiving a valid write packet, the device responds with an ACK frame on the TX pin.

Fourth UART frame, lower 8 bits of data packet

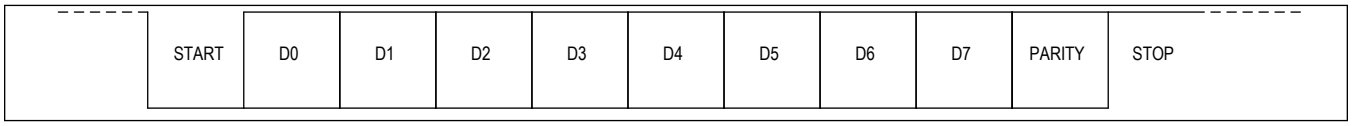


Figure 5. SYNC Frame

Fifth UART frame, upper 5 bits of data packet + 3 bits of CRC

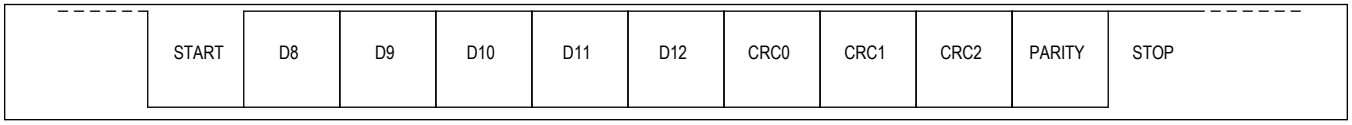


Figure 6. SYNC Frame

Read Transactions

Each read command consists of four UART frames on the RX pin. The first frame shall be the SYNC packet. The second frame consists of the Global/Cluster call flag, then the 6-bit device ID, and then the R/W bit. The R/W bit shall be high for a read command. The third frame shall be the register address being written to. The fourth and final frame shall include the 3-bit CRC code followed by 5 zeroes. Upon receiving a valid read command the device responds with three frames on the TX pin. The first frame shall be the ACK packet. The second frame shall be the lower 8 bits of the register being read. The third frame shall be the 3-bit CRC code followed by the 5 MSBs of the register being read.

CRC Error Checking

Read/Write transactions are protected using a 3-bit CRC on the frame. The CRC is provided by the master on last three data bits of each UART_RX packet. The MAX25606 calculates its own CRC using the same polynomial, and the transaction is only accepted if the CRC bits match. For response frames on read packets, the MAX25606 appends its own 3-bit CRC code to the 13-bit read data.

The input to the CRC calculation consists of the data bits from the device ID, address, and data frames.

The CRC calculation uses the polynomial $x^3 + x^1 + 1$ with a starting value of 000.

UART Watchdog Function

The MAX25606 UART Watchdog feature sets the switches into a preconfigured state in the event of UART

communication bus failures. If the EN_WATCHDOG bit is set in the CNFG_WATCHDOG register, the device asserts a UART_WATCHDOG fault when the UART_RX pin has been inactive for more than 4 seconds. When the UART_WATCHDOG fault is set, the $\overline{FLT}$ output is asserted low and the state of the channel switches is set to the value of the WD_LED_STATE register. The default value of WD_LED_STATE is x00, which opens all six switches in the event of a watchdog fault. The fault can be masked by setting the MSK_UART_ERR bit in the CNFG_MASK_GEN register. The fault status is cleared by writing a 1 to the UART_WATCHDOG bit. When the fault status is cleared, the switches resume operation according to the values of the PWM registers.

UART Communication Error Handling

In the event that the device receives a bad packet on UART_RX, it asserts the relevant fault status bit in STAT_UART and asserts the $\overline{FLT}$ output. The UART communications faults can be masked by setting the MSK_UART_ERR bit. Faults are cleared by writing 1 to the STAT_UART bits. The following communications errors result in fault assertion:

- UART Watchdog timeout: UART_RX stops transitioning for more than 4 seconds and EN_WATCHDOG bit is set.
- UART_RX timeout: UART_RX stops transitioning for more than 16 bit lengths after a UART start bit has been received but before the end of a valid command sequence.
- RX_CRC_ERR: An invalid CRC code is detected on a UART transaction.
- RX_SYNC_PERR: parity error in the SYNC frame
- RX_PL_ERR: parity error in the payload frame
- RX_STOP_ERR: frame is missing the stop bit

Thermal Protection

The IC features an on-chip temperature-protection circuit to prevent the device from overheating.

When the die temperature rises above the thermal-warning threshold (+140ºC), the TH_WARN bit is set, causing the $\overline{FLT}$ pin to be asserted but no action is taken with the switches. To clear the TH_WARN bit, a 1 must be written to the bit. If the die temperature is still above the threshold, the status bit is immediately set again.

When the die temperature rises above the thermal-shutdown threshold (+165ºC), the TH_SHDN bit is set, causing the $\overline{FLT}$ pin to be asserted and all switches to either be closed (LEDs turned off) or opened (LEDs turned on), depending on the value of the TH_SHDN_ACT register bit. Switches remain static and the $\overline{FLT}$ pin remains asserted until the fault status is cleared by writing 1 to the TH_SHDN bit. If the die temperature is still above the threshold, the fault status is immediately set again.

When the device recovers from thermal shutdown, it resumes operation from where it was before the thermal shutdown. The TH_WARN and TH_SHDN bits are cleared by writing a 1.

PWM Clock and Synchronous Operation with Multiple Devices

The PWM clock for the IC can be selected from the internal oscillator or from an external clock source driving the CLK pin. The CLK pin is bidirectional, allowing a single device to be the master clock, providing a common clock source to multiple devices. The PWM clock source and CLK pin direction are configured through PWM_CLK[1:0] in the CNFG_GEN (0x03) register. The default value is internal oscillator with the CLK pin disabled. For synchronous operation with multiple devices, use the PWM_CLK_SEL bits in the CNFG_GEN (0x03) register to set the master with internal oscillator and CLK pin output, and the slave devices with external oscillator and CLK pin input.
The PWM dimming frequency is programmable by setting the value of the DIV[1:0] bits in the CNFG_GEN (0x03) register, which sets the divide ratio for both the internal (16.384MHz) and external clock sources.

The CLK output mode requires a pullup resistor from CLK to VDD because the CLK output is an open-drain output. The pullup strength depends on the desired UART frequency, a 10kΩ resistor pullup works for most frequencies. If 500k baud rate is needed, then 1kΩ or 2kΩ pullup may be better.

Register Map

MAX25606

ADDRESS	NAME	MSB							LSB
USER COMMANDS									
0x00	NO_OP[15:8]	REV_ID[4:0]							
	NO_OP[7:0]	–	–	–	CONSTANT_TEST[4:0]				
0x01	SW_GO[15:8]				–	–	–	–	–
	SW_GO[7:0]	–	–	–	–	–	–	–	SW_GO_EN
0x02	CNFG_GEN[15:8]				VSTH_456[2:0]			VSTH_123[2:1]	
	CNFG_GEN[7:0]	VSTH_123[0]	LED_SLEW[2:0]		DIV[1:0]			PWM_CLK_SEL[1:0]	
0x03	CNFG_UART[15:8]				–	–	–	–	–
	CNFG_UART[7:0]	–	–	CID[5:0]					
0x04	CNFG_WATCHDOG[15:8]				EN_WATCHDOG	–	–	–	–
	CNFG_WATCHDOG[7:0]	–	–	WD_LED_STATE[5:0]					
0x05	CNFG_OPEN_OVRD[15:8]				–	–	–	–	–
	CNFG_OPEN_OVRD[7:0]	–	–	OPEN_LED_OVR[5:0]					
0x06	CNFG_GROUPA[15:8]				–	–	–	–	–
	CNFG_GROUPA[7:0]	–	–	GROUPA_SEL[5:0]					
0x07	CNFG_GROUPB[15:8]				–	–	–	–	–
	CNFG_GROUPB[7:0]	–	–	GROUPB_SEL[5:0]					
0x08	CNFG_MSK_GEN[15:8]				TH_SHDN_ACT	–	–	–	–
	CNFG_MSK_GEN[7:0]	–	MSK_UART_ERR	MSK_OPEN_TRACE	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CP_RDY_N	MSK_RADC_ERR	MSK_TH_WARN
0x09	CNFG_MSK_LED[15:8]				–	–	–	–	–
	CNFG_MSK_LED[7:0]	–	–	CNFG_MSK_LED[5:0]					
0x0A	STAT_GEN[15:8]				–	–	–	CONFIG_NOT_DONE	RADC_ERR
	STAT_GEN[7:0]	EXT_CLK_ERR	UART_ERR	OPEN_TRACE	OPEN_LED	SHORT_LED	CP_RDY_N	TH_SHDN	TH_WARN
0x0B	STAT_RADC[15:8]				–	–	–	–	–
	STAT_RADC[7:0]	–	RADC_DONE	R2_OVER_RANGE	R1_OVER_RANGE	R0_OVER_RANGE	R2_UNDER_RANGE	RES1_UNDR1_UNDER_RANGE	R0_UNDER_RANGE
0x0C	STAT_RES_CODE[15:8]				–	R2_CODE[3:0]			
	STAT_RES_CODE[7:0]	R1_CODE[3:0]				R0_CODE[3:0]			

ADDRESS	NAME	MSB							LSB
0x0D	STAT_UART[15:8]				–	–	–	–	UART_WATCHDOG
	STAT_UART[7:0]	RX_TIMEOUT_ERR	RX_CRC_ERR	RX_SYNC_PERR	RX_PL_PERR	RX_SYNC_STOP_ERR	RX_PL_STOP_ERR	RX_PL_START_ERR	–
0x0E	STAT_SHORT_LED[15:8]				–	–	–	–	–
	STAT_SHORT_LED[7:0]	–	–	SHORT_LED_STAT[5:0]					
0x0F	STAT_OPEN_LED[15:8]				–	–	–	–	–
	STAT_OPEN_LED[7:0]	–	–	OPEN_LED_STAT[5:0]					
0x10	STAT_OPEN_TRACE[15:8]				–	–	–	–	–
	STAT_OPEN_TRACE[7:0]	–	–	OPEN_TRACE_STAT[5:0]					
0x11	PSFT_GRP[15:8]				–	–	–	PSFT_GROUP[1:0]	
	PSFT_GRP[7:0]	PSFT[7:0]							
0x12	PSFT_0[15:8]				–	–	–	–	–
	PSFT_0[7:0]	PSFT_0[7:0]							
0x13	PSFT_1[15:8]				–	–	–	–	–
	PSFT_1[7:0]	PSFT_1[7:0]							
0x14	PSFT_2[15:8]				–	–	–	–	–
	PSFT_2[7:0]	PSFT_2[7:0]							
0x15	PSFT_3[15:8]				–	–	–	–	–
	PSFT_3[7:0]	PSFT_3[7:0]							
0x16	PSFT_4[15:8]				–	–	–	–	–
	PSFT_4[7:0]	PSFT_4[7:0]							
0x17	PSFT_5[15:8]				–	–	–	–	–
	PSFT_5[7:0]	PSFT_5[7:0]							
0x18	TDIM_GRP[15:8]				–	–	–	–	–
	TDIM_GRP[7:0]	–	–	TDIM_GROUP[1:0]		–	TDIM[2:0]		
0x19	TDIM_2_1_0[15:8]				–	–	TDIM_2[2:0]		
	TDIM_2_1_0[7:0]	–	TDIM_1[2:0]			–	TDIM_0[2:0]		
0x1A	TDIM_5_4_3[15:8]				–	–	TDIM_5[2:0]		
	TDIM_5_4_3[7:0]	–	TDIM_4[2:0]			–	TDIM_3[2:0]		
0x1B	PWM_GRPA_DUTY[15:8]				FADE_A	DUTY_A[11:8]			
	PWM_GRPA_DUTY[7:0]	DUTY_A[7:0]							
0x1C	PWM_GRPB_DUTY[15:8]				FADE_B	DUTY_B[11:8]			
	PWM_GRPB_DUTY[7:0]	DUTY_B[7:0]							
0x1D	PWM0[15:8]				FADE_0	DUTY_0[11:8]			

ADDRESS	NAME	MSB							LSB
	PWM0[7:0]	DUTY_0[7:0]							
0x1E	PWM1[15:8]				FADE_1	DUTY_1[11:8]			
	PWM1[7:0]	DUTY_1[7:0]							
0x1F	PWM2[15:8]				FADE_2	DUTY_2[11:8]			
	PWM2[7:0]	DUTY_2[7:0]							
0x20	PWM3[15:8]				FADE_3	DUTY_3[11:8]			
	PWM3[7:0]	DUTY_3[7:0]							
0x21	PWM4[15:8]				FADE_4	DUTY_4[11:8]			
	PWM4[7:0]	DUTY_4[7:0]							
0x22	PWM5[15:8]				FADE_5	DUTY_5[11:8]			
	PWM5[7:0]	DUTY_5[7:0]							

Register Details

NO_OP (0x00)

NO_OP is a read-only register that reads the content of RGRADE, revision ID, and test pattern.

BIT				12	11	10	9	8
Field				REV_ID[4:0]				
Reset				0b00000				
Access Type				Read Only				

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CONSTANT_TEST[4:0]				
Reset	–	–	–	0b10001				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
REV_ID	12:8	Revision Information: Reads back 5-bit hardware revision ID.
CONSTANT_TEST	4:0	Test Pattern: 0x11 is always returned in this location for interface checking.

SW_GO (0x01)

SW_GO us a read/write register that enables the PWN signals.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SW_GO_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SW_GO_EN	0	Switching Enable signal. Enables LED dimming operation and starts dimming counters. If SW_GO_EN = 0, all LED switches are closed and all PWM counters in the LED Controller are reset to 0. If SW_GO_EN = 1, all LED switches operate according to their programmed values and all PWM counters start counting from 0. The SW_GO_EN command should be issued after CP_RDY_N transitions low on STAT_GEN, ensuring CLK is present and CPP voltage is valid.	0x0: All LED switches are closed, and all PWM counters are reset to 0. 0x1: All LED switches operate according to their programmed values, and all PWM counters start counting from 0.

CNFG_GEN (0x02)

CNFG_GEN is a read/write access register that controls the dimming clock divider ratio, the slew rate of the LED switches, the threshold used for the short-LED fault-detection function, and the functionality of the CLK pin.

BIT				12	11	10	9	8
Field				VSTH_456[2:0]			VSTH_123[2:1]	
Reset								
Access Type				Write, Read			Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	VSTH_123[0]	LED_SLEW[2:0]			DIV[1:0]		PWM_CLK_SEL[1:0]	
Reset		0b000			0b00		0b00	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
VSTH_456	12:10	Sets the Short LED Threshold value for Switches 4,5 and 6.	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V
VSTH_123	9:7	Sets the Short LED Threshold value for Switches 1,2 and 3.	0x0: 1.4V 0x1: 3.6V 0x2: 4V 0x3: 5.5V 0x4: 6V 0x5: 6.6V 0x6: 7.2V 0x7: 7.7V

BITFIELD	BITS	DESCRIPTION	DECODE
LED_SLEW	6:4	Slew Control for the Internal LED Gate Driver: Updating the LED gate-driver slews can take time, up to a full PWM dimming cycle; therefore, consecutive writes to LED_SLEW should be at least 1 dimming cycle apart in time. In most cases, this register is set only once, prior to setting SW_GO_EN.	0x0: 10µs 0x1: 6.67µs 0x2: 5.0µs 0x3: 3.3µs 0x4: 2.5µs 0x5: 1.5µs 0x6: 1.0µs 0x7: 0.5µs
DIV	3:2	PWM Dimming-Frequency Select. The PWM dimming clock frequency, fpwm, is divided down from fosc by the chosen divider value. fosc can either be the internal oscillator clock or the external oscillator clock, depending on the PWM_CLK_SEL bit setting.	0x0: fpwm = fosc / 8192 0x1: fpwm = fosc / 16384 0x2: fpwm = fosc / 32768 0x3: fpwm = fosc / 65536
PWM_CLK_SEL	1:0	Determines internal/external PWM clock and direction of CLK pin.	0x0: Internal OSC, CLK pin disabled (default). 0x1: Internal OSC, CLK pin output. 0x2: External OSC, CLK pin input.[1 - 20Mhz clk] 0x3: External OSC, CLK pin input.[1..20Mhz clk]

CNFG_UART (0x03)

CNFG_UART is a read/write access register that controls the cluster ID assignment.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	CID[5:0]					
Reset	–	–	0b000001					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
CID	5:0	Cluster Identification: During a cluster call write transaction, the UART accepts the transaction if the received CID[5:0] matches the contents of this register.

CNFG_WATCHDOG (0x04)

BIT		12	11	10	9	8
Field		EN_WATCHDOG	–	–	–	–
Reset			–	–	–	–
Access Type		Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	WD_LED_STATE[5:0]					
Reset	–	–						
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
EN_WATCHDOG	12	When this bit is set and the UART_WATCHDOG bit is set: The active-low fault flag will be asserted. The state of the switches will be set according to the WD_LED_STATE register.	0x0: UART Watchdog timer is disabled 0x1: enable UART Watchdog
WD_LED_STATE	5:0	Sets the state of LEDs when UART timeout condition is detected.	0x0: Switch Open 0x1: Switch Closed

CNFG_OPEN_OVRD (0x05)

OPEN_OVRD is a read/write register that overrides the LED switching control signals. When this feature is disabled, the LED switch operates normally. When this feature is enabled, the LED switch is always forced to a closed position (i.e., the LED duty cycle is zero, regardless of the DUTY or TDIM settings).
The intent is to allow the µP to manually force the switch to stay closed after it has determined the particular LED is permanently opened. This further suppresses fault signals from the switch(es) since LED faults are only detected when the switch opens.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	OPEN_LED_OVR[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_LED_OVR	5:0	Open-LED Override: Program these bits to force the corresponding switch(es) to always be closed. This will override the state of the corresponding DUTY registers.	0x0: Normal 0x1: LED switch is always closed.

CNFG_GROUPA (0x06)

CNFG_GRPA is a read/write register that allows the user to assign particular LED drivers to a this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT_GRP (if PSFT_GROUP==0001)
- TDIM_GROUP (if TDIM_GROUP==0001)
- PWM_GRPA_DUTY

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	GROUPA_SEL[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GROUPA_SEL	5:0	Set high if assigning a register to GroupA. Example: writing a value of x07 will assign the first 3 switches to Group A.	0x0: Not assigned 0x1: Assigned

CNFG_GROUPB (0x07)

CNFG_GRPB is a read/write register that allows the user to assign particular LED drivers to a this group. LED drivers assigned to this group respond to qualified transactions on the following registers:

- PSFT_GRP (if PSFT_GROUP==00010)
- TDIM_GROUP (if TDIM_GROUP==0010)
- PWM_GRPB_DUTY

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	GROUPB_SEL[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GROUPB_SEL	5:0	Set high if assigning a register to GroupB.	0x0: Not assigned 0x1: Assigned

CNFG_MSK_GEN (0x08)

CNFG_MSK is a read/write access register that controls the masking of fault conditions from the acitve-low fault flag output.

BIT		12	11	10	9	8
Field		TH_SHDN_ACT	–	–	–	–
Reset		0b0	–	–	–	–
Access Type		Write, Read	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	MSK_UART_ERR	MSK_OPEN_TRACE	MSK_OPEN_LED	MSK_SHORT_LED	MSK_CP_RDY_N	MSK_RADC_ERR	MSK_TH_WARN
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TH_SHDN_ACT	12	Thermal-Shutdown Action: This bit selects whether to open or close the LED switches when a TH_SHDN is high.	0x0: Closes all LED switches. 0x1: Opens all LED switches.
MSK_UART_ERR	6	Masks SPI_ERR to FAULTB.	0x0: UART_ERR being set high asserts the active-low fault flag output. 0x1: UART_ERR bit does not assert the active-low fault flag output.
MSK_OPEN_TRACE	5	Masks all open-trace detections to FAULTB.	0x0: Any OPEN_TRACE__ detects assert the active-low fault flag output. 0x1: Any OPEN_TRACE__ detects do not assert the active-low fault flag output.
MSK_OPEN_LED	4	Masks all open-LED detections to FAULTB.	0x0: Any OPEN_LED__ detects assert the active-low fault flag output. 0x1: Any OPEN_LED__ detects do not assert the active-low fault flag output.
MSK_SHORT_LED	3	Masks all STAT_SHORT_LED detections to FAULTB.	0x0: Any STAT_SHORT_LED bits set high assert the active-low fault flag output. 0x1: Any STAT_SHORT_LED bits set high do not assert the active-low fault flag output.
MSK_CP_RDY_N	2	Mask CP_RDY_N to FAULTB.	0x0: CP_RDY_N asserts the active-low fault flag output. 0x1: CP_RDY_N does not assert the active-low fault flag output.
MSK_RADC_ERR	1	Masks SPI_ERR to FAULTB.	0x0: No masking of RADC_ERR. 0x1: Mask RADC_ERR from generating fault.
MSK_TH_WARN	0	Mask-Thermal Warning to FAULTB.	0x0: TH_WARN asserts the active-low fault flag output. 0x1: TH_WARN does not assert the active-low fault flag output.

CNFG_MSK_LED (0x09)

CNFG_MSK_LED prevents LED faults from asserting the active-low fault flag output. This allows the µP to instruct the part to ignore faults from a particular LED when that LED is deliberately not populated in the application.

BIT		12	11	10	9	8
Field		–	–	–	–	–
Reset		–	–	–	–	–
Access Type		–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	CNFG_MSK_LED[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
CNFG_MSK_LED	5:0	Set bit(s) high to mask OPEN_LED, SHORT_LED, and OPEN_TRACE faults from those LEDs asserting the active-low fault flag output.

STAT_GEN (0x0A)

STAT_GEN is a read-only access register that provides general operations and warnings. The active-low fault flag output is asserted whenever any of these bits is high, unless the corresponding MASK bit is set.

BIT				12	11	10	9	8
Field				–	–	–	CONFIG_NOT_DONE	RADC_ERR
Reset				–	–	–	0b0	0b0
Access Type				–	–	–	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	EXT_CLK_ERR	UART_ERR	OPEN_TRACE	OPEN_LED	SHORT_LED	CP_RDY_N	TH_SHDN	TH_WARN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONFIG_NOT_DONE	9	This bit indicates that the UART interface has not completed programming the LED switch configuration, triggered by writing CNFG_GEN. The master should ensure this bit is low before attempting to program CNFG_GEN. This bit does not assert the active-low fault flag output.	0x0: Configuration complete; ready for new CNFG_GEN command. 0x1: Configuration not complete.
RADC_ERR	8	This signal indicates that the RGRADE read operation is not complete. When the signal goes low, the read is complete and RGRADE[2:0] in register 0x0 is valid. This signal does not assert the active-low fault flag output.	0x0: RADC completes. 0x1: RADC error.
EXT_CLK_ERR	7	EXT_CLK_ERR is asserted when the part is configured to use an external clock (PWM_CLK_SEL = x2 or x3) and the external clock is slower than the minimum operating frequency. Using write 1 to clear will not clear this fault unless the clock source is changed back to the internal osc_clk before attempting to clear this fault.	0x0 0x1: External Clock Error
UART_ERR	6	SPI_ERR is asserted if any of the error bits in SNFG_SPI are set.	0x0: UART is operating normally. 0x1: At least 1 of UART errors has been asserted.

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_TRACE	5	OPEN_TRACE is asserted if any OPEN_TRACE_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has open-trace detected.
OPEN_LED	4	OPEN_LED is asserted if any OPEN_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has open detected.
SHORT_LED	3	SHORT_LED is asserted if any SHORT_LED_STAT bit is high.	0x0: All LED drivers operating normally. 0x1: At least one LED driver has short detected.
CP_RDY_N	2	CP_RDY_N is a read-only bit that indicates the charge-pump voltage is below the operating threshold.	0x0: CP operating normally. 0x1: CP is below V_{CPP_OK} threshold
TH_SHDN	1	Thermal Shutdown. Latched, write 1 clears. When set, the behavior of the switches will be controlled by TH_SHDN_ACT UART bit.	0x0: Normal Operation 0x1: Device has exceeded the Thermal Shutdown temperature threshold.
TH_WARN	0	Thermal Warning. Latched, write 1 to clear.	0x0: Normal operation 0x1: Device has exceeded the thermal-warning temperature threshold.

STAT_RADC (0x0B)

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	RADC_DONE	R2_OVER_RANGE	R1_OVER_RANGE	R0_OVER_RANGE	R2_UNDER_RANGE	RES1_UNDR1_UNDER_RANGE	R0_UNDER_RANGE
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RADC_DONE	6	radc measurement status.	0x0: RADC measurement incomplete 0x1: RADC measurement is complete
R2_OVER_RANGE	5	Status bit which indicates the A2 programming resistor is above the maximum code value.	0x0: Normal operation 0x1: Resistor2 Over Range, or an open is detected.
R1_OVER_RANGE	4	Status bit which indicates the A1 programming resistor is above the maximum code value.	0x0: Normal operation 0x1: Resistor1 Over Range, or an open is detected.
R0_OVER_RANGE	3	Status bit which indicates the A0 programming resistor is above the maximum code value.	0x0: Normal operation 0x1: Resistor0 Over Range, or an open is detected.
R2_UNDER_RANGE	2	Status bit which indicates the A2 programming resistor is below the minimum code value.	0x0: Normal operation 0x1: Resistor2 Under Range, or a short is detected.
RES1_UNDR1_UNDER_RANGE	1	Status bit which indicates the A1 programming resistor is below the minimum code value.	0x0: Normal operation 0x1: Resistor1 Under Range, or a short detected.

BITFIELD	BITS	DESCRIPTION	DECODE
R0_UNDER_RANGE	0	Status bit which indicates the A0 programming resistor is below the minimum code value.	0x0: Normal operation 0x1: Resistor0 under range, or a short detetcted.

STAT_RES_CODE (0x0C)

A2, A1, and A0 resistor code values. these resistor values are measured during power up and the corresponding 4 bit code is stored in this register.

BIT				12	11	10	9	8
Field				–	R2_CODE[3:0]			
Reset				–				
Access Type				–	Read Only			

BIT	7	6	5	4	3	2	1	0
Field	R1_CODE[3:0]				R0_CODE[3:0]			
Reset								
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
R2_CODE	11:8	4 bit code for the A2 resistor
R1_CODE	7:4	4 bit code for the A1 resistor. bits 4 and 5 are the MSBs of the UART device ID
R0_CODE	3:0	4 bit code for the A0 resistor. this code represents the 4 least significant bits of the UART device ID.

STAT_UART (0x0D)

BIT				12	11	10	9	8
Field				–	–	–	–	UART_WATCHDOG
Reset				–	–	–	–	
Access Type				–	–	–	–	Write 1 to Clear, Read

BIT	7	6	5	4	3	2	1	0
Field	RX_TIMEOUT_ERR	RX_CRC_ERR	RX_SYNC_PERR	RX_PL_PERR	RX_SYNC_STOP_ERR	RX_PL_STOP_ERR	RX_PL_START_ERR	–
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	–
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
UART_WATCHDOG	8	The UART Watchdog Timer will assert whenever there has been no activity on the UART_RX pin for at least 4 seconds.	0x0: UART WD not expired 0x1: UART WD has expired

BITFIELD	BITS	DESCRIPTION	DECODE
RX_TIMEOUT_ERR	7	This bit shall be asserted if there are no UART_RX transitions for more than 16 bit lengths during a UART packet. The bit length shall be determined by the SYNC frame of each packet.	0x0: Normal operation. 0x1: UART Rx times out.
RX_CRC_ERR	6	CRC Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: CRC Error: At least one UART transaction rejected due to a failed CRC check.
RX_SYNC_PERR	5	RX Sync Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: RX Sync Frame Parity Error detected.
RX_PL_PERR	4	RX payload parity Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: UART Rx payload parity error detected.
RX_SYNC_STOP_ERR	3	RX sync frame stop bit Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: Rx Sync Frame STOP bit error detected
RX_PL_STOP_ERR	2	RX payload frame stop bit Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: Rx Payload Frame STOP bit error
RX_PL_START_ERR	1	RX payload frame start bit Error Indicator. Read only, clear-on-read	0x0: Normal operation. 0x1: Rx Payload Frame START bit error

STAT_SHORT_LED (0x0E)

STAT_SHORT_LED is a read-only, write 1 to clear, access register that provides short-detect information on the 12 LED output drivers.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	SHORT_LED_STAT[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write 1 to Clear, Read					

BITFIELD	BITS	DESCRIPTION
SHORT_LED_STAT	5:0	Indicates an LED short has been detected.

STAT_OPEN_LED (0x0F)

STAT_OPEN is a read-only, write 1 to clear, access register that provides open-detect information on the 12 LED output drivers.

BIT		12	11	10	9	8
Field		–	–	–	–	–
Reset		–	–	–	–	–
Access Type		–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	OPEN_LED_STAT[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write 1 to Clear, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_LED_STAT	5:0	Indicates that an open-LED condition has been detected.	0x0: Normal 0x1: Open LED

STAT_OPEN_TRACE (0x10)

STAT_OPEN_TRACE is a read-only, write 1 to clear, register that provides open-trace fault information on the 12 LED output drivers.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	OPEN_TRACE_STAT[5:0]					
Reset	–	–	0x000					
Access Type	–	–	Write 1 to Clear, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN_TRACE_STAT	5:0	Indicates an open-trace has been detected.	0x0: Normal 0x1: Open trace

PSFT_GRP (0x11)

PSFT_GRP is a read/write register that allows the user to assign the same phase shift to one or more LED drivers.

The contents of PSFT are written to the desired group specified by PSFT_GROUP.

Example:

If PSFT_GROUP == Group A, PSFT == 0001, and LED11, LED9, and LED6 are assigned to Group A (through CNFG_GRPA), then PSFT_11, PSFT_9, and PSFT_6 will contain 0001 after the transaction is executed.

BIT				12	11	10	9	8
Field				–	–	–	PSFT_GROUP[1:0]	
Reset				–	–	–	0x1	
Access Type				–	–	–	Write, Read	

BIT	7	6	5	4	3	2	1	0
Field	PSFT[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_GROUP	9:8	Group Select: bit 0: Group A selected bit 1: Group B selected Multiple groups can be selected at a time. **Note:** 00 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.
PSFT	7:0	Phase select.

PSFT_0 (0x12)

PSFT_0 is a read/write register that controls the phase shift for LED drivers 0.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_0[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_0	7:0	LED 0 Phase Select.

PSFT_1 (0x13)

PSFT_1 is a read/write register that controls the phase shift for LED drivers 1.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_1[7:0]							
Reset	0x43							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_1	7:0	LED 0 Phase Select.

PSFT_2 (0x14)

PSFT_2 is a read/write register that controls the phase shift for LED drivers 2.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_2[7:0]							
Reset	0x85							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_2	7:0	LED 0 Phase Select.

PSFT_3 (0x15)

PSFT_3 is a read/write register that controls the phase shift for LED drivers 3.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_3[7:0]							
Reset	0x128							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_3	7:0	LED 0 Phase Select.

PSFT_4 (0x16)

PSFT_4 is a read/write register that controls the phase shift for LED drivers 4.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	PSFT_4[7:0]							
Reset	0x171							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_4	7:0	LED 0 Phase Select.

PSFT_5 (0x17)

PSFT_5 is a read/write register that controls the phase shift for LED drivers 5.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PSFT_5[7:0]							
Reset	0x213							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PSFT_5	7:0	LED 0 Phase Select.

TDIM_GRP (0x18)

TDIM_GRP is a read/write register that allows the user to assign the same dimming period to one or more LED drivers. The contents of TDIM are written to the desired group specified by TDIM_GROUP.

Example:

If TDIM_GROUP == Group A, PSFT == 001, and LED12, LED9, and LED6 are assigned to Group A (through CNFG_GRPA), then TDIM_12, TDIM_9, and TDIM_6 will contain 001 after the transaction is executed.

BIT				12	11	10	9	8
Field				–	–	–	–	–
Reset				–	–	–	–	–
Access Type				–	–	–	–	–
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	TDIM_GROUP[1:0]		–	TDIM[2:0]		
Reset	–	–	0x1		–	0b000		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_GROUP	5:4	Group Select: Bit 0: Group A selected Bit 1: Group B selected Multiple groups can be selected at a time. **Note:** 0000 is not a valid selection, the transaction is not executed and the 4-bit value is unchanged.	

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM	2:0	Dimming Period Select	0x0: update PWM duty cycle every 1 PWM period 0x1: update PWM duty cycle every 2 PWM periods 0x2: update PWM duty cycle every 4 PWM periods 0x3: update PWM duty cycle every 8 PWM periods 0x4: update PWM duty cycle every 16 PWM periods 0x5: update PWM duty cycle every 32 PWM periods 0x6: update PWM duty cycle every 32 PWM periods 0x7: update PWM duty cycle every 32 PWM periods 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_2_1_0 (0x19)

TDIM_2_1_0 is a read/write register that controls the dimming period for LED drivers 2, 1, and 0.

BIT				12	11	10	9	8
Field				–	–	TDIM_2[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	–	TDIM_1[2:0]			–	TDIM_0[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_2	10:8	LED 2 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_1	6:4	LED 1 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_0	2:0	LED 0 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

TDIM_5_4_3 (0x1A)

TDIM_5_4_3 is a read/write register that controls the dimming period for LED drivers 5, 4, and 3.

BIT				12	11	10	9	8
Field				–	–	TDIM_5[2:0]		
Reset				–	–	0b000		
Access Type				–	–	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	–	TDIM_4[2:0]			–	TDIM_3[2:0]		
Reset	–	0b000			–	0b000		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TDIM_5	10:8	LED 5 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_4	6:4	LED 4 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)
TDIM_3	2:0	LED 3 Dimming Period Select	0x0: Update PWM duty cycle every 1 PWM period. 0x1: Update PWM duty cycle every 2 PWM periods. 0x2: Update PWM duty cycle every 4 PWM periods. 0x3: Update PWM duty cycle every 8 PWM periods. 0x4: Update PWM duty cycle every 16 PWM periods. 0x5: Update PWM duty cycle every 32 PWM periods. 0x6: Update PWM duty cycle every 32 PWM periods. 0x7: Update PWM duty cycle every 32 PWM periods. 1 PWM period = 8192 clock cycles by default (PWM period configured by bits [3:2] of register address 0x02)

PWM_GRPA_DUTY (0x1B)

PWM_GRPA_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM

dimming to one or more LED drivers.

The contents of DUTY_A are written to LEDs assigned to Group A.

Example:

If DUTY_A == 0x0AA and LED11, LED8, and LED5 are assigned to Group A (through CNFG_GRPA), then DUTY_11, DUTY_8, and DUTY_5 will contain 0x0AA after the transaction is executed.

BIT				12	11	10	9	8
Field				FADE_A	DUTY_A[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_A[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_A	12	Group A PWM Dimming with Fade Enable
DUTY_A	11:0	Group A Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM_GRPB_DUTY (0x1C)

PWM_GRPB_DUTY is a read/write register that allows the user to assign the same duty cycle and enable/disable PWM dimming to one or more LED drivers.

The contents of DUTY_B are written to LEDs assigned to Group B.

Example:

If DUTY_B == 0x0AA and LED11, LED9, and LED6 are assigned to Group B (through CNFG_GRPB), then DUTY_11, DUTY_9, and DUTY_6 will contain 0x0AA after the transaction is executed.

BIT				12	11	10	9	8
Field				FADE_B	DUTY_B[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_B[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_B	12	Group B PWM Dimming with Fade Enable

BITFIELD	BITS	DESCRIPTION
DUTY_B	11:0	Group B Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM0 (0x1D)

PWM0 is a read/write register that configures the LED0 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_0	DUTY_0[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_0[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_0	12	LED0 PWM Dimming with Fade Enable
DUTY_0	11:0	LED0 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM1 (0x1E)

PWM1 is a read/write register that configures the LED1 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_1	DUTY_1[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_1[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_1	12	LED1 PWM Dimming with Fade Enable
DUTY_1	11:0	LED1 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM2 (0x1F)

PWM2 is a read/write register that configures the LED2 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_2	DUTY_2[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_2[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_2	12	LED2 PWM Dimming with Fade Enable
DUTY_2	11:0	LED2 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM3 (0x20)

PWM3 is a read/write register that configures the LED3 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_3	DUTY_3[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	DUTY_3[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_3	12	LED3 PWM Dimming with Fade Enable
DUTY_3	11:0	LED3 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM4 (0x21)

PWM4 is a read/write register that configures the LED4 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_4	DUTY_4[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_4[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_4	12	LED4 PWM Dimming with Fade Enable
DUTY_4	11:0	LED4 Duty-Cycle Selection: 0x000= off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

PWM5 (0x22)

PWM5 is a read/write register that configures the LED5 duty cycle and enables/disables PWM dimming.

BIT				12	11	10	9	8
Field				FADE_5	DUTY_5[11:8]			
Reset				0b0	0x000			
Access Type				Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	DUTY_5[7:0]							
Reset	0x000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FADE_5	12	LED5 PWM Dimming with Fade Enable
DUTY_5	11:0	LED5 Duty-Cycle Selection: 0x000 = Off 0x001 = 1/4095 duty cycle ... 0xfff = 100% duty cycle

Applications Information

Configuration

The first step when setting up the MAX25606 is to program the configuration register 0x02. This register controls the switch slew rates, clock setting, and short thresholds. These registers can only be programmed when the SW_GO_EN bit is set to 0. Do not attempt to program these registers when SW_GO_EN is set to 1.

Synchronized PWM Phase

The clock which controls the PWM phase is reset when the SW_GO_EN bit is set to 0. the PWM phase clock starts again when the SW_GO_EN bit is set to 1. Therefore, using the global/cluster call to send a UART packet to multiple devices at the same time, the SW_GO_EN bit can be set to 1 to ensure each device starts the PWM phase clock at the same instant.

Recommended LED Drivers

For high-performance applications, it is recommended to pair the MAX25606 with an LED driver which has excellent transient response to respond to the dynamic voltage changing that occurs each time a matrix manager switch is opened or closed. Example LED drivers include the MAX20078, MAX20096, MAX20097, and the MAX25601. These LED drivers utilize Maxim's F^3 buck LED driver architecture to achieve excellent transient response, which limits the LED current overshoot and undershoot during matrix manager switch transitions.

For applications with slower or less frequent switch transitions, a general purpose LED driver such as the MAX25600 or MAX25611 may be used. For these applications using a buck-boost or SEPIC LED driver, the transient response is not as fast as a buck LED driver. Therefore, the matrix manager slew rate should be increased to reduce the LED current transient spikes during switch transitions.

Thermal Considerations

Heat is primarily transferred from the IC to the PCB through the exposed pad. Connect the exposed pad to a large solid ground plane. The programmed slew rate impacts the switching power dissipated inside the IC. Faster slew rates reduce the switching power loss, and slower slew rates increase the switching power loss. The programmed PWM frequency also affects the switching power loss. Slower PWM frequencies reduce the switching power loss, and faster PWM frequencies increase the switching power loss.

Conduction loss depends on LED PWM duty cycle. Higher LED PWM duty cycles result in lower conduction loss inside the IC and higher conduction loss in the LEDs. Lower LED PWM duty cycles result in higher conduction loss inside the IC and lower conduction loss in the LEDs.

Layout Considerations

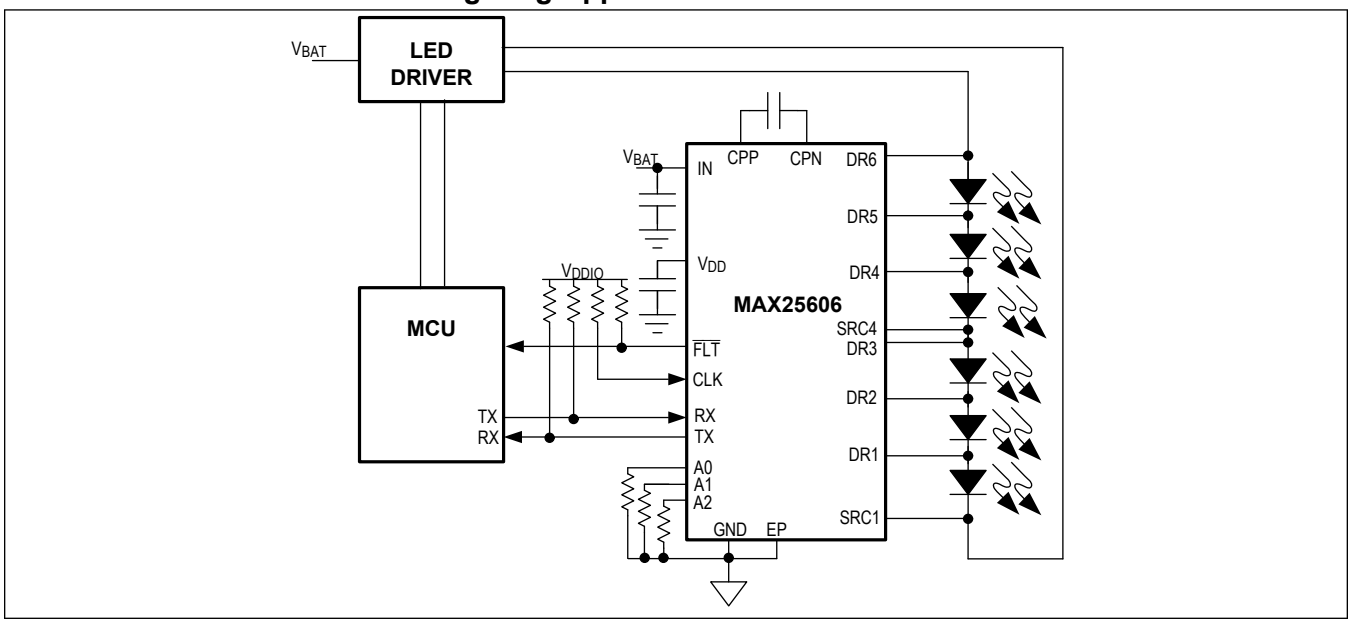
1. Connect the IN, VDD, CPP/CPN, and DR6 decoupling caps as close as possible to the IC.

2. Connect the exposed pad to a large, solid ground plane. The exposed pad is the primary path for heat to escape the device.

Refer to the evaluation kit for an example PCB layout.

Typical Application Circuits

MAX25606 in 6-Channel Matrix Lighting Application



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX25606ATP/VY+	-40°C to +125°C	20 TQFN-EP* (SW)
MAX25606AUP/V+	-40°C to +125°C	20 TSSOP-EP*

/V denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

** EP = Exposed pad.*

(SW) = Side wettable.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Release for Market Intro	—
1	4/22	Changes in General Description, Simplified Block Diagram, *Detailed Description* section; added text under the Internal Switches subheading of the *Detailed Description* section; added description of Read Transactions under the UART Serial Interface subheading; changes in *Typical Application Circuits* section; updated formatting of the Ordering Information table.	1, 11, 15, 17, 43