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Graphic Display Module

Part Number

G986AXGFGN02WR

Overview

98x64(33x33), FSTN, no backlight, reflective, positive mode, 12:00 (top view), extended temp range, parallel/ serial option, able to run at 3.3V

1. General Specification

Interface With PARALLE MPU

Display Mode: POSITIVE/REFLECTIVE/FSTN Type

Viewing Angle :**12:00** Clock

Display Duty:**1/64** Driving Bias:**1/9** Driving Voltage:**9.6V**

Lcd Supply Voltage:+3.3V

Mechanical Characteristics(Unit:mm)

Display Dot Matrix :**98*64**

Extenal Dimension: See Drawing

Dots Size:**0.22*0.27**

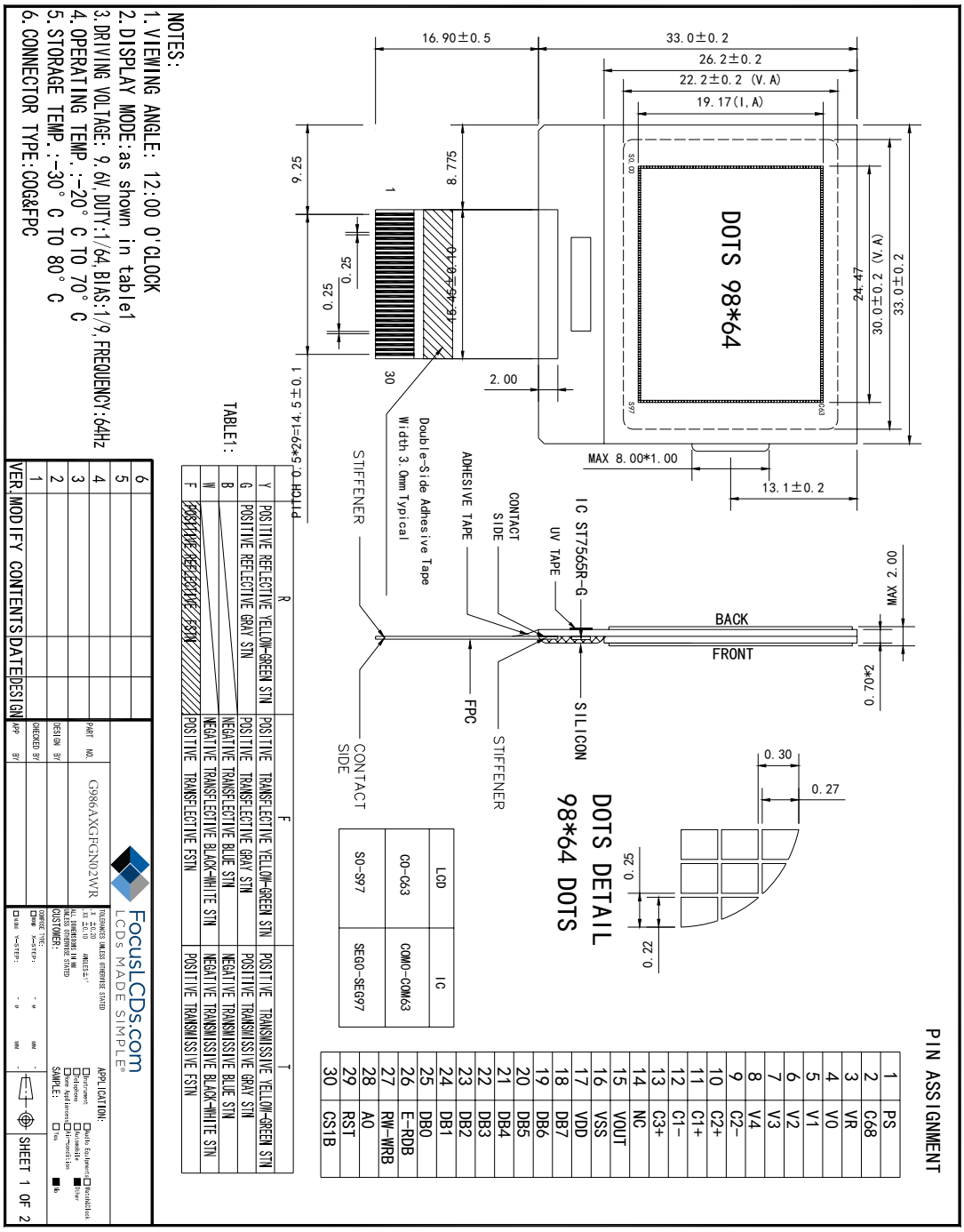
Dots Pitch:**0.25*0.30**

Temperature Specification

Operation Temperature: -20℃～70℃

Storage Temperature:-30℃～80℃

External Dimension



1	PS
2	C68
3	VR
4	V0
5	V1
6	V2
7	V3
8	V4
9	C2-
10	C2+
11	C1+
12	C1-
13	C3+
14	NC
15	VOUT
16	VSS
17	VDD
18	DB7
19	DB6
20	DB5
21	DB4
22	DB3
23	DB2
24	DB1
25	DB0
26	E-RDB
27	RW-WRB
28	A0
29	RST
30	CS1B

LCD	IC
S0-S97	SEG0-SEG97
C0-C63	COM0-COM63

Y	POSITIVE	REFLECTIVE	YELLOW-GREEN	STN	
G	POSITIVE	REFLECTIVE	GRAY	STN	
B	NEGATIVE	TRANSFLECTIVE	BLUE	STN	
W	NEGATIVE	TRANSFLECTIVE	BLACK-WHITE	STN	
F	POSITIVE	TRANSFLECTIVE		FSTN	

R	F	T
POSITIVE REFLECTIVE YELLOW-GREEN STN	POSITIVE TRANSFLECTIVE YELLOW-GREEN STN	POSITIVE TRANSMISSIVE YELLOW-GREEN STN
POSITIVE REFLECTIVE GRAY STN	POSITIVE TRANSFLECTIVE GRAY STN	POSITIVE TRANSMISSIVE GRAY STN
NEGATIVE TRANSFLECTIVE BLUE STN	NEGATIVE TRANSFLECTIVE BLUE STN	NEGATIVE TRANSMISSIVE BLUE STN
NEGATIVE TRANSFLECTIVE BLACK-WHITE STN	NEGATIVE TRANSFLECTIVE BLACK-WHITE STN	NEGATIVE TRANSMISSIVE BLACK-WHITE STN
POSITIVE TRANSFLECTIVE FSTN	POSITIVE TRANSFLECTIVE FSTN	POSITIVE TRANSMISSIVE FSTN

6			
5			
4			
3			
2			
1			
VER.	MODIFY CONTENTS	DATE	DESIGN

COM
S0
C0
COM31
COM0
COM32
COM63
S97
C63
SEG
S0
C0
SEG0
SEG63
S97
C63
FocusLCDs.com
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PART NO.
G9864AXGFGN02WR
DESIGN BY
CHECKED BY
APP BY
VER.
MODIFY CONTENTS
DATE
DESIGN
SHEET 2 OF 2

Input PIN Assignment

Recommended Connector: FH19C-30S-0.5SH(99)

Pin No	Symbol	I/O	Function
30	CS1B	I	This is the chip select signal. When CS1B = “L” and CS2 = “H”, then the chip select becomes active, and data/command I/O is enabled.
29	/RET	I	When /RES is set to "L",the settings are initialized. The reset opetation is performed by the /RES signal level.
28	A0	I	Select register. -A0 = "H": Indicates that DB0 to DB7 are display data -A0 = "L": Indicates that DB0 to DB7 are control data
27	/WR	I	When connected to 8080 series MPU, this pin is treated as the /WR signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to 6800 series MPU, this pin is treated as the /WR signal of the 6800 MPU and decides the access type : When R/W = H: Read. When R/W = L: Write.
26	/RD	I	When connected to 8080 series MPU, this pin is treated as the /RD signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is L. When connected to 6800 series MPU, this pin is treated as the /E signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
25--18	D5 to D0 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = “L”) : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 are set to high impedance.
17	VDD	Power Supply	Power supply
16	VSS	Power Supply	Ground.
15	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.
14	CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.

<table>
<tr><th>Pin No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>13</td><td>CAP1–</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.</td></tr>
<tr><td>12</td><td>CAP1+</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td></tr>
<tr><td>11</td><td>CAP2+</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>10</td><td>CAP2-</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.</td></tr>
<tr><td>9</td><td>CAP4+</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
<tr><td>8-4</td><td>V4, V3, V2, V1, V0,</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are
determined based on Vss, and must maintain the relative magnitudes shown below.
V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr>
<tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr>
<tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr>
<tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr>
</table></td></tr>
<tr><td>3</td><td>VR</td><td>I</td><td>Output voltage regulator terminal. Provides the voltage between VSS and V0 through a
resistive voltage divider.
IRS = “L” : the V0 voltage regulator internal resistors are not used.
IRS = “H” : the V0 voltage regulator internal resistors are used.</td></tr>
<tr><td>2</td><td>C86</td><td>I</td><td>This is the MPU interface selection pin.
C86 = H: 6800 Series MPU interface.
C86 = L: 8080 Series MPU interface.</td></tr>
<tr><td>1</td><td>PSB</td><td>I</td><td>This pin configures the interface to be parallel mode or serial mode.
P/S = H: Parallel data input/output.
P/S = L: Serial data input.</td></tr>
</table>

Absolute Maximun Ratings

VDD=3.0V,VSS=0V,Ta=25℃

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD		-0.3	+3.6	V
Input voltage	Vin		-0.3	VDD+0.3	V
DC Supply Voltage	VOUT		-0.3	+13.5	V
DC Supply Voltage	V0		-0.3	+13.5	V
Operating temperature	Topr		-10	50	℃
Storage temperature	Tstg		-20	60	℃

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VDD		1.8	3.0	3.3	V
Current consumption	IDD	Ta=25℃	-	1.0	-	mA

DC Characteristics

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V, Ta = –30 to 85°C

Table 18

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)		V_{DD}			1.8	—	3.3	V	V_{DD}*1
Operating Voltage (2)		V_{DD2}	(Relative to V_{SS})		2.4	—	3.3	V	V_{DD}
High-level Input Voltage		V_{IHC}			0.8 x V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}			V_{SS}	—	0.2 x V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA		0.8 x V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA		V_{SS}	—	0.2 x V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}	V_{IN} = V_{DD} or V_{SS}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative to V_{SS})	V_0 = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
				V_0 = 8.0 V	—	3.2	5.4		
Static Consumption Current		I_{SSQ}	V_0 = 13.0 V (Relative To V_{SS})		—	0.01	2	µA	V_{DD}, V_{DD2}
Output Leakage Current		I_{OQ}			—	0.01	10	µA	V_0
Input Terminal Capacitance		C_{IN}	Ta = 25°C, f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/65 duty 1/33 duty	Ta = 25°C	17	20	24	kHz	*8
	External Input	f_{CL}			17	20	24	kHz	CL
	Internal Oscillator	f_{OSC}	1/49 duty 1/53 duty 1/55 duty	Ta = 25°C	25	30	35	kHz	*8
	External Input	f_{CL}			25	30	35	kHz	CL

Table 19

Item		Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Internal Power	Input voltage	V_{DD2}	(Relative To V_{SS})	2.4	—	3.3	V	V_{DD}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative To V_{SS})	—	—	13.5	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative To V_{SS})	6.0	—	13.5	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_0	(Relative To V_{SS})	4.0	—	13.5	V	V_0 * 9
	Base Voltage	VRS	Ta = 25°C, (Relative To V_{SS}) –0.05%/°C	2.07	2.10	2.13	V	*10

TIMING CHARACTERISTICS

System bus read/write characteristics 1 (8080 Series MPU)

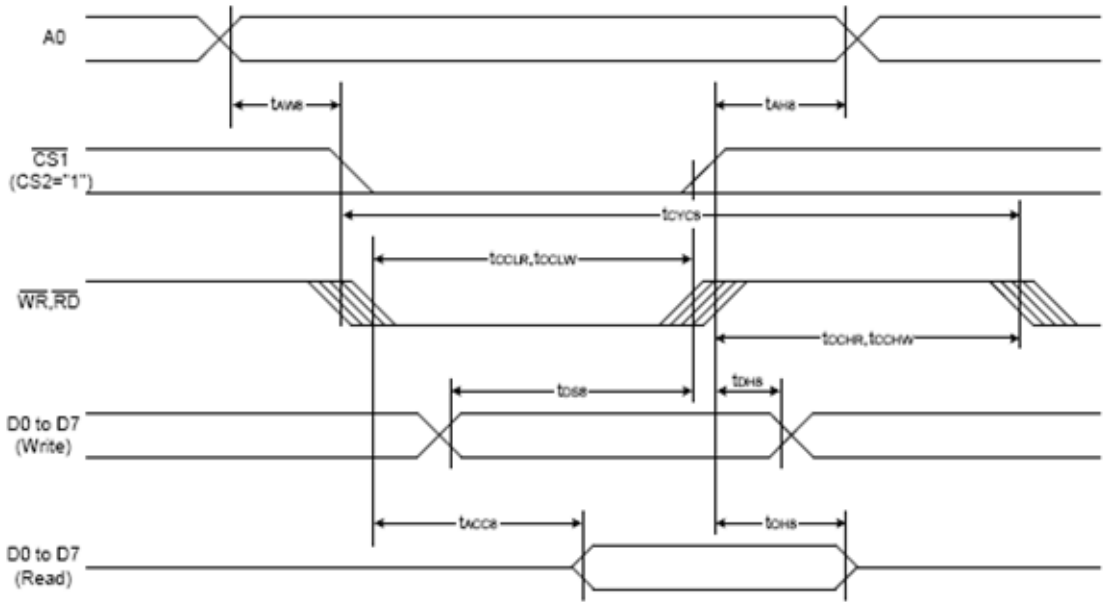


Figure 37

Table 24

(VDD = 3.3V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	Ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

Table 26

(VDD = 1.8V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

System bus read/write characteristics 2 (6800 Series MPU)

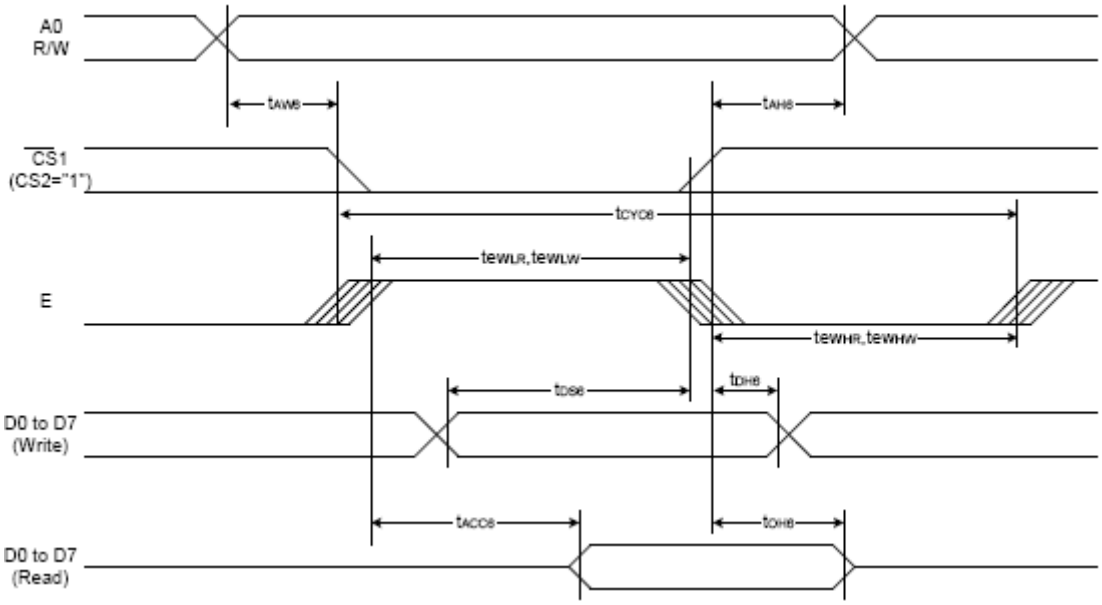


Figure 38

Table 27

(VDD = 3.3V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	CL = 100 pF	—	140	
READ Output disable time		t_{OH6}	CL = 100 pF	10	100	

Table 29

(VDD = 1.8V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	CL = 100 pF	—	240	
READ Output disable time		t_{OH6}	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.
*2 All timing is specified using 20% and 80% of VDD as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

IC Specification

See The Reference of ST Data Book----ST7565R-G.

Instruction Table

Table 16: Table of ST7565R Commands (Note) *: ignored data

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power save	0	1	0									Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

Instruction Description

1. Display ON/OFF

This command turns the display ON and OFF.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

2. Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

3. Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

4. Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

5. Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 131-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

6. Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

7. Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E /RD	R/W /WR	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

8. ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

9. Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H"
											LCD ON voltage (normal)
										1	RAM Data "L"
											LCD ON voltage (reverse)

10. Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

11. LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

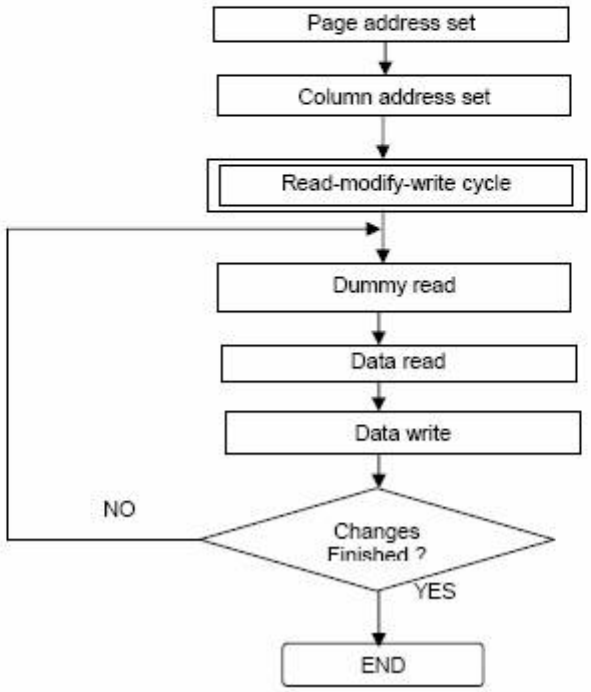
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status 1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

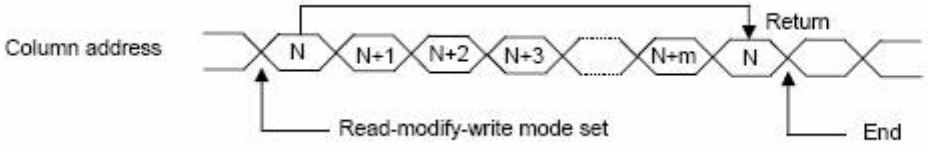
12. Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.





13. End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

14. Reset

This command initializes the display start line, the column address, the page address, the common output mode, the Vo voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

15. Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

E	R/W									Selected Mode					
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0 1	*	*	*	Normal Reverse	COM0→COM63 COM63→COM0	COM0→COM47 COM47→COM0	COM0→COM31 COM31→COM0	COM0→COM53 COM53→COM0	COM0→COM51 COM51→COM0

* Disabled bit

16. Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0 1			Booster circuit: OFF Booster circuit: ON
									0 1		Voltage regulator circuit: OFF Voltage regulator circuit: ON
										0 1	Voltage follower circuit: OFF Voltage follower circuit: ON

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the Vo voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and table 11 .

	E	R/W									
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0 0 0 ↓ 1 1	0 0 1 ↓ 1 1	0 1 0 1 1	Small ↓ Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

19. The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

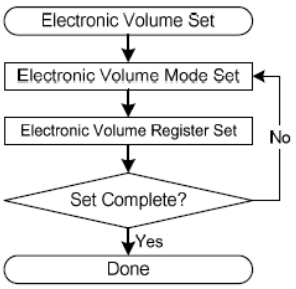
20. Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_0 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	| V_0 |
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set "0")
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

21. The Electronic Volume Register Set Sequence



22. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

23. Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

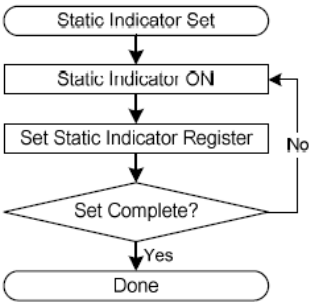
24. Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

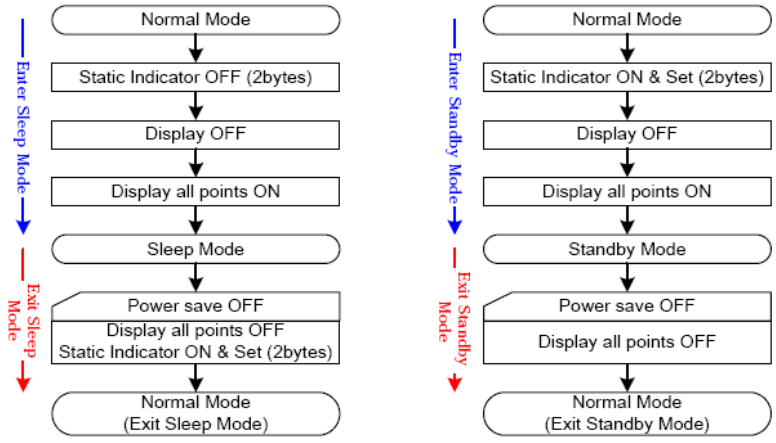
* Disabled bit (set "0")

25. Static Indicator Register Set Sequence



26. Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 28 for power save off sequence.



27. Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a Vss level.

28. Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a Vss level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The ST7565P series chips have a liquid crystal display blanking control terminal /DOF. This terminal enters an "L" state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

29. The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

30. Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

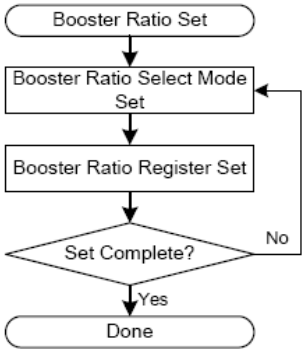
31. Booset Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set "0")
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode

32. The booster ratio Register Set Sequence



33. NOP

Non-Operation Command

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

34. Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the /RES input by the reset command or by using an NOP.

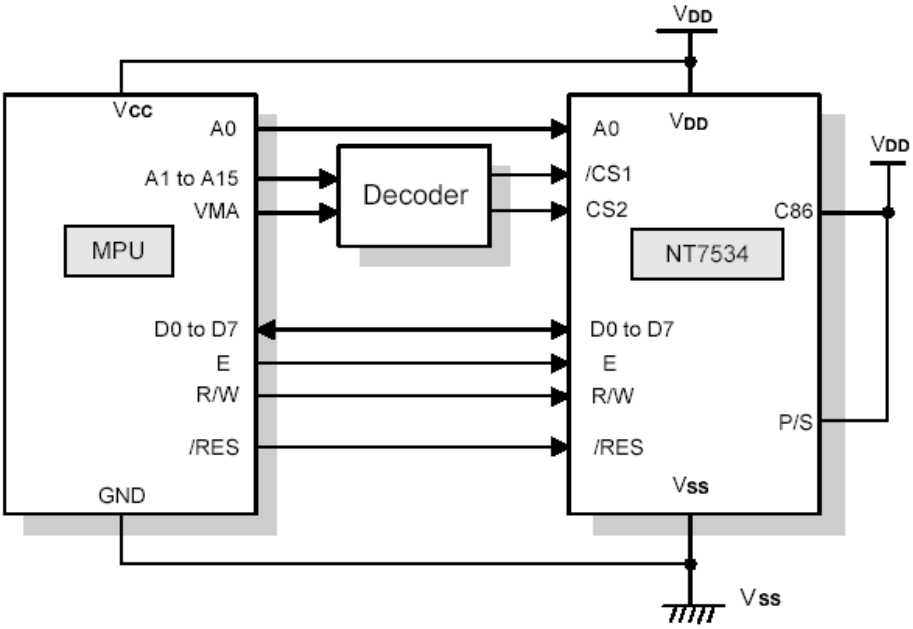
	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

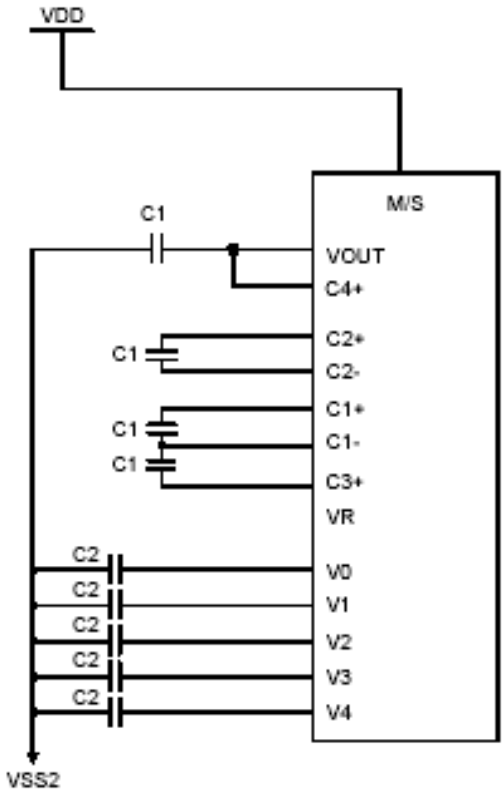
Note: The ST7565P maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565P . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Application Example

1.1 6800 Series MPU

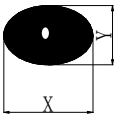


1.2

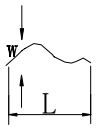


Inspection Standards:

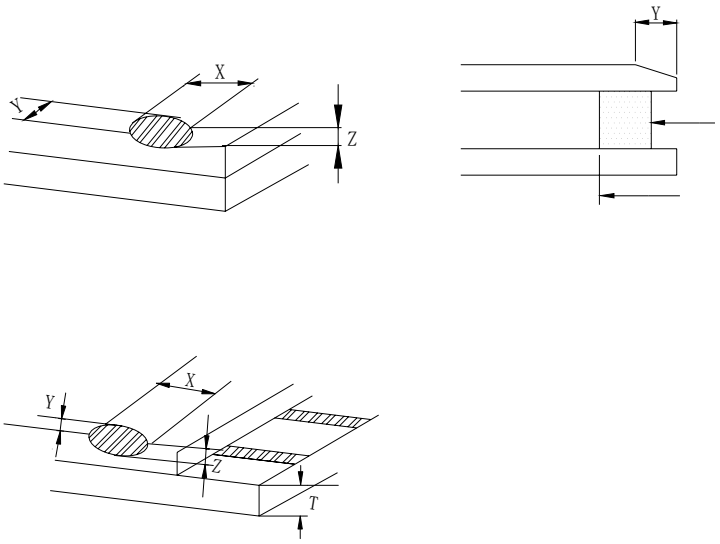
The Appearance Inspection Criteria (Unit： mm)

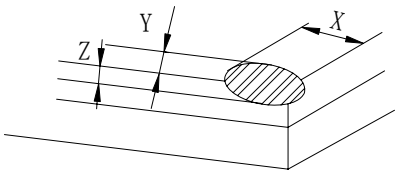
<table>
<tr><th>O</th><th>Item</th><th>Criteria</th><th>Defect Definition</th></tr>
<tr><td>1</td><td>1.1
Dot Defect (Round Dirty spot, Black spot, Leak light spot, Polarize upside down) (Outside V.A will be Ignored)</td><td>


<table>
<tr><th rowspan="2">Dimension</th><th>Acceptable Number</th></tr>
<tr><th>General Mode</th></tr>
<tr><td>Φ≦0.10</td><td>Ignore</td></tr>
<tr><td>0.10＜Φ≦0.20</td><td>2</td></tr>
<tr><td>0.20＜Φ≦0.25</td><td>1</td></tr>
</table>
Φ=（X+Y）/2

If Φ≦0.10, it will be ignored, But, concentrate is not acceptable, (Concentrate definition: If the diameter of the round is 5mm, the defect number over 5 Entries) and distance between two dots must≧10mm
</td><td>Minor Defect</td></tr>
<tr><td></td><td>1.2
Line Defect (Fiber, Glass and Polarizer scratch, Black line, Crack (Outside V.A will be Ignored)</td><td>


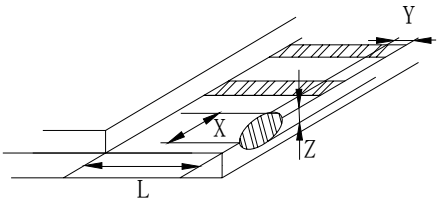
(1) L is meaning that the longest of the line defect.
<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Number</th></tr>
<tr><td>No limit</td><td>W≦0.02</td><td>Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.02≦W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.0</td><td>0.03≦W≦0.05</td></tr>
<tr><td>－</td><td>0.05<W</td><td>According to the Dot Criteria</td></tr>
</table>
(2) If there is line bending repetition, please use W to calculate the total width of the repetition lines!
(3) The distance between two lines must≧10mm
</td><td></td></tr>
</table>

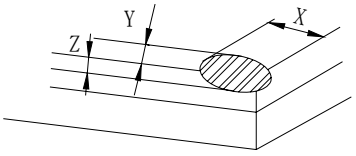
2	2.1 Chip out	Explain： (1) All of the Chip out couldn't in the Viewing Area (2) Chip out couldn't in the internal electrode line Code Name：(X：Crack Length；Y：Crack Width； Z： Crack thickness； A： LCD border length; W： The width electrode line； L： End length； T： The thickness of monolayer glass)	
		2.1.1A Chip out in the surface(Crack in one side)：  	Minor Defect

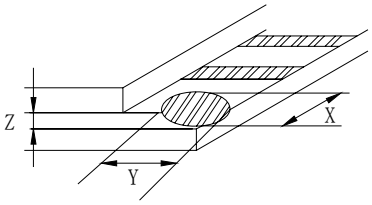
NO	Item	Criteria	Defect Definition
2	2.1 Chip out	 	

X	Y	Z
>1/8A	≦0. 3mm	≦1/2T
≦1/8A	Not in seal glue	≦T
	Not inside of seal glue	≦1/2T

2.1.1 B Chip out in the surface(Crack in the electrode foot)





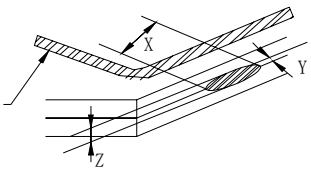


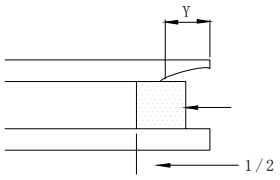
X	Y	Z
>1/8A	≦ 0.3mm	≦1/2T
≦1/8A	≦1/2L	≦T
≦1/8A 且≦2mm	≦L	≦1/2T

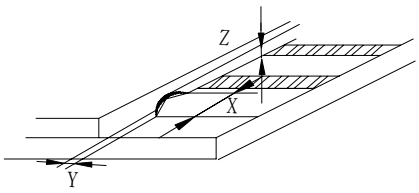
Note: The distance of chip out and electrode should be larger than one electrode.

Minor Defect

2.1.2 Chip out in the middle

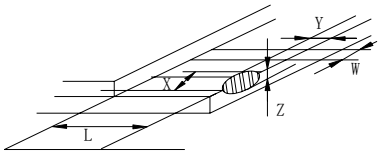


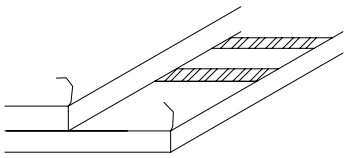
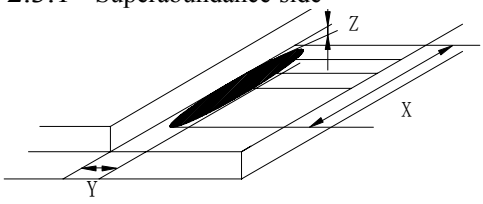




X	Y	Z
≦1/8A	Not in seal glue	Z≦2T
	Not in 1/2 width of seal glue	Z≦1/2T

Minor Defect

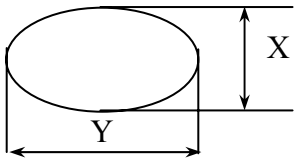
<table>
<tr><th>NO</th><th>Item</th><th>Criteria</th><th>Defect Definition</th></tr>
<tr><td rowspan="4">2</td><td>2.1
Chip out</td><td>2.1.4 Crack the electrode (including the electrode corner or side)
 

<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>>1/8A</td><td>≦1/5L</td><td rowspan="3">≦1/2T</td></tr>
<tr><td>≦1/8A</td><td>≦1/3L</td></tr>
<tr><td>≦1/4W</td><td>≦2/3L</td></tr>
</table></td><td>Minor Defect</td></tr>
<tr><td>Crack</td><td> 
(1) Around the seal glue is reject
(2) The length of crack in the electrode longer than 0.5mm is reject.</td><td>Minor Defect</td></tr>
<tr><td rowspan="2">2.3
Cutting/ Breaking defect</td><td>2.3.1 Superabundance side
 

<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>>1/8A</td><td rowspan="2">≤1/5L</td><td>≦1/2T</td></tr>
<tr><td>≦1/8A</td><td>1/2T≦ Z≦T</td></tr>
</table></td><td>Minor Defect</td></tr>
<tr><td>2.3.2 The side is not even
Over the tolerance of engineering drawing is reject;</td><td>Minor Defect</td></tr>
<tr><td>3</td><td>3.1
Polarizer upside down</td><td>Polarizer more, less or wrong stick is reject</td><td>Major Defect</td></tr>
</table>

<table>
<tr>
<td></td>
<td>3.2

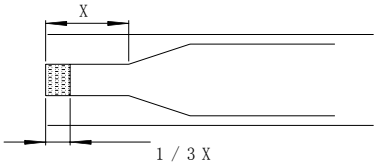
Void in Polarizer

Outside V.A will be Ignored)</td>
<td> 

Φ=(X+Y)/
<table>
<tr><th>Dimension</th><th>Acceptable number</th></tr>
<tr><td>Φ≦0.20</td><td>Ignore</td></tr>
<tr><td>0.20≦Φ≦0.40</td><td>2</td></tr>
<tr><td>0.40≦Φ</td><td>0</td></tr>
</table>
Note:
Air bubble should be in the same color, or will as 1.1mm dot defect, and the distance between the two dots should be larger than 10mm.</td>
<td>Minor Defect</td>
</tr>
<tr>
<td></td>
<td>3.3

Polarizer shift from its position</td>
<td>Polarizer extrudes glass edge and in the viewing area is reject.</td>
<td>Minor Defect</td>
</tr>
</table>

NO	Item	Criteria	Defect Definition
	3.5 Protective layer separated from polarizer	(1) If the protective layer could be stick once again, it will be acceptable; but if it isn't, and the long side should less than 1/3 of polarizer length, short side should less than 1/2 of polarizer length. (2) Protective layer separated from polarizer lead to the polarizer is evident crack or dirty is reject.	
4	Rainbow of backlight color	If it is evident has different color is reject or according to limited sample	Minor Defect
5	Different background color	One batch products have the different background color is reject or according to limited sample	Minor Defect
6	Contact Dot	Contact glue besides is reject	Minor

			Defect
7	End sealing	(1) Pressurize defect is reject	Major
		(2) End sealing in the viewing area is reject	Minor
		(3) Width less than 0.35mm is reject	Minor
		(4) There is liquid crystal and dirt in electrode line area and other ITO position is reject.	Minor Defect
		(5) There is air bubble in end sealing: need to keep 1/2 end sealing width	Minor
		(6) End sealing in the viewing area is reject, frame heave no more than 1/3 frame width, frame thin no more than 1/2 frame width	Minor Defect
8	8.1 Pressurize quality	Pressurize defect is reject.	Major Defect
	8.2 End sealing bearing	End sealing bearing should be the same as engineering drawing, or reject.	Minor Defect
	8.3 Glue dirty	Reject	Minor Defect
	8.4 End sealing dimension	Over engineering drawing is reject, end sealing deflect and don't cover the hatch is reject	Minor Defect
	8.5 End sealing over permeate	Into viewing area is reject  X: The deepness of the seal	Minor Defect Minor Defect
9	PIN defect	(1) The position of install pin should be according to engineering drawing; If it isn't note, the warp of middle of pin and middle of electrode should in 0.25mm (2) The thickness pin glue couldn't exceeds polarizer, and cover area couldn't cover polarizer	Minor Defect

		(3) Pin glue couldn't flow to PIN (4) Pin glue not enough: conduct electric pins should have glue in just and back sides, the less should cover the lowest of pin in back side. (5) The tolerance of PIN deflection should less than ±5° (Unless there's other prescribe, according to engineering drawing)	

NO	Item	Criteria	Defect Definition
9	PIN defect	(6) Pin crack couldn't lead to copper bareness (7) The surface of PIN couldn't be dirty or rusty (8) There's air bubble in PIN glue, but won't lead to break is acceptable (9) If the mode, number, length, bend angle, dimension of PIN won't according to engineering drawing is reject. (10) There couldn't have crimple or defile at PIN	Minor Defect

<table>
<tr>
<td>10</td>
<td>Printing ink print</td>
<td>
(1) Print figure should according to engineering drawing, couldn’t be wrong, lack, color wrong or not drying;

(2) Color of printing ink have evident warp is reject or according to limited sample.

(3) The line of printing frame discontinuity or thickness different is reject

(4) The incline of line of printing frame should less than ±1°

(5) Printing position excursion: according to engineering drawing to estimate; If the it isn’t sign tolerance, it couldn’t exceed ±0.20mm, and couldn’t affect the display font.

(6) Printing line width estimation：
<table>
<tr><th>W: Design width</th><th>P: Actual printing width</th></tr>
<tr><td>W≦0.40</td><td>|W-P|≦1/2W</td></tr>
<tr><td>W>0.40</td><td>|W-P|≦0.20</td></tr>
</table>
Note: If the engineering drawing has regulation, please according to it.
(7) Printing pattern concave dot, protruding dot, pin hole estimation:
<table>
<tr><th>Dimension</th><th>Acceptable number</th></tr>
<tr><td>Φ<0.10</td><td>Ignore</td></tr>
<tr><td>0.10<Φ≦0.25</td><td>2</td></tr>
<tr><td>0.25<Φ</td><td>0</td></tr>
</table>
Note: The distance between the two dots should larger than 5mm.
(8) Printing pattern have black dot, crack, please according to Dot and Line Defect Criteria
</td>
<td>Major Defect

Minor Defect

Minor Defect

Minor Defect

Minor Defect

Minor Defect

Minor Defect

Minor Defect</td>
</tr>
</table>

		(8)Burred: Wave range should no more than 0.20mm	Minor Defect