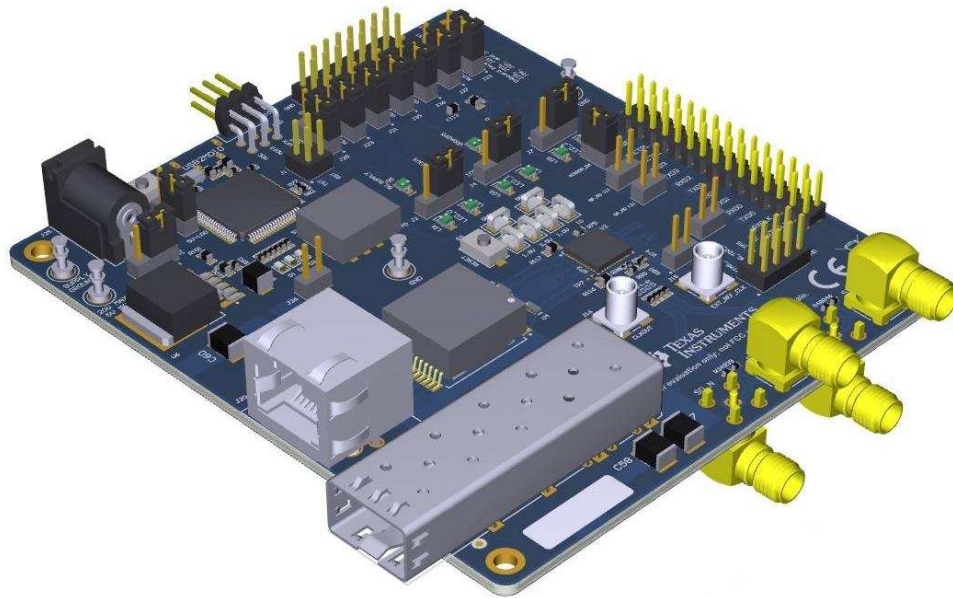


DP83869EVM User's Guide



This User's Guide discusses how to properly operate and configure the DP83869EVM. For best layout practices, schematic files, and Bill of Materials, see the associated support documents.

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1 Definitions

Table 1. Terminology

ACRONYM	DEFINITION
PHY	Physical Layer Transceiver
MAC	Media Access Controller
SMI	Serial Management Interface
MDIO	Management Data I/O
MDC	Management Data Clock
MII	Media Independent Interface
RMII	Reduced Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
SGMII	Serial Gigabit Media Independent Interface
VDDA	Analog Core Supply Rail
VDDIO	Digital Supply Rail
PD	Pulldown
PU	Pullup

2 Introduction

The DP83869 is a low power, fully-featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols. It also supports Fiber protocols 1000BASE-X and 100BASE-FX. Optimized for ESD protection, the DP83869 exceeds 8-kV IEC 61000-4-2 (direct contact). This device interfaces to the MAC layer through Reduced GMII (RGMII) and SGMII. Integrated Termination Impedance on RGMII helps reduce system BOM. The DP83869EVM will demonstrate all features of DP83869. The EVM will support Copper Ethernet protocols like 10BASE-Te, 100BASE-TX, and 1000BASE-T. It also supports Fiber protocols 1000BASE-X and 100BASE-FX. The EVM has connections to use the DP83869 MAC Interface in RGMII and SGMII mode. The EVM will also be optimized to demonstrate the robust EMI, EMC, and ESD performance of the DP83869 device.

2.1 Key Features

- Multiple Operating Modes
 - Media Support: Copper and Fiber
 - Media Conversion: Copper to Fiber
 - Bridge Conversion: RGMII to SGMII, SGMII to RGMII
- RGMII and SGMII MAC Interfaces
- 1000Base-X, 100Base-T, 100Base-TX, 10Base-Te
- USB-2-MDIO Support Through Onboard MSP430 for Easy Register Access
- Onboard LDO and External Power Supply Options
- Status LEDs
 - Link
 - Activity
 - Power
- Bootstraps for Hardware Configuration

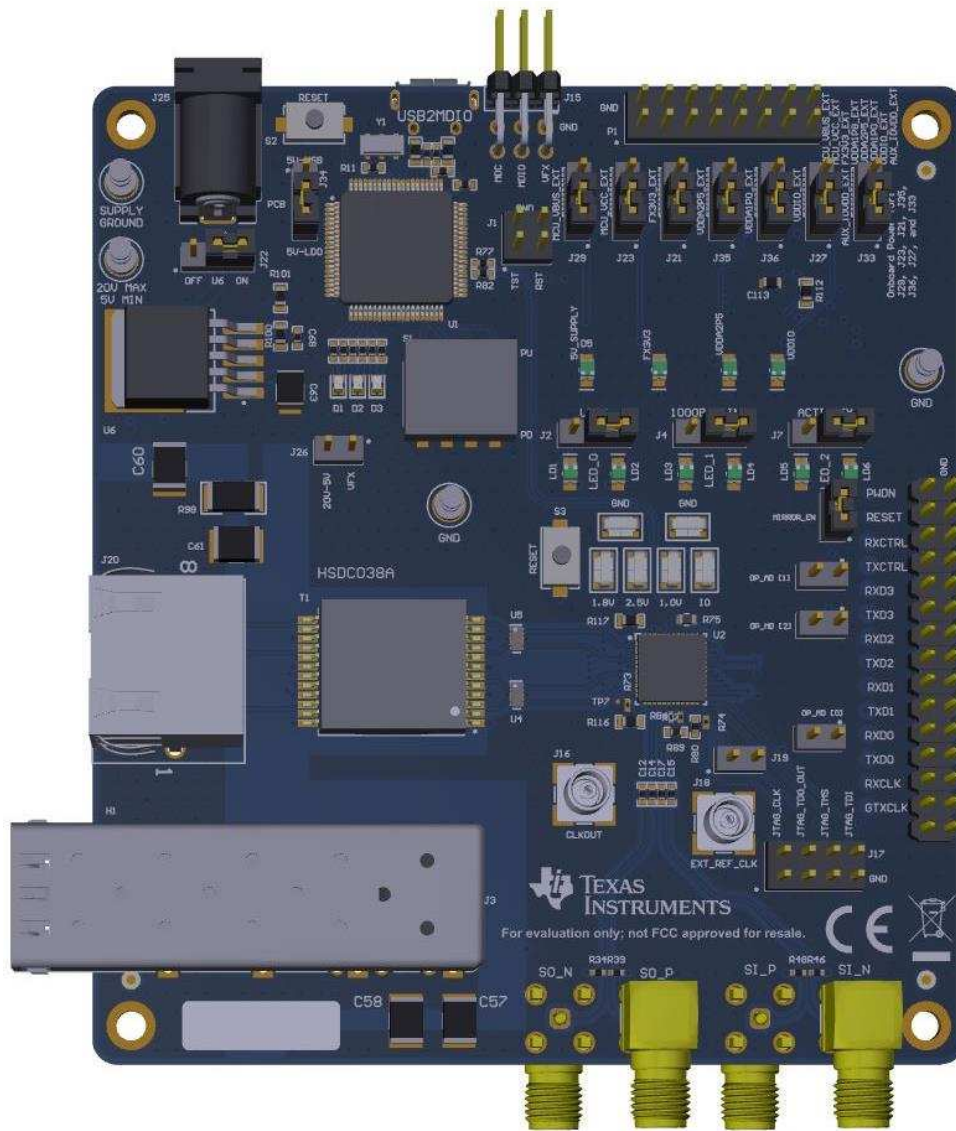


Figure 1. DP83869EVM – Top Side

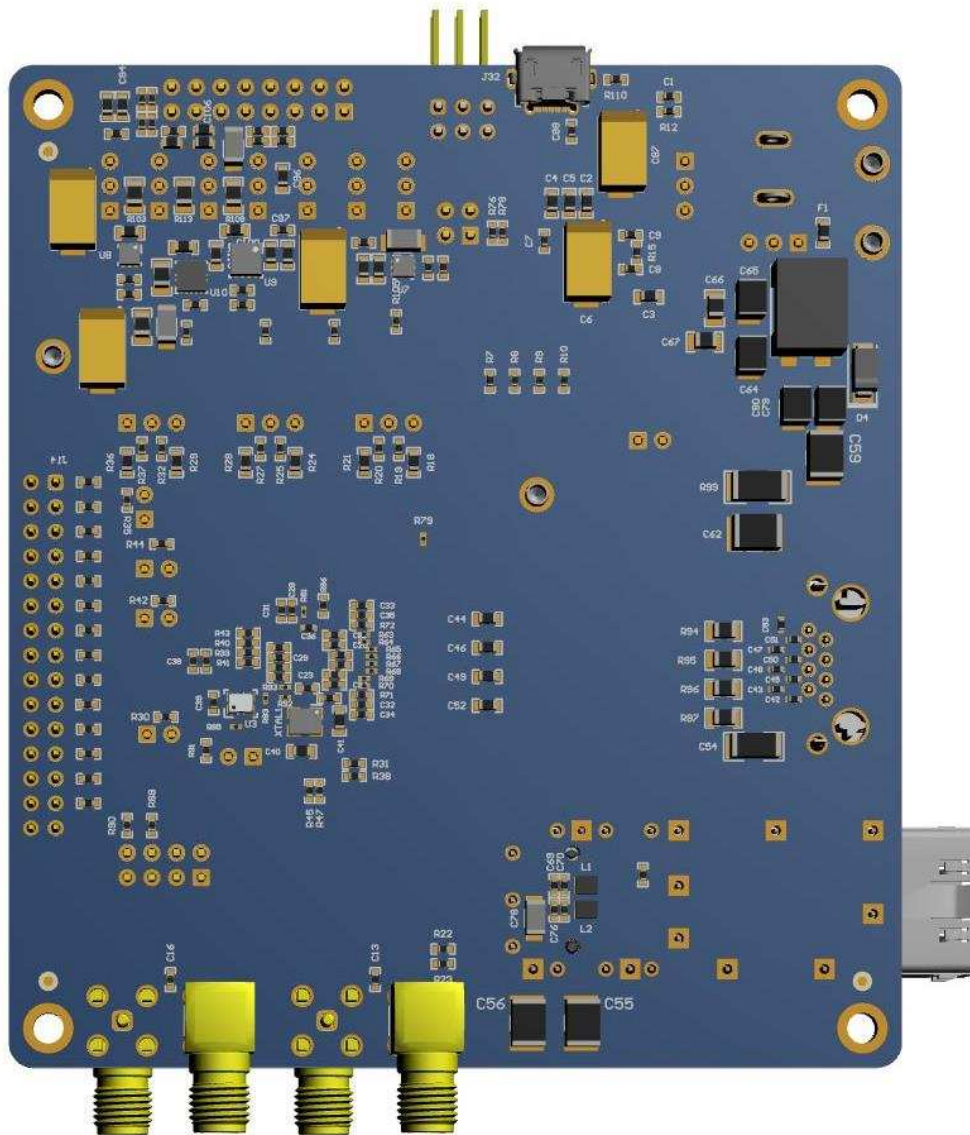


Figure 2. DP83869EVM – Bottom Side

2.2.3.2 USB-2-MDIO Software

Download the software from <http://www.ti.com/tool/usb-2-mdio>. The Web page also contains a User's Guide for installing and using the software.

The MSP430 is on board the EVM, so it is not required to purchase a separate MSP430 Launchpad kit and connect to the PHY using wires. The entire EVM can be powered and controlled through a USB connector. MSP430 and USB2MDIO utility can be used even when power is not supplied through a USB.

In case the onboard MSP430 cannot be used due to some reason, MDIO and MDC pins are also broken out on the J15 connector. Customers can connect a MSP430 launchpad or their own MDIO-MDC utility on J15 to access the PHY registers.

3 Board Setup Details

3.1 Block Diagram

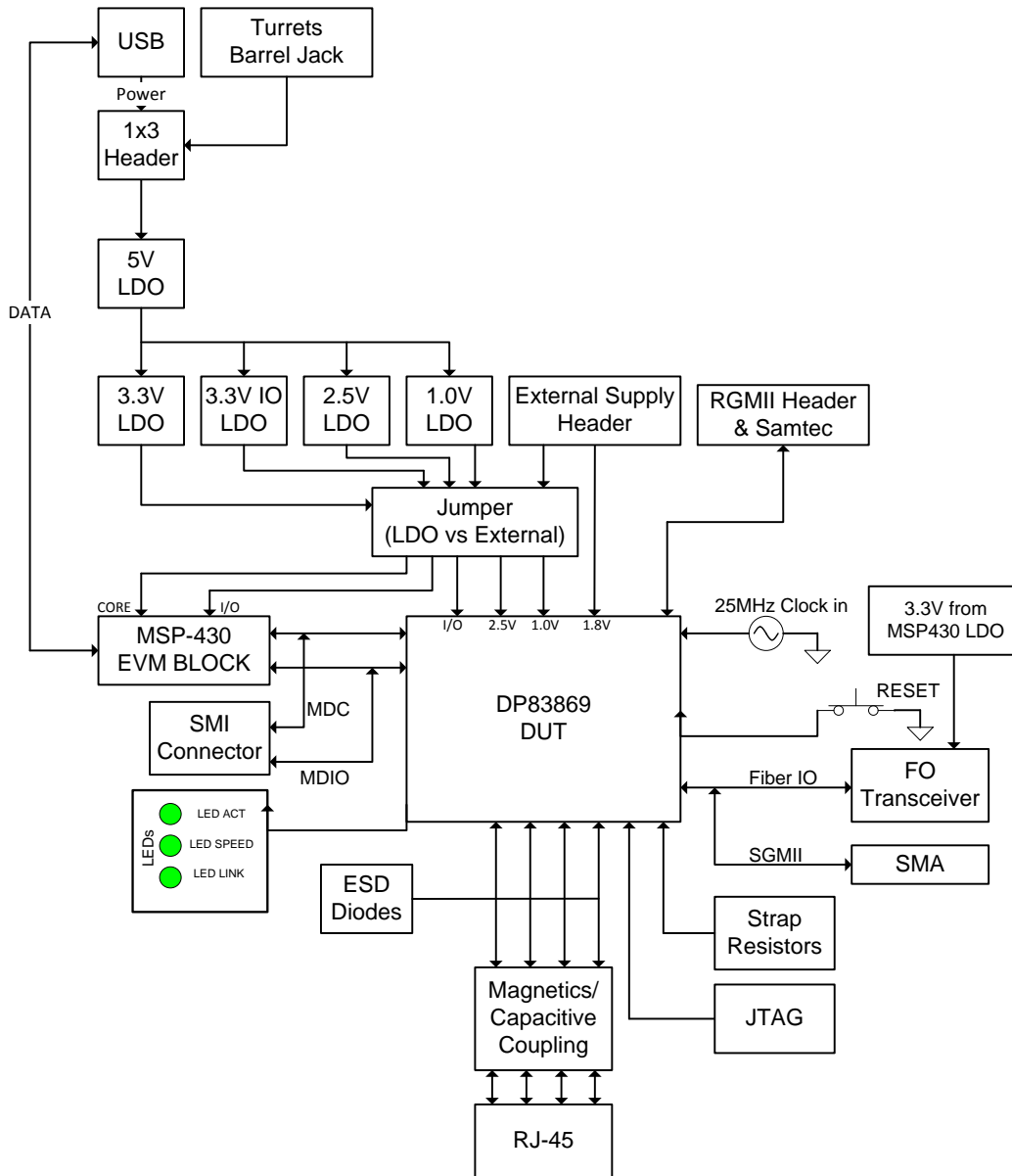


Figure 5. DP83869EVM Block Diagram

3.2 EVM High-Level Summary

The DP83869EVM supports SMI through J2 using pin 26 for MDIO and 28 for MDC. These pins can be connected to an MSP430 Launchpad, which can be used for USB-2-MDIO control.

Table 2. EVM Applications

NO.	DP83869 MODE	APPLICATIONS	HOW TO USE
1	RGMII to Copper	Run traffic between RGMII and Copper.	Connect to DP83867 RGMII EVM or MAC System using Header pins/Samtech connector.
		Perform IEEE and UNH compliance testing	Use onboard MSP430 to activate test mode waveform on DP83869
		Run EMI/EMC Test on EVM	Use internal PRBS and loopback
		Measure Power Dissipation	Connect external power supplies.
		External MAC loopback	Connect external MAC to headers/Samtech connector.
2	SGMII to Copper	Run traffic between SGMII and Copper.	Connect to DP83867 SGMII EVM or MAC System using SMA connector.
		Perform IEEE and UNH compliance testing	Use onboard MSP430 to activate test mode waveform on DP83869.
		Run EMI/EMC Test on EVM	Use internal PRBS and loopback
		External SGMII loopback	Use SMA cable for Passive Loopback.
3	RGMII to Fiber Ethernet	Run traffic between RGMII and Fiber Ethernet.	Straps to enable Fiber Ethernet. Connect to DP83867 RGMII EVM or MAC System using Header/Samtech.
		Perform IEEE and UNH compliance testing	Use onboard MSP430 to activate test mode waveforms.
		Run EMI/EMC Test on EVM	Use internal PRBS and loopback
		Measure Power Dissipation	Connect external power supplies.
4	100M Media Convertor	Demonstrate 100M functionality on EVM	Use SFP and RJ45 connector for fiber and copper ethernet. Straps will be used for unmanaged mode and MDIO for managed mode.
		Demonstrate FAR End fault capability	
		Demonstrate unmanaged mode of Media convertor	
5	1000M Media Convertor	Demonstrate 1000M functionality on EVM	Use SFP and RJ45 connector for fiber and copper ethernet. Straps will be used for unmanaged mode and MDIO for managed mode.
		Demonstrate Link Loss Pass Thru Capability	
		Demonstrate unmanaged mode of Media Convertor	
6	RGMII to SGMII bridge	Demonstrate SGMII as MAC able to link with SGMII i/f of Phy (DP83867)	Connect to DP83867 SGMII EVM over SMA connectors and monitor RGMII header on 869 EVM.
		Demonstrate SGMII link speed is reflected on RGMII	
		Demonstrate Complete Data path Use-case	Use DP83867 RGMII EVM and SGMII EVM with DP83869EVM.
7	SGMII to RGMII bridge	Demonstrate RGMII of DP83869 is able to link-up with RGMII of DP83867	Connect to DP83867 RGMII EVM over Samtech connectors and monitor SGMII SMA on 869 EVM.
		Demonstrate SGMII link speed is reflecting RGMII speed	
		Demonstrate Complete Data path Use-case	Use DP83867 RGMII EVM and SGMII EVM with DP83869EVM.

4 Configuration Options

4.1 Bootstrap Options

Except PHYADD straps, all other straps are only two-level straps in DP83869. EVM will support one pullup and one pulldown resistor pad on RX_D0 and RX_D2 for PHY address straps. There will be only one pullup resistor on all other strap pins with a jumper option to disconnect it.

Table 3. 4 Level Straps

STRAP VALUE	MODE 1	MODE 2	MODE 3	MODE 4
Resistor PU (kΩ)	Open	10	5.76	2.49
Resistor PD (kΩ)	Open	2.49	2.49	Open

Table 4. 2 Level Straps

STRAP VALUE	MODE 1	MODE 2
Resistor PU (kΩ)	2.49	Open
Resistor PD (kΩ)	Open	2.49

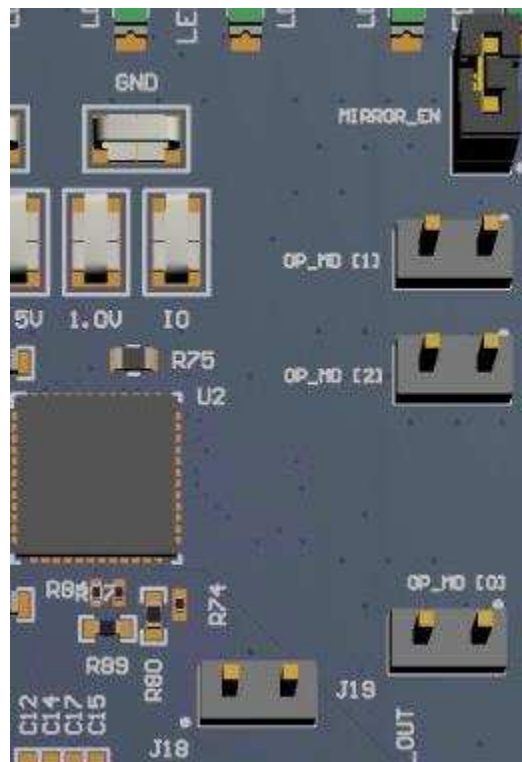


Figure 6. EVM Strap Jumpers

4.1.1 Straps for PHY Address

Table 5. PHY Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT			
RX_D0	PHY_ADD[1:0]	33	00	PHY_ADD1 PHY_ADD0		
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1
RX_D1	PHY_ADD[3:2]	34	00	PHY_ADD3 PHY_ADD2		
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1

4.1.2 Strap for DP83869 Functional Mode Selection

Table 6. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	OPMO DE_2	OPMO DE_1	OPMO DE_0	FUNCTIONAL MODES
JTAG_TDO/GP IO_1	OPMODE_0	22	0	0	0	0	RGMI to Copper(1000Base-T/100Base-TX/10Base-Te)
				0	0	1	RGMI to 1000Base-X
RX_D3	OPMODE_1	36	0	0	1	0	RGMI to 100Base-FX
				0	1	1	RGMI-SGMII Bridge Mode
RX_D2	OPMODE_2	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-T to 100Base-FX
				1	1	0	SGMII to Copper(1000Base-T/100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

4.1.3 Straps for RGMII/SGMII to Copper

Table 7. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN NO.	DEFAULT	ANEG _DIS	ANEG SEL_1	ANEG SEL_0	FUNCTION
LED_0	ANEG_DIS	47	0	0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	Reserved (JTAG for boundary scan)
				1	0	0	Forced 1000M, master, MDI mode

Table 7. Copper Ethernet Strap Table (continued)

PIN NAME	STRAP NAME	PIN NO.	DEFAULT				
LED_2	ANEGSEL_1	45	0	1	0	1	Forced 1000M, slave, MDI mode
				1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode
RX_CTRL	MIRROR_EN	38	0	0			Port Mirroring Disabled
				1			Port Mirroring Enabled

4.1.4 Straps for RGMII to 1000Base-X

Table 8. 1000Base-X Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
LED_0	ANEG_DIS	47	0	0	Fiber Auto-negotiation ON
				1	Fiber Force mode
LED_1	ANEGSEL_0	46	0	0	Signal Detect disable on Pin 24
				1	Configure Pin 24 as Signal Detect Pin

4.1.5 Straps for RGMII to 100Base-FX

Table 9. 100Base-X Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
LED_1	ANEGSEL_0	46	0	0	Signal Detect disable on Pin 24
				1	Configure Pin 24 as Signal Detect Pin

4.1.6 Straps for Bridge Mode (SGMII-RGMII)

Table 10. Bridge Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_CTRL	MIRROR_EN	38	0	0	RGMII to SGMII (RGMII : MAC I/F, SGMII : Phy I/F)
				1	SGMII to RGMII (SGMII : MAC I/F, RGMII : Phy I/F)

4.1.7 Straps for 100M Media Convertor

Table 11. 100M Media Convertor Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
LED_1	ANEGSEL_0	46	0	ANEGSEL_1	ANEGSEL_0	
LED_2	ANEGSEL_1	45	0	0	0	Copper : Auto-negotiation (100/10 Advertised), Auto MDIX
				1	1	Copper : Auto Negotiation (100 Advertised), Auto MDIX

Table 11. 100M Media Convertor Strap Table (continued)

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_CTRL	MIRROR_EN	38	0	0	Copper: Mirror Disable
				1	Copper: Mirror Enable
RX_CLK	LINK_LOSS	32	0	0	Link Loss Pass Thru Enabled
				1	Link Loss Pass Thru Disabled

4.1.8 Straps for 1000M Media Convertor

Table 12. 1000M Media Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
LED_0	ANEG_DIS	47	0	0	Fiber Auto Negotiation	
				1	Fiber Force Mode	
LED_1	ANEGSEL_0	46	0	ANEGSEL_1	ANEGSEL_0	
LED_2	ANEGSEL_1	45	0	0	0	Copper : Auto-negotiation (1000/100 Advertised), Auto MDIX
				1	1	Copper : Auto Negotiation (1000 Advertised), Auto MDIX

4.2 SGMII/Fiber Interface

SGMII Pins from the DUT are multipurpose pins functioning as SGMII and Fiber IO pins. By default, the EVM will be configured for Fiber operation.

NOTE: Fiber Transceiver is not a part of the EVM package. SFP cage and SFP connector will be mounted.

For routing signals to Fiber Transceiver, populate R31, R38, R45, and R47. Remove C12, C14, C15, and C17.

For routing signals to SGMII SMAs, populate C12, C14, C15, and C17. Remove R31, R38, R45, and R47.

4.3 RGMII

RGMII signals are routed to standard 2.54-mm header connectors on J14. RGMII can be used both in Copper mode and Fiber mode.

4.4 Clock Output

The EVM has a SMB connector to output clock from the PHY. A 50-Ω Coax cable with a SMB connector should be used for accessing the clock output.

4.5 Clock Input

The EVM is configured for default crystal input clock operation. It supports the option to provide clock from 25-MHz crystal, 25-MHz CMOS oscillator, and the External clock from the SMB connector. A 50-Ω Coax cable with a SMB connector should be used for providing clock input from external sources.

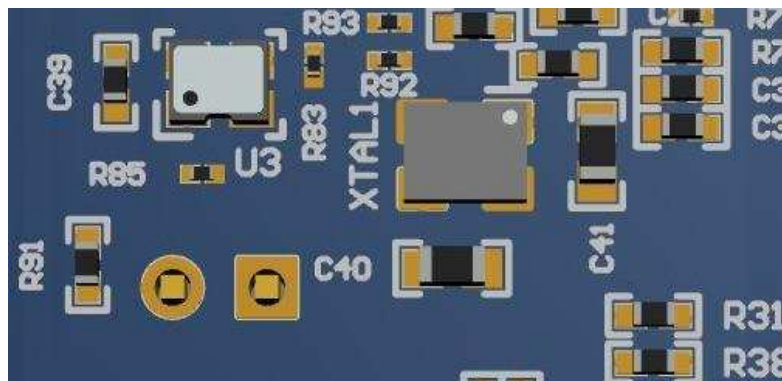


Figure 7. Onboard Clock



Figure 8. External Clock Input

4.6 Switch Configuration Options

The DP83869EVM includes a 4-pin dip switch (S3), which can be used for various test modes and feature displays. Some of the switch settings can also be used with the USB-2-MDIO GUI for additional control. Except for switch mode 15, all switch modes are hard-coded and can be used without USB-2-MDIO or any other serial com port. Refer to [Table 13](#) for switch configurations and LED outputs. For each switch, PU is 1 and PD is 0.

Table 13. 4-Pin Dip Switch Modes

Mode	SW[4:1]	Feature	LED Description	LED D14	LED D15	LED D16	USB2MDIO
0	0000	Normal Operation	USB-2-MDIO Active (Flashes very briefly red during read and green during write)	Red Green	Off	Off	Yes
			Program failed to read PHY register	Red	Off	Off	No
			Program failed to write PHY register	Green	Off	Off	
1	0001	Test Mode 1 - Droop	Successfully entered Test Mode 1	Red Green	Off	Green	Yes
			Failed to enter Test Mode 1 (Flashing LEDs)	Red	Red	Red	No
2	0010	Test Mode 2 - Clock Frequency, Master Jitter	Successfully entered Test Mode 2	Red Green	Off	Red	Yes
			Failed to enter Test Mode 2 (Flashing LEDs)	Red	Red	Red	No
3	0011	Test Mode 3 - Slave Jitter	Successfully entered Test Mode 3	Red Green	Off	Red Green	Yes
			Failed to enter Test Mode 3 (Flashing LEDs)	Red	Red	Red	No

Table 13. 4-Pin Dip Switch Modes (continued)

Mode	SW[4:1]	Feature	LED Description	LED D14	LED D15	LED D16	USB2MDIO
4	0100	Test Mode 4 - Distortion	Successfully entered Test Mode 4	Red Green	Green	Off	Yes
			Failed to enter Test Mode 4 (Flashing LEDs)	Red	Red	Red	No
5	0101	Test Mode 5	Successfully entered Test Mode 5	Red Green	Green	Green	Yes
			Failed to set Test Mode 5 (Flashing LEDs)	Red	Red	Red	No
6	0110	Force 100Mbps	Force 100-Mbps speed with force MDI	Red Green	Green	Red	Yes
			Program failed to program the PHY registers	Off	Green	Red	No
7	0111	Force 10Mbps	Force 10-Mbps speed with force MDI and PRBS on.	Off	Green	Red	No
			Program failed to program the PHY registers	Red	Red	Red	
8	1000	Reverse Loopback	Successfully entered Reverse Loopback	Red Green	Red	Off	Yes
			Failed to enter Reverse Loopback (Flashing LEDs)	Red	Red	Red	No
9	1001	xMII Loopback	Successfully entered xMII Loopback	Red Green	Red	Green	Yes
			Failed to enter xMII Loopback (Flashing LEDs)	Red	Red	Red	No
10	1010	Enable BIST	Enable BIST in Copper Ethernet Mode	Red	Green	Red Green	No
			Program failed to program the PHY registers	Red	Red	Red	
11 - 14	1011 - 1110	RESERVED	RESERVED	-	-	-	No
15	1111	LOOP: Read data continuously from a list of registers loaded to the MC	To upload a list of registers to continuously read from with USB-2-MDIO: Write the hex value of the register you want to add to the list to the register address "LOAD"	Red Green	Red Green	Red Green	Yes ⁽¹⁾
			To begin reading data continuously with USB-2-MDIO: Read the register address "OPEN"				
			To stop reading data continuously with USB-2-MDIO: Read the register address "STOP"				

⁽¹⁾ During the loop for Mode 15, USB-2-MDIO is not operational. However, other serial port terminals (that is, PuTTY) can be used to view real-time data.

When running switch mode 15, data is constantly sent to the serial port. USB-2-MDIO is not capable of supporting the constant read feature. However, other serial port terminals, that is, PuTTY, can be used. When using a serial port terminal, copy and paste data. Do not enter in the data slowly, because the firmware will execute as soon as the data is received.

To load a list of registers to read data from, follow this data format:

##LOADAAAAB/

- ## = Two digit PHY ID expressed in decimal form
- LOAD = the string 'LOAD' indicates to the MC to add a register to the list
- AAAA = Four character Register Address to read data from in hex form (that is, Read register 0x133h, set AAAA = 0133)

- B = use '*' for an extended access read and '=' for a direct access read
- / = end string with '/'

For example, to load register 0x462h with PHY_ID = 1 with extended access, copy and paste the following command into a serial com terminal: 01LOAD0462*/

To start reading data, continuously copy and paste the following into the serial com terminal: OPEN

To stop reading data, continuously copy and paste the following into the serial com terminal: STOP

NOTE: The "OPEN" and "STOP" commands are in no particular position, so the designer can copy "OPENSTOP" and paste it into the serial com terminal once to start reading data and then paste it again to stop reading data, for example.

NOTE: When the read loop is stopped, the list of registers to read is cleared.

5 Schematics

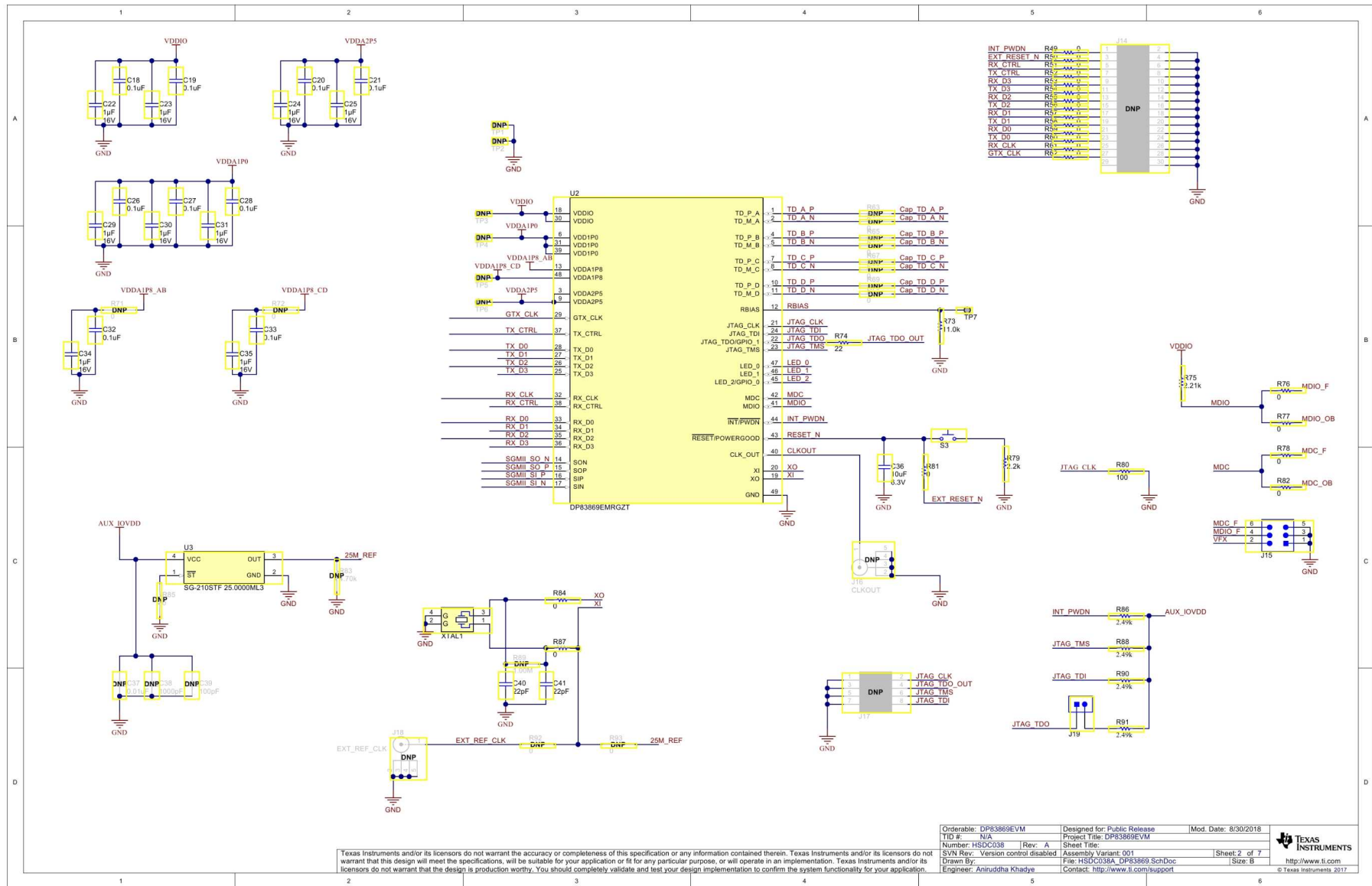


Figure 9. Schematic Page 1

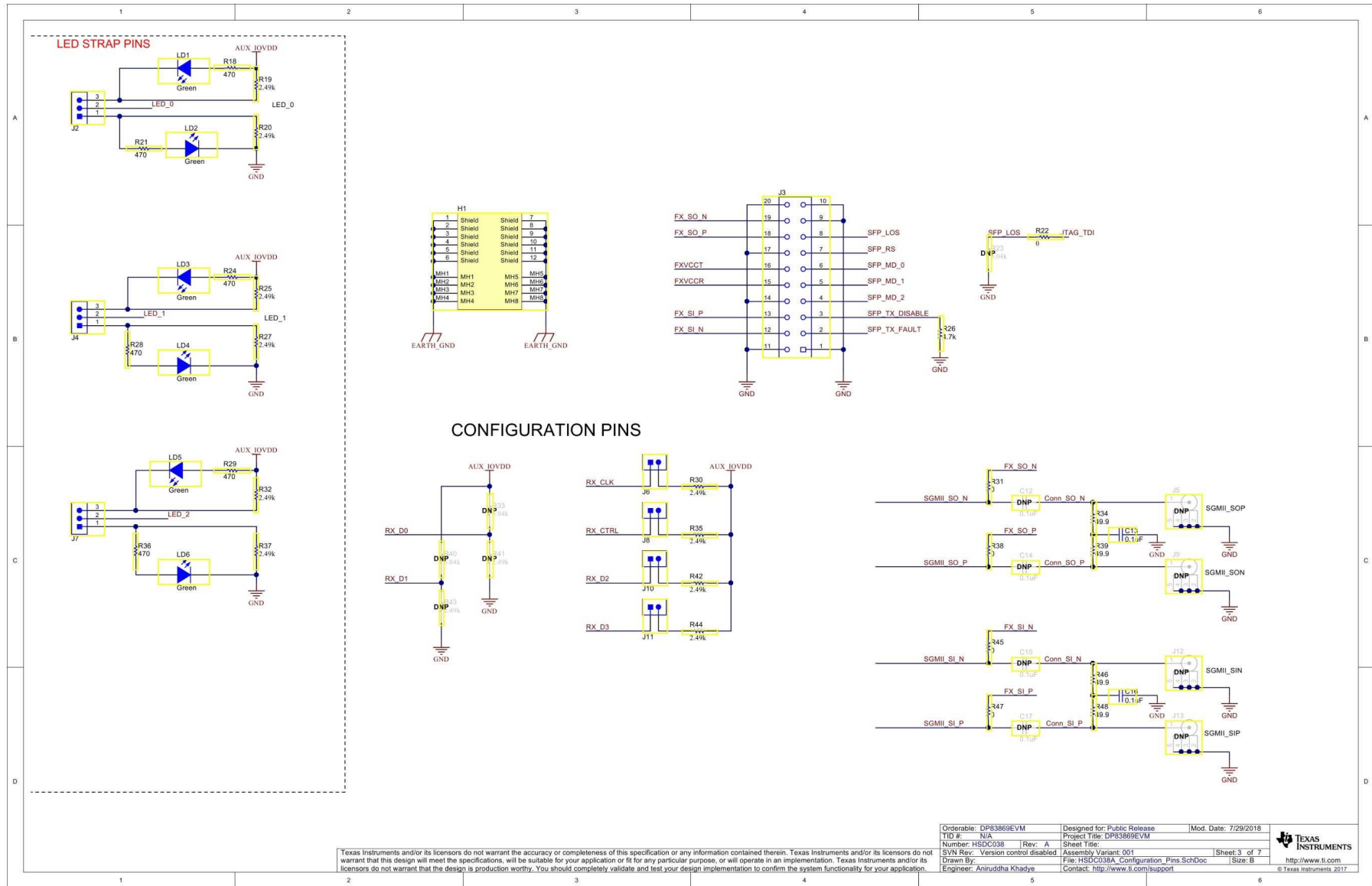
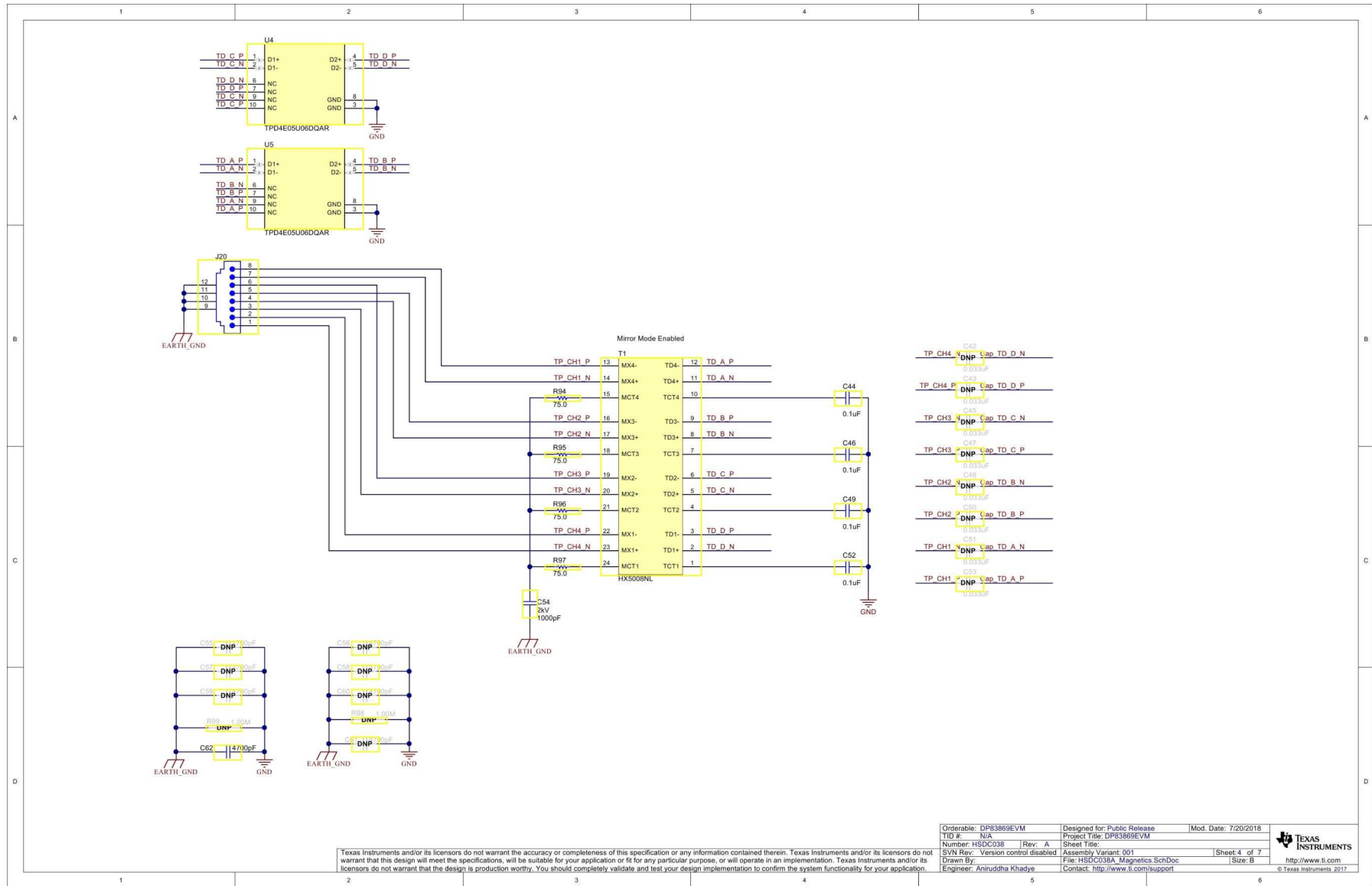


Figure 10. Schematic Page 2

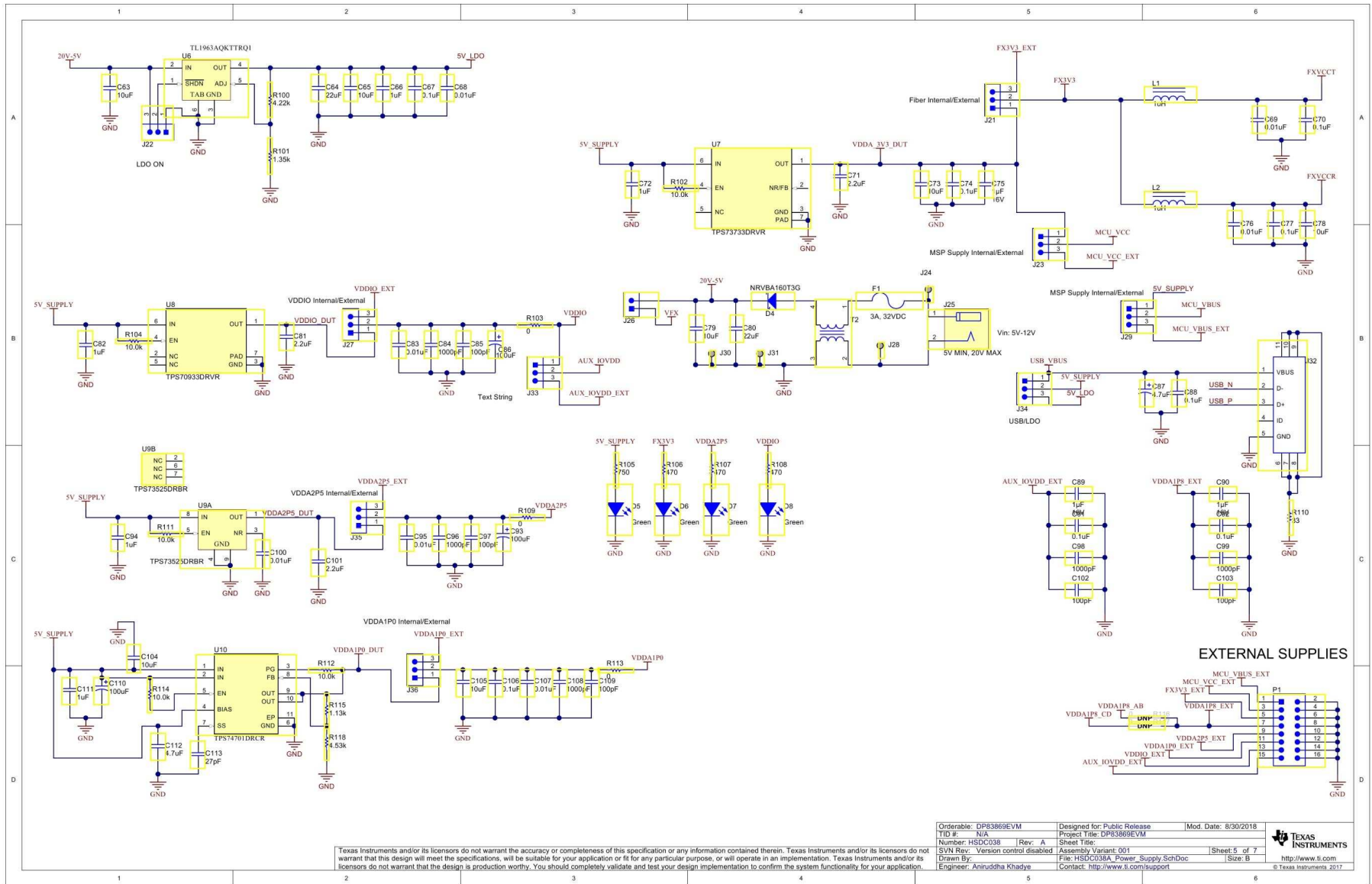


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Orderable: DP83869EVM	Designed for: Public Release	Mod. Date: 7/20/2018	
TID #: N/A	Project Title: DP83869EVM	Sheet Title:	
Number: HSDC038	Rev: A	Assembly Variant: 001	
S/N Rev: Version control disabled	File: HSDC038A_Magnetics_SchDoc	Sheet: 4 of 7	
Drawn By:	Contact: http://www.ti.com/support	Size: B	

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Figure 11. Schematic Page 3



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TID #: N/A	Project Title: DP83869EVM	
Number: HSDC038	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 7
Drawn By:	File: HSDC038A_Power_Supply_SchDoc	Size: B
Engineer: Aniruddha Khadye	Contact: http://www.ti.com/support	

Figure 12. Schematic Page 4

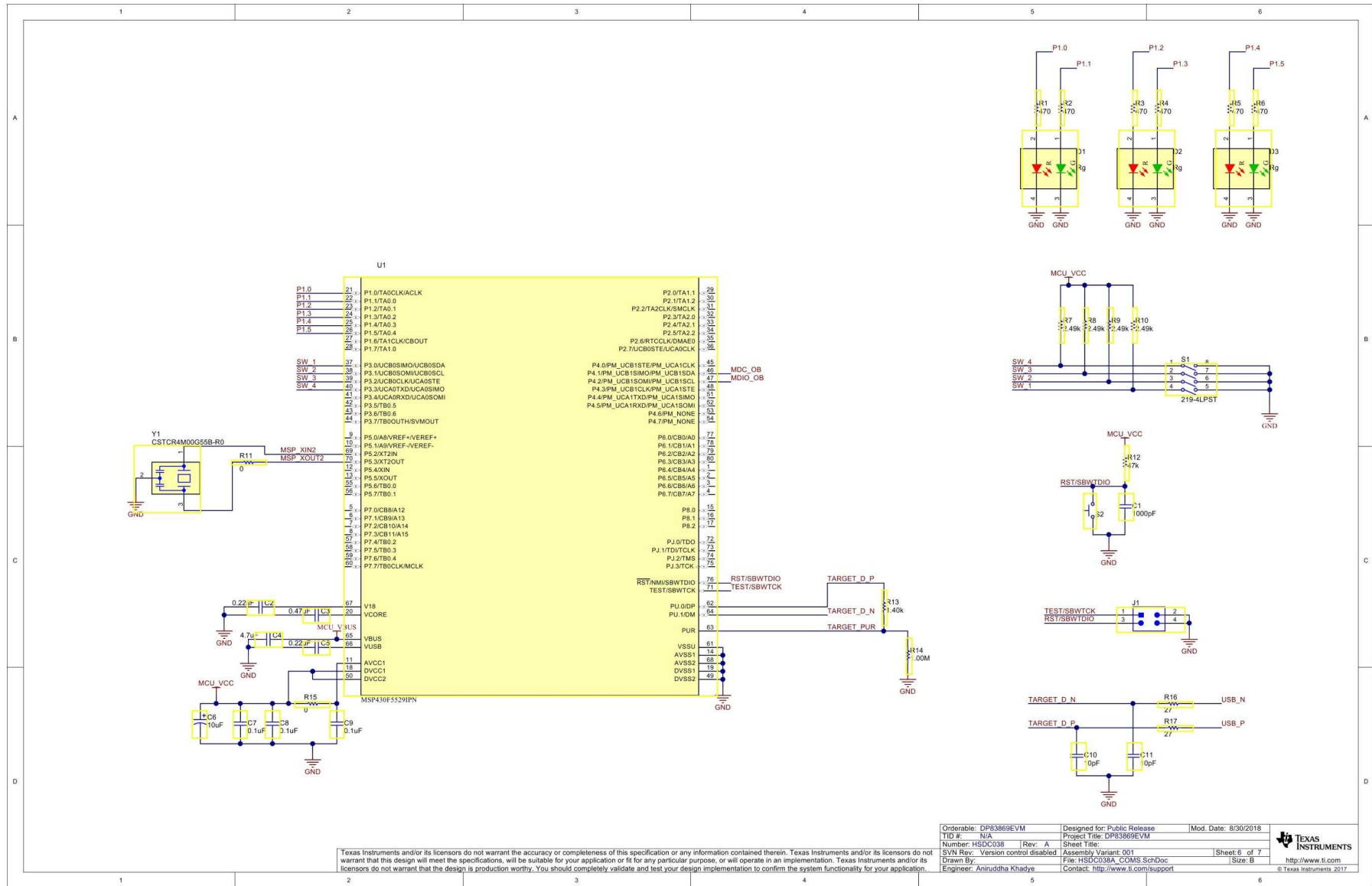


Figure 13. Schematic Page 5

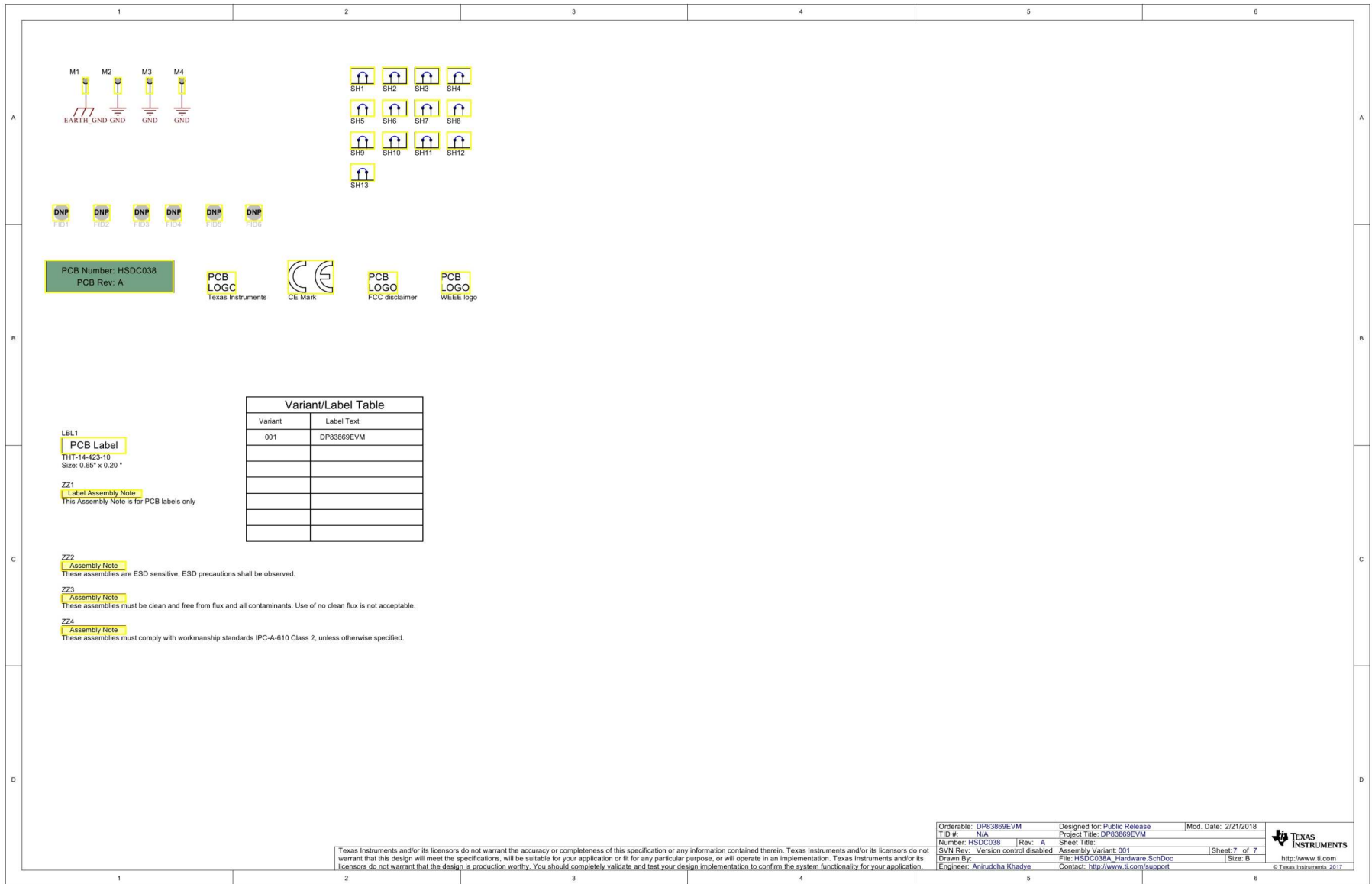


Figure 14. Schematic Page 6

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