# Integrated Driver and MOSFET

# NCP252163

The NCP252163 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP252163 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

### Features

- Capable of Average Currents up to 60 A
- Capable of Switching at Frequencies up to 2 MHz
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−Level PWM Inputs
- Option for Zero Cross Detection with 3−Level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning Output
- Thermal Shutdown
- This is a Pb−Free Device

### Applications

- Desktop and All−in−One Computers, V−Core and Non−V−Core DC−DC Converters
- High−Current DC−DC Point−of−Load Converters
- Small Form−Factor Voltage Regulator Modules

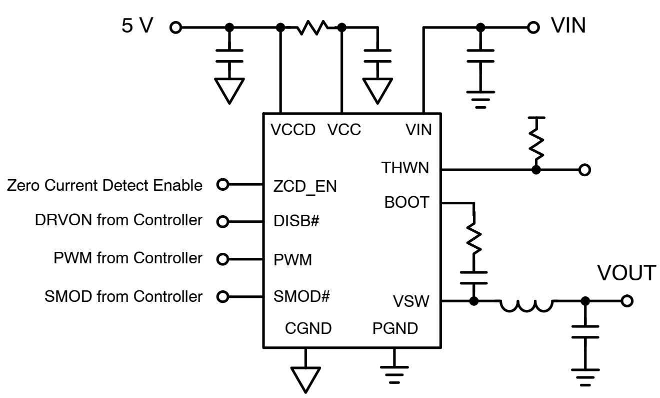
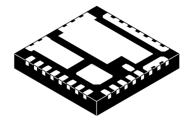
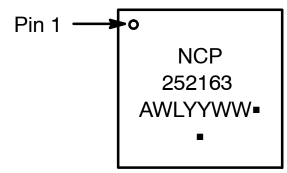



**Figure 1. Application Schematic**



**PQFN31 5X5, 0.5P
CASE 483BR**

### MARKING DIAGRAM




| | |
|---|---|
| NCP252163 | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NCP252163MNTWG | PQFN31 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## BLOCK DIAGRAM

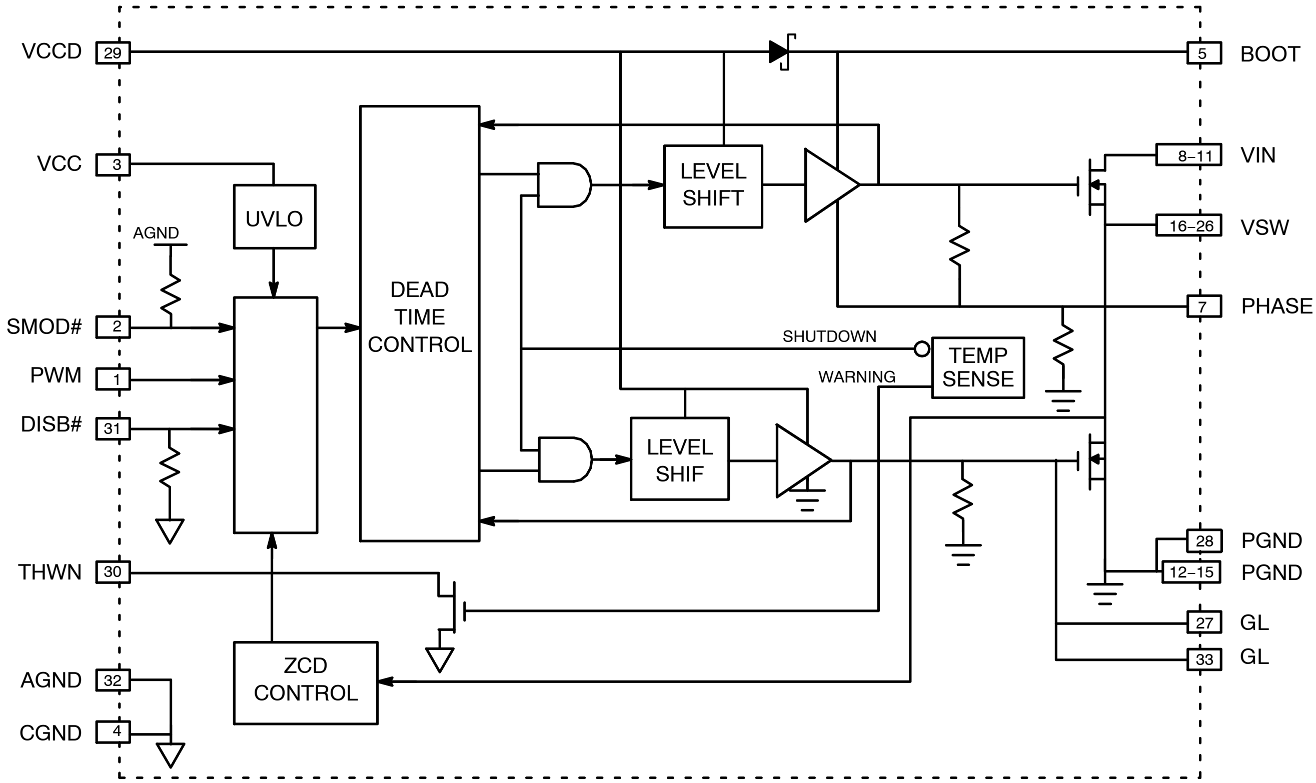



Figure 2. Block Diagram

## PINOUT DIAGRAM

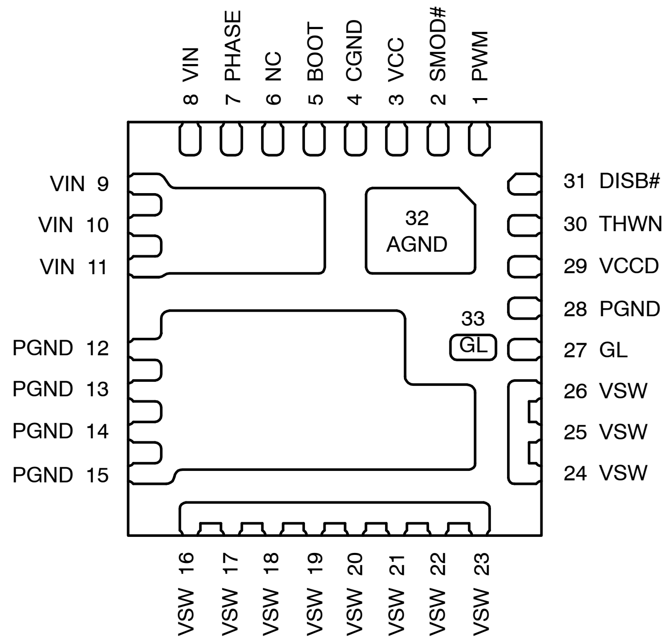



**Figure 3. Pinout Diagram**

**Table 1. PIN LIST AND DESCRIPTION**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | PWM | PWM Control Input and Zero Current Detection Enable: When DISB# = Low, the internal resistor divider will always be disconnected regardless SMOD# status. |
| 2 | SMOD# | Skip Mode pin. 3–state input (see Table 6):<br>SMOD# = High → State of PWM determine whether the NCP252163 performs ZCD or not.<br>SMOD# = Mid → Connects PWM to internal resistor divider placing a bias voltage on PWM pin. Otherwise, logic is equivalent to SMOD# in the high state.<br>SMOD# = Low → Placing PWM into mid−state pulls GH and GL low without delay.<br><br>There is an internal pull−up resistor to VCC on this pin |
| 3 | VCC | Control Power Supply Input |
| 4, 32 | CGND, AGND | Signal Ground (pin 4 and pad 32 are internally connected) |
| 5 | BOOT | Bootstrap Voltage |
| 6 | NC | Open pin (not used) |
| 7 | PHASE | Bootstrap Capacitor Return |
| 8–11 | VIN | Conversion Supply Power Input |
| 12–15, 28 | PGND | Power Ground |
| 16–26 | VSW | Switch Node Output |
| 27, 33 | GL | Low Side FET Gate Access (pin 27 and pad 33 are internally connected) |
| 29 | VCCD | Driver Power Supply Input |
| 30 | THWN | Thermal warning indicator. This is an open−drain output. When the temperature at the driver die reaches $T_{THWN}$, this pin is pulled low. |
| 31 | DISB# | Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull−down resistor on this pin. |

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Electrical Information – all signals referenced to PGND unless noted otherwise.)

| Pin Name / Parameter | Min | Max | Unit |
|---|---|---|---|
| VCC, VCCD | –0.3 | 6.5 | V |
| VIN | –0.3 | 25 | V |
| BOOT (DC) | –0.3 | 30 | V |
| BOOT (< 20 ns) | –0.3 | 35 | V |
| BOOT to PHASE (DC) | –0.3 | 6.5 | V |
| VSW, PHASE (DC) | –0.3 | 25 | V |
| VSW, PHASE (< 20 ns) | –5 | 30 | V |
| All Other Pins | –0.3 | $V_{VCC}$ + 0.3 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. THERMAL CHARACTERISTICS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance (under **onsemi** Thermal Board) | $\theta_{JA}$ | 12.4 | °C/W |
| | $\theta_{J-PCB}$ | 1.8 | °C/W |
| Operating Junction Temperature Range (Note 1) | $T_J$ | –40 to +150 | °C |
| Operating Ambient Temperature Range | $T_A$ | –40 to +125 | °C |
| Maximum Storage Temperature Range | $T_{STG}$ | –55 to +150 | °C |
| Moisture Sensitivity Level | MSL | 1 | |

1. The maximum package power dissipation must be observed.
2. JESD 51–5 (1S2P Direct–Attach Method) with 0 LFM.
3. JESD 51–7 (1S2P Direct–Attach Method) with 0 LFM.

**Table 4. RECOMMENDED OPERATING RANGES**

| Parameter | Pin Name | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage Range | VCC, VCCD | | 4.5 | 5.0 | 5.5 | V |
| BOOT to PHASE | $V_{BOOT-PHASE}$ | | 4.1 | 4.6 | 5.1 | V |
| Conversion Voltage | VIN | | 4.5 | 12 | 16 | V |
| Continuous Output Current | | $F_{SW}$ = 1 MHz, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.0 V, $T_A$ = 25°C | – | – | 55 | A |
| | | $F_{SW}$ = 300 kHz, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.0 V, $T_A$ = 25°C | – | – | 60 | A |
| Peak Output Current | | Duration = 5 μs, Period = 10 ms | – | – | 85 | A |
| Junction Temperature | | | –40 | – | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 5. ELECTRICAL CHARACTERISTICS**

($V_{VCC}$ = $V_{VCCD}$ = 5.0 V, $V_{VIN}$ = 12 V, $V_{DISB\#}$ = 2.0 V, $C_{VCCD}$ = $C_{VCC}$ = 0.1 F unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Operating | | DISB# = 5 V, PWM = 400 kHz | – | 1 | 2 | mA |
| No switching | | DISB# = 5 V, PWM = 0 V | – | – | 2 | mA |
| Disabled | | DISB# = 0 V, SMOD# = VCC | – | 0.4 | 1 | μA |
| | | DISB# = 0 V, SMOD# = GND | – | 6 | 15 | μA |
| UVLO Start Threshold | $V_{UVLO}$ | VCC rising | 2.89 | – | 3.37 | V |
| UVLO Hysteresis | | | 150 | – | – | mV |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($V_{VCC}$ = $V_{VCCD}$ = 5.0 V, $V_{VIN}$ = 12 V, $V_{DISB\#}$ = 2.0 V, $C_{VCCD}$ = $C_{VCC}$ = 0.1 F unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCCD SUPPLY CURRENT** | | | | | | |
| Enabled, No Switching | | DISB# = 5 V, PWM = 0 V | – | 175 | 300 | μA |
| Disabled | | DISB# = 0 V | – | 0.4 | 1 | μA |
| Operating | | DISB# = 5 V, PWM = 400 kHz | – | – | 30 | mA |
| **DISB# INPUT** | | | | | | |
| Input Resistance | | To Ground | – | 467 | – | kΩ |
| Upper Threshold | $V_{UPPER}$ | | – | – | 2.0 | V |
| Lower Threshold | $V_{LOWER}$ | | 0.8 | – | – | V |
| Hysteresis | | $V_{UPPER}$ − $V_{LOWER}$ | 200 | – | – | mV |
| Enable Delay Time | | Time from DISB# transitioning HI to when VSW responds to PWM. | – | – | 50 | μs |
| Disable Delay Time | | Time from DISB# transitioning LOW to when both output FETs are off. | – | 21 | 50 | ns |
| **SMOD# INPUT** | | | | | | |
| SMOD# Input Voltage High | $V_{SMOD\_HI}$ | | 2.65 | – | – | V |
| SMOD# Input Voltage Mid−state | $V_{SMOD\#\_MID}$ | | 1.4 | – | 2.0 | V |
| SMOD# Input Voltage Low | $V_{SMOD\_LO}$ | | – | – | 0.7 | V |
| SMOD# Input Resistance | $R_{SMOD\#\_DOWN}$ | Pull−up resistance to VCC | – | 455 | – | kΩ |
| SMOD# Propagation Delay, Falling | $T_{SMOD\#\_PD\_F}$ | SMOD# = Low to GL = 90%, PWM = MID | – | 34 | 42 | ns |
| SMOD# Propagation Delay, Rising | $T_{SMOD\#\_PD\_R}$ | SMOD# = High to GL = 10%, PWM = MID | – | 22 | 30 | ns |
| **PWM INPUT** | | | | | | |
| Input Voltage High | $V_{PWM\_HI}$ | | 2.65 | – | – | V |
| Input Mid−State Voltage | $V_{PWM\_MID}$ | | 1.4 | – | 2.1 | V |
| Input Low Voltage | $V_{PWM\_LO}$ | | – | – | 0.7 | V |
| Input Resistance | $R_{PWM\_HIZ}$ | SMOD# = $V_{SMOD\#\_LO}$ or $V_{SMOD\#\_HI}$ | 10 | – | – | MΩ |
| Input Resistance | $R_{PWM\_BIAS}$ | SMOD# = $V_{SMOD\#\_MID}$ | – | 68 | – | kΩ |
| PWM Input Bias Voltage | $V_{PWM\_BIAS}$ | SMOD# = $V_{SMOD\#\_MID}$ | – | 1.7 | – | V |
| Non−overlap Delay, Leading Edge | $T_{NOL\_L}$ | GL Falling = 1 V to Gh−VSW Rising = 1 V | – | 13 | – | ns |
| Non−overlap Delay, Trailing Edge | $T_{NOL\_T}$ | GH−VSW Falling = 1 V to GL Rising = 1 V | – | 12 | – | ns |
| PWM Propagation Delay, Rising | $T_{PWM,PD\_R}$ | PWM = High to GL = 90% | – | 13 | 35 | ns |
| PWM Propagation Delay, Falling | $T_{PWM,PD\_F}$ | PWM = Low to SW = 90% | – | 47 | 52 | ns |
| Exiting PWM Mid−state Propagation Delay, Mid−to−Low | $T_{PWM\_EXIT\_L}$ | PWM = Mid−to−Low to GL = 10% | – | 14 | 25 | ns |
| Exiting PWM Mid−state Propagation Delay, Mid−to−High | $T_{PWM\_EXIT\_H}$ | PWM = Mid−to−High to SW = 10% | – | 13 | 25 | ns |
| **ZCD FUNCTION** | | | | | | |
| Zero Cross Detect Threshold | $V_{ZCD}$ | | – | −6 | – | mV |
| ZCD Blanking + Debounce Time | $t_{BLNK}$ | | – | 330 | – | ns |
| **THERMAL WARNING** | | | | | | |
| Thermal Warning Temperature | $T_{THWN}$ | Temperature at Driver Die | – | 150 | – | °C |
| Thermal Warning Hysteresis | $T_{THWN\_HYS}$ | | – | 15 | – | °C |
| Thermal Shutdown Temperature | $T_{THDN}$ | Temperature at Driver Die | – | 180 | – | °C |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($V_{VCC}$ = $V_{VCCD}$ = 5.0 V, $V_{VIN}$ = 12 V, $V_{DISB\#}$ = 2.0 V, $C_{VCCD}$ = $C_{VCC}$ = 0.1 F unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **THERMAL WARNING** | | | | | | |
| Thermal Shutdown Hysteresis | $T_{THDN\_HYS}$ | | – | 25 | – | °C |
| THWM Open Drain Current | $I_{THWN}$ | | – | – | 5 | mA |
| **BOOST STRAP DIODE** | | | | | | |
| Forward Voltage | | Forward Bias Current = 2.0 mA | – | 300 | – | mV |
| **LOW−SIDE DRIVER** | | | | | | |
| Output Impedance, Sourcing | $R_{SOURCE\_GL}$ | Source Current = 100 mA | – | 0.9 | – | Ω |
| Output Impedance, Sinking | $R_{SINK\_GL}$ | Sink Current = 100 mA | – | 0.4 | – | Ω |
| GL Rise Time | $T_{R\_GL}$ | GL = 10% to 90% | – | 27 | – | ns |
| GL Fall Time | $T_{F\_GL}$ | GL = 90% to 10% | – | 13 | – | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 6. LOGIC TABLE**

| INPUT TRUTH TABLE | | | | |
|---|---|---|---|---|
| **DISB#** | **PWM** | **SMOD# (Note 4)** | **GH (not a pin)** | **GL** |
| L | X | X | L | L |
| H | H | X | H | L |
| H | L | X | L | H |
| H | MID | H or MID | L | ZCD (Note 5) |
| H | MID | L | L | L (Note 6) |

4. PWM input is driven to mid−state with internal divider resistors when SMOD# is driven to mid−state and PWM input is undriven externally.
5. GL goes low following 80 ns de−bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
6. There is no delay before GL goes low.

## TYPICAL PERFORMANCE CHARACTERISTICS

(Test Conditions: $V_{IN}$ = 12 V, $V_{CC}$ = $P_{VCC}$ = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH, $T_A$ = 25°C and natural convection cooling, unless otherwise noted)

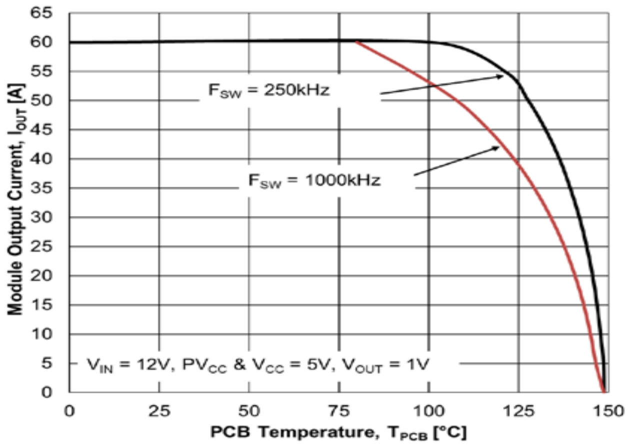



**Figure 4. Safe Operating Area with 12 $V_{IN}$**

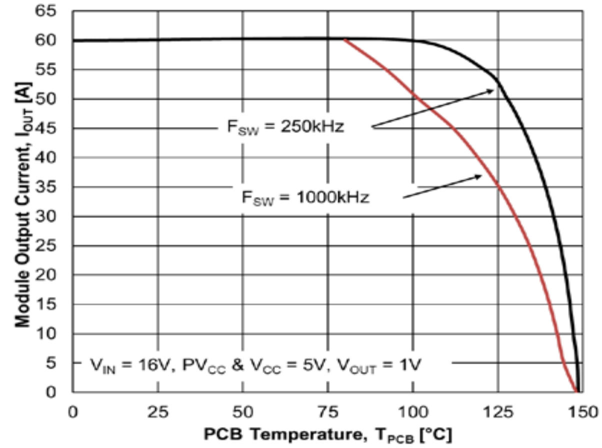



**Figure 5. Safe Operating Area with 16 $V_{IN}$**

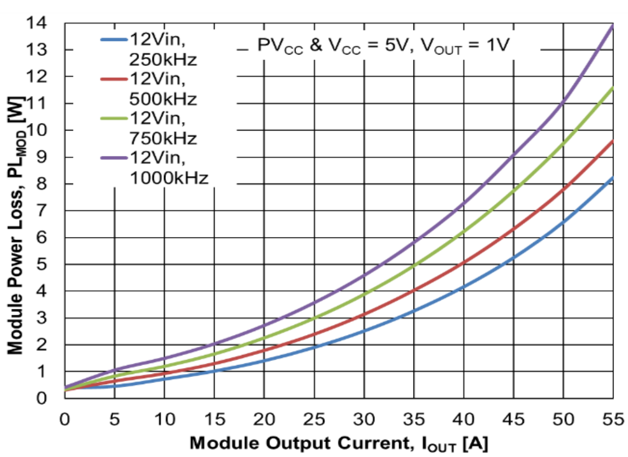



**Figure 6. Power Loss vs. Output Current with 12 $V_{IN}$**

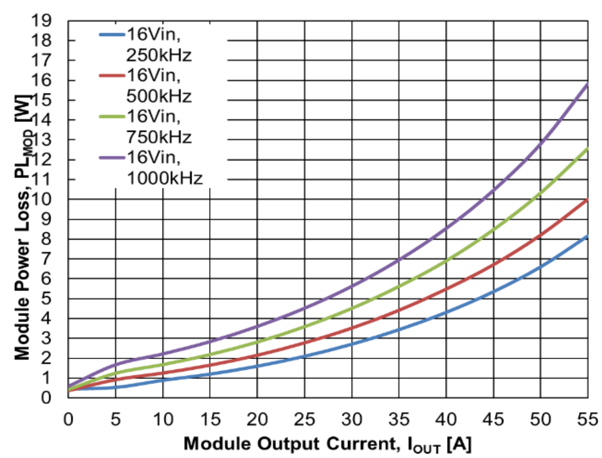



**Figure 7. Power Loss vs. Output Current with 16 $V_{IN}$**

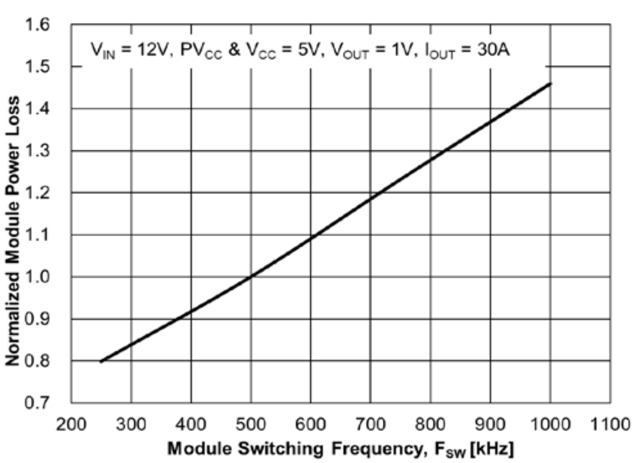



**Figure 8. Power Loss vs. Switching Frequency**

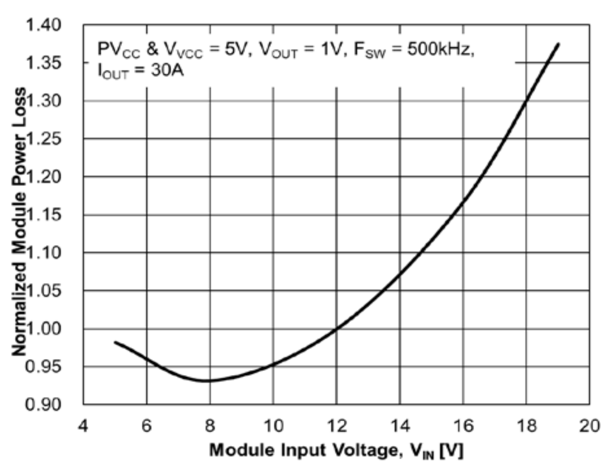



**Figure 9. Power Loss vs. Input Voltage**

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(Test Conditions: $V_{IN}$ = 12 V, VCC = $P_{VCC}$ = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH, $T_A$ = 25°C and natural convection cooling, unless otherwise noted)

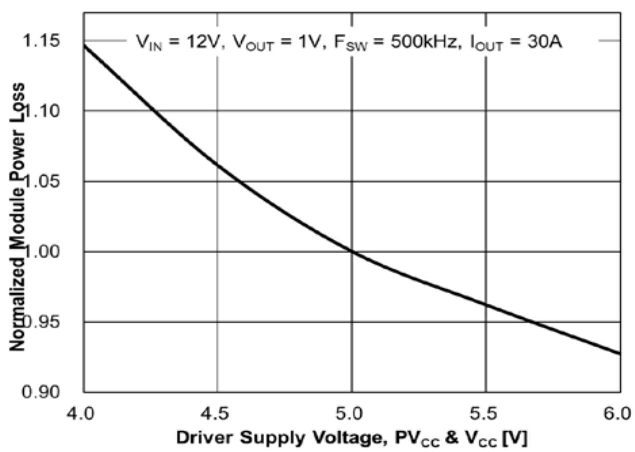



Figure 10. Power Loss vs. Driver Supply Voltage

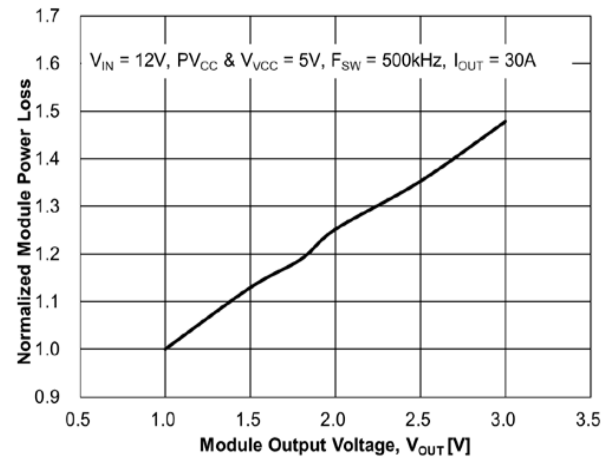



Figure 11. Power Loss vs. Output Voltage

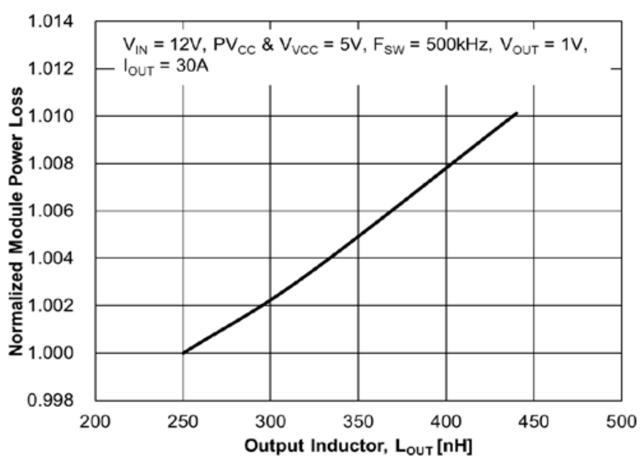



Figure 12. Power Loss vs. Output Inductor

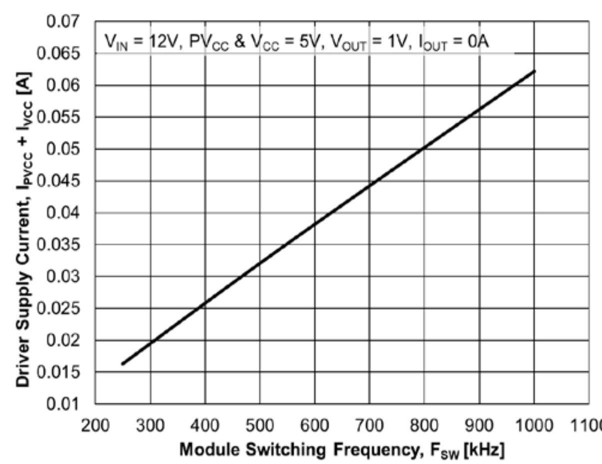



Figure 13. Driver Supply Current vs. Switching Frequency

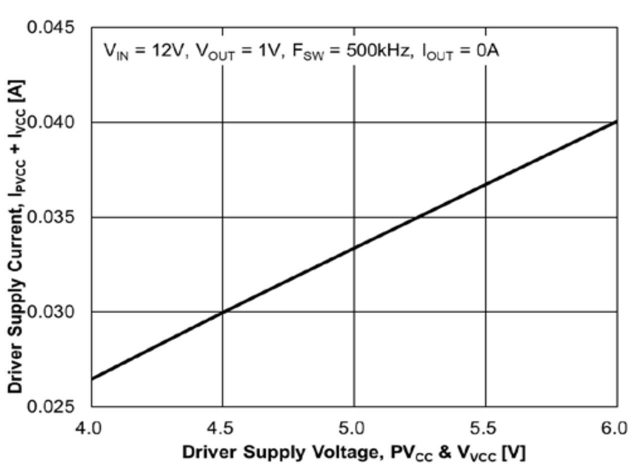



Figure 14. Driver Supply Current vs. Driver Supply Voltage

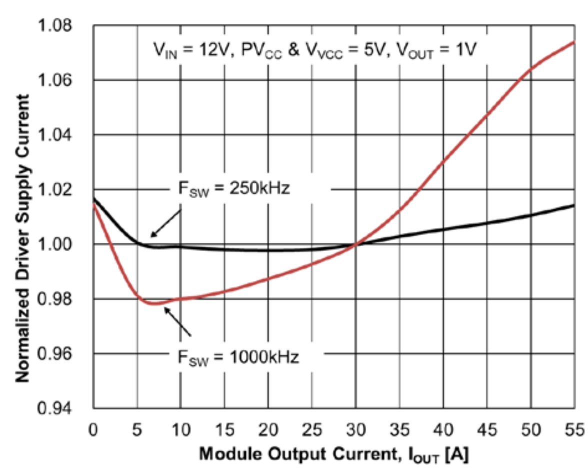



Figure 15. Driver Supply Current vs. Output Current

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(Test Conditions: $V_{IN}$ = 12 V, VCC = $P_{VCC}$ = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH, $T_A$ = 25°C and natural convection cooling, unless otherwise noted)

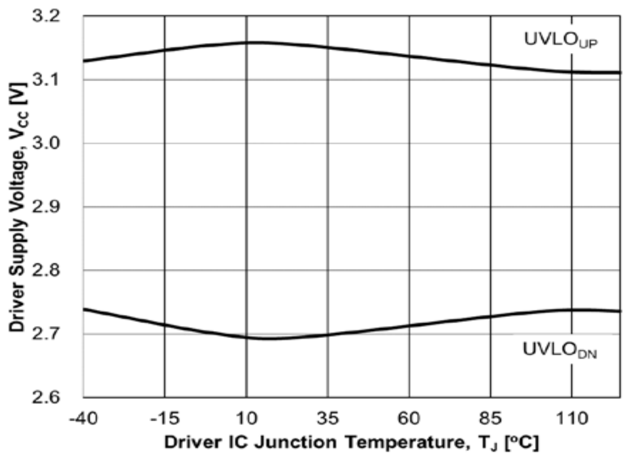



Figure 16. UVLO Threshold vs. Temperature

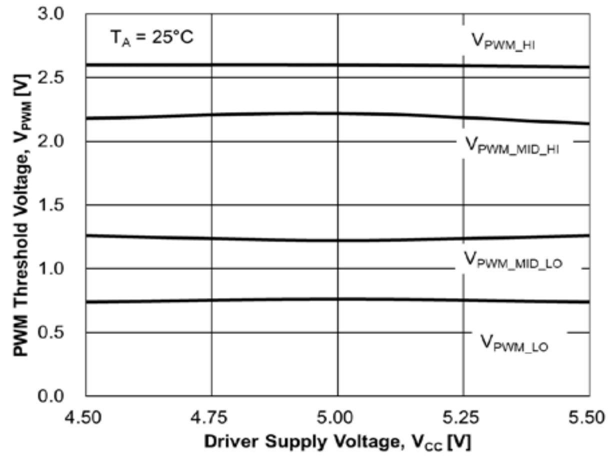



Figure 17. PWM Threshold vs. Driver Supply Voltage

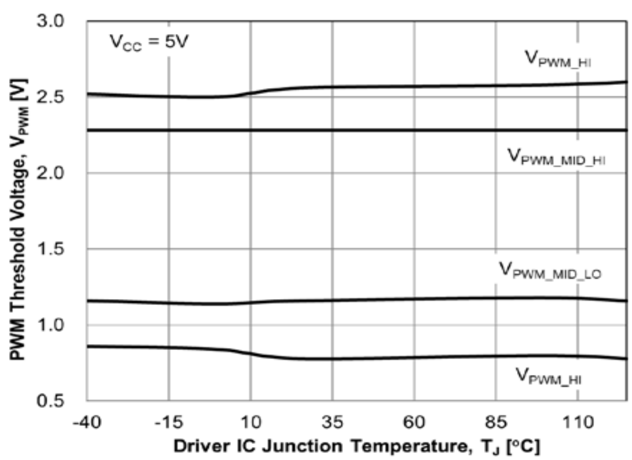



Figure 18. PWM Threshold vs. Temperature

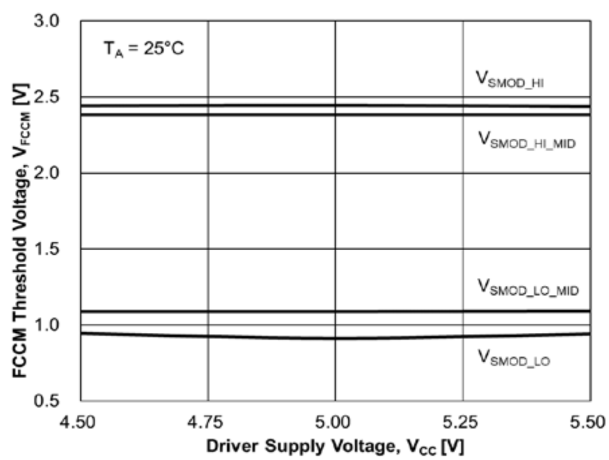



Figure 19. SMOD Threshold vs. Driver Supply Voltage

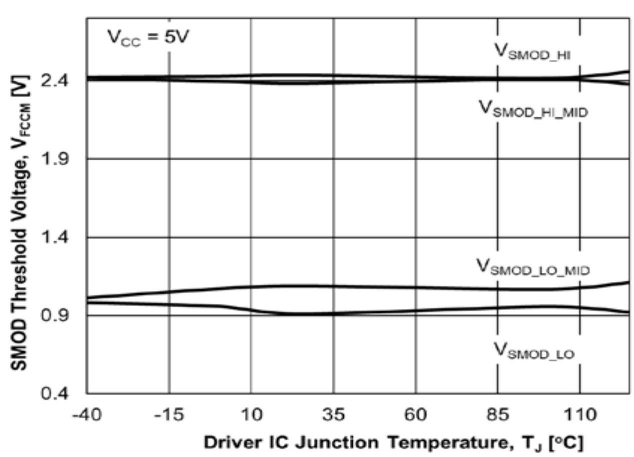



Figure 20. FCCM Threshold vs. Temperature

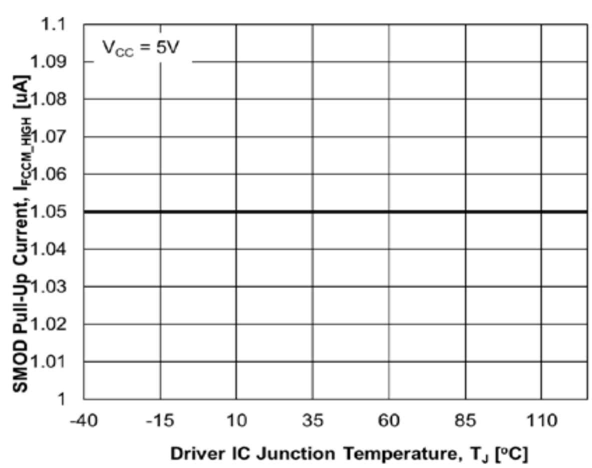



Figure 21. FCCM Pull−Up Current vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(Test Conditions: $V_{IN}$ = 12 V, VCC = $P_{VCC}$ = 5 V, $V_{OUT}$ = 1 V, $L_{OUT}$ = 250 nH, $T_A$ = 25°C and natural convection cooling, unless otherwise noted)

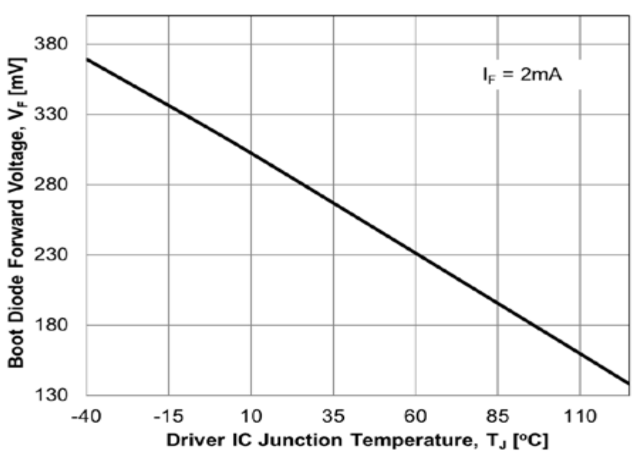



**Figure 22. Body Diode Forward Voltage vs. Temperature**

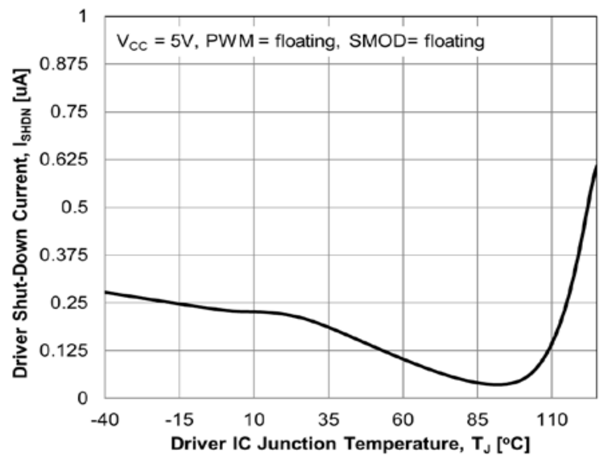



**Figure 23. Driver Shutdown vs. Temperature**

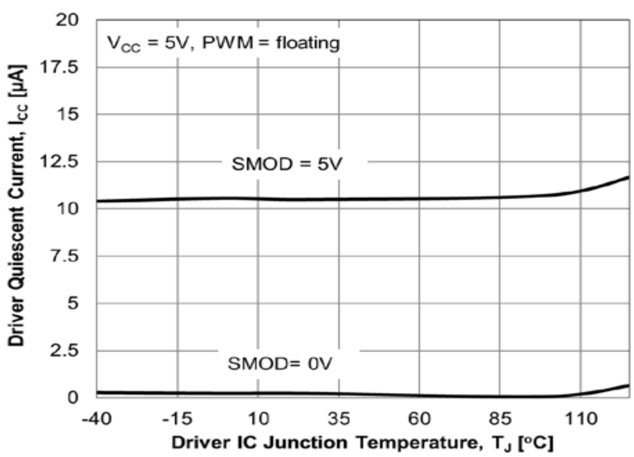



**Figure 24. Driver Quiescent Current vs. Temperature**

### Theory of Operation

The NCP252163 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP252163 supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

### Low−Side Driver

The low−side driver drives an internal, ground−referenced low−$R_{DS(on)}$ N−Channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCCD and PGND pins.

### High−Side Driver

The high−side driver drives an internal, floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSW and PHASE) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NCP252163 is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (See Figure 1). When the PWM input is driven high, the high−side driver turns on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the VSW and PHASE pins rises. When the high−side MOSFET is fully turned on, the switch node settles to VIN and the BST pin settles to VIN + VCCD − Vdiode (excluding parasitic ringing).

#### Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (CBST) and an integrated diode to provide current to the HS Driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the bootstrap capacitor. A 1 to 5 Ω resistor in series with the bootstrap capacitor can be used to decrease the VSW overshoot.

#### Power Supply Decoupling

The NCP252163 sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low−ESR capacitor should be placed near the power and ground pins. A multi−layer ceramic capacitor (MLCC) between 1 μF and 4.7 μF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 μF ceramic capacitor should be placed on this pin in close proximity to the NCP252163. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (2 − 10 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function (See Figure 1). It is recommended to connect the supply to VCCD and then VCC through the filter.

#### Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP252163 prevents cross−conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap (NOL) time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the gate of the low−side MOSFET (LSGATE) goes low after a propagation delay (TPWM_PD_R). The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate.

The NCP252163 monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer delays the turn−on of the high−side MOSFET. When the PWM input pin goes low, the gate of the high−side MOSFET (HSGATE) goes low after the propagation delay (TPWM_PD_F). The time to turn off the high−side MOSFET is dependent on the total gate charge of the high−side MOSFET. A timer is triggered once the high−side MOSFET stops conducting, to delay the turn−on of the low−side MOSFET.

#### Zero Current Detect

The Zero Current Detect PWM (ZCD_PWM) mode is enabled when SMOD# is HIGH or MID (see Tables 6 & 8).

With PWM set to > VPWM_HI, GL goes low and GH goes high after the non−overlap delay. When PWM is driven to < VPWM_HI and to > VPWM_LO, GL goes high after the non−overlap delay, and stays high for the duration of the ZCD blanking timer (TZCD_BLANK) and an 80 ns de−bounce timer. Once this timer expires, VSW is monitored for zero current detection, and GL is pulled low once zero current is detected. The threshold on VSW to determine zero current undergoes an auto−calibration cycle every time DISB# is brought from low to high. This auto−calibration cycle typically takes 25 μs to complete.

#### PWM Input

The PWM Input pin is a tri−state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. See Table 6 for logic operation. The PWM in some cases must operate with frequency programming resistances to ground. These resistances can range from 10 kΩ to 300 kΩ depending on the application. When SMOD# is set to > VSMOD#_HI or to < VSMOD#_LO, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin.

If SMOD# is set to < VSMOD#_HI and > VSMOD#_LO (Mid−State), the PWM pin undriven default voltage is set to Mid−State with internal divider resistances.

#### Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

**Table 7. UVLO/DISB# LOGIC TABLE**

| UVLO | DISB# | Driver State |
|---|---|---|
| L | X | Disabled (GH = GL = 0) |
| H | L | Disabled (GH = GL = 0) |
| H | H | Enabled (See Table 1) |
| H | Open | Disabled (GH = GL = 0) |

#### VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). A VCC voltage above the rising threshold enables the NCP252163.

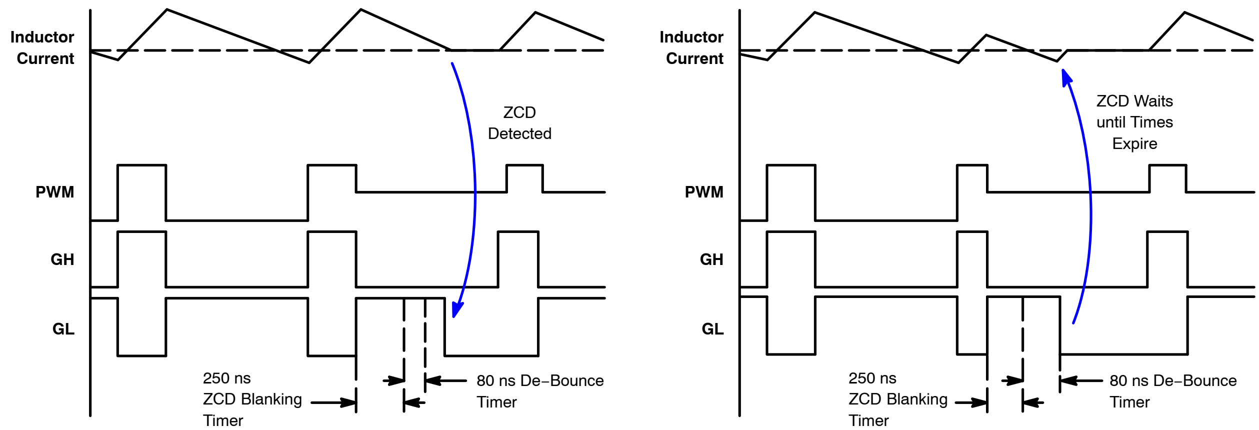
#### Thermal Warning

The THWN pin is an open drain output. When the temperature of the driver exceeds $T_{THWN}$, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops $T_{THWN\_HYS}$ below $T_{THWN}$, the THWN pin goes high. If the driver temperature exceeds $T_{THDN}$, the part enters thermal shutdown and turns off both MOSFETs. Once the temperature falls $T_{THDN\_HYS}$ below $T_{THDN}$, the part resumes normal operation.

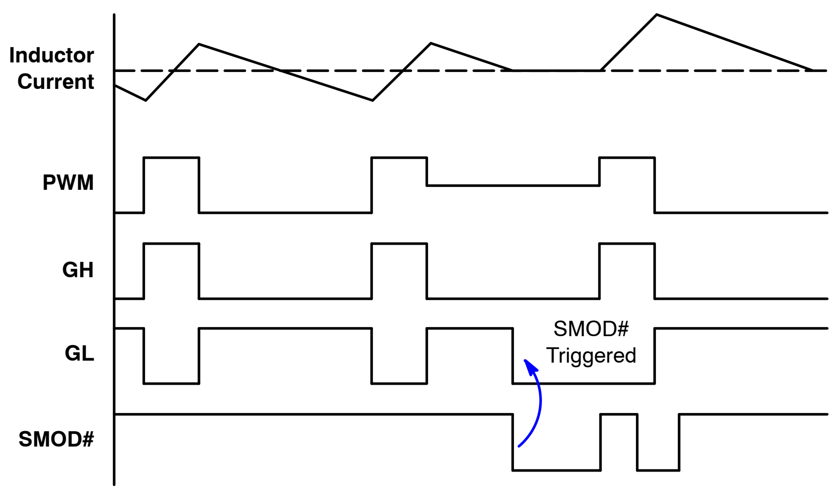
### Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven low, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low while PWM is in the mid−state, the low side MOSFET can be disabled to allow discontinuous mode operation.

The NCP252163 has the capability of internally connecting a resistor divider to the PWM pin. To engage ZCD, SMOD# needs to be placed into mid−state or high. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.




NOTE: If the Zero Current Detect circuit detects zero current after the ZCD Wait timer period, the GL is driven low by the Zero Current Detect signal.
If the Zero Current Detect circuit detects zero current before the ZCD Wait timer period expires, the Zero Current detect signal is ignored and the GL is driven low at the end of the ZCD Wait timer period.




NOTE: If the SMOD# input is driven low at any time after the GL has been driven high, the SMOD# Falling edge triggers the GL to go low.
If the SMOD# input is driven low while the GH is high, the SMOD# input is ignored.

**Figure 25. SMOD# Timing Diagram**

**For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:**

**Table 8. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH NO ZCD**

| PWM | SMOD# | GH (Not a Pin) | GL |
|---|---|---|---|
| H | H or MID | ON | OFF |
| M | H or MID | OFF | ZCD |
| L | H or MID | OFF | ON |

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP252163 to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NCP252163 has an internal pull−down resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid−state.

Whenever PWM transitions to mid−state, GH turns off and GL turns on. GL stays on for the duration of the de−bounce timer and ZCD blanking timers. Once these timers expire, the NCP252163 monitors the SW voltage and turns GL off when SW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

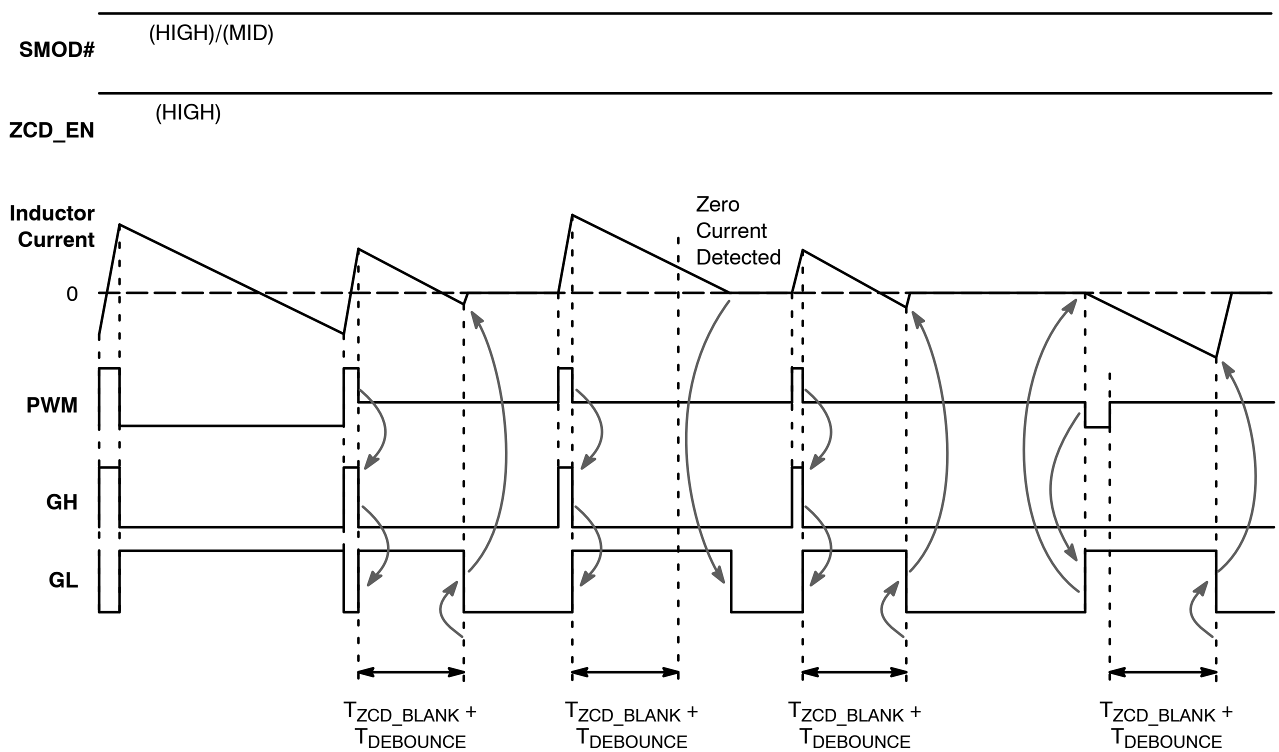



**Figure 26. Timing Diagram − 3−state PWM Controller, No ZCD**

**For Use with Controllers with 3−State PWM Controllers Detection Capability:**

**Table 9. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH ZCD**

| PWM | SMOD# | GH (Not a Pin) | GL |
|---|---|---|---|
| H | L | ON | OFF |
| M | L | OFF | OFF |
| L | L | OFF | ON |

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#\_LO}$).

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP252163 to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid−state, which causes the NCP252163 to pull both GH and GL to their off states without delay.

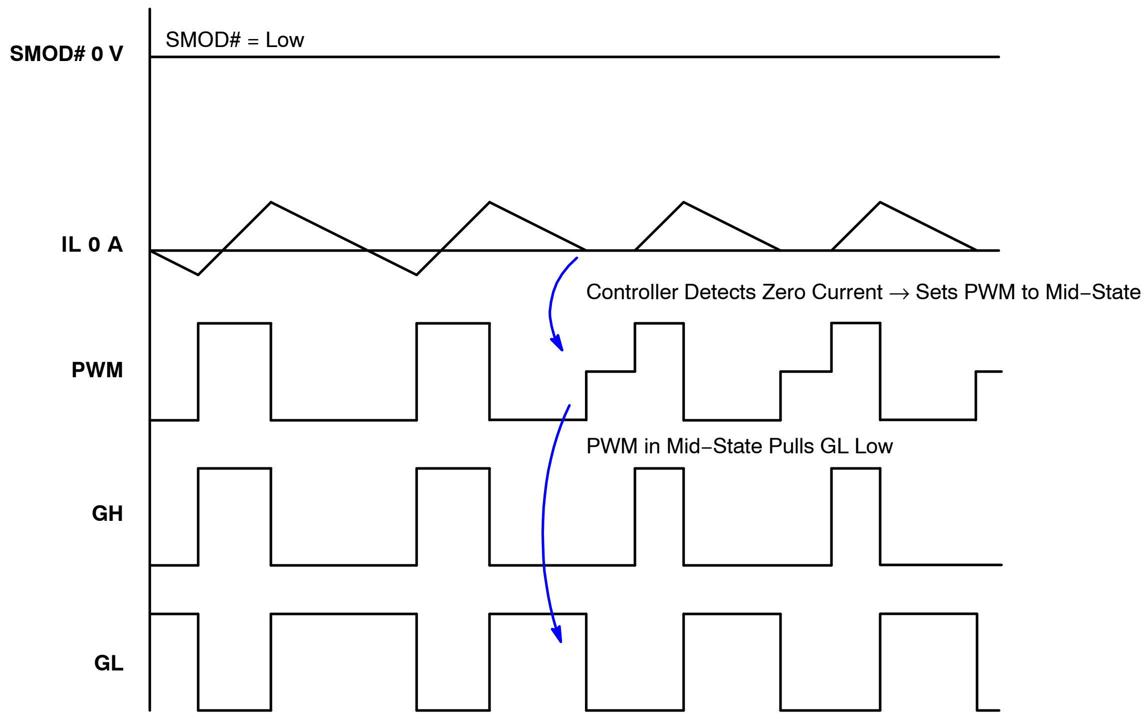



**Figure 27. Timing Diagram − 3−state PWM Controller, with ZCD**

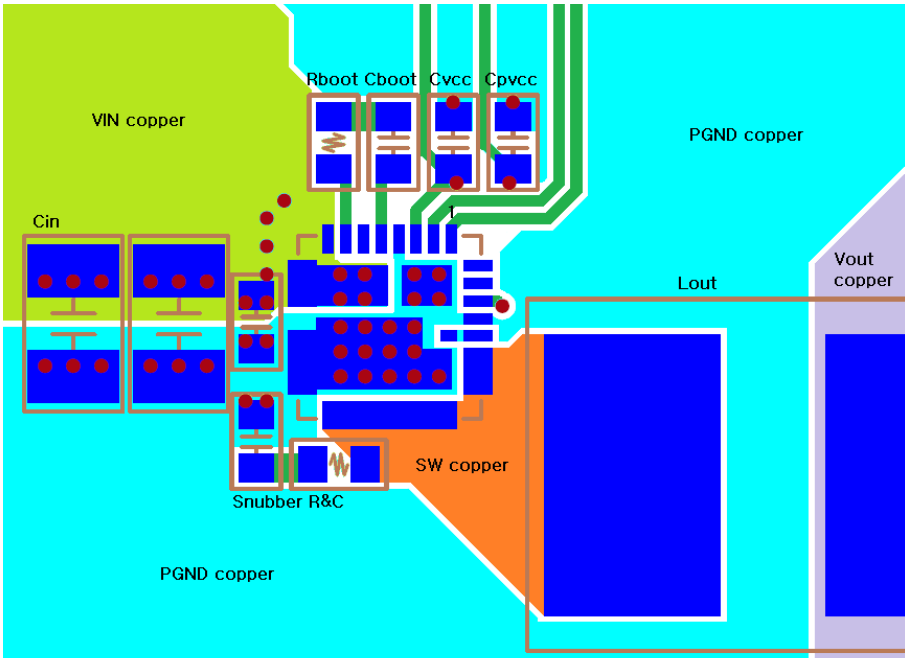



**Figure 28. Top Copper Layer**

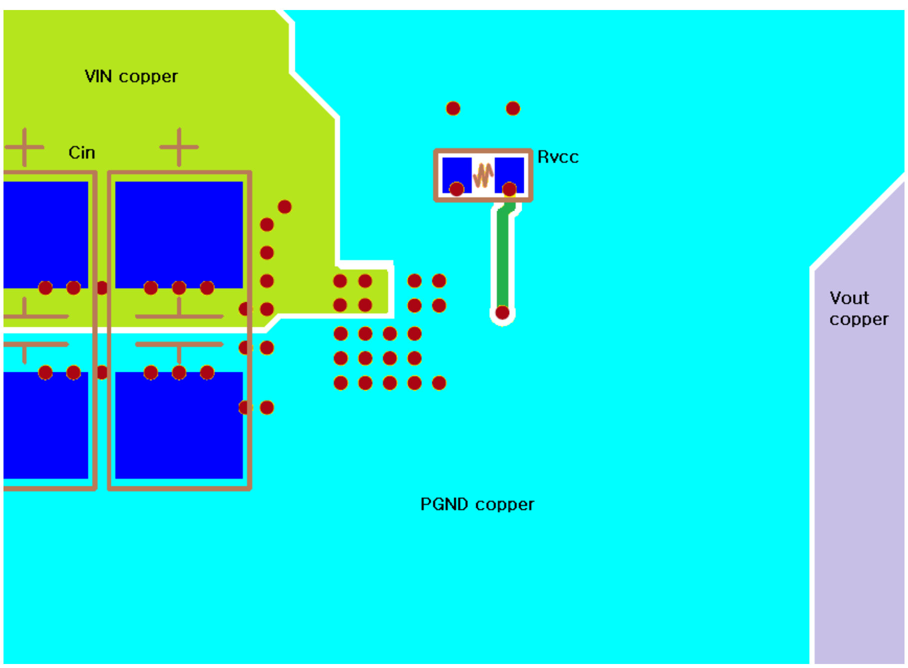



**Figure 29. Bottom Copper Layer**

**RECOMMENDED PCB FOOTPRINT**
**(OPTION 1)**

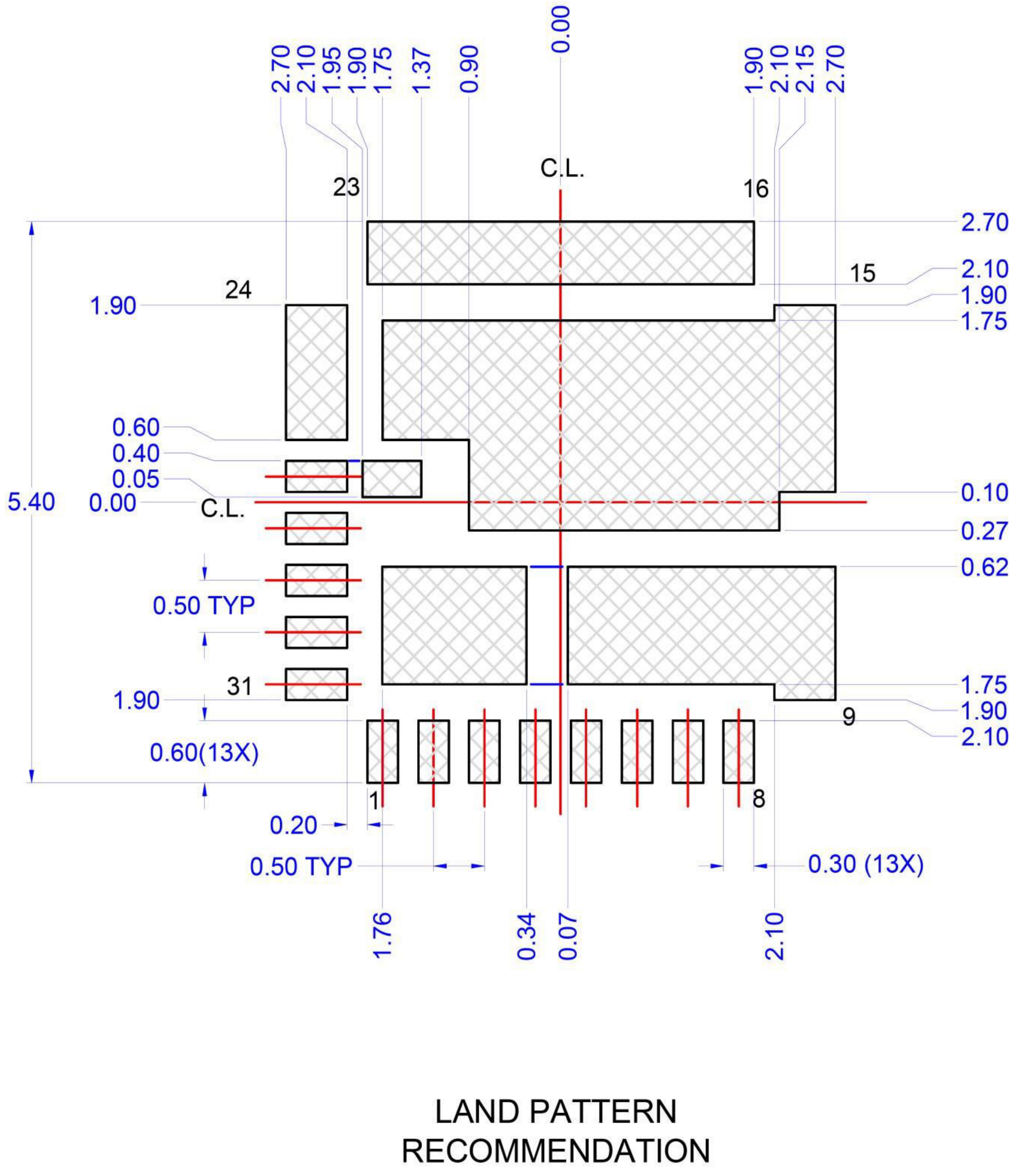



**Figure 30. Recommended PCB Footprint (Option 1)**

## RECOMMENDED PCB FOOTPRINT (OPTION 2)

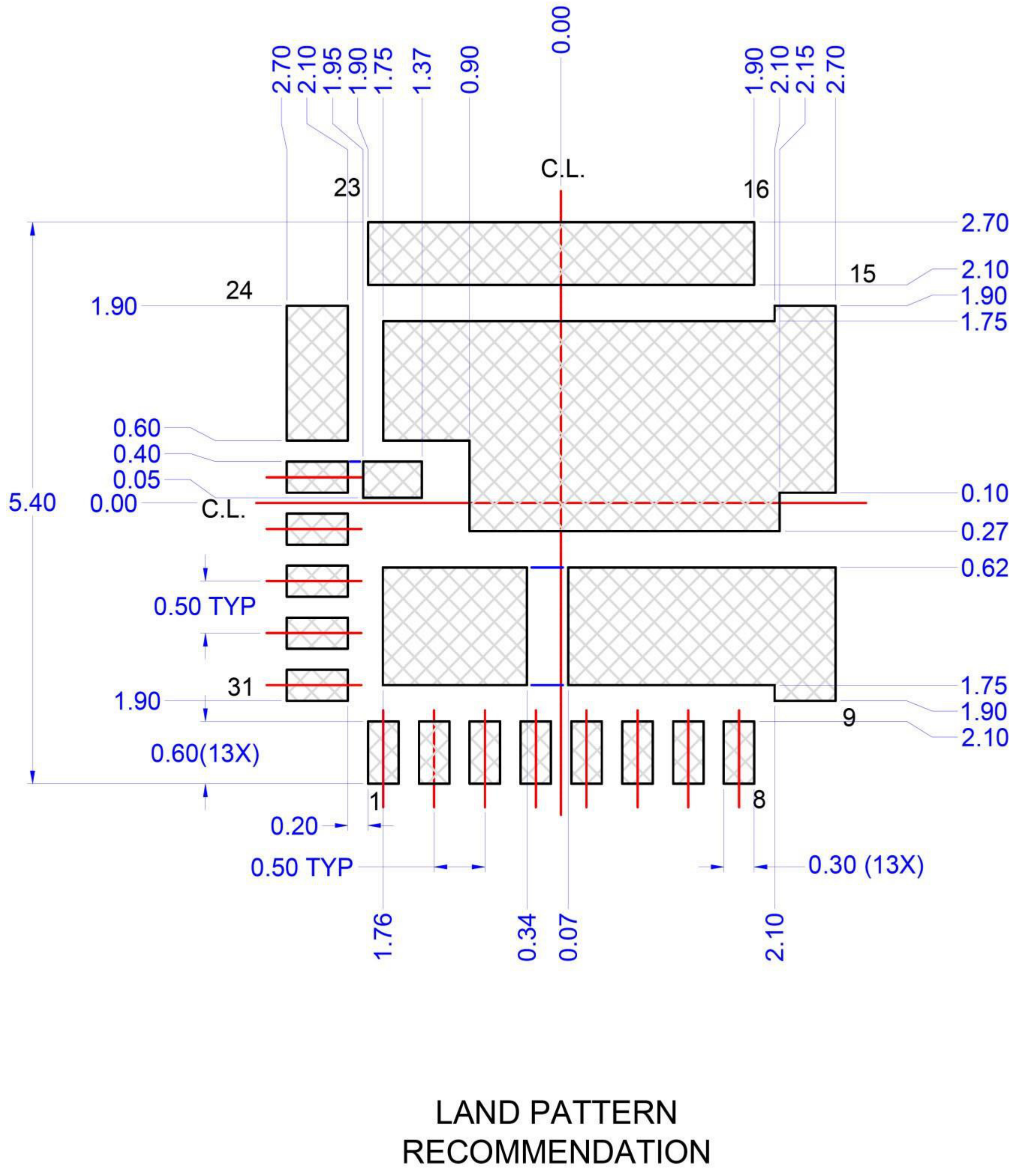
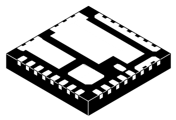



**Figure 31. Recommended PCB Footprint (Option 2)**

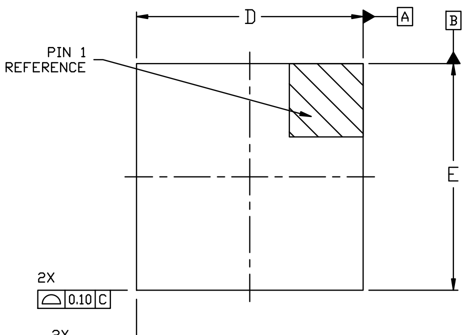
Intel and the Intel logo are trademarks of Intel Corporation or its subsidiaries.



SCALE 2.5:1

**PQFN31 5X5, 0.5P**
CASE 483BR
ISSUE D

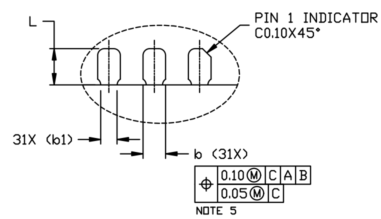
DATE 13 FEB 2023



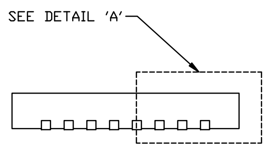

TOP VIEW

NOTES:

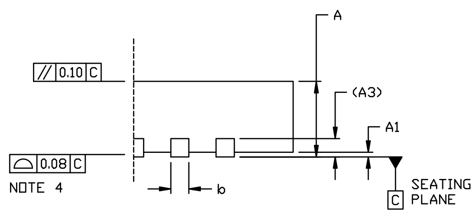
1. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, DATES MAY/2005.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS
4. DIMENSIONS DO NOT INCLUDE BURRS AND SMEAR OR MOLD FLASH.
   MOLD FLASH OR BURRS AND SMEAR DO NOT EXCEED 0.10MM.
5. DIMENSION b AND B1 APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.



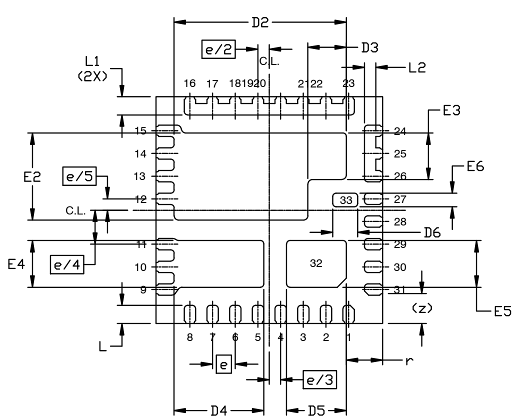

DETAIL 'B'
(SCALE 2:1)



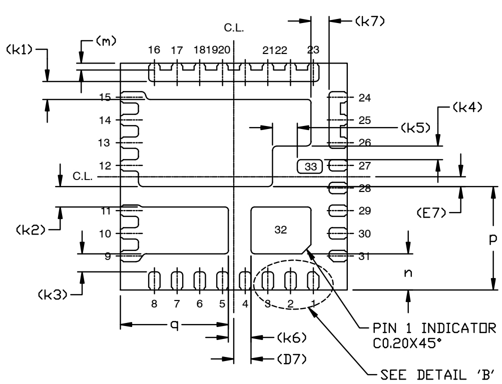

SIDE VIEW




DETAIL 'A'
(SCALE 2:1)




BOTTOM VIEW



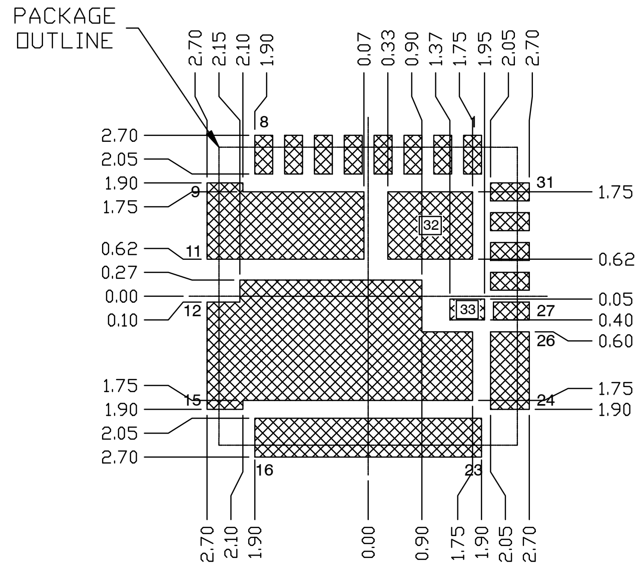

SUPPLEMENTAL
BOTTOM VIEW

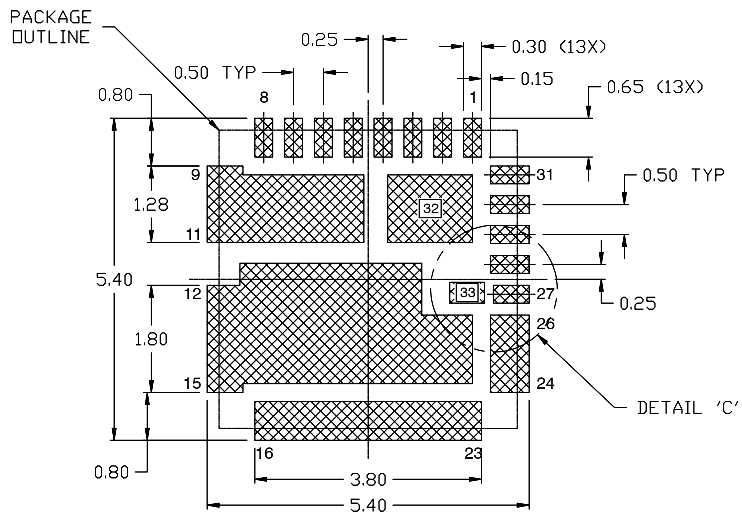
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | – | 0.05 |
| A3 | 0.15 | 0.20 | 0.25 |
| b | 0.20 | 0.25 | 0.30 |
| b1 | 0.13 | 0.18 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.70 | 3.80 | 3.90 |
| D3 | 0.75 | 0.85 | 0.95 |
| D4 | 1.88 | 1.98 | 2.08 |
| D5 | 1.22 | 1.32 | 1.42 |
| D6 | 0.45 | 0.55 | 0.65 |
| D7 | 0.38 REF | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 1.82 | 1.92 | 2.02 |
| E3 | 0.93 | 1.03 | 1.13 |
| E4 | 0.93 | 1.03 | 1.13 |
| E5 | 0.93 | 1.03 | 1.13 |
| E6 | 0.20 | 0.30 | 0.40 |
| E7 | 0.22 REF | | |
| e | 0.50 BSC | | |
| e/2 | 0.25 BSC | | |
| e/3 | 0.25 BSC | | |
| e/4 | 0.75 BSC | | |
| e/5 | 0.25 BSC | | |
| k1 | 0.40 REF | | |
| k2 | 0.45 REF | | |
| k3 | 0.40 REF | | |
| k4 | 0.30 REF | | |
| k5 | 0.55 REF | | |
| k6 | 0.50 REF | | |
| k7 | 0.40 REF | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.30 | 0.40 | 0.50 |
| L2 | 0.15 | 0.25 | 0.35 |
| m | 0.15 REF | | |
| n | 0.80 REF | | |
| p | 2.28 REF | | |
| q | 2.38 REF | | |
| r | 0.80 REF | | |
| z | 0.625 REF | | |

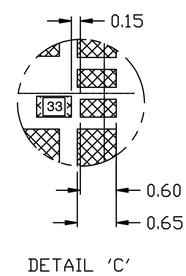
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13680G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **PQFN31 5X5, 0.5P** | **PAGE 1 OF 2** |

**PQFN31 5X5, 0.5P**
CASE 483BR
ISSUE D

DATE 13 FEB 2023




RECOMMENDED MOUNTING FOOTPRINT*
(2X SCALE)

* For additional information on our Pb-Free strategy and soldering details, please download the ONSEMI Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC**
**MARKING DIAGRAM***

XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13680G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **PQFN31 5X5, 0.5P** | **PAGE 2 OF 2** |

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative