VC-826

HCSL, LVPECL, LVDS Crystal Oscillator

Description

Vectron's VC-826 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off a 2.5 or 3.3 volt power supply in a hermetically sealed 3.2x2.5 mm ceramic package.

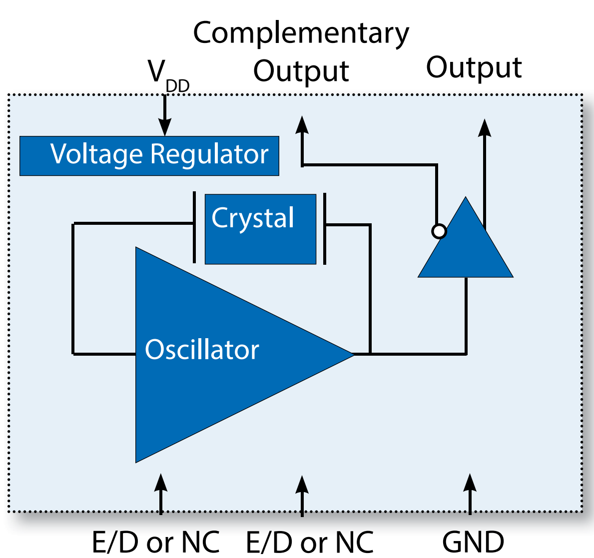
Features

- Ultra Low Jitter Performance, 3rd OT or Fundamental Crystal Design
- 20MHz -170MHz Output Frequencies
- Low Power
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 3.3 or 2.5V operation
- -10/70°C or -40/85°C Operation
- Hermetically Sealed 3.2x2.5 mm Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- Ethernet, GbE, Synchronous Ethernet
- Fiber Channel
- Enterprise Servers
- Telecom
- Clock source for A/D's, D/A's
- Driving FPGA's
- Test and Measurement
- PON
- Medical
- COTS

Block Diagram



Performance Specifications

Table 1. Electrical Performance, LVPECL Option

Parameter	Symbol	Min	Typical	Maximum	Units
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current[2], 3.3V 2.5V	I_{DD}			45 42	mA mA
Frequency					
Nominal Frequency	f_N	20		170	MHz
Stability[3] (Ordering Option)		±25, ±50 or ±100			ppm
Outputs					
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.025 V_{DD}-1.810		 V_{DD}-0.880 V_{DD}-1.620	 V V
Output Rise and Fall Time[2]	t_R/t_F			500	ps
Load		50 ohms into V_{DD}-1.3V			
Duty Cycle[4]		45		55	%
Phase Noise, 3.3V, 100MHz[5] 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 20MHz 40MHz			 -70 -100 -126 -140 -146 -149 -157 -157		 dBc/Hz
Jitter[5], 100MHz 12kHz -20MHz	 ϕJ		 170	 200	 fs
Enable/Disable					
Outputs Enabled[6] Outputs Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		3.2 x 2.5 x 1.05			mm

1. The VC-826 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 1 defines the test circuit and Figure 2 defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C.
6. Outputs will be Enabled if Enable/Disable is left open.

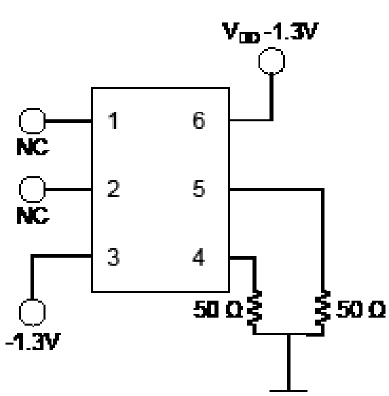


Figure 1.

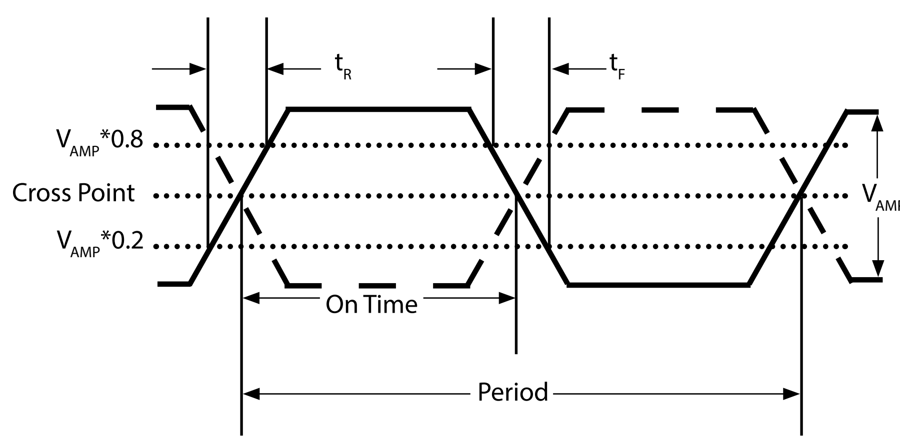


Figure 2.

Performance Specifications

Table 2. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
			Supply		
Voltage[1]	V_{DD}	3.135 2.375	3.3 2.5	3.465 2.625	V V
Current[2], 3.3V 2.5V	I_{DD}			17 14	mA mA
			Frequency		
Nominal Frequency	f_N	20		170	MHz
Stability[3] (Ordering Option)		±25, ±50 or ±100			ppm
			Outputs		
Output Logic Levels[2] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9	 1.43 1.10	 1.6	 V V
Output Amplitude		247	350	454	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current, Outputs Disabled				10	uA
Output Rise and Fall Time[3]	t_R/t_F			500	ps
Load		100 ohms differential			
Duty Cycle[4]		45		55	%
Phase Noise, 3.3V, 100MHz[5] 10Hz 100Hz 1kHz 10kHz 100kHz 1MHz 20MHz 40MHz			 -73 -101 -128 -140 -147 -150 -156 -156		 dBc/Hz
Jitter[5], 100MHz 12kHz - 20MHz	 ϕJ		 170	 200	 fs
			Enable/Disable		
Outputs Enabled[6] Outputs Disabled	V_{IH} V_{IL}	$0.7*V_{DD}$		 $0.3*V_{DD}$	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		3.2 x 2.5 x 1.05			mm

1. The VC-826 power supply pin should be filtered, eg, a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 2 defines these parameters and Figure 3 defines the test circuit.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On/Time Period.
5. Measured using an Agilent E5052 Signal Source Analyzer at 25 °C
6. Outputs will be Enabled if Enable/Disable is left open.

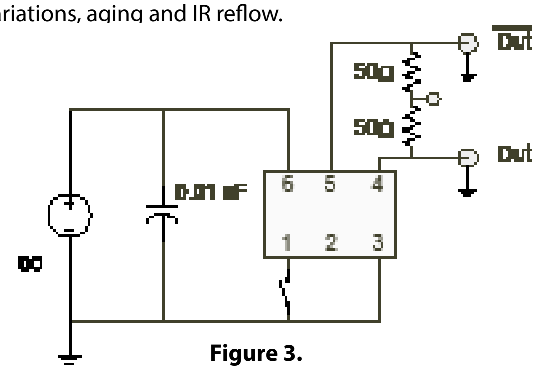


Figure 3.

Performance Specifications

Table 3. Electrical Performance, HCSL Output

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	2.375 3.165	2.5 3.3	2.625 3.465	V V
Current[2]	I_{DD}			39	mA
Frequency					
Nominal Frequency	f_N	13.5		170	MHz
Stability[3] (Ordering Options)		±25, ±50 or ±100			ppm
Outputs					
Output High, 3.3V Output High, 2.5V	V_{OH}	600 580		850 850	mV mV
Output Low	V_{OL}	-150		150	mV
Output Logic Swing, 3.3V Output Logic Swing, 2.5V	V_{OPP}	0.65 0.60			V V
Output Rise and Fall Time[3]	t_R/t_F			500	ps
Load		50 ohms to ground			
Duty Cycle[4]		45		55	%
Jitter[5] (12 kHz - 20 MHz) 100.000MHz	ϕJ			300	fs
Jitter[5], 100.000MHz	ϕJ	PCIe Gen1-Gen5 Compliant			
Enable/Disable					
Outputs Enabled[6] Outputs Disabled	V_{IH} V_{IL}	$0.7*V_{DD}$		 $0.3*V_{DD}$	V V
Disable Time	t_D			200	ns
Enable/Disable Leakage Current	$I_{E/D}$			±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		3.2 x 2.5 x 1.05			mm

1. The VC-826 power supply pin should be filtered, e.g., a 10uf, 0.1uf and 0.01uf capacitor.
2. Figure 4 defines the test circuit and Figure 5 defines these parameters.
3. Includes calibration tolerance, operating temperature, supply voltage variations, aging and IR reflow.
4. Duty Cycle is defined as the On Time/Period.
5. Measured using an Agilent E5052.
6. Outputs will be Enabled if the Enable/Disable pad is left open.

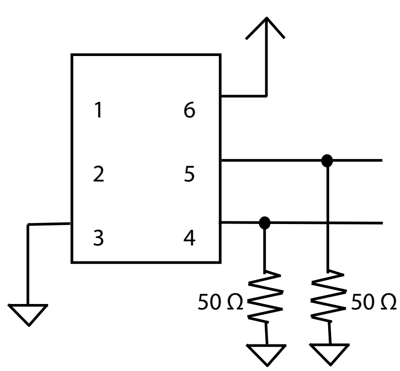


Figure 4.

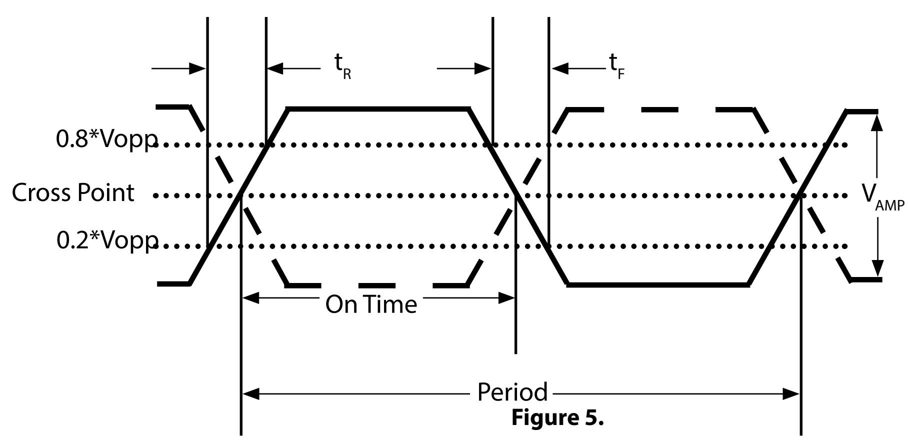
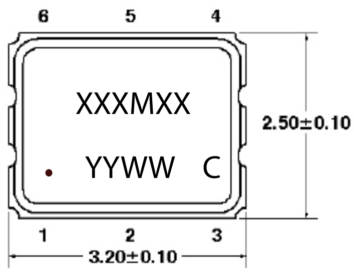
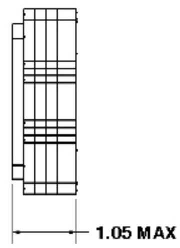


Figure 5.

Package Outline Drawing and Pad Layout





Marking Information

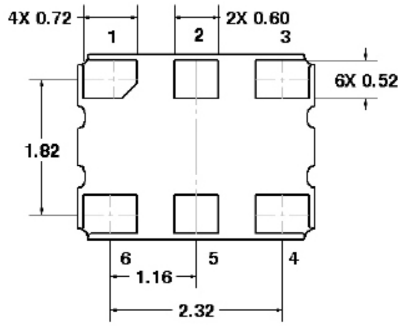
XXXMXX - Frequency (Example: 100M00)

YY - Year of Manufacture

WW - Week of the Year

C - Manufacturing Location

• - Pin 1 Indicator



Dimensions in mm

Table 4. Pinout

Pin #	Symbol	Function
1	E/D or NC	Enable/Disable or No Connection
2	E/D or NC	Enable/Disable or No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

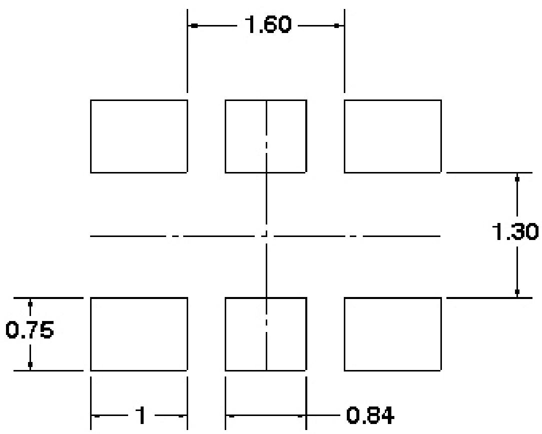
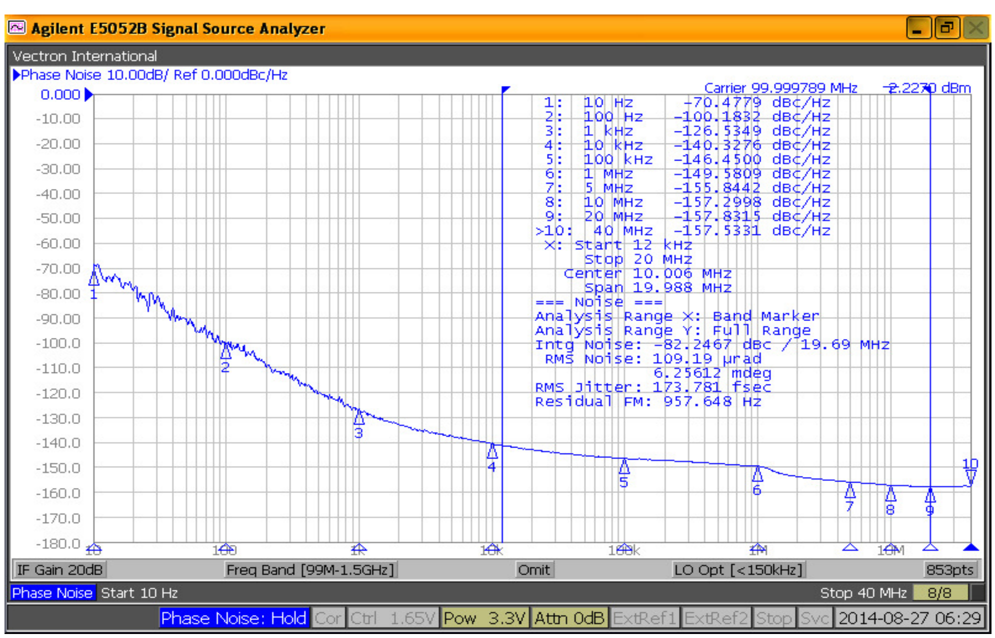


Table 5. Enable Disable Function

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

Phase Noise (LV-PECL Output)



LVPECL Application Diagrams

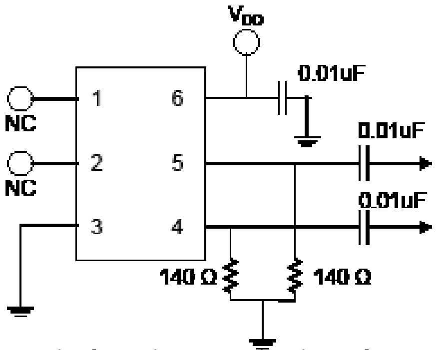


Figure 4. Single Resistor Termination Scheme
Resistor values are typically 140 ohms for 3.3V operation and 84 ohms for 2.5V operation.

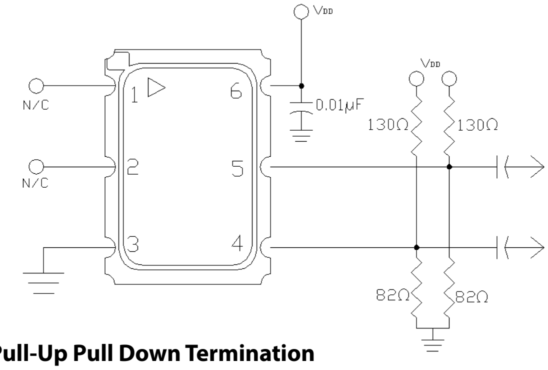


Figure 5. Pull-Up Pull Down Termination
Resistor values shown are typical for 3.3 V opertaion. For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 250 ohms

The VC-826 incorporates a standard PECL output scheme, which are un-terminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 4, or for best 50 ohm matching a pull-up/pull-down scheme as shown in Figure 5 should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

LVDS Application Diagrams

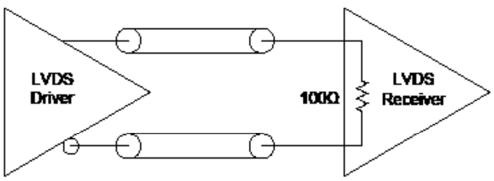


Figure 6. LVDS to LVDS Connection, Internal 100ohm Resistor
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

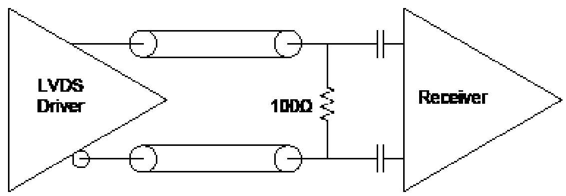


Figure 7. LVDS to LVDS Connection
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Environmental and IR Compliance

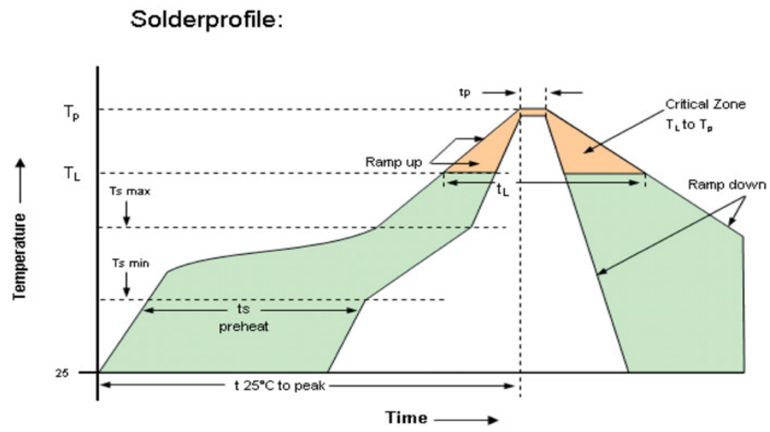
Table 6. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-202 Method 215
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3-1.0um) over Nickel
ThetaJC (bottom of case)	30 °C/W
Weight	25 mg

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 6. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 7. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	30 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



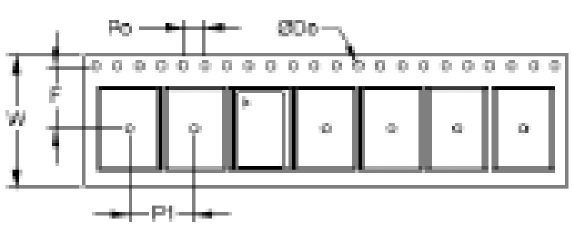
Maximum Ratings, Tape & Reel

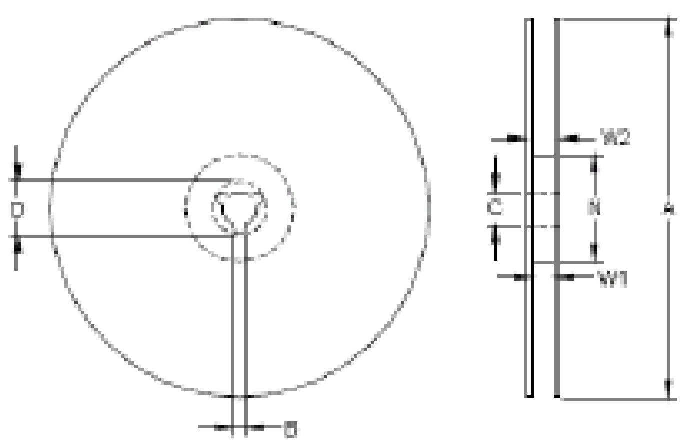
Absolute Maximum Ratings and Handling Precautions

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Although ESD protection circuitry has been designed into the VC-826, proper precautions should be taken when handling and mounting, Vectron employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 8. Maximum Ratings		
Parameter		Unit
Storage Temperature	-55 to 125	°C
Junction Temperature	150	C
Supply Voltage	-0.5 to 5.0	V
Enable Disable Voltage	-0.5 to V_{DD}+0.5	V
ESD, Human Body Model	1500	V
ESD, Charged Device Model	1500	V

Table 9. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
8	3.5	1.5	4	4	178	2	13	21	60	10	14	3000





Ordering Information

VC-826- E C E - K A A N - xxxMxxxxxxXX

Product
XO

Package
3.2x2.5mm

Voltage Options
E: +3.3 Vdc ±5%
H: +2.5 Vdc ±5%

Output
C: LVPECL
D: LVDS
H: HCSL

Temp Range
W: -10/70°C
E: -40/85°C

Packaging
TR: Tape and Reel
blank: Cut Tape / non Tape and Reel quantities
_SNPB: Tin lead solder dipped

Frequency in MHz

Other (Future Use)
N: Standard

Enable/Disable Pin
A: Pin 1 (Pin 2 = No Connection)
B: Pin 2 (Pin 1 = No Connection)

Enable/Disable Logic
A: Output is Enabled with a Logic High or open, Output is Disabled with a Logic Low

Stability
F: ±25ppm
K: ±50ppm
S: ±100ppm

Example:

VC-826-EDE-KAAN-125M000000TR	**Tape and Reel**
VC-826-EDE-KAAN-125M000000	**Cut Tape**
VC-826-EDE-KAAN-125M000000_SNPB	**Tin lead solder dipped**

Revision History

Revision Date	Approved	Description
Sep 05, 2014	VN	VC-826 Product Initial Release.
Dec 12, 2014	VN	Added min and max values for LVDS output amplitude.
Apr 27, 2016	VN	Updated LVDS 100MHz noise information and added maximum jitter numbers.
Aug 10, 2018	FB	Update logo and contact information, add SNPBDIP ordering option
May 10, 2019	FB	Update logo, comtact info and SNPB ordering optin
April 30, 2020	FB	Add tape and reel ordering option, add HCSL option, updates and corrections as needed

Contact Information

USA:

100 Watts Street
Mt Holly Springs, PA 17065
Tel: 1.717.486.3411
Fax: 1.717.486.5920

Europe:

Landstrasse
74924 Neckarbischofsheim
Germany
Tel: +49 (0) 7268.801.0
Fax: +49 (0) 7268.801.281