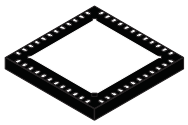
Document Number: MC34848
Rev. 1.0, 5/2010

8-Channel LED Driver with Differential Interface

MC34848

POWER MANAGEMENT IC



EP SUFFIX (PB-FREE)
98ARH99048A
48-PIN QFN

The 34848 is a high efficiency, 8-channel LED driver for use in LCD backlighting applications. It is designed to support up to 160 mA / channels in scan backlight mode, or 80 mA/channels in local dimming mode. Current reference is set using a single resistor to GND and LED current tolerance is accurate to ±1% channel-to-channel and IC-to-IC. The current can be programmed in both local dimming and scan modes.

Each channel has independent PWM control with 10-bit resolution, programmed with high speed differential interface. The frequency between ICs is synchronized and derived from Controller (LED Driver Controller) signals. When the SCAN pin is pulled high, it enables the Scan mode. In this mode, each of 8 channels is on for nominally 3/8 of the frame.

The integrated boost controller is used to generate the minimum output voltage required to keep all LEDs illuminated with the selected current, providing the highest efficiency possible. The integrated boost clock can be programmed from 200 kHz to 1.2 MHz.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34848EP	-40°C to 85°C	48 QFN EP

Features

- Drives 8 LED channels: ±1% current tolerance
- Local dimming mode, scan mode (2/8, 3/8, 4/8, 5/8), test mode
- Output voltage up to 45 V supporting up to 12 LEDs
- Auto drive voltage (V_{OUT}) selection: Minimum feedback voltage 500 mV for low power
- Differential Interface: Initial setup (LED current, f_{PWM}, OVP, etc.), PWM data in normal operation
- Integrated PLL for synchronization: 177 to 200 Hz in 1.0 Hz steps
- 10-bit PWM control per channel: Dimming ratio: >1000:1, turn-on time: <200 ns
- Pb-free packaging designated by suffix code EP”

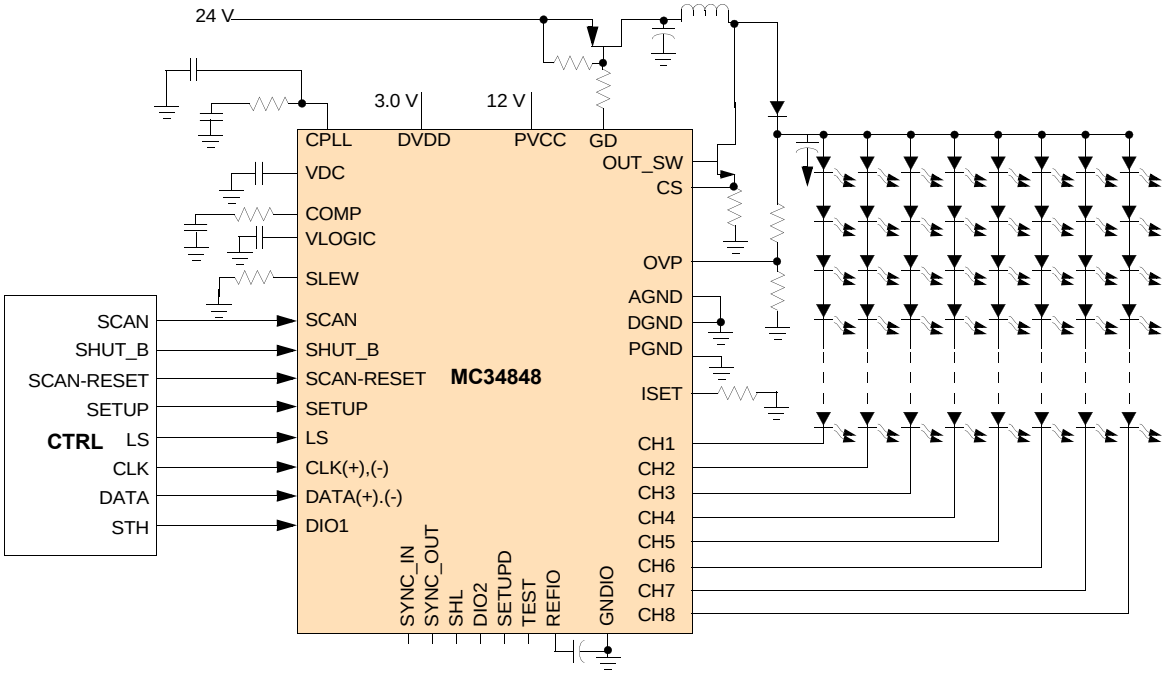


Figure 1. 34848 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

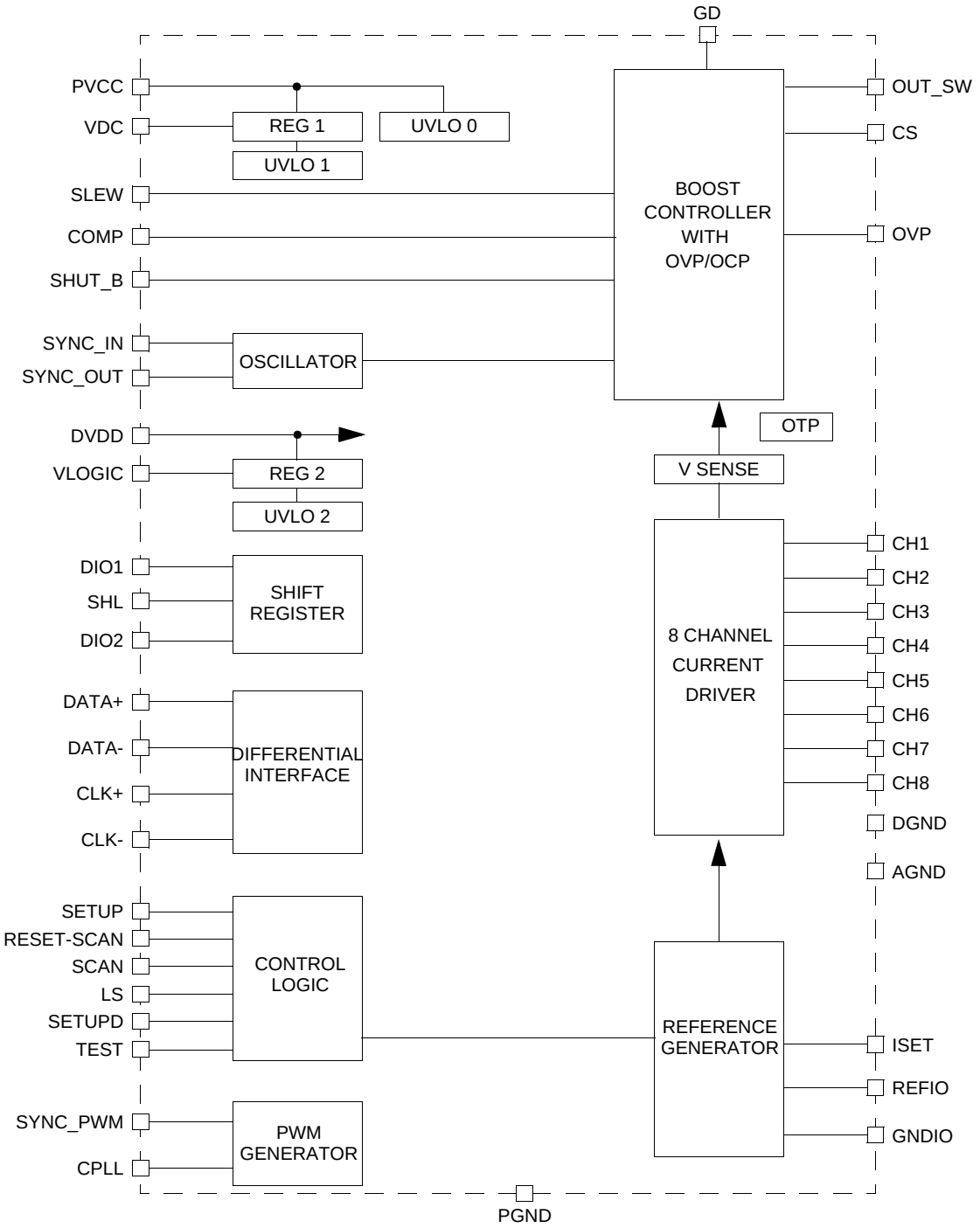


Figure 2. 34848 Simplified Internal Block Diagram

PIN CONNECTIONS

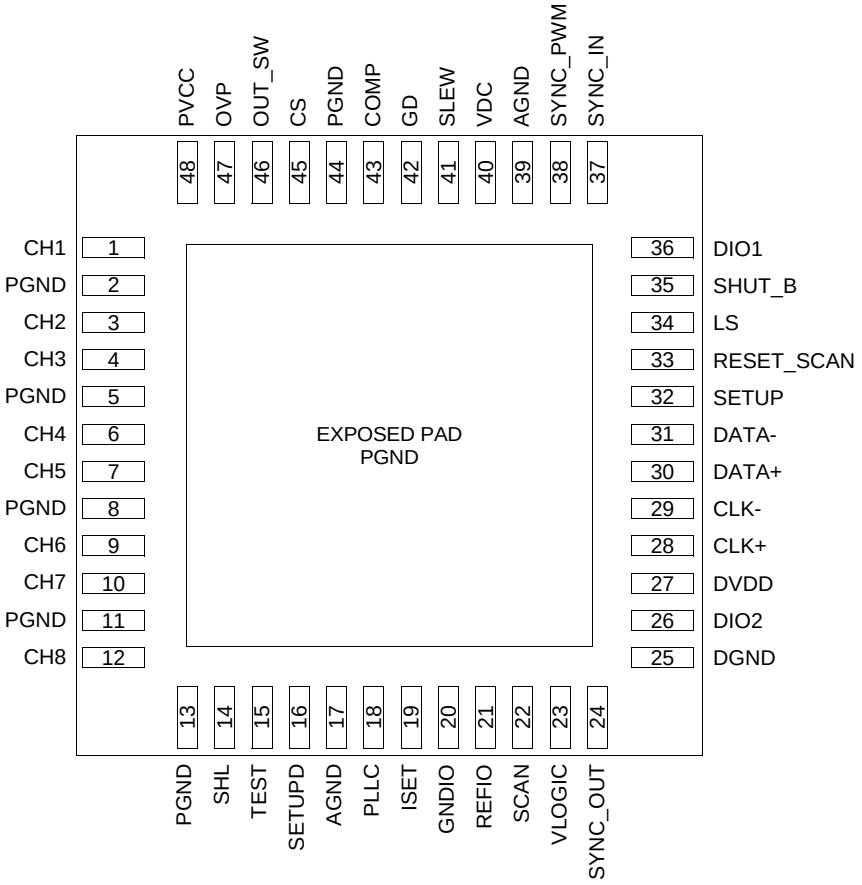


Figure 3. 34848 Pin Connections

Table 1. 34848 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	CH1			LED connection - channel 1
2, 5, 8, 11, 13, 44	PGND			Power ground
3	CH2			LED connection - channel 2
4	CH3			LED connection - channel 3
6	CH4			LED connection - channel 4
7	CH5			LED connection - channel 5
9	CH6			LED connection - channel 6
10	CH7			LED connection - channel 7
12	CH8			LED connection - channel 8
14	SHL			Shift register direction (‘H’ - DIO1 input, CH1 - CH8, DIO2 output, ‘L’ - - DIO2 input, CH8 - CH1, DIO1 output)
15	TEST			Enable test mode
16	SETUPD			Setup default value select

Table 1. 34848 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
17, 39	AGND	Ground		Analog ground
18	PLLC			PLL compensation network connection
19	ISET			Current reference setting
20	GNDIO			Ground reference REFIO supply
21	REFIO			Reference voltage supply
22	SCAN			Enable scan made (‘H’ enabled, ‘L’ disabled)
23	VLOGIC			Decouple for internally generated 2.5 V rail
24	SYNC-OUT			Boost clock output
25	DGND			Digital ground
26	DIO2			Data shift register I/O2
27	DVDD			Logic supply voltage
28	CLK+			Differential interface clock+
29	CLK-			Differential interface clock -
30	DATA+			Data+
31	DATA-			Data-
32	SETUP	Input		SETUP input. Setup mode and clear data register when high
33	RESET_SCAN	Input		RESET_SCAN input. Reset internal counter
34	LS			Data Latch
35	SHUT_B			Shutdown pin, active low
36	DIO1			Data shift register I/O1
37	SYNC_IN	Input		Boost clock input
38	SYNC_PWM	Input		PWM sync input
40	VDC			Decouple for internal gate driver voltage
41	SLEW			Boost driver slew rate control
42	GD			Control to power switch for input voltage V_{IN}
43	COMP			Boost compensation pin
45	CS	Input		Current sense input pin
46	OUT-SW	Output		FET driver output
47	OVP			Over-voltage protection sense pin
48	PVCC			Switch driver power supply
Exposed Pad	PGND	Ground		Power ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Maximum Pin Voltage	V_{MAX}		V
CH1 - CH8		45	
GD		28	
PVCC		14	
VDC, OUT_SW		6.2	
PLLC, ISET, REFIO, VLOGIC, OVP, CS, COMP, SLEW, SYNC_PWM, CLK, DATA		2.6	
All other pins		3.6	
VIN Input Voltage Range	V_{IN}	12 to 28	V
PVCC Input Voltage Range	P_{VCC}	6.0 to 14	V
DVDD Input Voltage Range	D_{VDD}	2.6 to 3.6	V
Maximum LED Current - Local Dimming Mode	I_{LED_LDM}	82	mA
Maximum LED Current - Scan Mode	I_{LED_SM}	164	mA
ESD Voltage[1]	V_{ESD}		V
Human Body Model (HBM)		±2000	
Machine Model (MM)		±200	
THERMAL RATINGS			
Ambient Temperature Range	T_A	-40 to 85	°C
Storage Temperature	T_{STO}	-40 to150	°C
Peak Package Reflow Temperature During Reflow[2],	T_{PPRT}	Note 2	°C
Maximum Junction Temperature	T_{J_MAX}	150	°C
Thermal Resistance, Junction to Ambient[3]	$R_{\theta J\text{-}A}$	28	°C/W
Thermal Resistance, Junction to Case[4]	$R_{\theta J\text{-}C}$	2.0	°C/W

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-2), and the Machine Model (MM) (AEC-Q100-003), R_{ZAP} = 0 Ω).
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
3. Thermal resistance measured in accordance with EIA/JESD51-2.
4. Theoretical thermal resistance from the die junction to the exposed pad.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions V_{IN} = 24 V, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, I_{LED} = 70 mA (Local Dimming Mode); 140 mA (Scan Mode), f_S = 700 kHz, f_{PWM} = 660 Hz, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY					
Supply Voltage at PVCC	V_{PVCC}	6.0	12	14	V
Supply Current at PVCC, Device Enabled SHUT_B = High, V_{PVCC} = 14 V	I_{PVCC}	-	18.5	22	mA
Supply Current at PVCC, Device Disabled SHUT_B = Low, V_{PVCC} = 14 V	$I_{PVCC-DIS}$	-	14.5	18	mA
PVCC Under-voltage Lockout V_{PVCC} Falling	V_{PVCC_UVLO}	-	-	5.5	V
PVCC Under-voltage Lockout Hysteresis V_{PVCC} Rising	$V_{PVCC\_UVLO\_HYST}$	-	0.24	-	V
Supply Voltage at DVDD	V_{DVDD}	2.6	3.3	3.6	V
Supply Current at DVDD, Device Enabled SHUT_B = High, V_{DVDD} = 3.6 V	I_{DVDD}	-	7.5	12	mA
Supply Current, Device Disabled SHUT_B = Low, V_{DVDD} = 3.6 V	$I_{DVDD-DIS}$	-	7.5	12	mA
DVDD Under-voltage Lockout V_{DVDD} Falling	V_{DVDD_UVLO}	2.3	2.4	2.55	V
DVDD Under-voltage Lockout Hysteresis V_{PVCC} Rising	$V_{DVDD\_UVLO\_HYST}$	-	0.15	-	V
VDC Output Voltage[5] C_{VDC} = 2.2 µF	V_{DC}	5.8	6.0	6.2	V
V_{LOGIC} Output Voltage[5] C_{VLOGIC} = 2.2 µF	V_{LOGIC}	2.4	2.5	2.6	V

Notes

5. This pin is for internal use only, and not to be used for other purposes.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 24 V, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, I_{LED} = 70 mA (Local Dimming Mode); 140 mA (Scan Mode), f_S = 700 kHz, f_{PWM} = 660 Hz, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BOOST CONVERTER					
SW Output Voltage	V_{SW}	5.8	6.0	6.2	V
CS Sense Voltage R_{CS} = 50 mΩ, I_{LIMIT} Threshold = 3.5 A	V_{CS}	- -	0.175 -	- -	V
Boost Efficiency[6] I_{LOAD} = 0.5 A	EFF_{BOOST}	- -	94 -	- -	%
Boost Line Regulation (V_{IN} = 24 V ±15%, I_{LOAD} = 0.5 A)	I_{OUT}/V_{IN}	- -	0.1 -	- -	%/V
Current Sense Amplifier Gain	A_{CSA}	-	4.5	-	
Slope Compensation Voltage Ramp	V_{SLOPE}	-	0.34	-	V
LED CURRENT DRIVER					
Maximum sink current Local Dimming Mode Scan Mode	I_S	 - -	 - -	 82 164	mA
Regulated Minimum voltage across drivers	V_{MIN}	400	500	600	mV
Off-state Leakage Current, all channels (V_{CH} = 45 V)	I_{CH_LEAK}	 -	 -	 10	µA
LED Current Tolerance Channel-to-Channel/ Chip-to-Chip	$I_{TOLERANCE}$	 -1	 -	 +1	%
ISET pin voltage	V_{SET}	1.252	1.265	1.277	V
Local Dimming Mode Drive Current IL = 000 IL = 111	I_{LDM}	 61.8 79.2	 62.5 80	 63.2 80.8	mA
Scan Mode Drive Current IS = 00000 IS = 11111	I_{SCAN}	 120.0 158.4	 121.2 160	 122.4 161.6	mA
FAULT PROTECTION					
Over-temperature Threshold	O_{TT}	140	150	160	°C
Short Failure Detection Voltage C = 00 C = 01 C = 10 C = 11	S_{FDV}	 - 2.7 3.6 4.5	 Disabled 3.0 4.0 5.0	 - 3.3 4.4 5.5	V

Notes

6. Boost efficiency test is performed under the following conditions: f_{SW} = 700 kHz, V_{IN} = 24 V, T_A = 25°C, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, and R_L = 70 Ω. The following external components are used: FDS3692 (Boost FET), FDS4675 (Q-FET), L = 22 µH (DCR = 54 mΩ), C_{TOUT} = 30 µF, SS36-E3 (Schottky diode). The measurement does not include Q-FET losses. Note: Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 24 V, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, I_{LED} = 70 mA (Local Dimming Mode); 140 mA (Scan Mode), f_S = 700 kHz, f_{PWM} = 660 Hz, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVP Threshold[7]	O_{VP}				V
V = 000		27.9	31	34.1	
V = 001		29.7	33	36.3	
V = 010		31.5	35	38.5	
V = 011		33.3	37	40.7	
V = 100		35.1	38	42.9	
V = 101		36.9	41	45.1	
V = 110		38.7	43	47.3	
V = 111		40.5	45	49.5	
LOGIC INPUTS (SHUT_B, DIO1, DIO2, RESET, LS, SHL)					
Input Threshold Low	V_{IL}	-	-	0.8	V
Input Threshold High	V_{IH}	2.0	-	-	V
SHUT_B Input Leakage Current V_{SHUT_B} = 1.0 V	$I_{SHUT\_B\_LEAK}$	-	-	10	µA
DIO1, DIO2 Input Leakage Current V_{DIO} = 1.0 V	I_{DIO_LEAK}	-	-	10	µA
SETUP, RESET_SCAN Input Leakage Current V = 1.0 V	I_{LEAK}	-	-	10	µA
LS Input Leakage Current V_{LS} = 1.0 V	I_{LS_LEAK}	-	-	10	µA
SHL Input Leakage Current V_{SHL} = 1.0 V	I_{SHL_LEAK}	-	-	10	µA

Notes
7. Measurements performed using a resistor divider network with a ratio of 23.71.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{IN} = 24 V, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, I_{LED} = 70 mA (Local Dimming Mode); 140 mA (Scan Mode), f_S = 700 kHz, f_{PWM} = 660 Hz, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

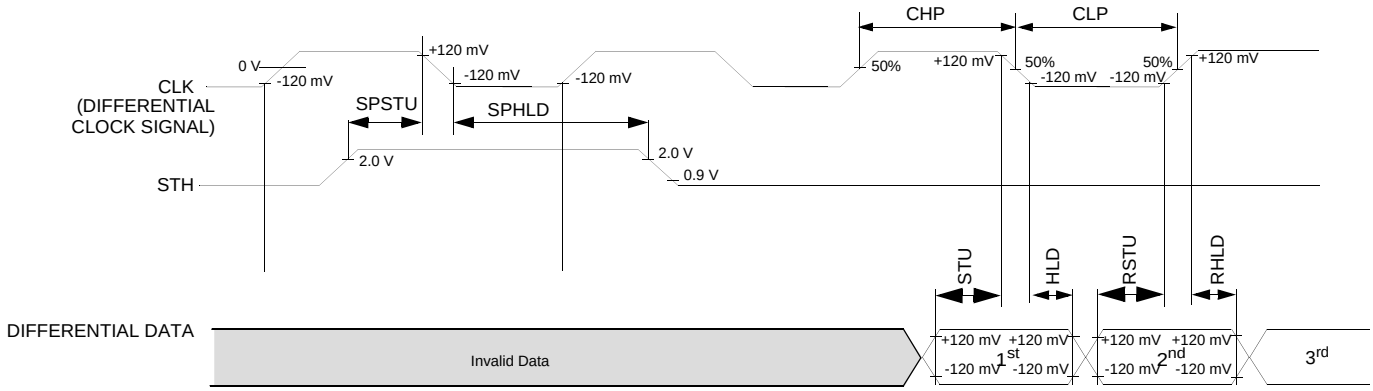
Characteristic	Symbol	Min	Typ	Max	Unit
BOOST CONVERTER					
Minimum duty cycle	D_{MIN}	25	-	75	ns
Maximum duty cycle	D_{MAX}	-	-	98	%
Switching Frequency	f_S				kHz
F = 000		160	200	240	
F = 001		240	300	360	
F = 010		320	400	480	
F = 011		400	500	600	
F = 100		480	600	720	
F = 101		560	700	840	
F = 110		720	900	1080	
F = 111		960	1200	1440	
Soft Start Period	t_{SS}	-	20	-	ms
SW Drive	SW_{DR}				ns
Rise time (10% to 90%), C_{LOAD} = 1.2 nF, VSW = 6.0 V, R_{SLEW} = 4.7 kΩ		-	12.5	-	
Fall time (90% to 10%), C_{LOAD} = 1.2 nF, VSW = 6.0 V, R_{SLEW} = 4.7 kΩ		-	16.5	-	
PWM GENERATOR					
RESET_SCAN Frequency	F_{RESET_SCAN}	80	120	180	Hz
PWM frequency[8]	f_{PWM}				Hz
P = 0000000000					
F_{RESET_SCAN} = 80 Hz		112	118	124	
F_{RESET_SCAN} = 120 Hz		168	177	186	
F_{RESET_SCAN} = 180 Hz		253	266	279	
P = 1111111111					
F_{RESET_SCAN} = 80 Hz		760	800	840	
F_{RESET_SCAN} = 120 Hz		1140	1200	1260	
F_{RESET_SCAN} = 180 Hz		1710	1800	1890	
PWM Synchronization Frequency[8]	f_{SYNC_PWM}				kHz
f_{PWM} = 177 Hz		172	181	190	
f_{PWM} = 1200 Hz		1166	1228	1289	
LED CURRENT DRIVER					
Channel Rise Time - 10% to 90%, I_{LED_PEAK} = 70 mA	t_R	-	-	200	ns
Channel Fall Time - 90% to 10%, I_{LED_PEAK} = 70 mA	t_F	-	-	200	ns

Notes

8. For Slave mode, the IC to IC matching is under ±1%

TIMING DIAGRAMS

The differential interface for data and clock control is specified as below.



NOTE: Max CLK Frequency - 85 MHz

Figure 4. Timing Specifications 1

Table 5. Timing Specification 1

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
CHP	Clock (CLK) High Period	f = 85 MHz	-	5.7	-	ns
CLP	Clock (CLK) Low Period	f = 85 MHz	-	5.8	-	ns
STU	(R.G.B.) Setup to falling or rising edge of CLK	f = 85 MHz	1.875	-	-	ns
HLD	(R.G.B.) Hold from falling or rising edge of CLK	I_{PI} = 100 µA, f = 85 MHz	0.225	-	-	ns
SPSTU	STH rising to CLK falling	R_T = 100 Ω, C_T = 5.0 pF, f = 85 MHz	3.0	-	-	ns
SPHLD	STH falling to CLK falling	R_T = 100 Ω, C_T = 5.0 pF, f = 85 MHz	1.5	-	-	ns

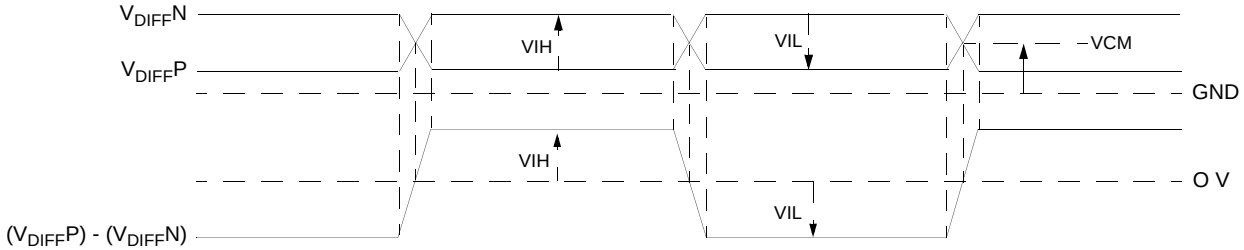


Figure 5. CLK and Data input Specification

Table 6. Timing Specification 1

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{IH}	High Input Voltage	V_{CM} = +1.2 V[9]	70	200	-	mV
V_{IL}	Low Input Voltage	V_{CM} = +1.2 V[9]	-	-200	-70	
V_{CM}	Common Mode Input Voltage Range	V_{IH} = +70 mV, V_{IL} = -70 mV	0.9	1.2	1.4	V
I_{DL}	Input Leakage Current	DxxP, DxxN, CLKP, CLKN	-10	-	10	µA

Notes:

9. **VCM = (VCLKP+VCLKN)/2 or VCM = (VDxxP+VDxxN)/2**
   The positive sign means that DxxP (or CLKP) is higher than ground DxxN (or CLKN)
   The negative sign means that DxxP (or CLKP) is lower than ground DxxN (or CLKN)

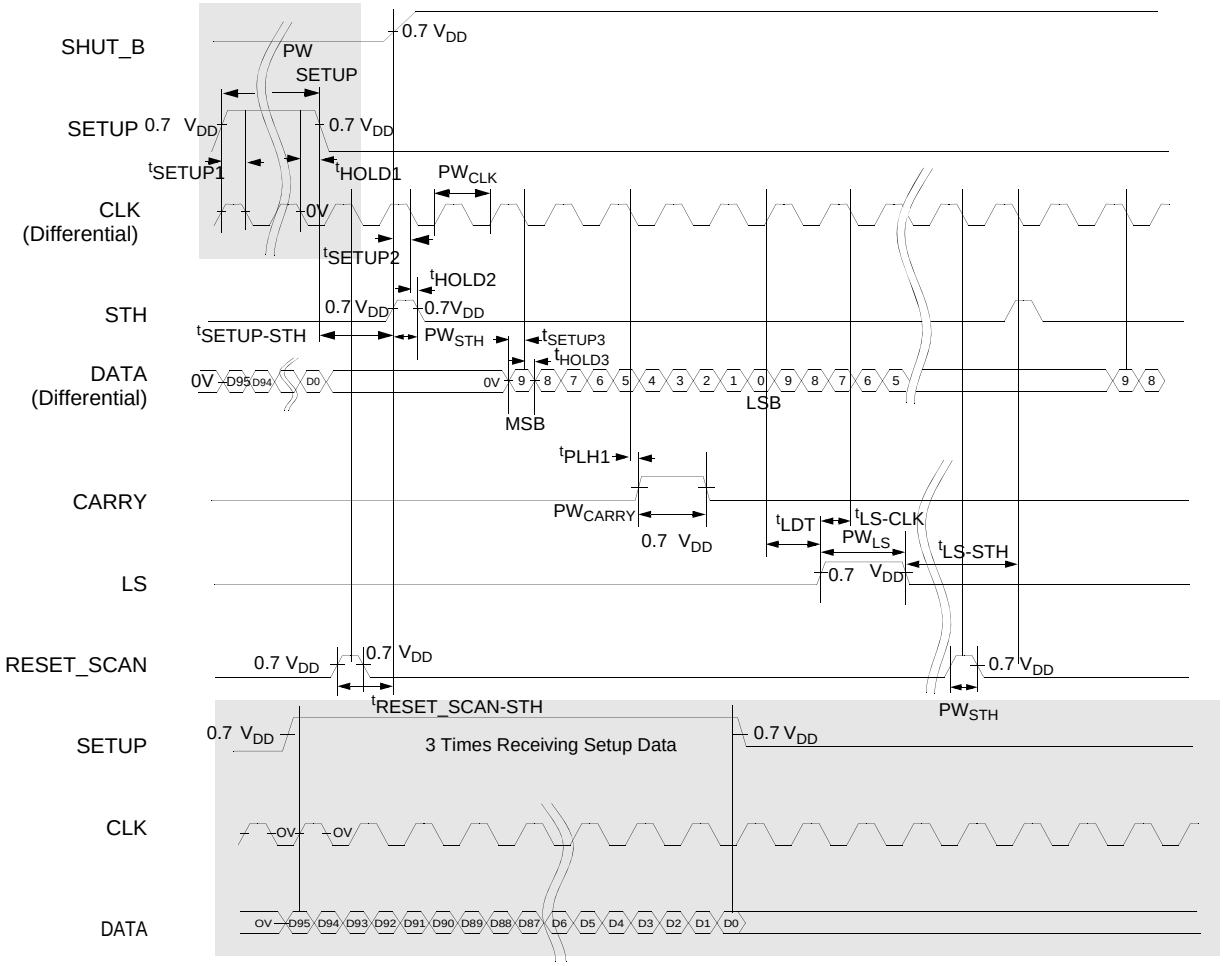


Figure 6. Total Interface Detailed Timing

Table 7. Interface Timing Specifications

Symbol	Min	Typ	Max	Unit
t_{SHUT_DVDD}	200	-	-	ms
$t_{SETUP-DVDD}$	1.0	-	-	ms
t_{SETUP1}	2.0	-	-	ns
t_{HOLD1}	2.0	-	-	ns
PW_{SETUP}	48	-	-	CLK
$t_{SETUP-STH}$	2.0	-	-	CLK
PW_{CLK}	11.7	-	333	ns
t_{SETUP2}	2.0	-	-	ns
t_{HOLD2}	2.0	-	-	ns
t_{LS-CLK}	4.0	-	-	
PW_{STH}	1.0	-	2.0	CLK
t_{SETUP3}	2.0	-	-	ns
t_{HOLD3}	2.0	-	-	ns

Table 7. Interface Timing Specifications

Symbol	Min	Typ	Max	Unit
PW_{CARRY}	-	-	1.0	CLK
t_{PLH1} (CL = 15 pf)	1.0	-	10.7	ns
t_{LDT}	1.0	-	-	CLK
t_{LS-STH}	2.0	-	-	CLK
$t_{RESET\_SCAN-STH}$	1.0	-	-	CLK
PW_{LS}	5.0	-	-	CLK

CONFIGURATION

When the SETUPD pin is high, the configuration registers are set to the default values in Table 8. When the SETUPD pin is low, the configuration registers can be programmed via the differential interface.

When the SETUPD and SHUT_B pins are low and SETUP is high, data can be written to the set-up register through the differential interface. Once the register has been programmed, the data is locked and the register cannot be reprogrammed again until a complete POR (Power-on-reset) is applied. Although the setup register is only 32 bits, the 34848 requires the data to be written 3 times (i.e. 96 bits). When SETUP is taken low, the 3 sets of data are compared. If 2 or more sets match, then that data is used. Otherwise, the default values are used. This interface programs the LED current, boost frequency, PWM frequency, OVP voltage, and LED short detection voltage.

Table 8. Setup Interface Registers

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IL2	IL1	IL0	IS4	IS3	IS2	IS1	IS0	P9	P8	P7	P6	P5	P4	P3	P2
P1	P0	F2	F1	F0	V2	V1	V0	S1	S0	C1	C0	R3	R2	R1	R0

- IL[2:0] = Local dimming mode current control (‘000’ = 62.5 mA, ‘111’ = 80 mA). Default = ‘011’ = 70 mA
- IS[4:0] = Scan mode current control (‘00000’ = 121.25 mA, ‘11111’ = 160 mA) Default = ‘01111’ = 140 mA
- P[9:0] = PWM frequency (‘0000000000’ = 177 Hz, ‘1111111111’ = 1200 Hz). Default = ‘0111100011’ = 660 Hz
- F[2:0] = Boost switching frequency (000 = 200 kHz, 001 = 300 kHz, 010 = 400 kHz, 011 = 500 kHz, 100 = 600 kHz, 101 = 700 kHz, 110 = 900 kHz, 111 = 1.2 MHz). Default = ‘101’ = 700 kHz
- V[2:0] = Over-voltage protection threshold (‘000’ = 31 V, ‘111’ = 45 V). Default = ‘111’ = 45 V
- S[1:0] = Scan mode row count (‘00’ = 2/8 row, ‘01’ = 3/8 row, ‘10’ = 4/8 row, ‘11’ = 5/8 row). Default = ‘01’ 3/8
- C[1:0] = LED short detection voltage (‘00’ = disabled, ‘01’ = 3.0 V, ‘10’ = 4.0 V, ‘11’ = 5.0 V). Default = ‘10’ = 4.0 V
- R[3:0] = reserved

TEST MODE

The TEST input can be used to place the 34848 into test mode. In this mode, the device is placed in to a pre-determined mode of operation as follows:

- Control register loaded with default values
- All PWM drivers set to 95% duty cycle
- No input data and clock (no CLK, no LS)
- Master device needs to use an on-chip oscillator to serve as the reference frequency to PLL

ELECTRICAL PERFORMANCE CURVES

TYPICAL PERFORMANCE CURVES (T_A=25°C)

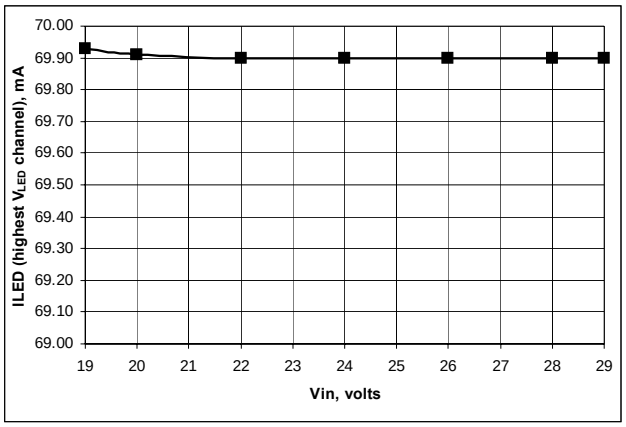


Figure 7. Line Regulation, V_{IN} Changing

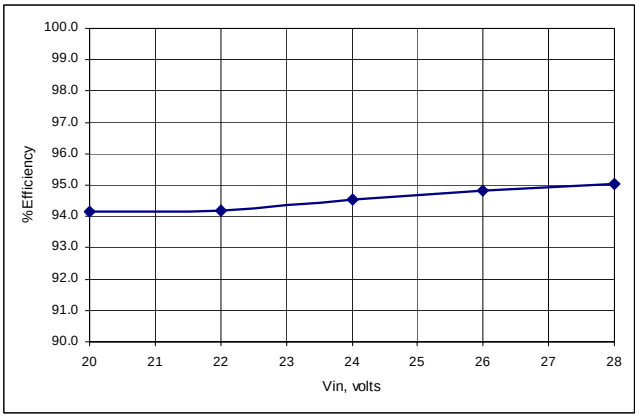


Figure 10. Boost Efficiency vs Input Voltage

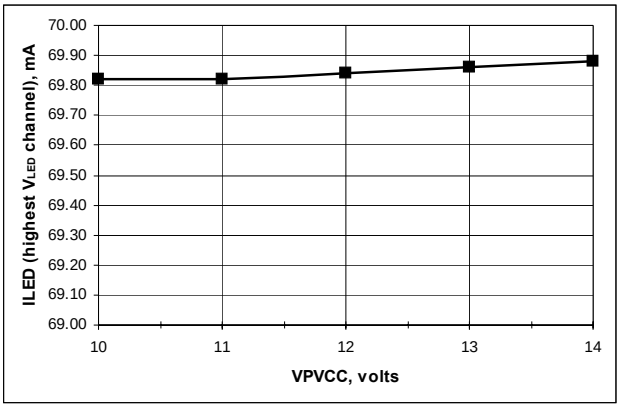


Figure 8. Line Regulation, V_{PVCC} Changing

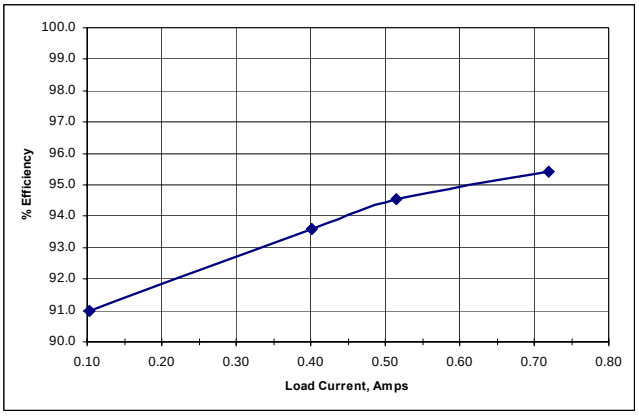


Figure 11. Boost Efficiency vs Load Current

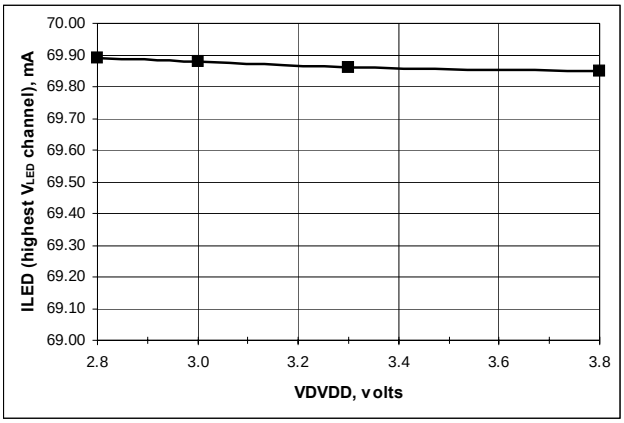


Figure 9. Line Regulation, V_{DVDD} Changing

Note: Typical Performance Curves were performed under the following conditions: f_{SW} = 700 kHz, V_{IN} = 24 V, V_{PVCC} = 12 V, V_{DVDD} = 3.3 V, and R_L = 70 Ω. The following external components are used: FDS3692 (Boost FET), FDS4675 (Q-FET), L = 22 µH (DCR = 54 mΩ), C_{TOUT} = 30 µF, SS36-E3 (Schottky diode). The efficiency measurements do not include Q-FET losses.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34848 is a high efficiency, 8-channel LED driver for use in LCD backlighting applications. The 34848 is designed to support up to 160 mA per channel in scan backlight mode, or 80 mA per channel in local dimming mode. The current reference is set using a single resistor to GND, and LED current tolerance is accurate to ±1% channel-to-channel and IC-to-IC. The current can be programmed in both local dimming and scan modes independently.

Each channel has independent PWM control with 10-bit resolution, programmed via the high speed differential interface. The frequency between ICs is synchronized and derived from Controller signals. When the SCAN pin is pulled high, it enables the scan mode. In this mode, each of 8 channels is on for nominally 3/8 (programmable from 2/8 to 5/8) of the frame.

The integrated boost controller is used to generate the minimum output voltage required to keep all LEDs illuminated with the selected current, providing the highest efficiency possible. The integrated boost clock can be programmed from 200 kHz and 1.2 MHz using the control interface.

FUNCTIONAL PIN DESCRIPTION

LED CONNECTION (CH1 - CH8)

LED current driver inputs, with maximum sink current capabilities in local dimming mode of 80 mA, and in scan mode of 160 mA.

POWER GROUND (PGND)

Power ground of the IC. Internal LED drivers and regulators are referenced to this pin.

SHIFT REGISTER DIRECTION (SHL)

The direction of the internal shift register is set by this pin.

TEST MODE (TEST)

This pin is used to enable the test mode.

SETUP DATA (SETUPD)

When this pin is high, the configuration registers are set to the default values. When this pin is low, the configuration registers can be programmed via the differential interface.

ANALOG GROUND (AGND)

Analog ground of the IC. Internal analog signals are referenced to this pin.

PLL NETWORK (PLLC)

PLL compensation network connection.

CURRENT REFERENCE SETTING (ISET)

The LED current is set with a 2.0 k resistor connected from this pin to ground. The precision of the resistor is recommended to be no higher than 0.1%.

REFERENCE VOTALGE SUPPLY (REFIO)

This voltage supply pin is used as a reference for achieving high current matching ratios when two or more ICs are connected together.

GROUND FOR REFIO SUPPLY (GNDIO)

Ground reference for the REFIO pin.

ENABLE SCAN MODE (SCAN)

If this pin is taken high, the IC enters in scan mode from the local dimming mode.

DECOUPLED LOGIC INTERNAL VOLTAGE (VLOGIC)

This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 µF is connected between this pin and ground for decoupling purposes.

BOOST CLOCK OUTPUT (SYNC_OUT)

Boost converter frequency is the output on this pin.

DIGITAL GROUND (DGND)

Digital ground of the IC. Internal digital signals are referenced to this pin.

DATA SHIFT REGISTER INPUT/OUTPUT (DIO1/DIO2)

These pins are used as inputs and outputs to the shift register depending on the status of SHL.

LOGIC SUPPLY VOLTAGE (DVDD)

Input voltage pin which ranges from 2.6 to 3.6 V, and used to power the internal logic circuits.

CLOCK SIGNALS (CLK+,CLK-)

Differential data clock signals.

DATA SIGNALS (DATA+, DATA-)

Differential data signals.

SETUP INPUT (SETUP)

When this pin is taken high, the differential interface programs the data registers and the device is in the setup mode.

RESET_SCAN INPUT (RESET_SCAN)

This pin is taken high at the start of each frame to reset the internal counter.

DATA LATCH (LS)

When this pin is pulsed, the PWM data in each of the Sample and Hold blocks is transferred to the corresponding PWM controller to start the PWM for the LED driver, and increase the internal counter by 1 in each LED driver device.

SHUT_B

When this pin is high, the boost and LED drivers are enabled.

BOOST CLOCK INPUT (SYNC_IN)

The Boost converter frequency can be synchronized to an external signal if provided at this pin. If this pin is connected to ground, an On-Chip oscillator is used to generate the boost frequency.

PWM SYNC CONNECTIONS (SYNC_PWM)

When the IC is operated as a Master, the resulting clock for PWM pulse generation is output on this pin. For Slave chips, this pin acts as an input for the reference clock for the PWM generator.

DECOUPLED INTERNAL GATE DRIVER VOLTAGE (VDC)

This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 µF is connected between this pin and ground for decoupling purposes.

BOOST DRIVER SLEW RATE CONTROL (SLEW)

This pin is used to control the slew rate on the OUT_SW pin for different application needs. The slew rate can be adjusted by connecting a resistor with a value of 4.7 k, 14 k, or 24 k, from this pin to GND.

Q-FET CONTROL (GD)

This pin is used to control the ON/OFF operation of the Q-FET.

BOOST COMPENSATION (COMP)

Boost converter compensation network connects to this pin.

POWER MOSFET DRIVER OUTPUT (OUT_SW)

Boost converter power MOSFET driver output.

CURRENT SENSE (CS)

Boost power MOSFET current is sensed across a resistor connected to this pin and ground, as well as for over-current protection (OCP) and current sensing for current mode control.

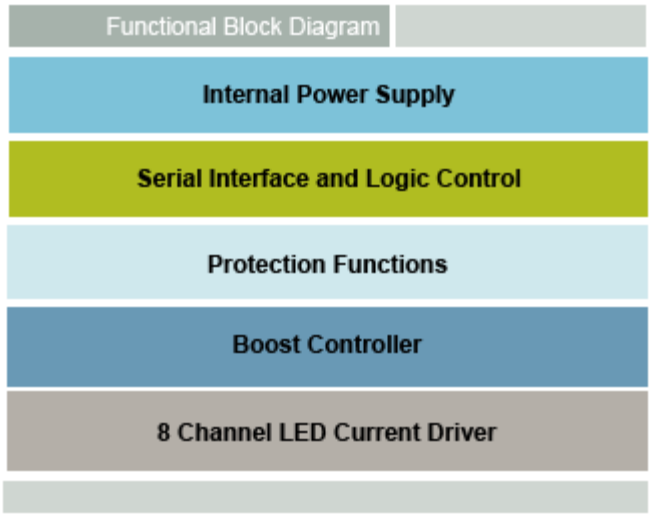
USER PRGRAMABLE OVER-VOLTAGE PROTECTION (OVP)

Over-voltage protection sense pin.

SWITCH DRIVER POWER SUPPLY (PVCC)

Input voltage pin that can range from 6.0 to 14 V and used to power the LED drivers and gate drive for the boost controller.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION



INTERNAL POWER SUPPLY

The internal circuitry of the 34848 uses two separate power supplies. The first is a high voltage input at PVCC that can range from 6.0 to 14 V, and is used to power the LED drivers and gate drive for the boost controller. The external Boost low side FET gate drive is equal to the input voltage at VDC. The second supply is DVDD, which ranges from 2.6 to 3.6 V, and is used to power the internal logic circuits.

Internally there are two regulators, which both have external decoupling capacitors. VDC is used to regulate the PVCC input to produce a constant drive voltage for the internal LED drivers, and is decoupled on the VDC pin. VLOGIC is used to produce 2.5 V for internal logic from the DVDD supply and is decoupled using a capacitor on the VLOGIC pin.

If the input voltage at either supply falls below their respective UVLO threshold, the device automatically enters the power down mode. Likewise, operation of the device is only possible when the two input voltages are above the UVLO threshold levels.

In addition to the above, PVCC voltage is also monitored for UVLO.

The SHUT_B pin can be used to enable/disable the Boost Controller and LED drivers.

DIFFERENTIAL INTERFACE AND CONTROL LOGIC

The 34848 uses a differential interface. The clock rate supported is up to 85 MHz. In addition, 6 logic pins are also used as part of the interface.

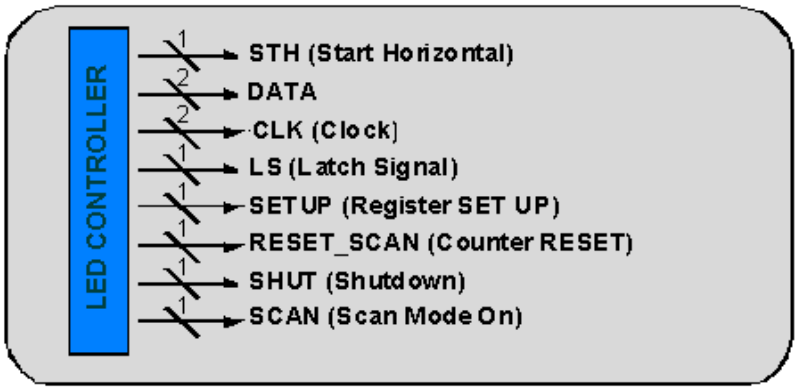


Figure 12. Control Interface

When SETUP is taken high the interface programs data registers which are in setting mode. An integrated 10-bit shift register selects which bit is being written. After the pulsing from SETUP and RESET_SCAN, the STH triggers the PWM data in from the differential interface. An internal counter (SIC) selects which channel is being written. The 10-bit shift register in multiple devices are connected to generate a long

chain of bit selects through all of the LED driver ICs in a system (10 x N bits. N = # of LED Driver IC).

RESET_SCAN is taken high at the start of each frame to reset the internal counter. Following the STH pulsing the input to the 10-bit register, the Controller is set to 1, which ripples through the connected shift registers with each data write. Once 10-bit data for this LED Driver has been written, the DIO1 (or DIO2) pin is taken high. This latches the data in the Sample and Hold (S/H) of the corresponding PWM channel (selected by SIC counter) for this LED Driver device. The DIO1 (or DIO2) pulsing from this LED Driver is input to the next LED Driver, as its STH signal at DIO2 (or DIO1) pin. Then the next 10-bit data can be written to the S/H of the selected PWM channel for this LED Driver device. This process continues until all the 10-bit data is written to the S/Hs in all LED Driver ICs, respectively. When LS is pulsed, the 10-bit PWM data is transferred from S/H to the PWM controller to start the PWM for LED driver, and the SIC counter increases by 1 in each LED Driver device.

For multiple devices, another 10 x N bits are then written for the next selected PWM channels in each LED Drivers using the same procedure. This continues and repeats for the N = 8 PWM channels in each LED Driver device.

The direction of the internal shift register is set using the SHL input. The DIO1 and DIO2 pins are used as inputs and output to the shift register depending on the status of SHL.

The differential interface control also features a default configuration mode for device setup. This is enabled by taking the SETUPD pin high.

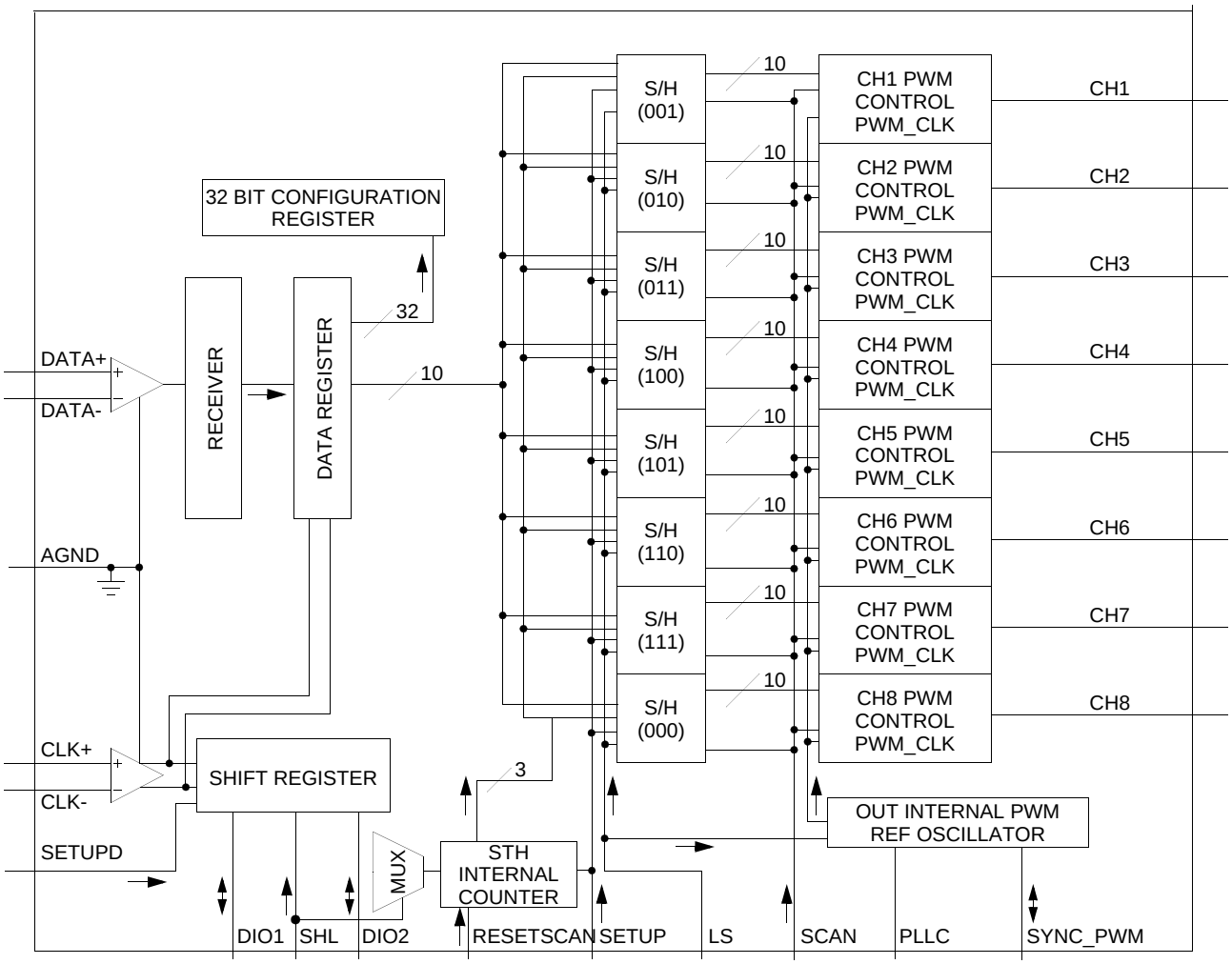


Figure 13. Control Register Block Diagram

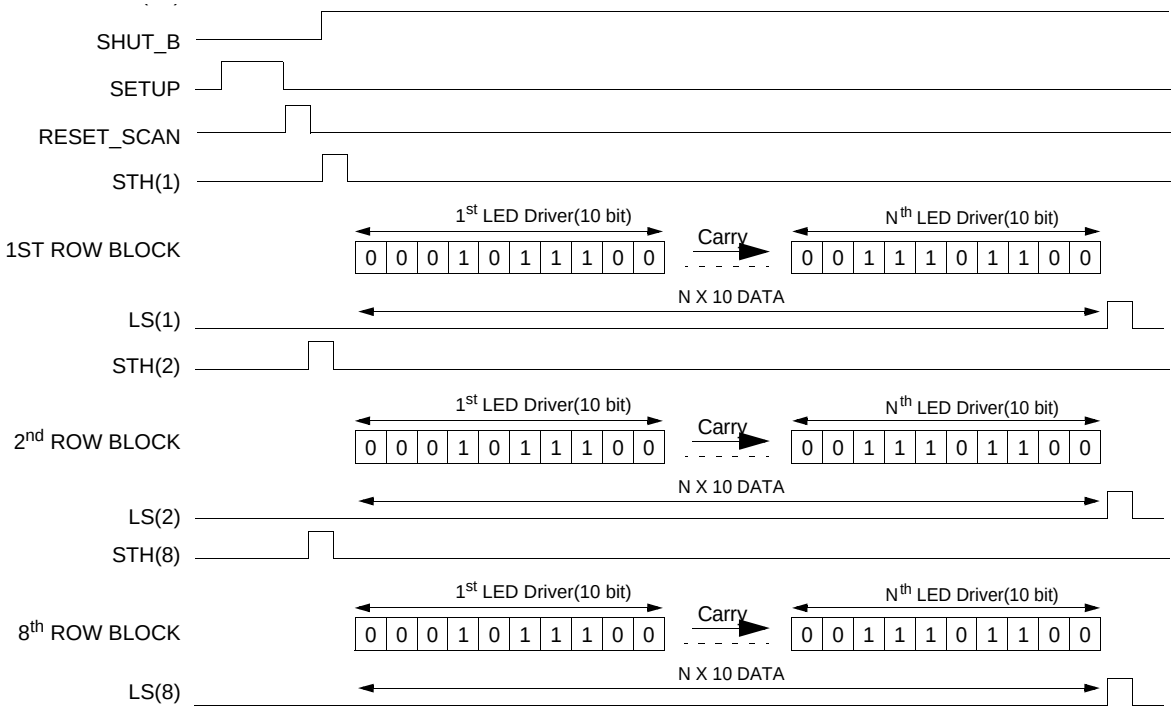


Figure 14. differential Interface Control

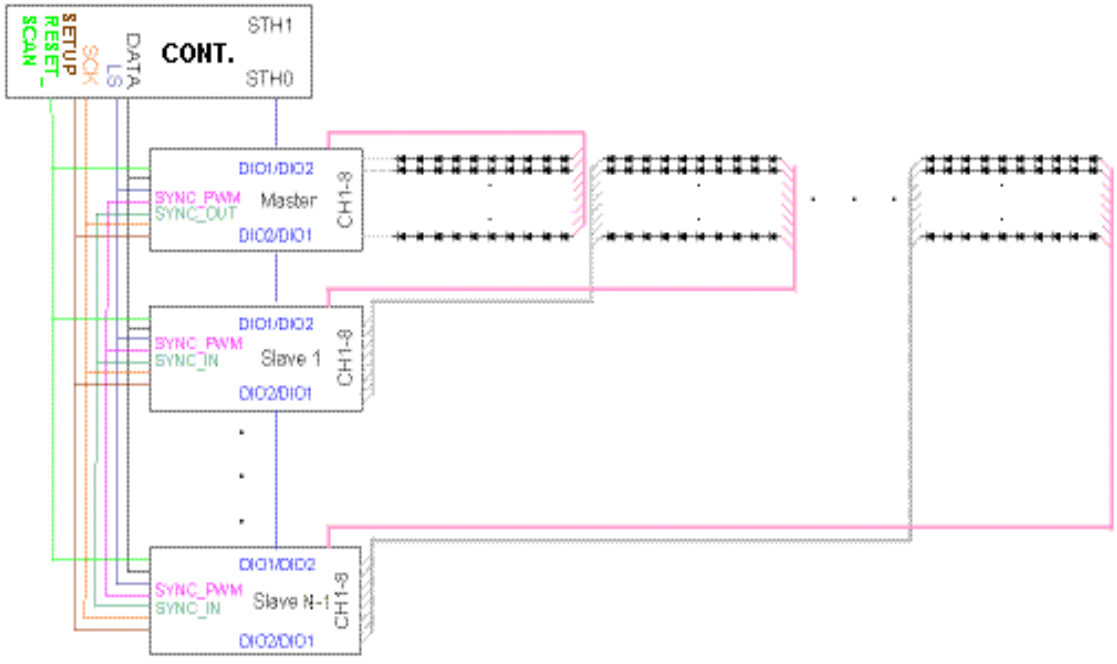
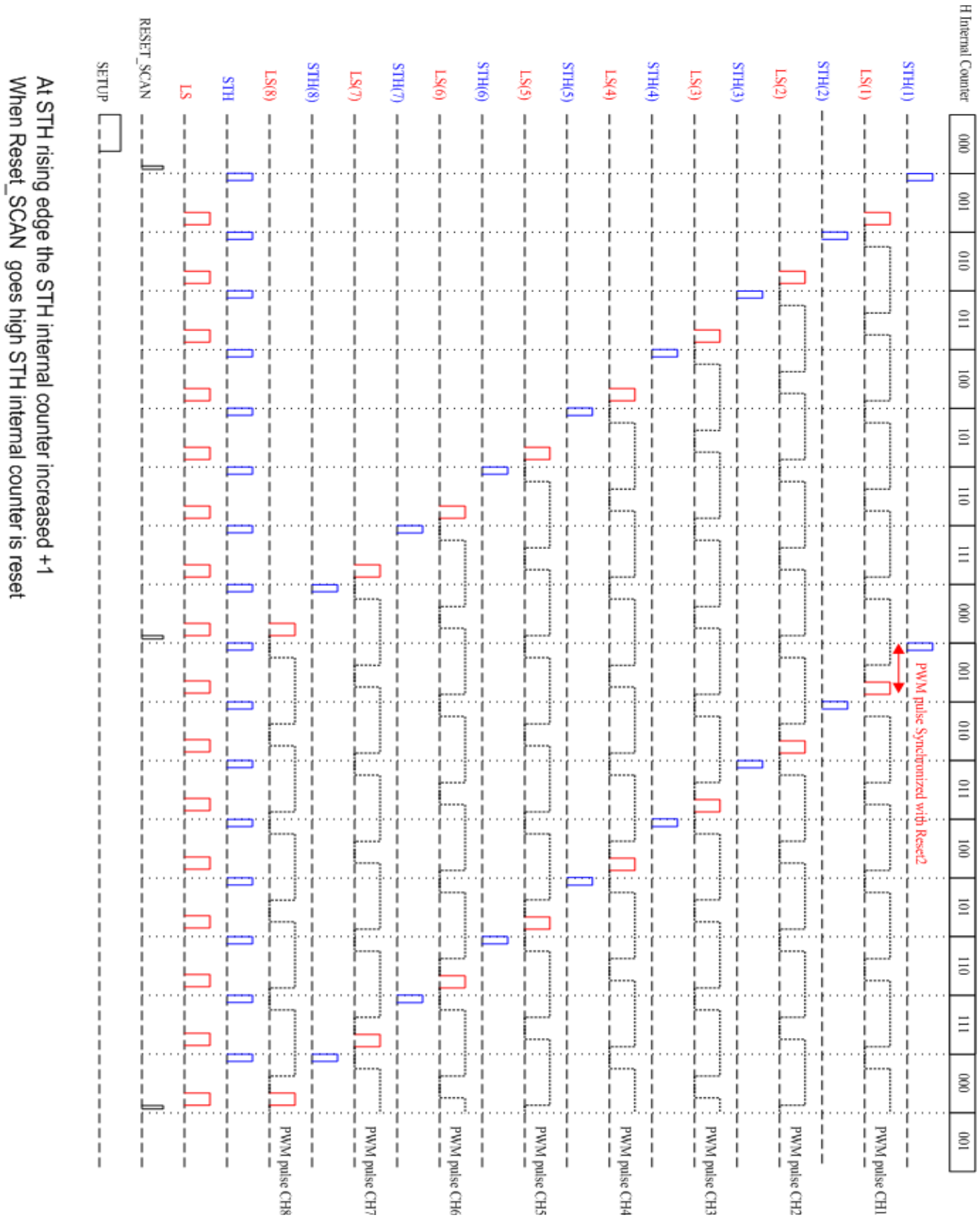
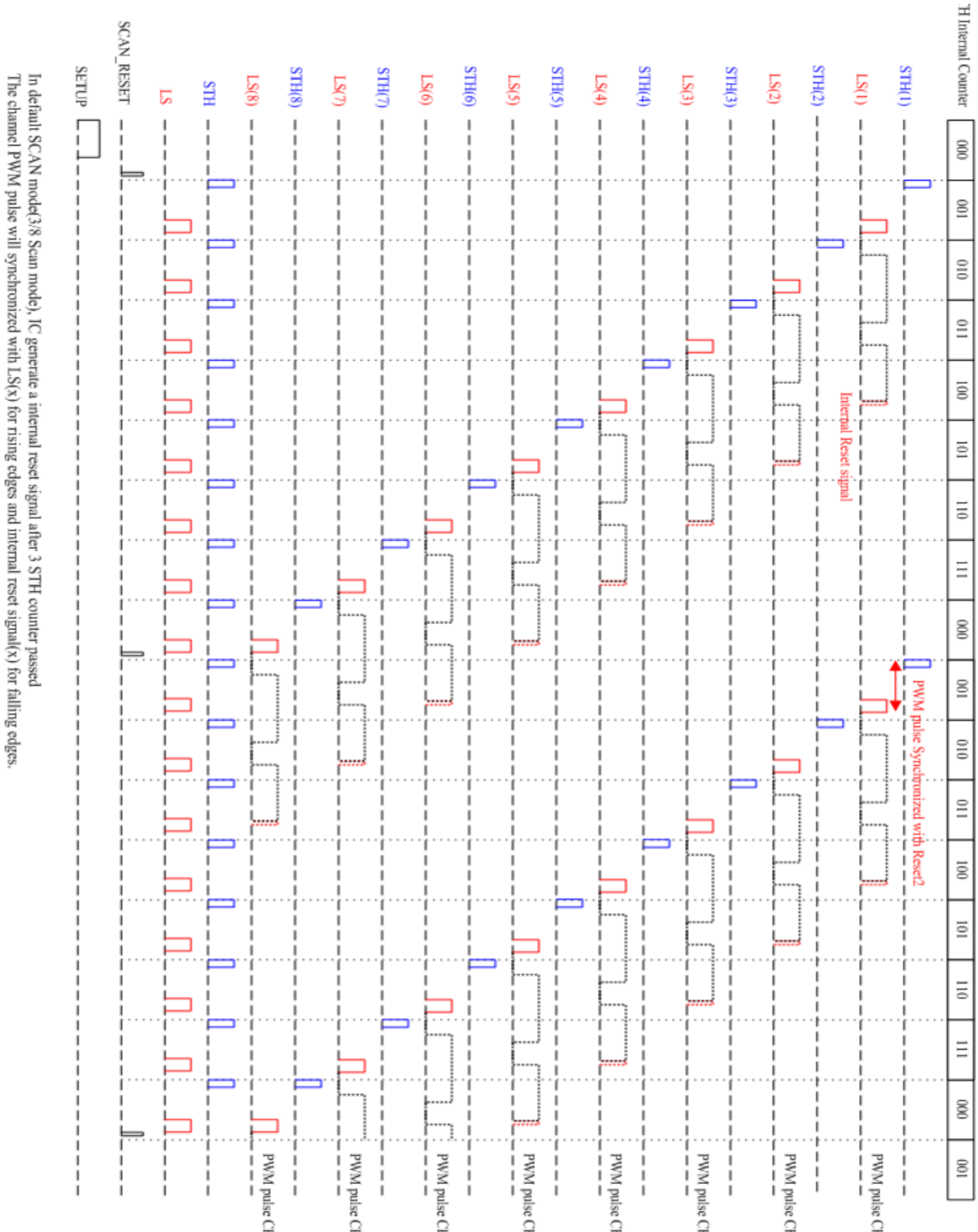


Figure 15. Connection Among LED Drivers Thru the Differential Interface Control and to the LED Panels



At STH rising edge the STH internal counter increased +1
When Reset_SCAN goes high STH internal counter is reset

Figure 16. Local Dimming Mode Control



In default SCAN mode(3/8 Scan mode), IC generate a internal reset signal after 3 STH counter passed
The channel PWM pulse will synchronized with LS(x) for rising edges and internal reset signal(x) for falling edges.

Figure 17. Scan Mode Control

PROTECTION FUNCTIONS

The 34848 monitors the backlighting application from several fault conditions to protect itself and the LED strings. See Protection and Diagnostic Features for a detailed description.

BOOST CONTROLLER

The integrated boost controller operates in non-synchronous mode and uses an external boost low side FET. Current is sensed across the sense resistor between the low side FET and ground, and is used for over-current protection (OCP) and current sensing for current mode control.

8 CHANNEL LED CURRENT DRIVER

The programmable current driver matches the current in up to 8 LED strings to within ±1%. The current can be programmed independently for scan and local dimming modes. In scan mode, the current can be programmed from 121.25 to 160 mA in 32 steps. In local dimming mode, the current range is from 62.5 to 80 mA in 8 steps. To provide this high matching ratio between ICs, the voltage references used in the ICs are connected between each chip using the REFIO and GNDIO pins.

The current driver circuits are also used to disable current flow in the LEDs when the LEDs are in the Off state, or when PWM is off. This enhances the performance of the PWM dimming function by maintaining a constant current through the LEDs when illuminated.

FUNCTIONAL DEVICE OPERATION

BOOST

An integrated sense circuit is used to sense the voltage at the LED current driver inputs and automatically sets the output voltage to the minimum voltage needed to keep all LEDs biased with the required current. Care has been taken to ensure that the minimum required output voltage (also the minimum VF of the LEDs) is used in order to minimize on-chip power dissipation. The boost frequency is programmed in the setup routine (see 'Configuration' below) from 200 kHz to 1.2 MHz, or can be synchronized to an input signal if provided at the SYNC_IN pin. If SYNC_IN is connected to GND, an on-chip oscillator is used to generate the boost frequency and the boost frequency is output on the SYNC_OUT pin.

The boost converter also features Over-current Protection (OCP). The OCP operates on a cycle by cycle basis. However, if the OCP condition remains for more than 60 ms then the boost regulator is latched off and GD asserts high to shutoff the Q-FET. The device can only be restarted by recycling the power supply.

The SLEW pin is used to limit the slew on the OUT_SW pin to reduce noise and avoid EMI problems. If the slew rate is reduced too much, the efficiency of the device will reduce. The slew rate can be changed by tying a resistor from the SLEW pin to GND.

The Boost converter has been designed to operate over a wide range of switching frequencies. Table 9 shows the recommended external components to ensure stable operation under all operating conditions.

Table 9. Recommended External Components (V_{IN} = 24 V ±10%)

Switching Frequency [kHz]	L [µH]	C_O [µF]	R_{COMP} [kΩ]	C_{COMP1} [nF]	C_{COMP2} [pF]
200	100	150	130	1.5	59
300	68	100	130	1.0	39
400	47	68	130	0.7	29
500	33	47	130	0.6	24
600	33	47	130	0.5	20
700	22	33	130	0.4	-
900	22	33	130	0.3	-
1200	15	22	130	0.2	-

The output capacitor C_O should be a low ESR type, preferably a MLCC. If an electrolytic capacitor is used, a small value ceramic capacitor should be connected in parallel to C_O to reduce the ESR, thus reducing the output ripple voltage of the converter.

PWM DIMMING

Each channel has an independently programmable 10-bit PWM generator. The data for the PWM generator is programmed using the differential interface in standard operating mode. If the channel is programmed with 0 duty cycle, that channel is programmed off, and is ignored for automatic output voltage control and for LED failure detection (see Protection and Diagnostic Features).

The PWM generator frequency can be programmed from 177 to 1200 Hz in 1.0 Hz step using a register in the start-up control registers, and is generated by a PLL using RESET-SCAN as the frequency reference. To operate in Master mode, the SYNC_IN pin is connected to GND. The resulting clock for PWM pulse generation is output on the SYNC_PWM pin. A compensation network is connected between the PLLC pin and GND. For Slave mode, the SYNC_PWM pin acts as an input for the reference clock for the PWM generator. In this manner, one device can be used as the master IC, SYNC_IN tied to GND, (compensation network on PLLC, and SYNC_PWM as output) and the remainder as slaves (PLLC grounded, SYNC_PWM as input) just by connecting the SYNC_PWM pins together.

The default Frame Frequency is 120 Hz. However, the RESET-SCAN frequency input range can be between 80 and 180 Hz. Therefore, the resulting PWM frequency is given by ($F_{RESET-SCAN}$/120) x F_{PWM}.

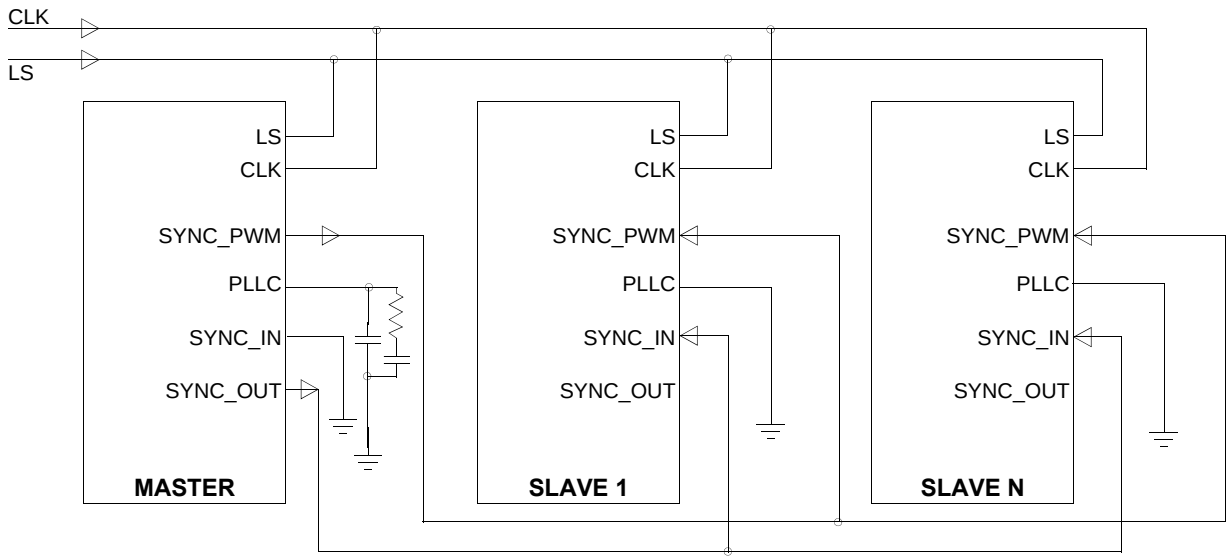


Figure 18. PWM, Boost Clock and Current Synchronization

SCAN

When the SCAN pin is set high, the 34848 enters scan mode. In this mode, the LED current is set as determined in the IS register. The number of banks illuminated at any one time is set using the configuration register. (See Figure 19) When the scan pin is set low, the 34848 device goes into local dimming mode.

PWM FREQUENCY

For master mode the PWM frequency is set by the internal register while for slave mode it is synchronized to SYNC_PWM.

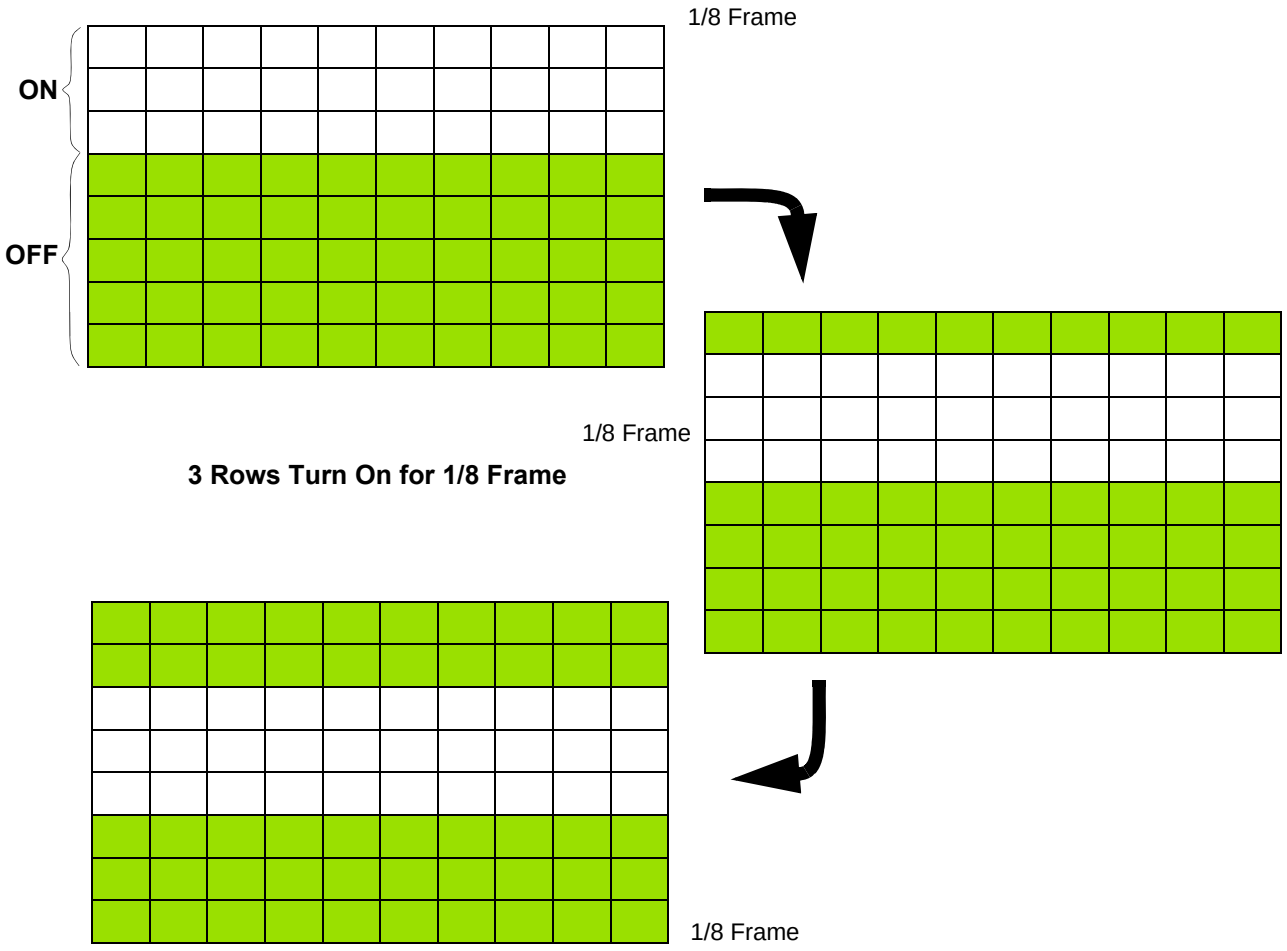


Figure 19. Scan Mode Operation

PROTECTION AND DIAGNOSTIC FEATURES

OVER-CURRENT PROTECTION

The boost converter features Over-current Protection (OCP). The OCP operates on a cycle by cycle basis. However, if the OCP condition remains for more than 60 ms then the boost regulator is latched off and GD asserts high to shutoff the Q FET. The device can only be restarted by cycling the power supply.

OVER-VOLTAGE PROTECTION

The 34848 features user programmable Over-voltage Protection (OVP). The OVP level can be programmed between 31 and 45 V in 2.0 V steps. When OVP is reached, the V_{OUT} voltage is clamped at the OVP level, and the 50 ms timer is started. If the V_{OUT} is clamped at the OVP level for more than 50 ms, the V_{OUT} voltage is lowered by 4.0 V, the DHC is turned off, and another 150 ms timer starts After the 150 ms timer has elapsed, the DHC is turned on again.

If V_{OUT} drops below the OVP before the 50 ms timer expires, normal operation continues. However, if OVP is still reached after the 50 ms timer expires, the device will repeat the OVP sequence two more times. If the OVP fault condition is still present after the third sequence, the Q-FET, LED drivers, and boost are turned off.

The 34848 uses an internal ADC to measure the voltage level at the OVP pin and compares it with the configured OVP level. A resistor divider network needs to be added between V_{OUT} and ground, with the center tap connected to OVP. The typical value for the upper divider resistor R_{UPPER} is 243 k (1%) and 10.7 k (1%) for the lower resistor R_{LOWER}.

This results in a divider ratio of 23.71 (R_{UPPER} + R_{LOWER} / R_{LOWER}), which sets the max OVP value.

The OVP voltage can be programmed from 31 to 45 V.

LED OPEN PROTECTION

The 34848 monitors the LED status at all 8 channels. The output voltage is continuously maintained at the minimum voltage possible to drive all LEDs, i.e. the maximum forward voltage of the 8 strings plus the minimum threshold needed (0.5 V, typ) for the current sense circuit and the current driver to regulate.

If an LED fails open, the voltage at the CHx pin for the effected LED string falls close to ground, and therefore the correspondent LED channel will be disabled.

LED SHORT PROTECTION

The 34848 also protects against LED short failures. If delta V_{FB}, $|V_{FB\_MAX} - V_{FB\_MIN}|$, is higher than SFDV and PWM duty of each channels are more than 0%, then this V_{FB_MAX} channel is disabled.

OVER-TEMPERATURE PROTECTION

The 34848 has an on-chip temperature sensor that measures die temperature. If the IC temperature exceeds the OTP threshold, the IC will turn off. While off, the GD pin is set to high-impedance to turn off the Q-FET. The device turns back on after recycling the power.

TYPICAL APPLICATIONS

INTRODUCTION

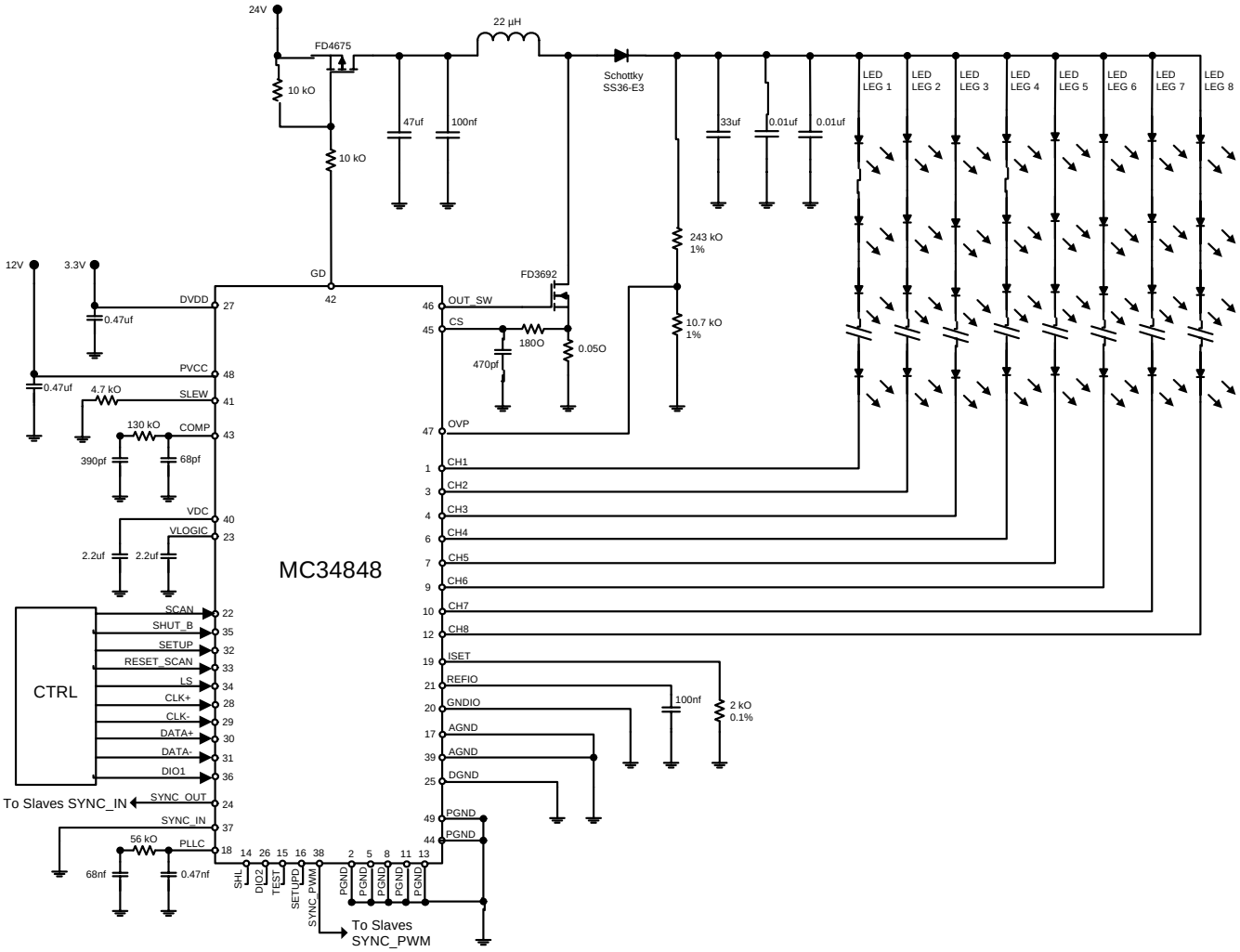


Figure 20. Typical Application Circuit for Master Mode Operation (10 LEDs per channel, V_F = 3.3 V typical)

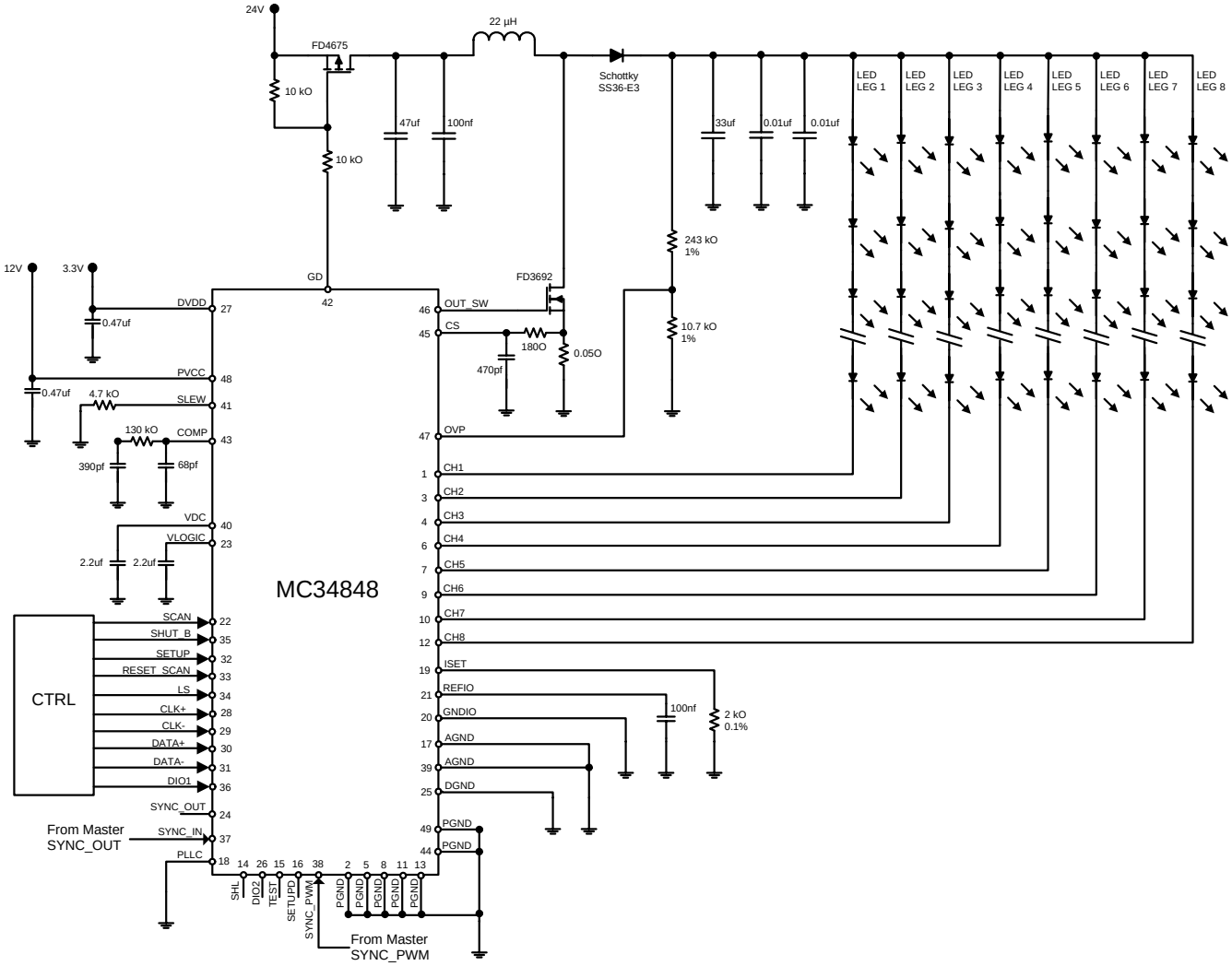


Figure 21. Typical Application Circuit for Slave Mode Operation (10 LEDs per channel, V_F = 3.3 V typical)

COMPONENT SELECTION AND PCB DESIGN CONSIDERATIONS

This section provides a comprehensive procedure for the selection of external components to achieve proper device operation. It also explains PCB layout design considerations.

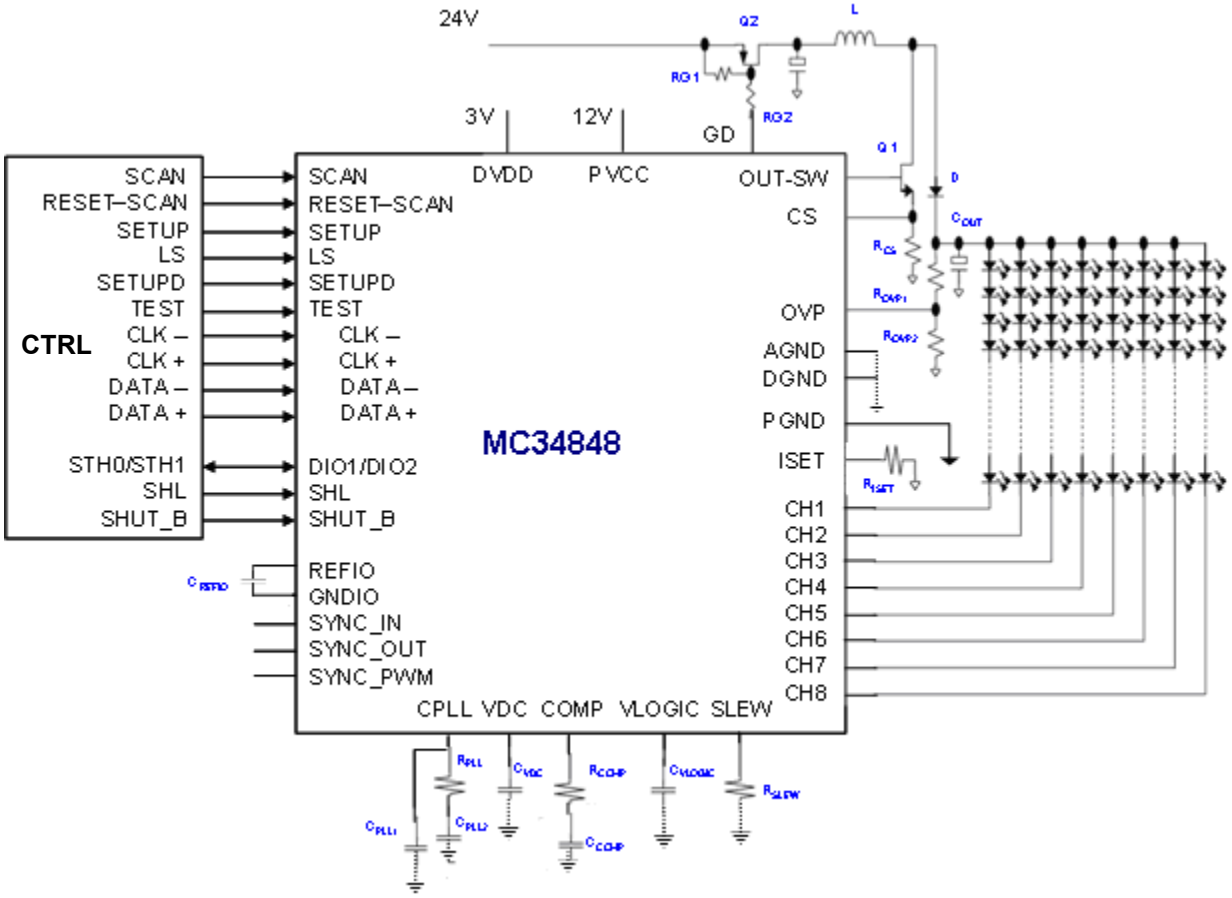


Figure 22. Component Selection Application Diagram for the 34848

COMPONENT SELECTION

ASSUMPTIONS FOR CALCULATIONS

V_{IN} = 21.6 V	I_{OUT} = 0.9 A.
V_{PVCC} = 12 V	f_{SW} = 700 kHz
V_{DVDD} = 3.3 V	R_{MAP} = 0.23 V/A
V_{OUT} = 39 V	ESR = 10 mΩ

SELECTING THE INDUCTOR FOR THE BOOST CONVERTER

A first approach to determine the value of the inductor is to consider the continuous conduction mode, that is, the current of the inductor never falls to zero. Then the following formula is used,

$$L = \frac{V_{OUT} + V_D}{I_{OUT} \times r \times f_{SW}} \times D(1-D)^2$$

where:

$r = \frac{\Delta I}{I_L}$	Current ripple ratio = 0.4, which is a good design target for any switching frequency.

$I_L = \frac{I_{OUT}}{1-D}$	Average inductor current.
V_D	Diode forward voltage drop, e.g. 0.7 V
D	Boost converter duty cycle, $\frac{V_{OUT}+V_D-V_{IN}}{V_{OUT}+V_D} = 0.46$

⇒ L ≅ 21 µH. An off the shelf inductor value of 22 µH can be used.

Note: When selecting an inductor, make sure that both the saturation current (I_{SAT}) & RMS current (I_{RMS}) > I_L + (ΔI / 2).

The saturation current (I_{SAT}) is the current at which the inductance value drops a specified amount below its measured value with no DC current. The inductance drop is attributed to core saturation.

The RMS current (I_{RMS}) is the root mean square current that causes the temperature of the part to rise a specific amount above 25°C ambient. The temperature rise is attributed to I^2R losses.

SELECTING THE OUTPUT CAPACITOR FOR THE BOOST CONVERTER

The minimum output capacitor can be determined as follows:

$$C_{OUT} = \frac{D}{\left[\frac{V_{OUT}}{I_{OUT}} \times f_{SW} \times \left(\frac{\Delta V_{OUT}}{2V_{OUT}}\right)\right]}$$

where:

ΔV_{OUT}	Peak to peak output voltage ripple, e.g. 50 mV

⇒ C_{OUT} ≅ 23 µF. The next bigger off the shelf capacitor value of 33 µF is chosen. In the case of switching power supplies, it is a good practice to use electrolytic capacitors (to increase the ripple current capability) and ceramic capacitors (to reduce the ESR effects) together, and consider their capacitance value over temperature.

SELECTING THE INPUT CAPACITOR FOR THE BOOST CONVERTER

What matters most about the input capacitor selection is its RMS current capability, ESR, and the voltage rating, more than the value itself. As a result, when selecting the input capacitor, the user must take into consideration:

1. The RMS current rating of the capacitor(s) should be equal or higher than:

$$I_{RMS\_IN} = \frac{I_{OUT}}{1-D} \times \frac{r}{\sqrt{12}}$$

2. The lower the ESR, the lower the conduction losses and the input ripple voltage, which implies less input noise and EMI effects
3. The voltage rating must be at least 50% higher than the maximum input voltage.
4. The bigger the capacitor, the smaller the input ripple voltage. Nevertheless, the bigger the capacitor, the higher the inrush current the input protection MOSFET should handle, probably causing turn on failures.

SELECTING THE COMPENSATION NETWORK COMPONENTS

As Freescale´s 34848 uses current mode control for the boost converter output voltage regulation, the ramp to the PWM modulator is derived from the inductor-switch current. As a result, there is no double LC pole anymore, and a simple Type-II network compensation is implemented by using a Transconductance Operational Amplifier.

The most common way of producing the ramp is to simply sense the forward drop across a current sense resistor. This small sensed voltage is then amplified by a current sense amplifier to get the voltage ramp, which is applied to the PWM modulator.

One of the subtleties of current mode of control is that it needs a small ramp to the comparator ramp, which is called slope compensation. Its purpose is to prevent an odd artifact of current mode control called sub-harmonic instability.

The following design equations are presented for the compensation network [1][2],

$$R_{COMP} = \frac{A}{g_m \frac{V_{ref}}{V_{OUT}}} = \frac{A}{12.6528 \times 10^{-6}}$$

where,

$$A = 10^{\left(\frac{G}{20}\right)}$$

$$G = ABS\left(20\times\log\left|G(s)\right|\right) = ABS\left(20\times\log\left|G_0\frac{\left(1+\frac{s}{F_{ESR}}\right)\left(1-\frac{s}{F_{RHP}}\right)}{\left(1+\frac{s}{F_{P1}}\right)\left(1+\frac{s}{F_{P2}}\right)}\right|\right)$$

$$G_0 = \frac{\frac{V_{OUT}}{I_{OUT}}(1-D)}{R_{MAP}\times K_D}$$

$$F_{ESR} = \frac{1}{2\pi\times ESR\times C_{OUT}}$$

$$F_{RHP} = \frac{\left(\frac{V_{OUT}}{I_{OUT}}\right)(1-D)^2}{2\pi\times L}$$

$$F_{P1} = \frac{1}{2\pi\times C_{OUT}}\left(\frac{2I_{OUT}}{V_{OUT}} + \frac{(1-D)^2}{R_{MAP}}\left(\frac{1}{K_M}+\frac{K}{1-D}\right)\right)$$

$$F_{P2} = \frac{K_M R_{MAP}}{2\pi\times L}$$

$$K_D = 2 + \frac{\frac{V_{OUT}}{I_{OUT}}(1-D)^2}{R_{MAP}}\left(\frac{1}{K_M}+\frac{K}{1-D}\right)$$

$$K_M = \frac{1}{(0.5-D)\times R_{MAP}\times\left(\frac{1}{L\times f_{SW}}+\frac{V_{PP}}{V_{OUT}}\right)}$$

$$V_{PP} = \frac{V_{OUT}-V_{IN}}{L}\times\left(1-\frac{0.18}{D}\right)\times\frac{R_{MAP}}{f_{SW}}$$

$$K = 0.5\times R_{MAP}\times\frac{D(1-D)}{L\times f_{SW}}$$

In order to determine the value of the R_{COMP} resistor it is necessary to choose the crossover frequency. Although the typical target is one-third of the switching frequency, it is necessary to confirm that this crossover frequency is significantly below the location of the RHP zero. As a result, one fifth of the RHP frequency it´s a good approach. Then:

$$F_{CROSS} = \frac{\left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \times L} \times \frac{(1-D)^2}{5} \approx 18.6\,\text{kHz}$$

Plotting the transfer function of G(s) and locating the crossover frequency, the DC gain needed for the compensator can be obtained, as shown in Figure 23.

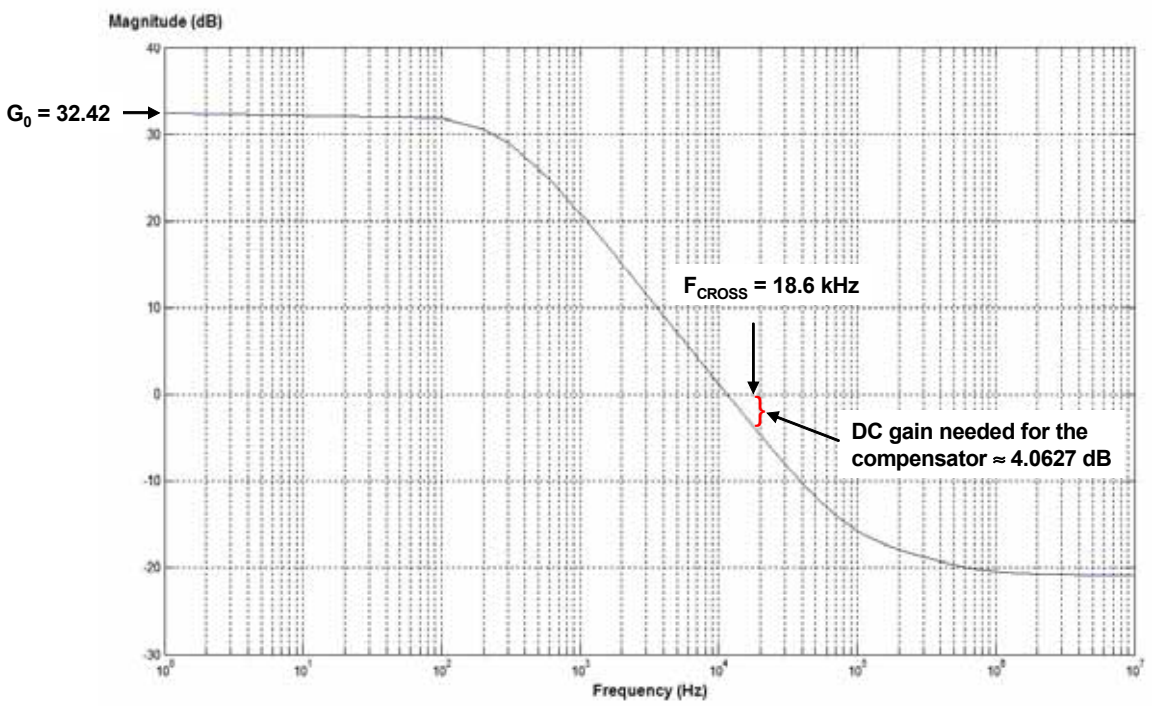


Figure 23. Transfer Function of G(s).

This DC gain needed for the compensator is actually the value of ***G***, whose value can be substituted above. As a result, R_{COMP} = 126.16 kΩ. A precision 130 kΩ @ 1% resistor is chosen.

The steps to calculate the compensation capacitors are as follows:

1. Knowing the frequency of the ***Right Half Plane Zero***,

$$F_{RHPZ} = \frac{\left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \times L} \times (1-D)^2 \approx 92.8\,\text{kHz}$$

2. Set a pole F_Z at the Right Half Plane Zero, $F_P = F_{RHZP}$, then:

$$C_{COMP2} = \frac{1}{2\pi \times R_{COMP} \times F_P} \cong 15\,\text{pF}$$

3. Set a zero at one fifth of the crossover frequency that compensates the pole, that comes from the output capacitor and the "load resistor = V_{OUT}/I_{OUT},

$$F_Z = \frac{F_{CROSS}}{5} \approx 3.7\,\text{kHz}$$

Then,

$$C_{COMP1} = \frac{1}{2\pi \times R_{COMP} \times F_Z} \cong 390\,\text{pF}$$

Note: Some jitter (noise) may be present in the switching frequency of the converter due to certain instability. The designer should corroborate this effect by using a spectrum analyzer. Using this instrument, the designer should play with

the value of the C_{COMP2} capacitor, until acquiring an appropriate stability of the converter. For the previous design a 56 pF capacitor was used.

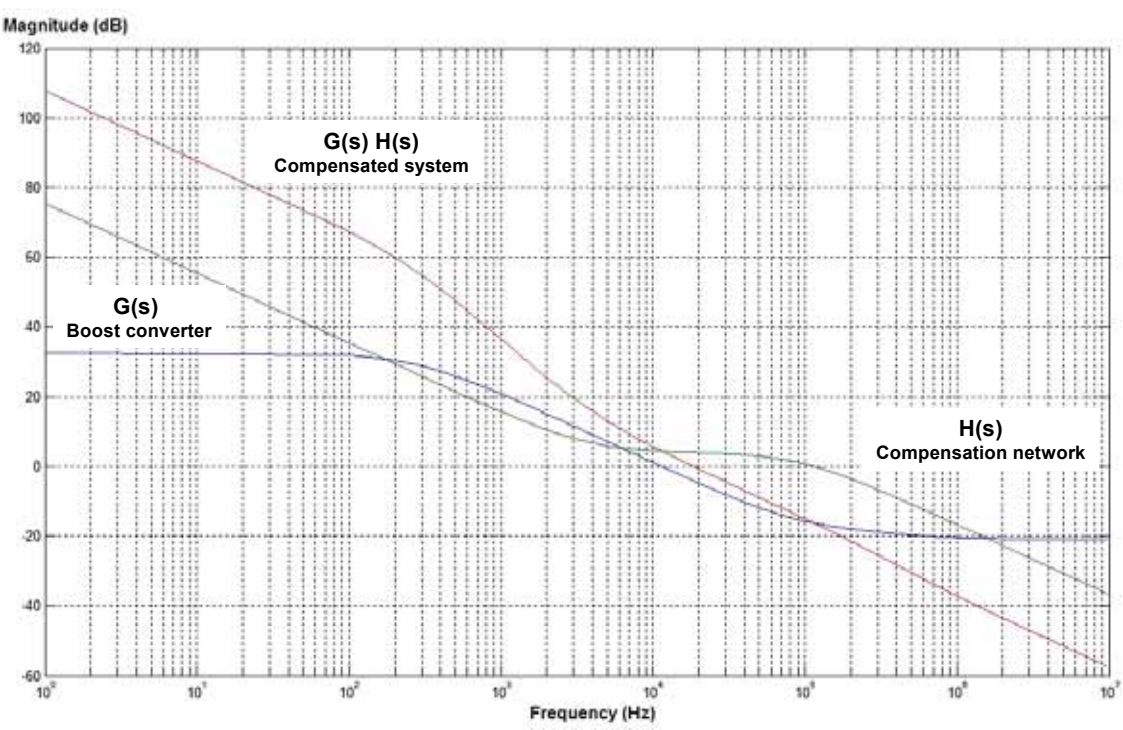


Figure 24. Plotting the Results for the Transconductance Op-amp Based Compensation Example.

SELECTING THE SLEW RATE OF THE SWITCHING RATE

The SLEW pin is used to limit the slew on the OUT_SW pin to reduce noise and avoid EMI problems. If the slew rate is reduced too much, it will reduce the efficiency of the device. The slew rate can be changed by tying a resistor from the SLEW pin to GND. The lower the value of this resistor, the steeper the rising and the falling times of the switching frequency. The value of this resistor could be within three different ranges:

- $R_{SLEW} < 10\ k\Omega$.
- $10\ k\Omega \leq R_{SLEW} < 20\ k\Omega$.
- $R_{SLEW} > 20\ k\Omega$.

SELECTING THE CS LOW PASS FILTER TO REDUCE NOISE.

Since any changes in the PCB layout (track length, grounding, component connections, etc.) around the switching FET and the current sense circuitry has an impact on the PCB parasitics, a low pass RC filter is recommended to be added at the CS pin for noise reduction.

The selection of this filter should be made based on the amplitude and frequency of the ringing across the sense resistor, so the noise can be attenuated properly while the current sense signal is kept as close as possible to its original shape (a trapezoid in CCM or a triangle in DCM). The ringing frequency should be attenuated by 20 dB at least through the selection of the proper low pass RC filter.

An example: let's assume that the sense signal (CS) shows a ringing of 60 MHz, and you want to attenuate it at a rate of 20 dB per decade. Based on these conditions, the cut-off frequency (-3.0 dB) of the low pass filter should be set to 6.0 MHz which still allows passing the maximum boost switching frequency signal of 1.2 MHz. The following formula is used for calculating the RC components:

$f\_3\ db = 1 / (2\pi RC)$

It is important to consider that the value of the resistor (R) should be no higher than 200 ohms, to avoid adding a significant offset in the CS signal. A resistor of 180 ohms is selected for this example. The capacitor (C) of the filter is then selected as follows:

$C = 1 / (2\pi * 180 * 6E6)$

$C = 147\ pf$

Once the filter is added on the CS pin, as shown on figures 20 and 21, measurements should be performed again to confirm that the noise has been reduced.

SELECTING SEMICONDUCTORS

Input Protection P-MOSFET

- V_{DSS} should be at least 1.5 times $V_{IN} \Rightarrow V_{DSS} \geq 1.5 \times 21.6\ V = 32.4\ V$.
- I_D should be higher than $I_{OUT}/(1\text{-}D) \Rightarrow I_D \geq 1.67\ A$
- The pulsed drain current capability of the MOSFET should be of several tens of amps due to the inrush current. If this current causes serious problems to the transistor during turn on, a small capacitor of approximately 100 nF can be placed in parallel with the triggering resistor RG1, to minimize and smooth such an effect.

As this transistor will be on at all times, the power dissipation must be considered ($I_D^2 \times R_{DS\text{-}ON}$), as well as the thermal dissipation pad.

Switching MOSFET

- V_{DSS} should be at least 1.5 times $V_{OUT} + V_D \Rightarrow V_{DSS} \geq 1.5 \times (39\ V + 0.7\ V) \approx 60\ V$
- I_D should be higher than,

$$\frac{I_{OUT}}{1-D} + \frac{\Delta I}{2}$$

$\Rightarrow I_D \geq 1.67 + 0.33 = 2.0\ A$

Switching Diode

- V_{RRM} should be at least 1.2 times than $V_{OUT} \Rightarrow V_{RRM} \geq 1.2 \times 39\ V \approx 47\ V$.
- $I_{F\text{-}AV}$ should be higher than,

$$\frac{I_{OUT}}{1-D} + \frac{\Delta I}{2}$$

$\Rightarrow I_{F\text{-}AV} \geq 1.67 + 0.33 = 2.0\ A$

PCB LAYOUT RECOMMENDATIONS

LAYOUT HINTS AND TIPS

- Connect the exposed pad of the IC to the ground planes of the board using as many vias as possible. These ground planes must be as large as possible to dissipate the heat from the IC.
- All references pins, i.e. PGND, AGND and DGND must be connected together. Their corresponding ground planes must be joined together with as many vias as possible.
- Try to place all components on just one Layer.
- When tracing differential pairs, it is advisable:
  - to know that routing between planes eliminates the potential for coupling external noise.
  - to route other signals al least 5*h* (microstrip) or 4*h* (stripline) away from the differential pairs.
  - to know that is it not essential to route them together, if the traces are inner layered and have the same length.
  - to design a PCB with 4 or more layers in order to get better results on the impedances of the traces (referenced to a next layer ground plane), as well as to minimize capacitive and inductive cross talk between layers. As a result, the following PCB layer stacking is suggested [3]:

Ground	Signal/Poured	Power	Signal/Power
Signal/Power	Ground	Signal/Ground	Ground
Signal/Power	Ground	Power	Signal/Power
Ground	Signal/Poured	Ground	Ground
		Signal/Power	Power
		Ground	Signal/Ground

Figure 25. Recommended PCB Layer Stacking.

- Never trace the Feedback and Control signals like CS, COMP, SLEW, GD and OVP close to the switching node.
- Make sure that each of the channel traces are capable of handling the LED currents. As a directly proportional reference, a 10 mils trace with a thickness of 1.0 oz/ft^2 is capable of handling one ampere.

REFERENCES

[1] MANIKTALA, Sanjaya. *Switching Power Supplies A to Z.* US: Newnes, 2006.

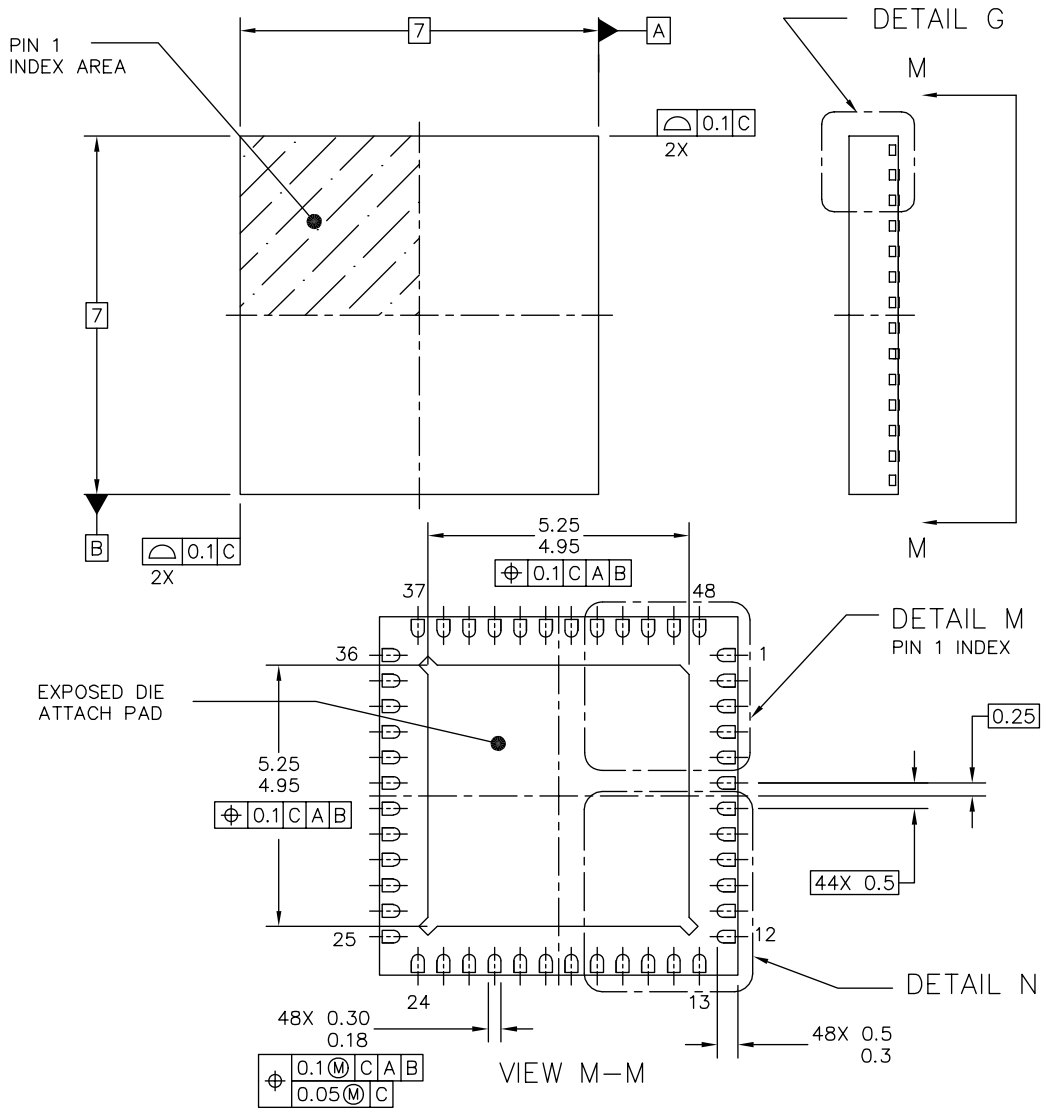
[2] ERICKSON, Robert W and MAKSIMOVIC, Dragan. *Fundamentals of Power Electronics*, Second Edition, University of Colorado.

[3] HARTLEY, Rick. *Signal Integrity and EMI Control in High Speed Circuits and PCBs.* US: Lectures notes for Freescale Semiconductor Mexico presentation,2008.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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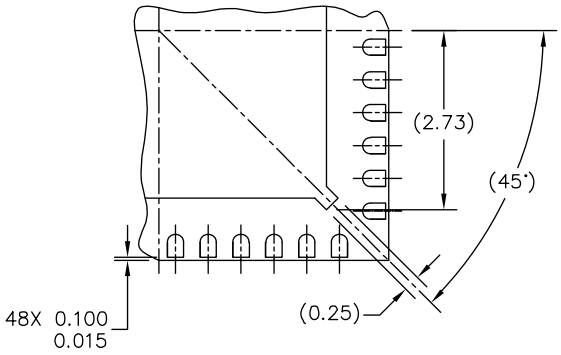
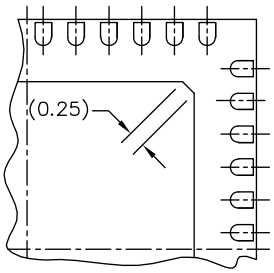
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

EP SUFFIX
48-PIN
98ARH99048A
REVISION F

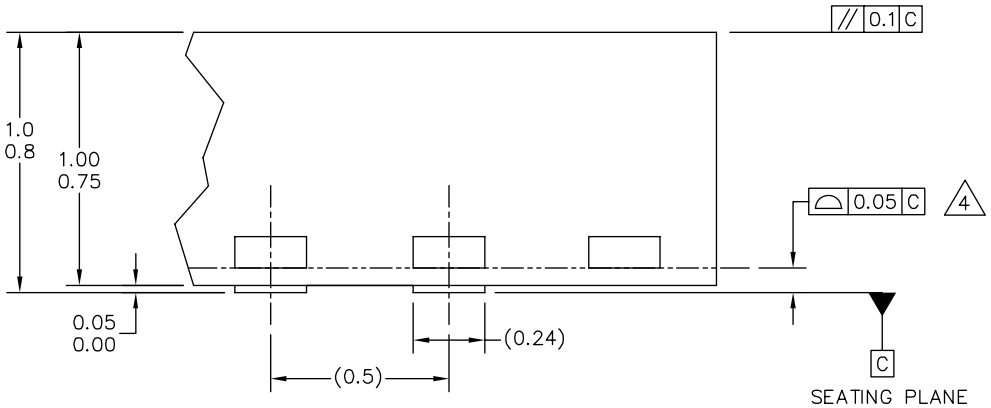
34848



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

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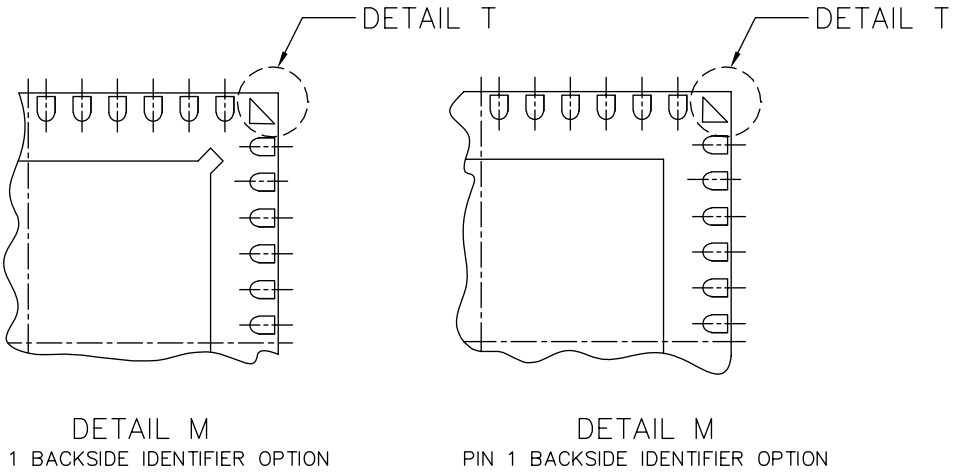
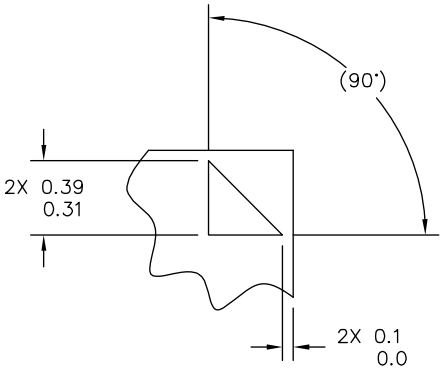
REVISION F





DETAIL T

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EP SUFFIX
48-PIN
98ARH99048A
REVISION F

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	5/2010	• Initial release

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Japan:
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Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
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