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Graphics Display Module

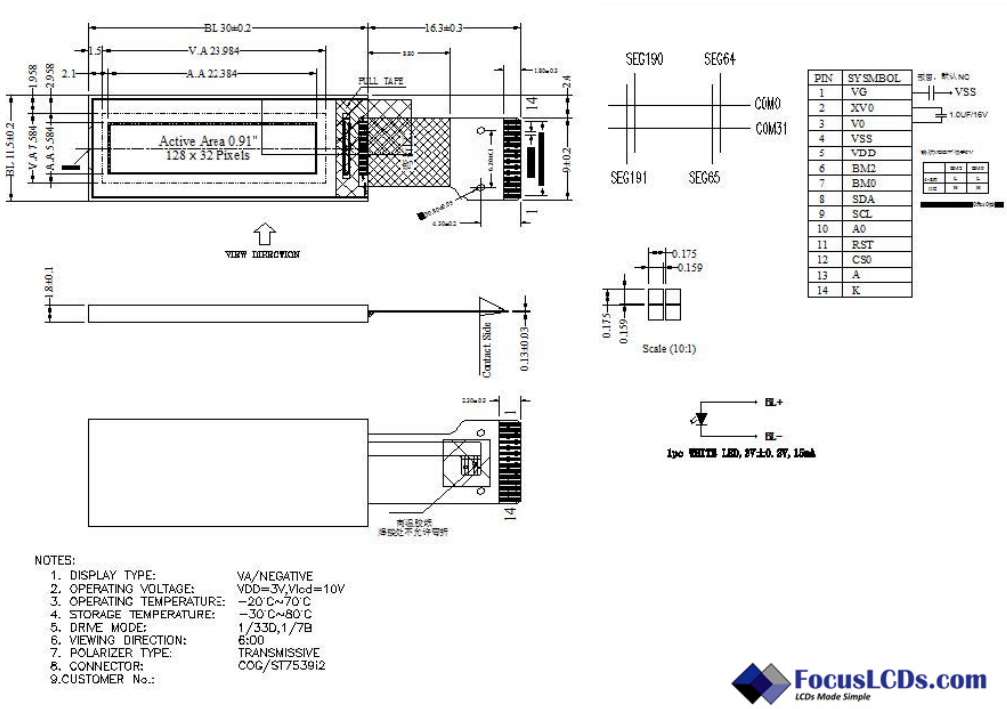
Part Number

G132AUGVKLW6WN33XAC

Overview

128X32(30x11.5), VATN, Black background, White LED, Bottom view, Wide temp, Transmissive (negative), 3.0V LCD, 3.0V LED, Controller=ST7539i2, RoHS Compliant

DIMENSIONAL OUTLINE



PIN	SYSMBOL
1	VG
2	XV0
3	V0
4	VSS
5	VDD
6	BM2
7	BM0
8	SDA
9	SCL
10	A0
11	RST
12	CS0
13	A
14	K

NOTES:

1.	DISPLAY TYPE:	VA/NEGATIVE
2.	OPERATING VOLTAGE:	VDD=3V,Vlcd=10V
3.	OPERATING TEMPERATURE:	-20°C~70°C
4.	STORAGE TEMPERATURE:	-30°C~80°C
5.	DRIVE MODE:	1/33D,1/7B
6.	VIEWING DIRECTION:	6:00
7.	POLARIZER TYPE:	TRANSMISSIVE
8.	CONNECTOR:	COG/ST7539i2
9.	CUSTOMER No.:	

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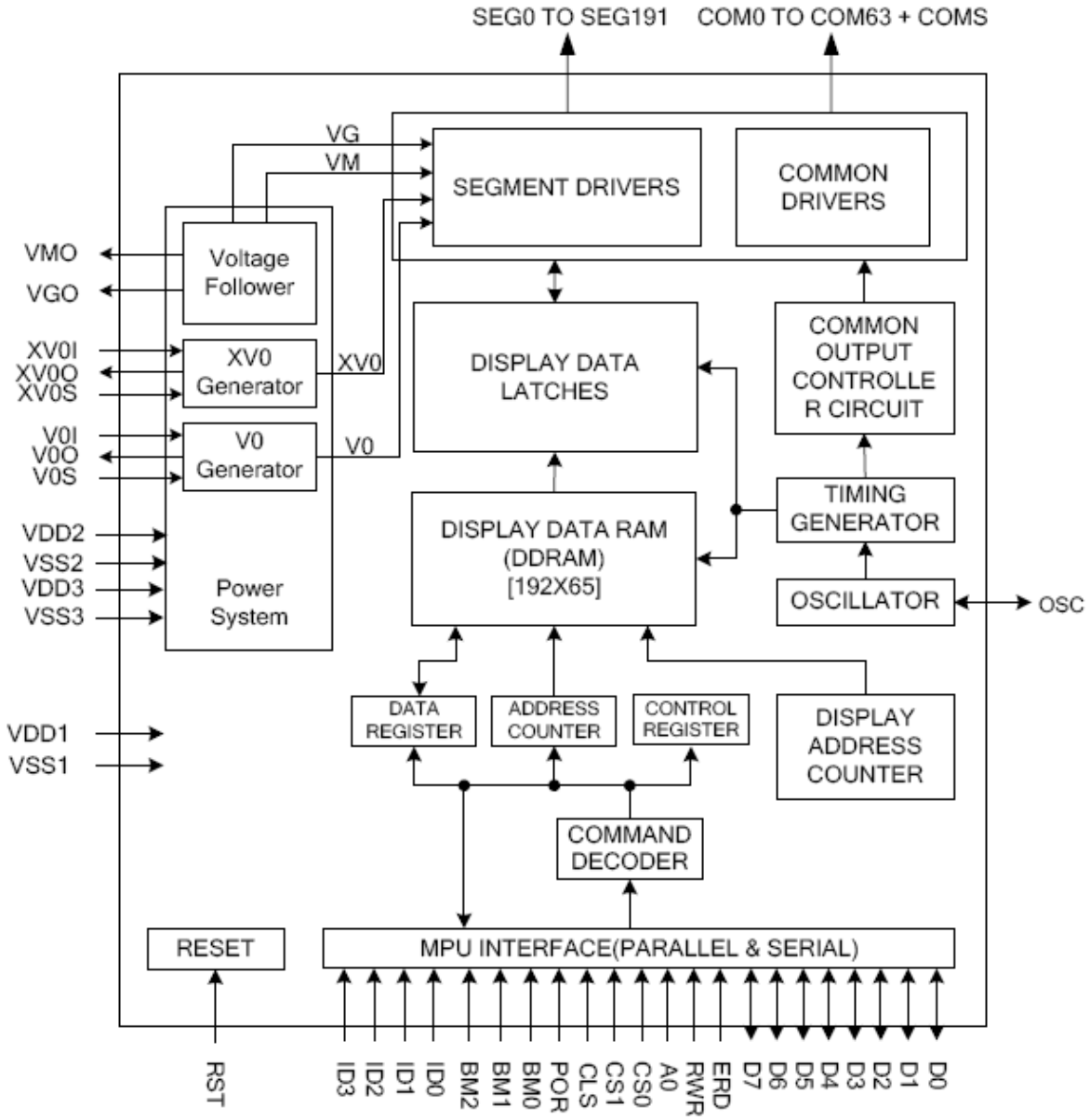
FUNCTIONS & FEATURES

2-1. Format	: 128X32 Dots
2-2. LCD mode	: VA, NEGATVE, TransmissiveMode
2-3. Viewing direction	: 6 o'clock
72-4. Driving scheme	: 1/33 Duty cycle, 1/7 Bias
2-5. Low power operation	: Power supply voltage range (V_{DD}): 3.0V
2-6. Operating temperature	: -20℃~70℃
2-7. Storage temperature	: -30℃~80℃

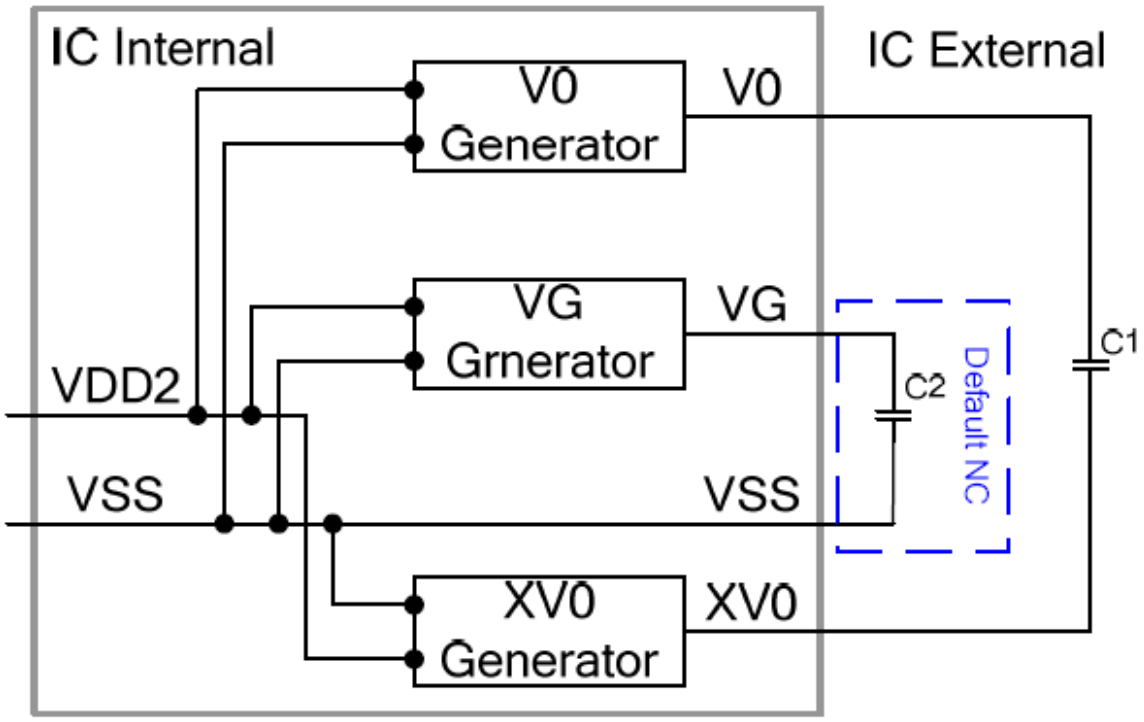
MECHANICAL SPECIFICATIONS

3-1. Module size	: 30.0mm(L)*11.5mm(W)*1.8mm(H)
3-2. Viewing area	: 23.984mm(L)*7.584mm(W)
3-3. Dot pitch	: 0.175mm(L)*0.175mm(W)
3-4. Dot size	: 0.159mm(L)*0.159mm(W)

BLOCK DIAGRAM



POWER SUPPLY



PIN DESCRIPTION

Pin no.	Symbol	Function
1	VG	LCD driving voltage for segments.
2	XVO	LCD driving voltage for commons at negative frame.
3	VO	LCD driving voltage for commons at negative frame.
4	VSS	Ground
5	VDD	Supply voltage for logic circuit +3.0V
6	BM2	Microprocessor interface select pins.
7	BM0	Microprocessor interface select pins.
8	SDA	Serial data input terminal
9	SCL	Serial clock input terminal
10	AO	Select register data when A0= “H”, and instruction when A0= “L”
11	RST	When RST is “L”, internal initialization is executed.
12	CS0	Interface access is enabled when CS0 is “L” and CS1 is “H” in parallel interface (8080/6800)and SPI interface (4-SPI).
13	A	Supply voltage for backlight +3V
14	K	Supply voltage for backlight Ground

MAXIMUM ABSOUTE LIMIT (T=25°C)

Item	Symbol	Standard value	Unit
Power supply voltage for logic	V_{DD}	-0.3~+3.1	V
LCD Power supply voltage	V0-XV0	-0.3~13.0	V
LCD Power driving voltage	VG,VM	-0.3~V_{DD}	V
Operating temperature	Topr	-20~+70	°C
Storage temperature	Tstg	-30~+80	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:

V0 ≥ VDD > VG > VM > VSS ≥ XV0

ELECTRICAL CHARACTERISTICS

DC Characteristics

VSS=VSS1=VSS2=VSS3=0V; Bare chip, Temp. = -30˚C to +85˚C; unless otherwise specified.

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		1.65	—	3.6	V	VDD1
Operating Voltage (2)	VDD2 VDD3		2.4	—	3.6	V	VDD2 VDD3
LCD Voltage	Vop		5.625	—	13.351	V	V0-XV0
Input High-Level Voltage	V_{IHC}		0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-Level Voltage	V_{ILC}		VSS1	—	0.3 x VDD1	V	MPU Interface
Output High-Level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V	0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-Level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V	VSS1	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		-1.0	—	1.0	μA	MPU Interface
LCD Driver ON Resistance	R_{ON}	Ta=25˚C, Vop=10V, ΔV=1.0V	—	0.7	—	KΩ	COMx
		Bias=1/9, VG=2.2V, ΔV=0.22V	—	0.7	—	KΩ	SEGx
Frame Frequency	fFR	1/65 Duty, FR[1:0]=(0,0), Ta = 25°C	72	76	80	Hz	

Note:

- The LCD Output Voltage (Vop) range of the measurement environment is as follows:
  V0 to XV0 : 1uF
- The maximum possible Vop voltage that may be generated is dependent on voltage, temperature and panel loading.

Bare chip current consumption with internal power system:

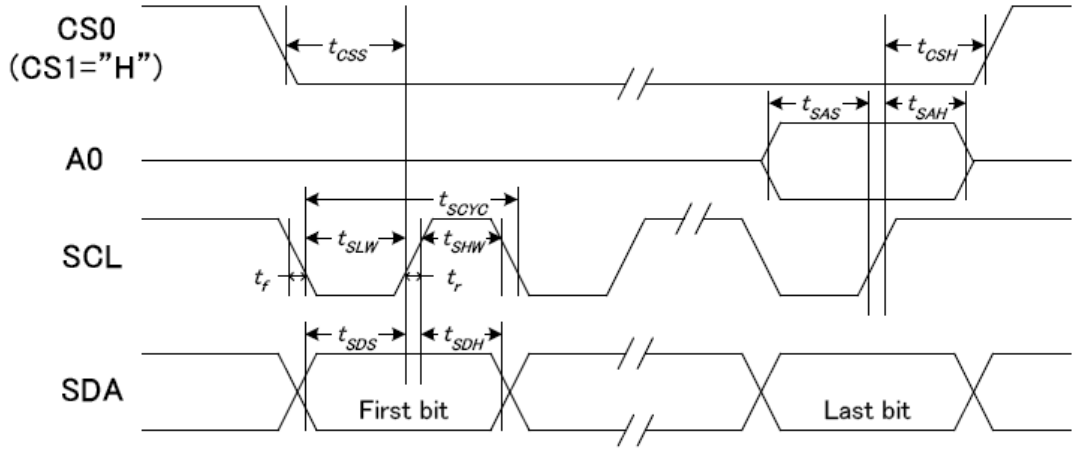
Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=VDD3=3V, Vop=10.977V, Bias=1/8, Frame Rate=76Hz, Ta=25˚C	—	150	220	μA	
Power Down	ISS	VDD1=VDD2=VDD3=3V, Ta=25˚C	—	1	5	μA	

Note:

The Current Consumption is DC characteristics.

AC Characteristics

SERIAL INTERFACE (4-Line Interface)



(VDD1 = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		60	-	ns
SCL "H" pulse width		tSHW		15	-	
SCL "L" pulse width		tSLW		15	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		10	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		15	-	
CS0 hold time		tCSH		10	-	

(VDD1 = 2.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		70	-	ns
SCL “H” pulse width		tSHW		20	-	
SCL “L” pulse width		tSLW		20	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		15	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		15	-	
CS0 hold time		tCSH		10	-	

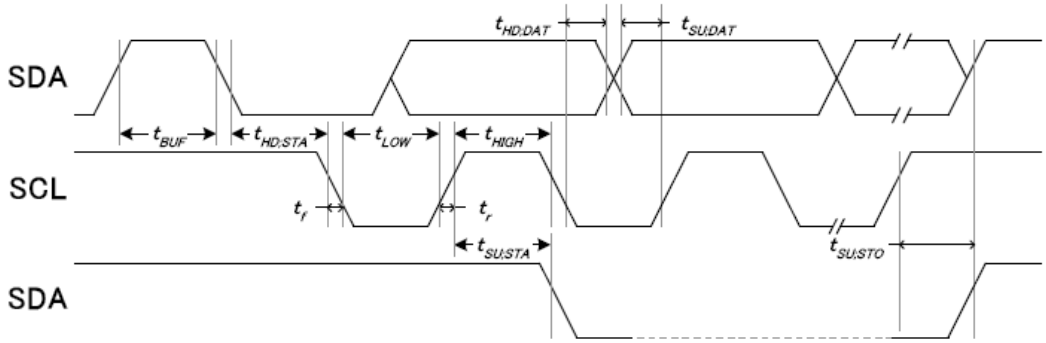
(VDD1 = 1.8V , Ta =25˚C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		110	-	ns
SCL “H” pulse width		tSHW		40	-	
SCL “L” pulse width		tSLW		40	-	
Address setup time	A0	tSAS		10	-	
Address hold time		tSAH		10	-	
Data setup time	SDA	tSDS		20	-	
Data hold time		tSDH		10	-	
CS0 setup time	CS0	tCSS		20	-	
CS0 hold time		tCSH		10	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the standard.
2. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

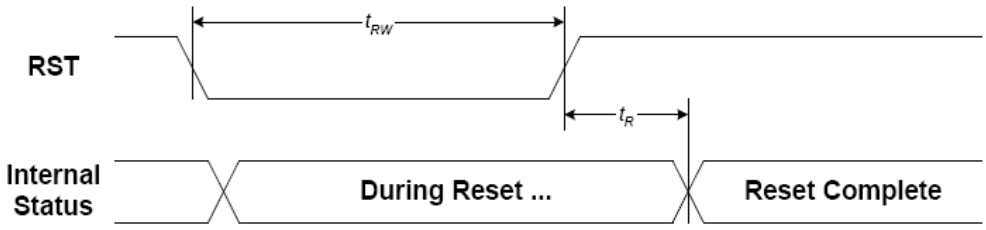
SERIAL INTERFACE (I^2C Interface)



(VDD1 = 1.8V ~ 3.3V, Ta=25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCL	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	-	
Data setup time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Signal rise time	SDA SCL	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

RESET TIMING



(VDD1 = 1.8V ~ 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	1	ms
Reset "L" pulse width	tRW		1	-	

9.CONTROL AND DISPLAY COMMAND

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	POR	0	0	0	ID3	ID2	ID1	
Read Status Byte (4-SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte Only for 4 line SPI
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	POR	0	0	0	ID3	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	1	1	1	1	Set test command table
			--	--	--	--	--	--	H1	H0	

Note: 1. Do not use instructions not listed in these tables (Command Table).

2. "--" = Disabled bit. It can be either logic 0 or 1.