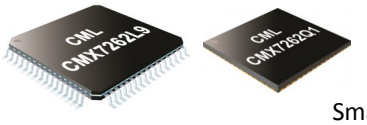
CML Microcircuits
COMMUNICATION SEMICONDUCTORS

Product Preview

PP7262/5 November 2013

CMX7262
TWELP™ Vocoder
Professional Radio Vocoder



Small 64-pin VQFN/LQFP Packages

Introduction

There is a growing requirement for digital voice communication and digital voice storage in the wireless communications market.

The new narrowband digital two-way radio systems aspire to provide all the advantages of digital communication as well as voice quality equal to that of the original analogue voice.

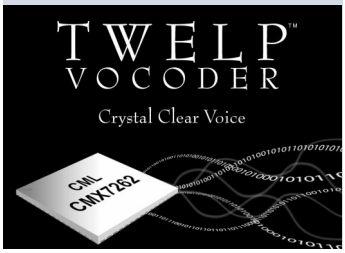
Low bit rate Vocoders have been around for some time but have found it difficult to achieve natural sounding voice reproduction and to allow the transportation of non-voice signals, sirens etc.

TWELP has been specifically designed to address these issues. The TWELP voice coding scheme is not a combination of old, well-known voice coding schemes.

TWELP it is a new state-of-the-art voice coding system, designed to meet the needs of the demanding digital wireless narrowband radio systems.

Applications

- Half duplex digital radio systems
- Personal area network voice links
- Secure digital voice communications
- Secure door access
- Wireless PBX
- VoIP applications
- Digital Software Defined Radio (SDR)



CMX7262 Brief Description

The CMX7262 TWELP Vocoder IC is a device supporting Tri-Wave Excited Linear Prediction (TWELP) vocoder functionality in a single chip. The CMX7262 is capable of encoding analogue voice into TWELP-encoded frames and decoding TWELP-encoded frames back to analogue voice.

TWELP is the latest state-of-the-art vocoder technology providing the highest quality natural sounding voice and good reproduction of non-voiced signals such as: police, fire and ambulance sirens. TWELP is also extremely tolerant to acoustic noise and includes an advanced noise reduction system to suppress background noise.

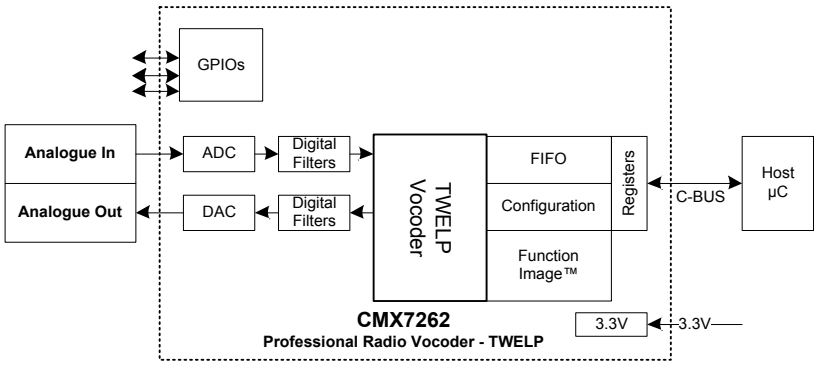
The robust FEC algorithm acts on individual vocoder frames for minimum latency and provides optimal performance mitigating bit errors inherent over narrowband radio channels. Modem soft decision bits are also supported to further maximise performance.

Input and output signals may be passed through the C-BUS interface or the on-chip analogue-to-digital and digital-to-analogue converters (ADC/DAC).

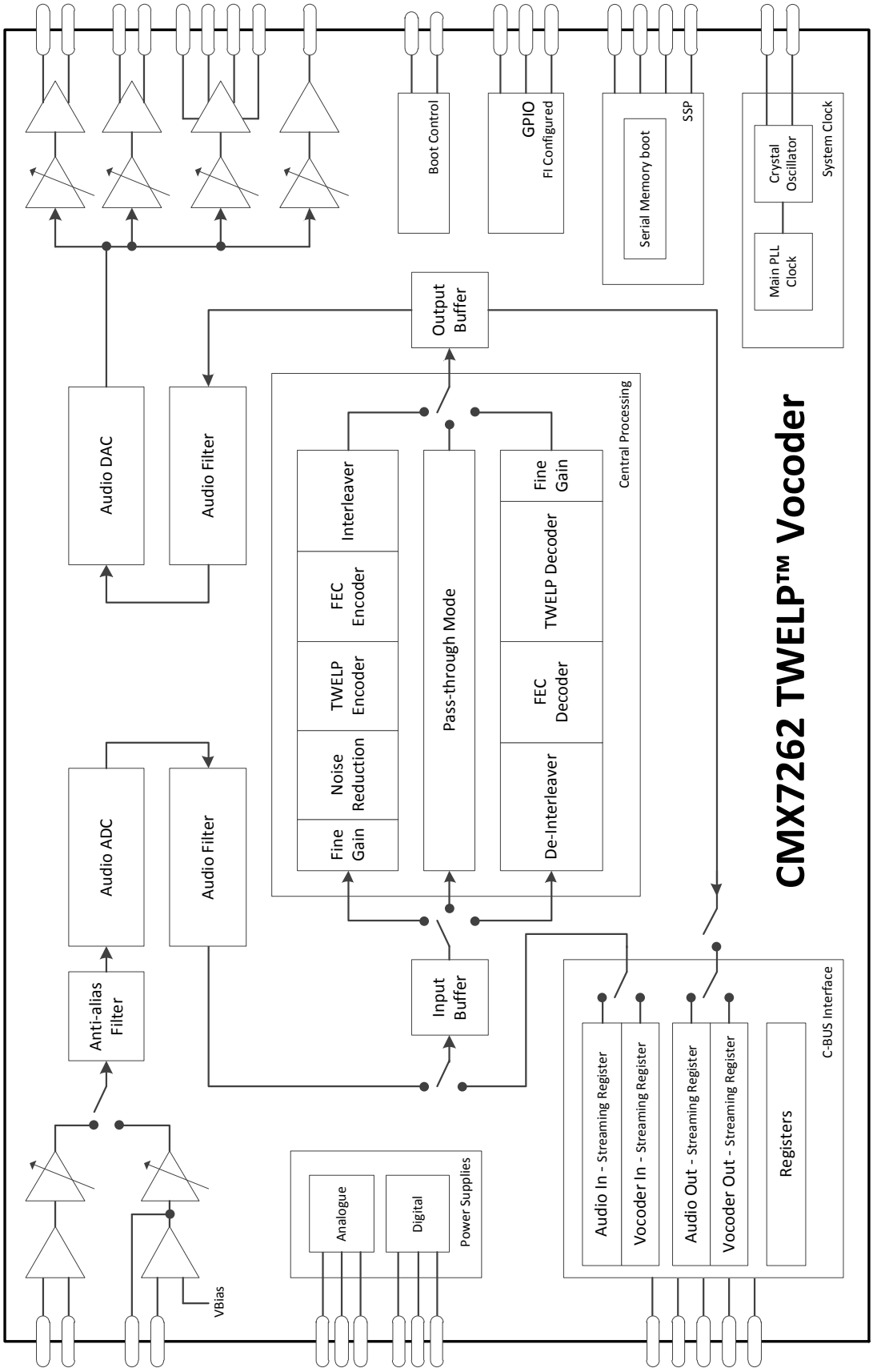
The CMX7262 operates from a 3.0 - 3.6V supply, includes selectable power saving modes and is available in 64-pin VQFN/LQFP packages.

Features

- High-performance, low bit rate (2.4kbps) vocoder
- Uses TWELP (Tri-wave Excited Linear Prediction) technology
- Crystal clear natural-sounding voice
- High quality non-voiced signals such as emergency services sirens
- Excellent performance in real-life radio operation
- Half-duplex operation
- FEC built in to each vocoder frame
- Noise Reduction system
- Integrated voiceband audio codec (no external DSP or codecs required)
- High speed serial interface (C-BUS) with streaming input/output registers
- Flexible signal input/output routing options, single ended, differential and a speaker driver.
- Choice of input/output sources – C-BUS transfer to host, analogue audio input/output
- Analogue input/output gain adjustment
- Low power 3.0V—3.6V operation with powersave functions
- Small 64-pin VQFN/LQFP packages



CMX7262 Block Diagram

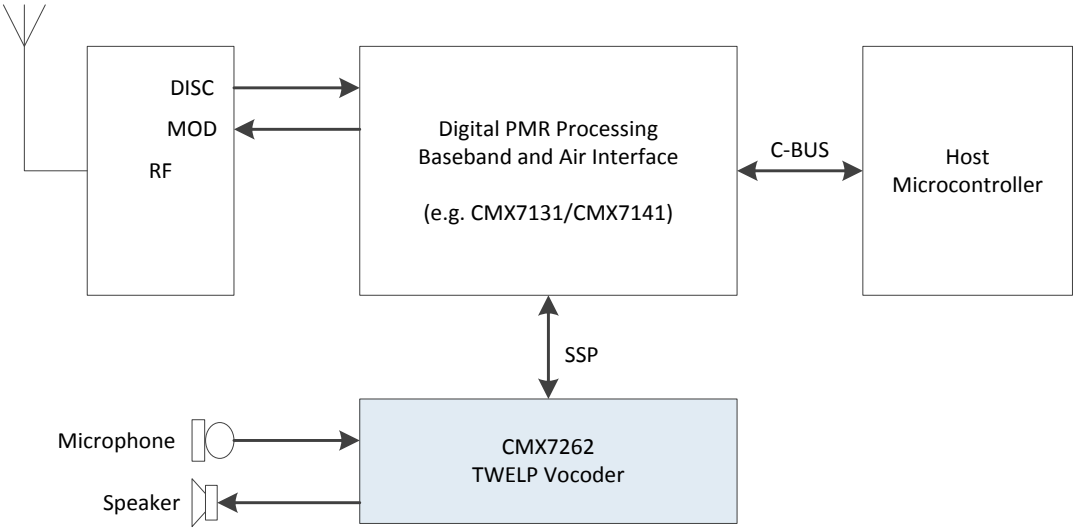


CMX7262 Demonstrator

The CMX7262 is designed to be flexible and easy to interface to a microcontroller or digital PMR baseband processor. The CMX7262 can interface directly to the CMX7131/7141 Digital PMR Processor to build a highly integrated digital PMR radio.

The device utilises CML's proprietary *FirmASIC* component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host microcontroller over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

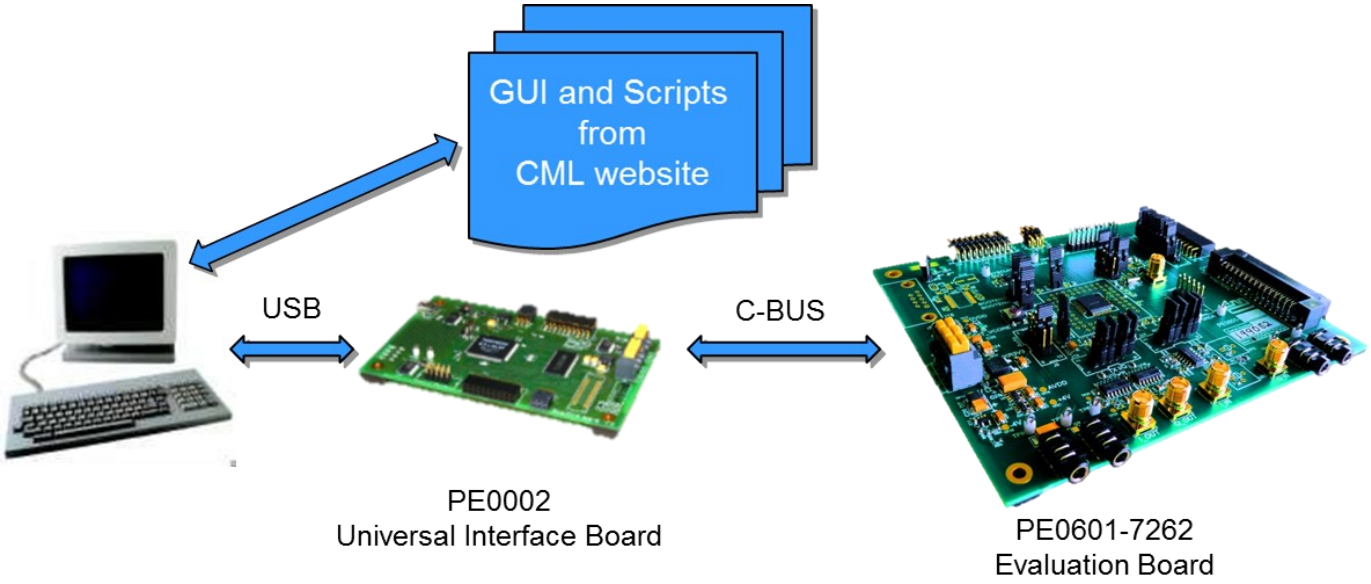
The CMX7262 Function Image™ (7262FI-1.x) can be downloaded from the CML technical portal (registration and access permissions are required).



Typical Digital PMR Implementation

Evaluation/Demonstration Support

Scripts are available for download from the CML Website to allow fast and easy demonstration of the core functions of the device.

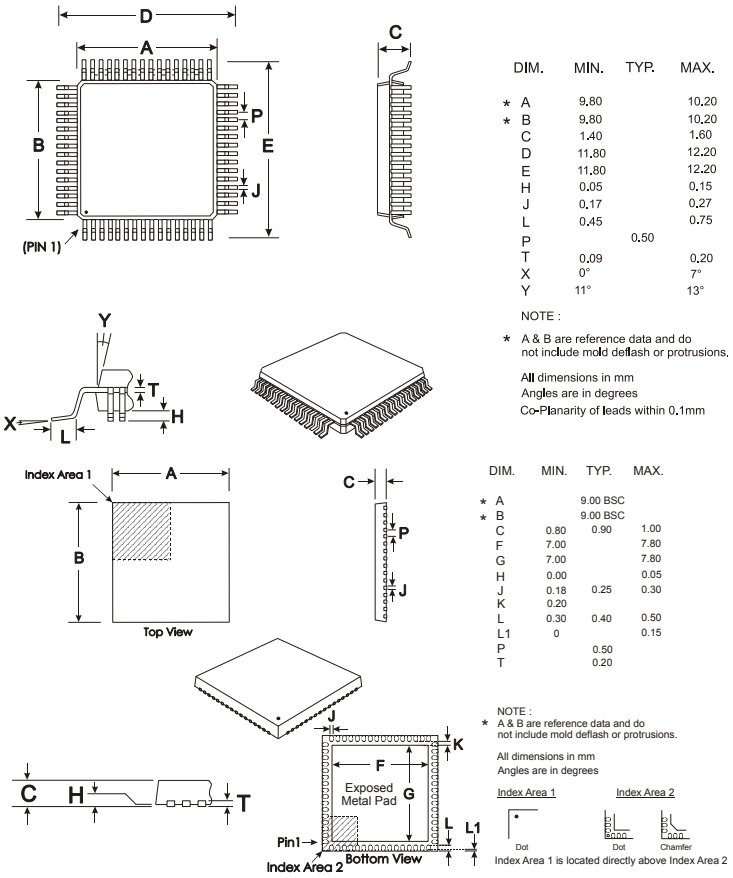


CMX7262 Electrical Specification Summary

Operating Limits	Min	Typ	Max	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$	3.0	3.3	3.6	V
$DV_{CORE} – DV_{SS}$	1.7	1.8	1.9	V
$AV_{DD} – AV_{SS}$	3.0	3.3	3.6	V
SPKR1 V_{DD} – SPKR1 V_{SS}	3.0	3.3	3.6	V
Operating Temperature	-40	-	+85	°C
Xtal Frequency	4.0	-	12.288	MHz
External Clock Frequency	9.6	-	24.576	MHz

DC Parameter - Supply Current	Min	Typ	Max	Unit
Encoding	-	23	-	mA
Decoding	-	10	-	mA
Analogue input port				
DI_{DD} (DV_{DD} = 1.8V)	-	4.5	-	mA
AI_{DD} (AV_{DD} = 3.3V)	-	3.3	-	mA
Analogue output port				
DI_{DD} (DV_{DD} = 1.8V)	-	0.7	-	mA
AI_{DD} (AV_{DD} = 3.3V)	-	4	-	mA

CMX7262 Package Options



DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

64-pin LQFP Mechanical Outline (L9)

Order as part no. CMX7262L9

DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

64-pin VQFN Mechanical Outline (Q1)

Order as part no. CMX7262Q1

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Comprehensive technical datasheet and support material is available from the CML website.

Click here to link to the CML website or search for: **CMX7262**

TWELP™ The TWELP™ voice coding technology embodied in this product is protected by intellectual property rights, copyrights and trade secrets of DSP Innovations, Inc. This technology is licensed solely for use within this microchip. The TWELP™ voice coding technology is provided by DSP Innovations, Inc. www.dspini.com, www.twelp.Pro.

Infinite Capabilities . . . FirmASIC® . . . Maximum Flexibility

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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