

NUP4102XV6

6-Pin Bi-Directional Quad TVS Array

This 6-Pin bi-directional transient suppressor array is designed for applications requiring transient overvoltage protection capability. It is intended for use in transient voltage and ESD sensitive equipment such as computers, printers, cell phones, medical equipment, and other applications. Its integrated design provides bi-directional protection for four separate lines using a single SOT-563 package. This device is ideal for situations where board space is a premium.

Features

- Bi-directional Protection for Four Lines in a Single SOT-563 Package
- Peak Power Dissipation – 75 W (8x20 μ sec Waveform)
- Low Leakage Current (100 nA @ 12 V)
- Low Capacitance (< 15 pF)
- Provides ESD Protection for JEDEC Standards JESD22
 - Machine Model = Class C
 - Human Body Model = Class 3B
- Provides ESD Protection for IEC 61000-4-2, 15 kV (Air), 8 kV (Contact)

Mechanical Characteristics

- Void Free, Transfer-Molded, Thermosetting Plastic Case
- Corrosion Resistant Finish, Easily Solderable
- Package Designed for Optimal Automated Board Assembly
- Small Package Size for High Density Applications

Applications

- GSM Handsets and Accessories
- Other Telephone Sets
- Computers / Printers / Set-Top Boxes

MAXIMUM RATINGS ($T_J=25^\circ\text{C}$, unless otherwise specified)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8x20 μ sec Double Exponential Waveform, (Note 1)	P_{PK}	75	W
Operating Junction Temperature Range	T_J	-40 to 125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 sec)	T_L	260	$^\circ\text{C}$
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Air (ESD) IEC 61000-4-2 Contact (ESD)	ESD	16 0.4 30 30	kV

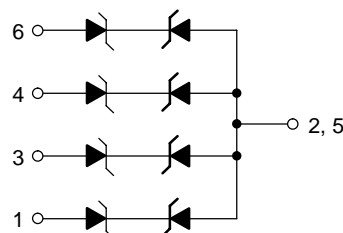
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Non-repetitive current pulse per Figure 3.



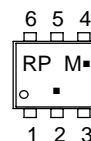
ON Semiconductor[®]

<http://onsemi.com>



**SOT-563
CASE 463A
PLASTIC**

MARKING DIAGRAM



RP = Device Marking
M = One Digit Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NUP4102XV6T1G	SOT-563 (Pb-Free)	4000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP4102XV6

ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	(Note 2)	V _{RWM}			12	V
Breakdown Voltage	I _T = 1 mA, (Note 3)	V _{BR}	13.6		17.8	V
Reverse Leakage Current	V _{RWM} = 12 V	I _R		10	100	nA
Clamping Voltage	I _{PP} = 3 A, (8x20 μsec Waveform)	V _C			25	V
Maximum Peak Pulse Current	8x20 μsec waveform	I _{PP}			3.0	A
Capacitance	V _R = 0 V, f=1 MHz (Line to GND)	C _j		13	15	pF

- TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
- V_{BR} is measured at pulse test current I_T; Pulse Width 1 ms.

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise specified)

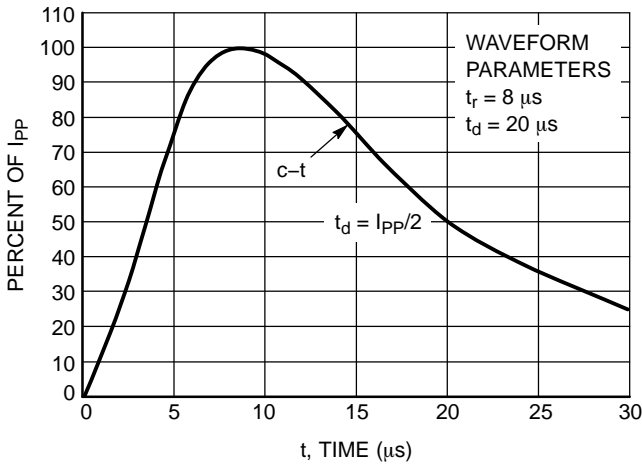


Figure 1. Pulse Waveform

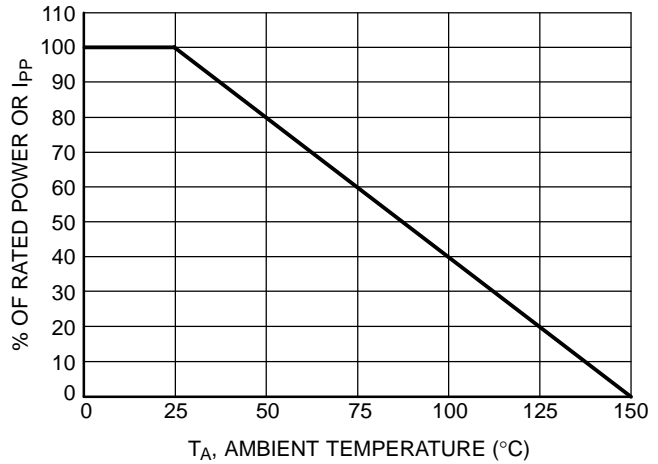


Figure 2. Power Derating Curve

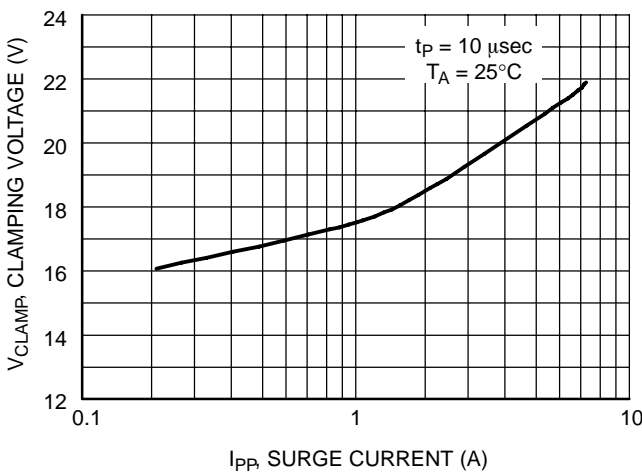


Figure 3. Clamping Voltage vs. Peak Pulse Current (10 μsec Square Wave Pulse)

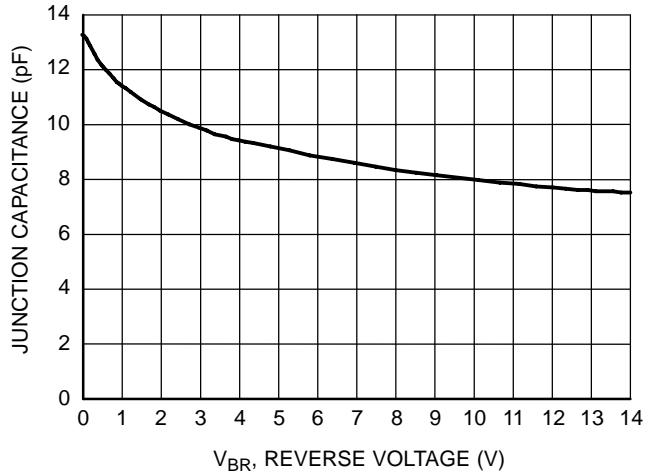
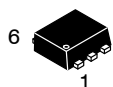


Figure 4. Junction Capacitance vs. Reverse Voltage

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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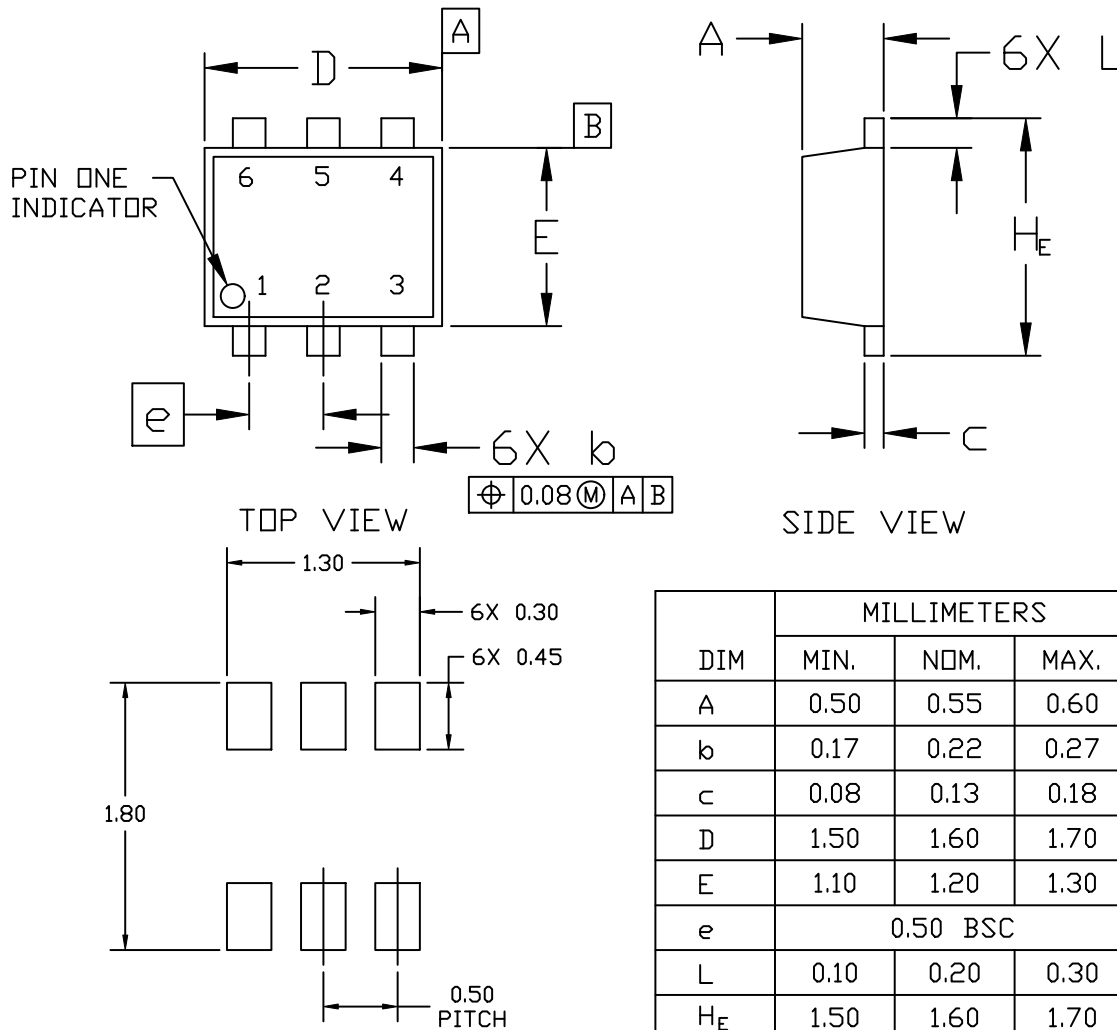
SCALE 4:1

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ISSUE H

DATE 26 JAN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

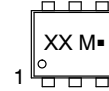
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***



XX = Specific Device Code
M = Month Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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