ISL62875

PWM DC/DC Controller with VID Inputs for Portable GPU Core-Voltage Regulator

FN6905
Rev 1.00
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The ISL62875 is a Single-Phase Synchronous-Buck PWM voltage regulator featuring Intersil's Robust Ripple Regulator (R^3) Technology™. The wide 3.3V to 25V input voltage range is ideal for systems that run on battery or AC-adapter power sources. The ISL62875 is a low-cost solution for applications requiring dynamically selected slew-rate controlled output voltages. The soft-start and dynamic setpoint slew-rates are capacitor programmed. Voltage identification logic-inputs select four resistor-programmed setpoint reference voltages that directly set the output voltage of the converter between 0.5V to 1.5V, and up to 3.3V using a feedback voltage divider. Robust integrated MOSFET drivers and Schottky bootstrap diode reduce the implementation area and component cost.

Intersil's R^3 Technology™ combines the best features of both fixed-frequency and hysteretic PWM control. The PWM frequency is 500kHz during static operation, becoming variable during changes in load, setpoint voltage, and input voltage when changing between battery and AC-adapter power. The modulators ability to change the PWM switching frequency during these events in conjunction with external loop compensation produces superior transient response. For maximum efficiency, the converter automatically enters diode-emulation mode (DEM) during light-load conditions such as system standby.

Features

- Input Voltage Range: 3.3V to 25V
- Output Voltage Range: 0.5V to 3.3V
- Output Load up to 30A
- Extremely Flexible Output Voltage Programmability
  - 2-Bit VID Selects Four Independent Setpoint Voltages
  - Simple Resistor Programming of Setpoint Voltages
  - Accepts External Setpoint Reference such as DAC
- ±0.75% System Accuracy: -10°C to +100°C
- Fixed 500kHz PWM Frequency in Continuous Conduction
- Integrated High-current MOSFET Drivers and Schottky Boot-Strap Diode for Optimal Efficiency

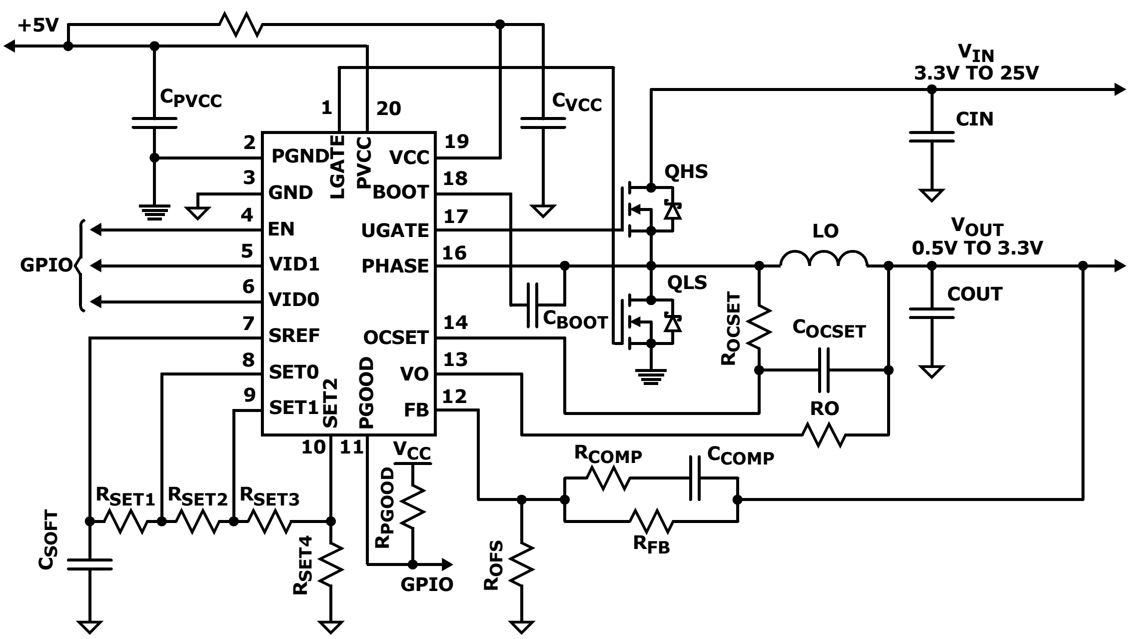
Applications* (see page 21)

- Mobile PC GPU Core Power
- Mobile PC I/O Controller Hub (ICH) VCC Rail
- Tablet PCs/Slates and Netbooks
- Hand-Held Portable Instruments

Related Literature* (see page 21)

- TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"

Typical Application



Application Schematics

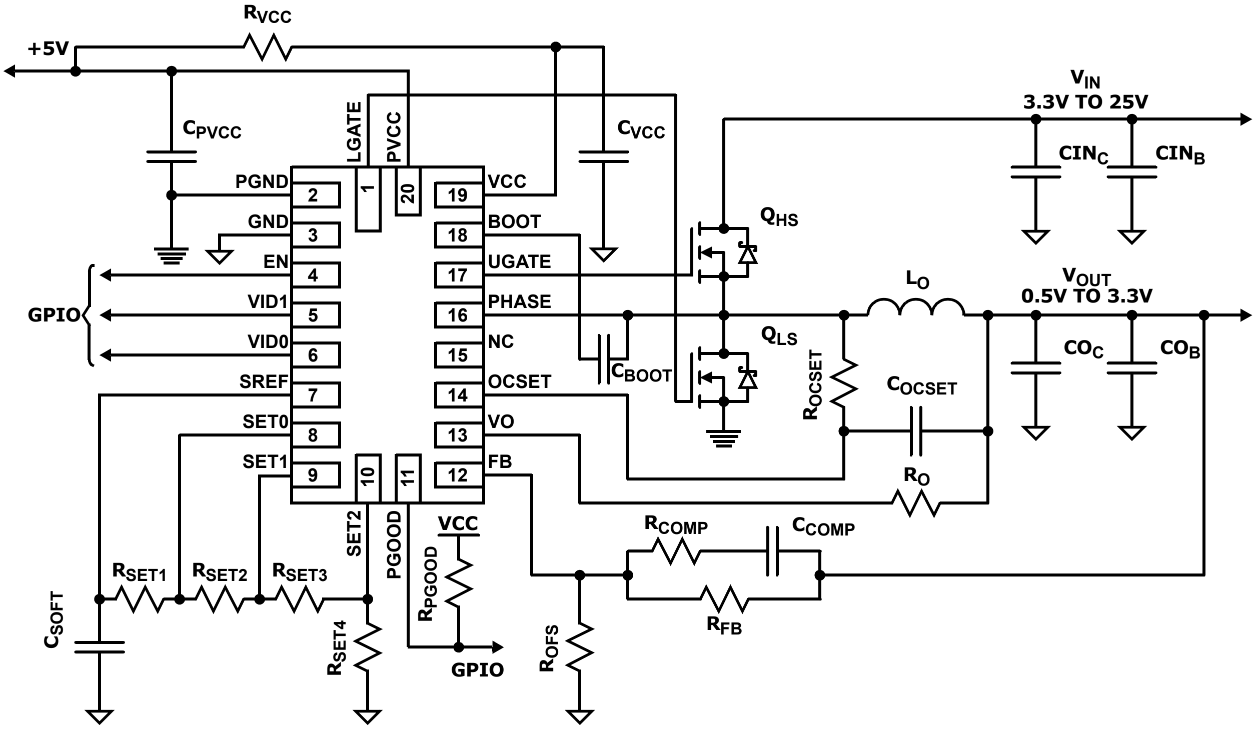


FIGURE 1. ISL62875 APPLICATION SCHEMATIC WITH FOUR OUTPUT VOLTAGE SETPOINTS AND DCR CURRENT SENSE

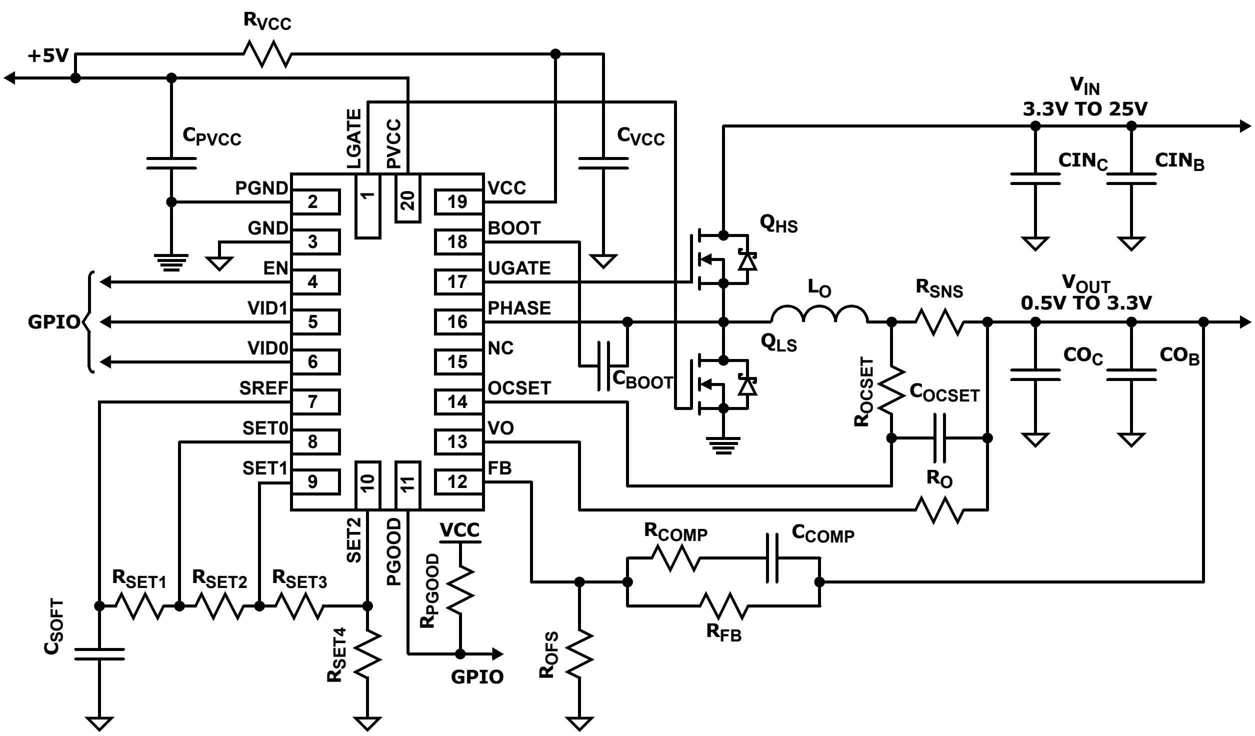


FIGURE 2. ISL62875 APPLICATION SCHEMATIC WITH FOUR OUTPUT VOLTAGE SETPOINTS AND RESISTOR CURRENT SENSE

Application Schematics (Continued)

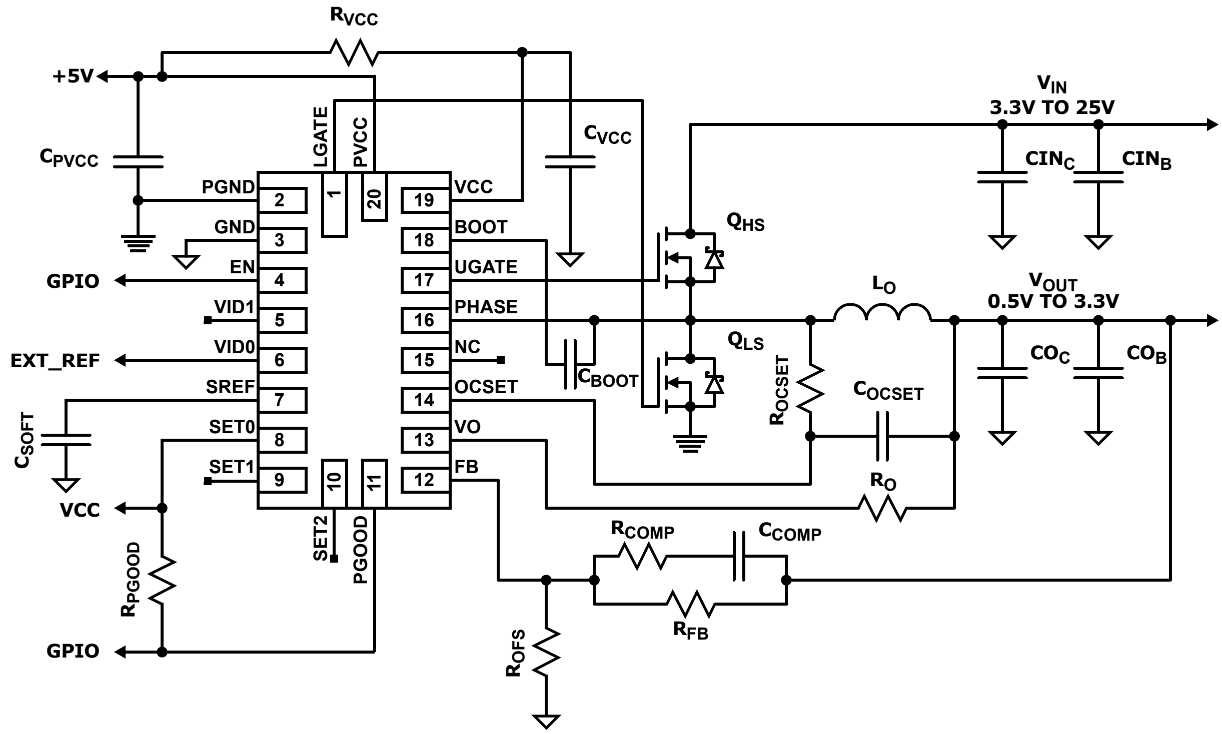


FIGURE 3. ISL62875 APPLICATION SCHEMATIC WITH EXTERNAL REFERENCE INPUT AND DCR CURRENT SENSE

Block Diagram

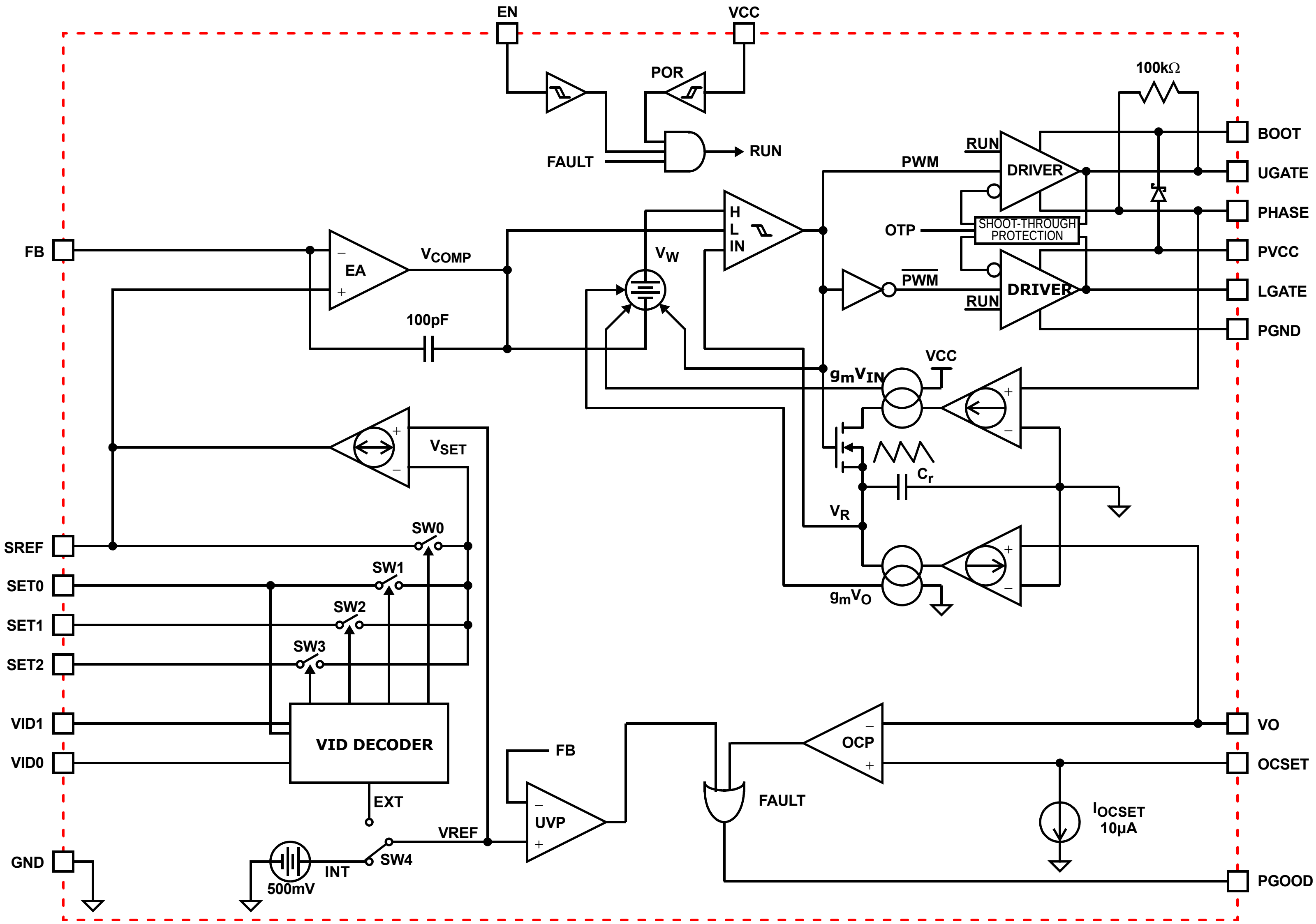
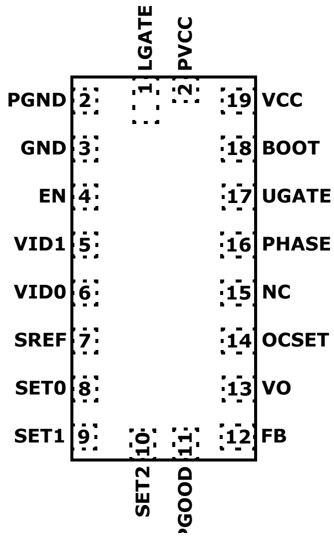


FIGURE 4. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF ISL62875

Pin Configuration

ISL62875
(20 LD 3.2X1.8 MTQFN)
TOP VIEW



ISL62875 Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	LGATE	Low-side MOSFET gate driver output. Connect to the gate terminal of the low-side MOSFET of the converter.
2	PGND	Return current path for the LGATE MOSFET driver. Connect to the source of the low-side MOSFET.
3	GND	IC ground for bias supply and signal reference.
4	EN	Enable input for the IC. Pulling EN above the V_{ENTHR} rising threshold voltage initializes the soft-start sequence.
5	VID1	Logic input for setpoint voltage selector. Use in conjunction with the VID0 pin to select among four setpoint reference voltages.
6	VID0	Logic input for setpoint voltage selector. Use in conjunction with the VID1 pin to select among four setpoint reference voltages. External reference input when enabled by connecting the SET0 pin to the VCC pin.
7	SREF	Soft-start and voltage slew-rate programming capacitor input. Setpoint reference voltage programming resistor input. Connects internally to the inverting input of the V_{SET} voltage setpoint amplifier.
8	SET0	Voltage set-point programming resistor input.
9	SET1	Voltage set-point programming resistor input.
10	SET2	Voltage set-point programming resistor input.
11	PGOOD	Power-good open-drain indicator output. This pin changes to high impedance when the converter is able to supply regulated voltage. The pull-down resistance between the PGOOD pin and the GND pin identifies which protective fault has shut down the regulator.
12	FB	Voltage feedback sense input. Connects internally to the inverting input of the control-loop error amplifier. The converter is in regulation when the voltage at the FB pin equals the voltage on the SREF pin. The control loop compensation network connects between the FB pin and the converter output.
13	VO	Output voltage sense input for the R^3 modulator. The VO pin also serves as the reference input for the overcurrent detection circuit.

ISL62875 Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
14	OCSET	Input for the overcurrent detection circuit. The overcurrent setpoint programming resistor R_{OCSET} connects from this pin to the sense node.
15	NC	No internal connection. Pin 15 should be connected to the GND pin.
16	PHASE	Return current path for the UGATE high-side MOSFET driver. V_{IN} sense input for the R^3 modulator. Inductor current polarity detector input. Connect to junction of output inductor, high-side MOSFET, and low-side MOSFET. See Figures 1 and 2 on page 2.
17	UGATE	High-side MOSFET gate driver output. Connect to the gate terminal of the high-side MOSFET of the converter.
18	BOOT	Positive input supply for the UGATE high-side MOSFET gate driver. The BOOT pin is internally connected to the cathode of the Schottky boot-strap diode. Connect an MLCC between the BOOT pin and the PHASE pin.
19	VCC	Input for the IC bias voltage. Connect +5V to the VCC pin and decouple with at least a 1µF MLCC to the GND pin. See “Application Schematics” (Figures 1 and 2) on page 2.
20	PVCC	Input for the LGATE and UGATE MOSFET driver circuits. The PVCC pin is internally connected to the anode of the Schottky boot-strap diode. Connect +5V to the PVCC pin and decouple with a 10µF MLCC to the PGND pin. See “Application Schematics” (Figures 1 and 2) on page 2.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL62875HRUZ-T*	GAR	-10 to +100	20 Ld 3.2x1.8 µTQFN (Tape and Reel)	L20.3.2x1.8

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62875. For more information on MSL please see techbrief TB363.

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Absolute Maximum Ratings

VCC, PVCC, PGOOD to GND. . . . . -0.3V to +7.0V
VCC, PVCC to PGND . . . . -0.3V to +7.0V
GND to PGND . . . . -0.3V to +0.3V
EN, SET0, SET1, SET2, VO,
VID0, VID1, FB, OCSET, SREF . . . -0.3V to GND, VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . -0.3V to 33V
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage . . . . GND - 0.3V to 28V
GND -8V (<20ns Pulse Width, 10µJ)
UGATE Voltage. . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
20 Ld µTQFN Package (Notes 4, 5). 84
Junction Temperature Range . . . . -55°C to +150°C
Operating Temperature Range . . . . -10°C to +100°C
Storage Temperature. . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range . . . . -10°C to +100°C
Converter Input Voltage to GND . . . . 3.3V to 25V
VCC, PVCC to GND . . . . .5V ±5%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
VCC and PVCC						
VCC Input Bias Current	I_{VCC}	EN = 5V, VCC = 5V, FB = 0.55V, SREF < FB	-	1.1	**1.5**	mA
VCC Shutdown Current	I_{VCCoff}	EN = GND, VCC = 5V	-	0.1	**1.0**	µA
PVCC Shutdown Current	$I_{PVCCoff}$	EN = GND, PVCC = 5V	-	0.1	**1.0**	µA
VCC POR THRESHOLD						
Rising VCC POR Threshold Voltage	V_{VCC_THR}		**4.40**	4.49	**4.60**	V
Falling VCC POR Threshold Voltage	V_{VCC_THF}		**4.10**	4.22	**4.35**	V
REGULATION						
Reference Voltage	$V_{REF(int)}$		-	0.50	-	V
System Accuracy		VID0 = VID1 = GND, PWM Mode = CCM	**-0.75**	-	**+0.75**	%
PWM						
Switching Frequency	F_{SW}	PWM Mode = CCM	**450**	500	**550**	kHz
VO						
VO Input Voltage Range	V_{VO}		**0**	-	**3.6**	V
VO Input Impedance	R_{VO}	EN = 5V	-	600	-	kΩ
VO Reference Offset Current	I_{VOSS}	V_{ENTHR} < EN, SREF = Soft-Start Mode	-	10	-	µA
VO Input Leakage Current	I_{VOoff}	EN = GND, VO = 3.6V	-	0.1	-	µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}	EN = 5V, FB = 0.50V	**-20**	-	**+50**	nA
SREF						
SREF Operating Voltage Range	V_{SREF}	Nominal SREF Setting with 1% Resistors	**0.5**	-	**1.5**	V
Soft-Start Current	I_{SS}	SREF = Soft-Start Mode	**10**	20	**30**	µA

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Voltage Step Current	I_{VS}	SREF = Setpoint-Stepping Mode	**±60**	±100	**±140**	µA
EXTERNAL REFERENCE						
EXTREF Operating Voltage Range	V_{EXT}	SET0 = VCC	**0**	-	**1.5**	V
EXTREF Accuracy	V_{EXT_OFS}	SET0 = VCC, VID0 = 0V to 1.5V	**-0.5**	-	**+0.5**	%
POWER GOOD						
PGOOD Pull-down Impedance	R_{PG_SS}	PGOOD = 5mA Sink	**75**	95	**150**	Ω
	R_{PG_UV}	PGOOD = 5mA Sink	**75**	95	**150**	Ω
	R_{PG_OV}	PGOOD = 5mA Sink	**50**	65	**90**	Ω
	R_{PG_OC}	PGOOD = 5mA Sink	**25**	35	**50**	Ω
PGOOD Leakage Current	I_{PG}	PGOOD = 5V	**-**	0.1	**1.0**	µA
PGOOD Maximum Sink Current (Note 6)	I_{PG_max}		**-**	5.0	**-**	mA
GATE DRIVER						
UGATE Pull-Up Resistance (Note 6)	R_{UGPU}	200mA Source Current	**-**	1.0	**1.5**	Ω
UGATE Source Current (Note 6)	I_{UGSRC}	UGATE - PHASE = 2.5V	**-**	2.0	**-**	A
UGATE Sink Resistance (Note 6)	R_{UGPD}	250mA Sink Current	**-**	1.0	**1.5**	Ω
UGATE Sink Current (Note 6)	I_{UGSNK}	UGATE - PHASE = 2.5V	**-**	2.0	**-**	A
LGATE Pull-Up Resistance (Note 6)	R_{LGPU}	250mA Source Current	**-**	1.0	**1.5**	Ω
LGATE Source Current (Note 6)	I_{LGSRC}	LGATE - GND = 2.5V	**-**	2.0	**-**	A
LGATE Sink Resistance (Note 6)	R_{LGPD}	250mA Sink Current	**-**	0.5	**0.9**	Ω
LGATE Sink Current (Note 6)	I_{LGSNK}	LGATE - PGND = 2.5V	**-**	4.0	**-**	A
UGATE to LGATE Deadtime	t_{UGFLGR}	UGATE falling to LGATE rising, no load	**-**	21	**-**	ns
LGATE to UGATE Deadtime	t_{LGFUGR}	LGATE falling to UGATE rising, no load	**-**	21	**-**	ns
PHASE						
PHASE Input Impedance	R_{PHASE}		**-**	33	**-**	kΩ
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA	**-**	0.58	**-**	V
Reverse Leakage	I_R	V_R = 25V	**-**	0.2	**-**	µA
CONTROL INPUTS						
EN High Threshold Voltage	V_{ENTHR}		**2.0**	-	**-**	V
EN Low Threshold Voltage	V_{ENTHF}		**-**	-	**1.0**	V
EN Input Bias Current	I_{EN}	EN = 5V	**1.5**	2.0	**2.5**	µA
EN Leakage Current	I_{ENoff}	EN = GND	**-**	0.1	**1.0**	µA
VID<0,1> High Threshold Voltage	V_{VIDTHR}		**0.6**	-	**-**	V
VID<0,1> Low Threshold Voltage	V_{VIDTHF}		**-**	-	**0.5**	V
VID<0,1> Input Bias Current	I_{VID}	EN = 5V, V_{VID} = 1V	**-**	0.5	**-**	µA
VID<0,1> Leakage Current	I_{VIDoff}		**-**	0	**-**	µA

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
PROTECTION						
OCP Threshold Voltage	V_{OCPTH}	V_{OCSET} - V_O	**-1.75**	-	**1.75**	mV
OCP Reference Current	I_{OCP}	EN = 5.0V	**9.0**	10	**11**	µA
OCSET Input Resistance	R_{OCSET}	EN = 5.0V	**-**	600	**-**	kΩ
OCSET Leakage Current	I_{OCSET}	EN = GND	**-**	0	**-**	µA
UVP Threshold Voltage	V_{UVTH}	V_{FB} = %V_{SREF}	**81**	84	**87**	%
OTP Rising Threshold Temperature (Note 6)	T_{OTRTH}		**-**	150	**-**	°C
OTP Hysteresis (Note 6)	T_{OTHYS}		**-**	25	**-**	°C

NOTES:

6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Theory of Operation

The modulator features Intersil's R^3 Robust-Ripple-Regulator technology, a hybrid of fixed frequency PWM control and variable frequency hysteretic control. The PWM frequency is maintained at 500kHz under static continuous-conduction-mode operation within the entire specified envelope of input voltage, output voltage, and output load. If the application should experience a rising load transient and/or a falling line transient such that the output voltage starts to fall, the modulator will extend the on-time and/or reduce the off-time of the PWM pulse in progress. Conversely, if the application should experience a falling load transient and/or a rising line transient such that the output voltage starts to rise, the modulator will truncate the on-time and/or extend the off-time of the PWM pulse in progress. The period and duty cycle of the ensuing PWM pulses are optimized by the R^3 modulator for the remainder of the transient and work in concert with the error amplifier V_{ERR} to maintain output voltage regulation. Once the transient has dissipated and the control loop has recovered, the PWM frequency returns to the nominal static 500kHz.

Modulator

The R^3 modulator synthesizes an AC signal V_R, which is an analog representation of the output inductor ripple current. The duty-cycle of V_R is the result of charge and discharge current through a ripple capacitor C_R. The current through C_R is provided by a transconductance amplifier g_m that measures the input voltage (V_{IN}) at the PHASE pin and output voltage (V_{OUT}) at the VO pin. The positive slope of V_R can be written as Equation 1:

$$V_{RPOS} = (g_m) \cdot (V_{IN} - V_{OUT}) / C_R \qquad \text{(EQ. 1)}$$

The negative slope of V_R can be written as Equation 2:

$$V_{RNEG} = g_m \cdot V_{OUT} / C_R \qquad \text{(EQ. 2)}$$

Where, g_m is the gain of the transconductance amplifier.

A window voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP}, creating an envelope into which the ripple voltage V_R is compared. The amplitude of V_W is controlled internally by the IC. The V_R, V_{COMP}, and V_W signals feed into a window comparator in which V_{COMP} is the lower threshold voltage and V_W is the higher threshold voltage. Figure 5 shows PWM pulses being generated as V_R traverses the V_W and V_{COMP} thresholds. The PWM switching frequency is proportional to the slew rates of the positive and negative slopes of V_R; it is inversely proportional to the voltage between V_W and V_{COMP}.

Synchronous Rectification

A standard DC/DC buck regulator uses a free-wheeling diode to maintain uninterrupted current conduction through the output inductor when the high-side MOSFET switches off for the balance of the PWM switching cycle. Low conversion efficiency as a result of the conduction loss of the diode makes this an unattractive option for all but the lowest current applications. Efficiency is dramatically improved when the free-wheeling diode is replaced with a MOSFET that is turned on whenever the high-side MOSFET is turned off. This modification to the standard DC/DC buck regulator is referred to as synchronous rectification, the topology implemented by the ISL62875 controller.

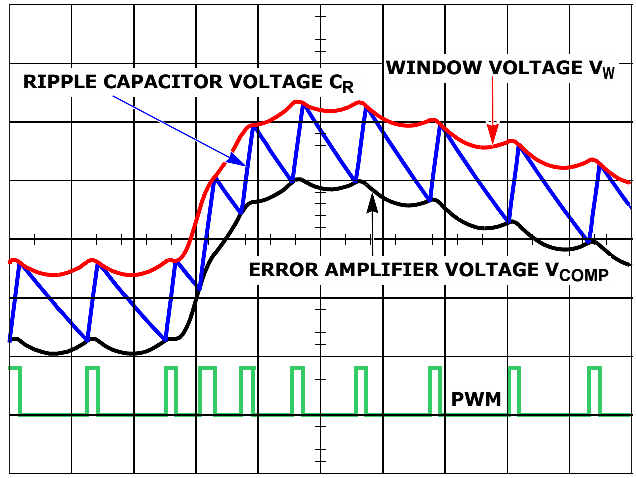


FIGURE 5. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

Diode Emulation

The polarity of the output inductor current is defined as positive when conducting *away* from the phase node, and defined as negative when conducting towards the phase node. The DC component of the inductor current is positive, but the AC component known as the ripple current, can be either positive or negative. Should the sum of the AC and DC components of the inductor current remain positive for the entire switching period, the converter is in continuous-conduction-mode (CCM.) However, if the inductor current becomes negative or zero, the converter is in discontinuous-conduction-mode (DCM.)

Unlike the standard DC/DC buck regulator, the synchronous rectifier can sink current from the output filter inductor during DCM, reducing the light-load efficiency with unnecessary conduction loss as the low-side MOSFET sinks the inductor current. The ISL62875 controller avoids the DCM conduction loss by making the low-side MOSFET emulate the current-blocking behavior of a diode. This smart-diode operation called diode-emulation-mode (DEM) is triggered when the negative inductor current produces a positive voltage drop across the $r_{DS(ON)}$ of the low-side MOSFET for eight consecutive PWM cycles while the LGATE pin is high. The converter will exit DEM on the next PWM pulse after detecting a negative voltage across the $r_{DS(ON)}$ of the low-side MOSFET.

It is characteristic of the R^3 architecture for the PWM switching frequency to decrease while in DCM, increasing efficiency by reducing unnecessary gate-driver switching losses. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency is forced to fall approximately 30% by forcing a similar increase of the window voltage V_W. This measure is taken to prevent oscillating between modes at the boundary between CCM and DCM. The 30% increase of V_W is removed upon exit of DEM, forcing the PWM switching frequency to jump back to the nominal CCM value.

Power-On Reset

The IC is disabled until the voltage at the VCC pin has increased above the rising power-on reset (POR) threshold voltage V_{VCC_THR}. The controller will become disabled when the voltage at the VCC pin decreases below the falling POR threshold voltage V_{VCC_THF}. The POR detector has a noise filter of approximately 1µs.

V_{IN} and PVCC Voltage Sequence

Prior to pulling EN above the V_{ENTHR} rising threshold voltage, the following criteria must be met:

- V_{PVCC} is at least equivalent to the VCC rising power-on reset voltage V_{VCC_THR}
- V_{VIN} must be 3.3V or the minimum required by the application

Start-Up Timing

Once VCC has ramped above V_{VCC_THR}, the controller can be enabled by pulling the EN pin voltage above the input-high threshold V_{ENTHR}. Approximately 20µs later, the voltage at the SREF pin begins slewing to the designated VID set-point. The converter output voltage at the FB feedback pin follows the voltage at the SREF pin. During soft-start, The regulator always operates in CCM until the soft-start sequence is complete.

PGOOD Monitor

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. The PGOOD pin is an undefined impedance if the VCC pin has not reached the rising POR threshold V_{VCC_THR}, or if the VCC pin is below the falling POR threshold V_{VCC_THF}. The PGOOD pull-down resistance corresponds to a specific protective fault, thereby reducing troubleshooting time and effort. Table 1 maps the pull-down resistance of the PGOOD pin to the corresponding fault status of the controller.

TABLE 1. PGOOD PULL-DOWN RESISTANCE

CONDITION	PGOOD RESISTANCE
VCC Below POR	Undefined
Soft-Start or Undervoltage	95Ω
Overcurrent	35Ω

LGATE and UGATE MOSFET Gate-Drivers

The LGATE pin and UGATE pins are MOSFET driver outputs. The LGATE pin drives the low-side MOSFET of the converter while the UGATE pin drives the high-side MOSFET of the converter.

The LGATE driver is optimized for low duty-cycle applications where the low-side MOSFET experiences long conduction times. In this environment, the low-side MOSFETs require exceptionally low $r_{DS(ON)}$ and tend to have large parasitic charges that conduct transient currents within the devices in response to high dv/dt switching present at the phase node. The drain-gate charge in particular can conduct sufficient current through the driver pull-down resistance that the $V_{GS(th)}$ of the device can be exceeded and turned on. For this reason the LGATE driver has been designed with low pull-down resistance and high sink current capability to ensure clamping the MOSFETs gate voltage below $V_{GS(th)}$.

Adaptive Shoot-Through Protection

Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 6 is extended by the additional period that the falling gate voltage remains above the 1V threshold. The high-side gate-driver output voltage is measured across the UGATE and PHASE pins while the low-side gate-driver output voltage is measured across the LGATE and PGND pins. The power for the LGATE gate-driver is sourced directly from the PVCC pin. The power for the UGATE gate-driver is supplied by a boot-strap capacitor connected across the BOOT and PHASE pins. The capacitor is charged each time the phase node voltage falls a diode drop below PVCC such as when the low-side MOSFET is turned on.

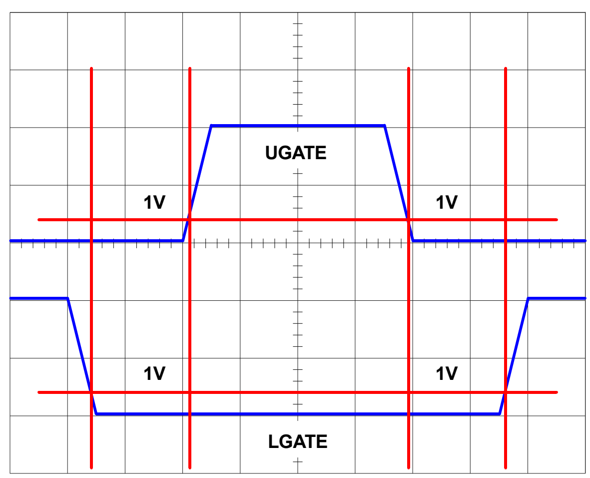


FIGURE 6. GATE DRIVER ADAPTIVE SHOOT-THROUGH

Setpoint Reference Voltage Programming

Voltage identification (VID) pins select user-programmed setpoint reference voltages that appear at the SREF pin. The converter is in regulation when the FB pin voltage (V_{FB}) equals the SREF pin voltage (V_{SREF}.) The IC measures V_{FB} and V_{SREF} relative to the GND pin, not the PGND pin. The setpoint reference voltages use the naming convention $V_{SET(x)}$ where (x) is the first, second, third, or fourth setpoint reference voltage where:

- $V_{SET1} < V_{SET2} < V_{SET3} < V_{SET4}$
- $V_{OUT1} < V_{OUT2} < V_{OUT3} < V_{OUT4}$

The V_{SET1} setpoint is fixed at 500mV because it corresponds to the closure of internal switch SW0 that configures the V_{SET} amplifier as a unity-gain voltage follower for the 500mV voltage reference V_{REF}.

A feedback voltage-divider network may be required to achieve the desired reference voltages. Using the feedback voltage-divider allows the maximum output voltage of the converter to be higher than the 1.5V maximum setpoint reference voltage that can be programmed on the SREF pin. Likewise, the feedback voltage-divider allows the minimum output voltage of the converter to be higher than the fixed 500mV setpoint reference voltage of V_{SET1}. Scale the voltage-divider network such that the voltage V_{FB} equals the voltage V_{SREF} when the converter output voltage is at the desired level. The voltage-divider relation is given in Equation 3:

$$V_{FB} = V_{OUT} \cdot \frac{R_{OFS}}{R_{FB} + R_{OFS}} \qquad \text{(EQ. 3)}$$

Where:

- $V_{FB} = V_{SREF}$
- R_{FB} is the loop-compensation feedback resistor that connects from the FB pin to the converter output
- R_{OFS} is the voltage-scaling programming resistor that connects from the FB pin to the GND pin

The attenuation of the feedback voltage divider is written as:

$$K = \frac{V_{SREF(lim)}}{V_{OUT(lim)}} = \frac{R_{OFS}}{R_{FB} + R_{OFS}} \qquad \text{(EQ. 4)}$$

Where:

- ***K*** is the attenuation factor
- $V_{SREF(\boldsymbol{lim})}$ is the V_{SREF} voltage setpoint of either 500mV or 1.50V
- $V_{OUT(\boldsymbol{lim})}$ is the output voltage of the converter when $V_{SREF} = V_{SREF(\boldsymbol{lim})}$

Since the voltage-divider network is in the feedback path, all output voltage setpoints will be attenuated by ***K***, so it follows that all of the setpoint reference voltages will be attenuated by ***K***. It will be necessary then to include the attenuation factor ***K*** in all the calculations for selecting the R_{SET} programming resistors.

The value of offset resistor R_{OFS} can be calculated only after the value of loop-compensation resistor R_{FB} has been determined. The calculation of R_{OFS} is written as Equation 5:

$$R_{OFS} = \frac{V_{SET(x)} \cdot R_{FB}}{V_{OUT} - V_{SET(x)}} \qquad \text{(EQ. 5)}$$

The setpoint reference voltages are programmed with resistors that use the naming convention $R_{SET(x)}$ where (x) is the first, second, third, or fourth programming resistor connected in series starting at the SREF pin and ending at the GND pin. When one of the internal switches closes, it connects the inverting input of the V_{SET} amplifier to a specific node among the string of R_{SET} programming resistors. All the resistors between that node and the SREF pin serve as the feedback impedance R_F of the V_{SET} amplifier. Likewise, all the resistors between that node and the GND pin serve as the input impedance R_{IN} of the V_{SET} amplifier. Equation 6 gives the general form of the gain equation for the V_{SET} amplifier:

$$V_{SET(X)} = V_{REF} \cdot \left(1 + \frac{R_F}{R_{IN}}\right) \qquad \text{(EQ. 6)}$$

Where:

- V_{REF} is the 500mV internal reference of the IC
- $V_{SET(x)}$ is the resulting setpoint reference voltage that appears at the SREF pin

Calculating Setpoint Voltage Programming Resistor Values

TABLE 2. ISL62875 VID TRUTH TABLE

VID STATE		RESULT		
VID1	**VID0**	**CLOSE**	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

First, determine the attenuation factor ***K***. Next, assign an initial value to R_{SET4} of approximately 100kΩ then calculate R_{SET1}, R_{SET2}, and R_{SET3} using Equations 7, 8, and 9 respectively. The equation for the value of R_{SET1} is written as Equation 7:

$$R_{SET1} = \frac{R_{SET4} \cdot KV_{SET4} \cdot (KV_{SET2} - V_{REF})}{V_{REF} \cdot KV_{SET2}} \qquad \text{(EQ. 7)}$$

The equation for the value of R_{SET2} is written as Equation 8:

$$R_{SET2} = \frac{R_{SET4} \cdot KV_{SET4} \cdot (KV_{SET3} - KV_{SET2})}{KV_{SET2} \cdot KV_{SET3}} \qquad \text{(EQ. 8)}$$

The equation for the value of R_{SET3} is written as Equation 9:

$$R_{SET3} = \frac{R_{SET4} \cdot (KV_{SET4} - KV_{SET3})}{KV_{SET3}} \qquad \text{(EQ. 9)}$$

The sum of all the programming resistors should be approximately 300kΩ as shown in Equation 10 otherwise adjust the value of R_{SET4} and repeat the calculations.

$$R_{SET1} + R_{SET2} + R_{SET3} + R_{SET4} \cong 300k\Omega \qquad \text{(EQ. 10)}$$

Equations 11, 12, 13 and 14 give the specific V_{SET} gain equations for the ISL62875 setpoint reference voltages.

The ISL62875 V_{SET1} setpoint is written as Equation 11:

$$V_{SET1} = V_{REF} \qquad \text{(EQ. 11)}$$

The ISL62875 V_{SET2} setpoint is written as Equation 12:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \qquad \text{(EQ. 12)}$$

The ISL62875 V_{SET3} setpoint is written as Equation 13:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \qquad \text{(EQ. 13)}$$

The ISL62875 V_{SET4} setpoint is written as Equation 14:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \qquad \text{(EQ. 14)}$$

External Setpoint Reference

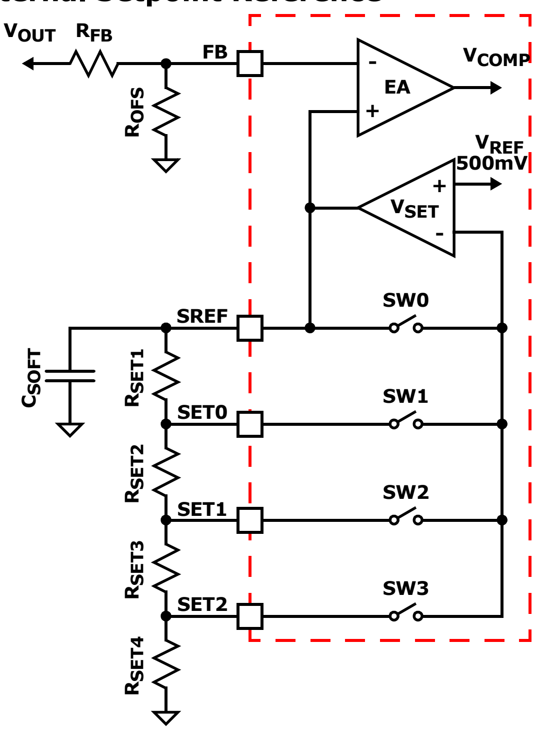


FIGURE 7. VOLTAGE PROGRAMMING CIRCUIT

The IC can use an external setpoint reference voltage as an alternative to VID-selected, resistor-programmed setpoints. This is accomplished by removing all setpoint programming resistors, connecting the SET0 pin to the VCC pin, and feeding the external setpoint reference voltage to the VID0 pin. When SET0 and VCC are tied together, the following internal reconfigurations take place:

- VID0 pin opens its 500nA pull-down current sink
- Reference source selector switch SW4 moves from INT position (internal 500mV) to EXT position (VID0 pin)
- VID1 pin is disabled

The converter will now be in regulation when the voltage on the FB pin equals the voltage on the VID0 pin. As with resistor-programmed setpoints, the reference voltage range on the VID0 pin is 500mV to 1.5V. Use Equations 3, 4, and 5 beginning on page 13 should it become necessary to implement an output voltage-divider network to make the external setpoint reference voltage compatible with the 500mV to 1.5V constraint.

Soft-Start and Voltage-Step Delay

Circuit Description

When the voltage on the VCC pin has ramped above the rising power-on reset voltage V_{VCC_THR}, and the voltage on the EN pin has increased above the rising enable threshold voltage V_{ENTHR}, the SREF pin releases its discharge clamp and enables the reference amplifier V_{SET}. The soft-start current I_{SS} is limited to 20µA and is sourced out of the SREF pin into the parallel RC network of capacitor C_{SOFT} and resistance R_T. The resistance R_T is the sum of all the series connected R_{SET} programming resistors and is written as Equation 15:

$$R_T = R_{SET1} + R_{SET2} + \dots R_{SET(n)} \qquad \text{(EQ. 15)}$$

The voltage on the SREF pin rises as I_{SS} charges C_{SOFT} to the voltage reference setpoint selected by the state of the VID inputs at the time the EN pin is asserted. The regulator controls the PWM such that the voltage on the FB pin tracks the rising voltage on the SREF pin. Once C_{SOFT} charges to the selected setpoint voltage, the I_{SS} current source comes out of the 20µA current limit and decays to the static value set by $V_{SREF} \div R_T$. The elapsed time from when the EN pin is asserted to when V_{SREF} has reached the voltage reference setpoint is the soft-start delay t_{SS} which is given by Equation 16:

$$t_{SS} = -(R_T \cdot C_{SOFT}) \cdot LN\left(1 - \frac{V_{START\text{-}UP}}{I_{SS} \cdot R_T}\right) \qquad \text{(EQ. 16)}$$

Where:

- $\mathbf{I_{SS}}$ is the soft-start current source at the 20µA limit
- $V_{START\text{-}UP}$ is the setpoint reference voltage selected by the state of the VID inputs at the time EN is asserted
- R_T is the sum of the R_{SET} programming resistors

The end of soft-start is detected by I_{SS} tapering off when capacitor C_{SOFT} charges to the designated V_{SET} voltage reference setpoint. The SSOK flag is set, the PGOOD pin goes high, and the I_{SS} current source changes over to the voltage-step current source I_{VS} which has a current limit of ±100µA. Whenever the VID inputs or the external setpoint reference, programs a different setpoint reference voltage, the I_{VS} current source charges or discharges capacitor C_{SOFT} to that new level at ±100µA. Once C_{SOFT} charges to the selected setpoint voltage, the I_{VS} current source comes out of the 100µA current limit and decays to the static value set by $V_{SREF} \div R_T$. The elapsed time to charge C_{SOFT} to the new voltage is called the voltage-step delay t_{VS} and is given by Equation 17:

$$t_{VS} = -(R_T \cdot C_{SOFT}) \cdot LN\left(1 - \frac{(V_{NEW} - V_{OLD})}{I_{VS} \cdot R_T}\right) \quad \text{(EQ. 17)}$$

Where:

- $\mathbf{I_{VS}}$ is the ±100µA setpoint voltage-step current
- V_{NEW} is the new setpoint voltage selected by the VID inputs
- V_{OLD} is the setpoint voltage that V_{NEW} is changing from
- R_T is the sum of the R_{SET} programming resistors

Component Selection For C_{SOFT} Capacitor

Choosing the C_{SOFT} capacitor to meet the requirements of a particular soft-start delay t_{SS} is calculated with Equation 18, which is written as:

$$C_{SOFT} = \frac{-t_{SS}}{\left(R_T \cdot LN\left(1 - \frac{V_{START\text{-}UP}}{I_{SS} \cdot R_T}\right)\right)} \quad \text{(EQ. 18)}$$

Where:

- $\mathbf{t_{SS}}$ is the soft-start delay
- $\mathbf{I_{SS}}$ is the soft-start current source at the 20µA limit
- $V_{START\text{-}UP}$ is the setpoint reference voltage selected by the state of the VID inputs at the time EN is asserted
- R_T is the sum of the R_{SET} programming resistors

Choosing the C_{SOFT} capacitor to meet the requirements of a particular voltage-step delay t_{VS} is calculated with Equation 19, which is written as:

$$C_{SOFT} = \frac{-t_{VS}}{\left(R_T \cdot LN\left(1 - \frac{V_{NEW} - V_{OLD}}{\pm I_{VS} \cdot R_T}\right)\right)} \quad \text{(EQ. 19)}$$

Where:

- $\mathbf{t_{VS}}$ **is the voltage-step delay**
- V_{NEW} is the new setpoint voltage
- V_{OLD} is the setpoint voltage that V_{NEW} is changing from
- $\mathbf{I_{VS}}$ is the ±100µA setpoint voltage-step current; positive when $V_{NEW} > V_{OLD}$, negative when $V_{NEW} < V_{OLD}$
- R_T is the sum of the R_{SET} programming resistors

Compensation Design

Figure 8 shows the recommended Type-II compensation circuit. The FB pin is the inverting input of the error amplifier. The COMP signal, the output of the error amplifier, is inside the chip and unavailable to users. C_{INT} is a 100pF capacitor integrated inside the IC, connecting across the FB pin and the COMP signal. R_{FB}, R_{COMP}, C_{COMP} and C_{INT} form the Type-II compensator. The frequency domain transfer function is given by Equation 20:

$$G_{COMP}(s) = \frac{1 + s \cdot (R_{FB} + R_{COMP}) \cdot C_{COMP}}{s \cdot R_{FB} \cdot C_{INT} \cdot (1 + s \cdot R_{COMP} \cdot C_{COMP})} \quad \text{(EQ. 20)}$$

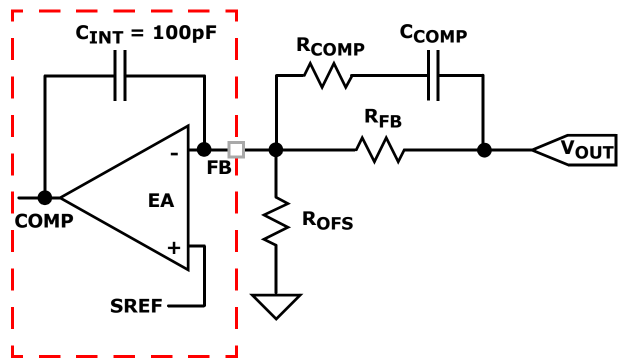


FIGURE 8. COMPENSATION REFERENCE CIRCUIT

The LC output filter has a double pole at its resonant frequency that causes rapid phase change. The R^3 modulator used in the IC makes the LC output filter resemble a first order system in which the closed loop stability can be achieved with the recommended Type-II compensation network. Intersil provides a PC-based tool that can be used to calculate compensation network component values and help simulate the loop frequency response.

Fault Protection

Overcurrent

The overcurrent protection (OCP) setpoint is programmed with resistor R_{OCSET} which is connected across the OCSET and PHASE pins. Resistor R_O is connected between the VO pin and the actual output voltage of the converter. During normal operation, the VO pin is a high impedance path, therefore there is no voltage drop across R_O. The value of resistor R_O should always match the value of resistor R_{OCSET}.

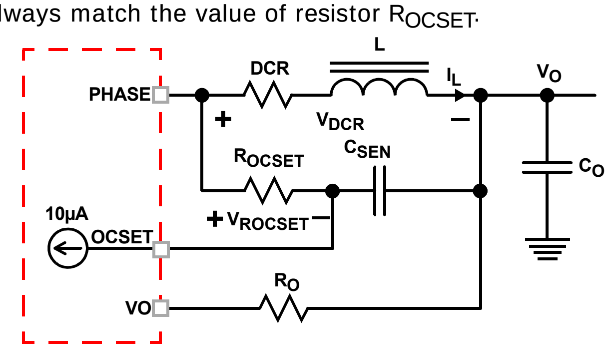


FIGURE 9. OVERCURRENT PROGRAMMING CIRCUIT

Figure 9 shows the overcurrent set circuit. The inductor consists of inductance L and the DC resistance DCR. The inductor DC current I_L creates a voltage drop across DCR, which is given by Equation 21:

$$V_{DCR} = I_L \cdot DCR \quad \text{(EQ. 21)}$$

The I_{OCSET} current source sinks 10µA into the OCSET pin, creating a DC voltage drop across the resistor R_{OCSET}, which is given by Equation 22:

$$V_{ROCSET} = 10\mu A \cdot R_{OCSET} \quad \text{(EQ. 22)}$$

The DC voltage difference between the OCSET pin and the VO pin, which is given by Equation 23:

$$V_{OCSET} - V_{VO} = V_{DCR} - V_{ROCSET} = I_L \cdot DCR - I_{OCSET} \cdot R_{OCSET} \quad \text{(EQ. 23)}$$

The IC monitors the voltage of the OCSET pin and the VO pin. When the voltage of the OCSET pin is higher than the voltage of the VO pin for more than 10µs, an OCP fault latches the converter off.

Component Selection for R_{OCSET} and C_{SEN}

The value of R_{OCSET} is calculated with Equation 24, which is written as:

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{I_{OCSET}} \quad \text{(EQ. 24)}$$

Where:

- R_{OCSET} (Ω) is the resistor used to program the overcurrent setpoint
- I_{OC} is the output DC load current that will activate the OCP fault detection circuit
- DCR is the inductor DC resistance

For example, if I_{OC} is 20A and DCR is 4.5mΩ, the choice of R_{OCSET} is = 20A x 4.5mΩ/10µA = 9kΩ.

Resistor R_{OCSET} and capacitor C_{SEN} form an R-C network to sense the inductor current. To sense the inductor current correctly not only in DC operation, but also during dynamic operation, the R-C network time constant R_{OCSET} C_{SEN} needs to match the inductor time constant L/DCR. The value of C_{SEN} is then written as Equation 25:

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR} \quad \text{(EQ. 25)}$$

For example, if L is 1.5µH, DCR is 4.5mΩ, and R_{OCSET} is 9kΩ, the choice of C_{SEN} = 1.5µH/(9kΩ x 4.5mΩ) = 0.037µF.

When an OCP fault is declared, the PGOOD pin will pull-down to 35Ω and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}.

Overvoltage

The ISL62875 does not feature overvoltage fault protection.

Undervoltage

The UVP fault detection circuit triggers after the FB pin voltage is below the undervoltage threshold V_{UVTH} for more than 2µs. For example, if the converter is programmed to regulate 1.0V at the FB pin, that voltage would have to fall below the typical V_{UVTH} threshold of 84% for more than 2µs in order to trip the UVP fault latch. In numerical terms, that would be 84% x 1.0V = 0.84V. When a UVP fault is declared, the PGOOD pin will pull-down to 95Ω and latch-off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}.

Over-Temperature

When the temperature of the IC increases above the rising threshold temperature T_{OTRTH}, it will enter the OTP state that suspends the PWM, forcing the LGATE and UGATE gate-driver outputs low. The status of the PGOOD pin does not change nor does the converter latch-off. The PWM remains suspended until the IC temperature falls below the hysteresis temperature T_{OTHYS} at which time normal PWM operation resumes. The OTP state can be reset if the EN pin is pulled below the falling EN threshold voltage V_{ENTHF} or if VCC has decayed below the falling POR threshold voltage V_{VCC_THF}. All other protection circuits remain functional while the IC is in the OTP state. It is likely that the IC will detect an UVP fault because in the absence of PWM, the output voltage decays below the undervoltage threshold V_{UVTH}.

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is expressed in Equation 26:

$$D = \frac{V_O}{V_{IN}} \quad \text{(EQ. 26)}$$

The output inductor peak-to-peak ripple current is expressed in Equation 27:

$$I_{P\text{-}P} = \frac{V_O \cdot (1 - D)}{F_{SW} \cdot L} \quad \text{(EQ. 27)}$$

A typical step-down DC/DC converter will have an I_{P-P} of 20% to 40% of the maximum DC output load current. The value of I_{P-P} is selected based upon several criteria, such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated using Equation 28:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 28)}$$

Where, I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops a corresponding ripple voltage V_{P-P} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are expressed in Equations 29 and 30:

$$\Delta V_{ESR} = I_{P-P} \cdot ESR \quad \text{(EQ. 29)}$$

$$\Delta\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot F_{SW}} \quad \text{(EQ. 30)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at F_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a preferred rating. Figure 10 is a graph of the input RMS ripple current, normalized relative to output load current, as a function of duty cycle that is adjusted for converter efficiency. The ripple current calculation is written as Equation 31:

$$I_{IN\_RMS} = \frac{\sqrt{\left(I_{MAX}^{2} \cdot (D - D^{2})\right) + \left(x \cdot I_{MAX}^{2} \cdot \frac{D}{12}\right)}}{I_{MAX}} \quad \text{(EQ. 31)}$$

Where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- x is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter

Duty cycle is written as Equation 32:

$$D = \frac{V_O}{V_{IN} \cdot EFF} \quad \text{(EQ. 32)}$$

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

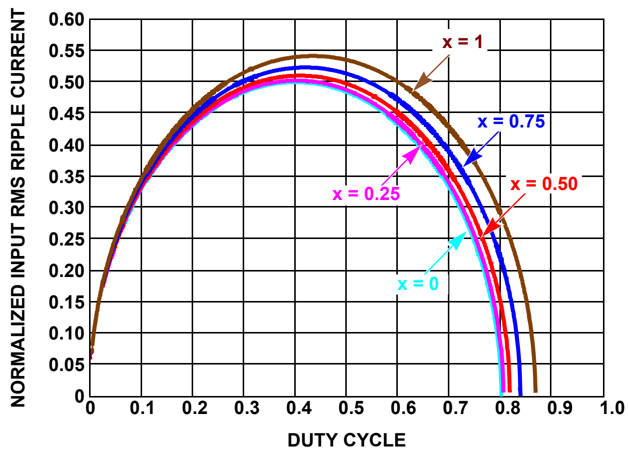


FIGURE 10. NORMALIZED RMS INPUT CURRENT FOR x = 0.8

Selecting The Bootstrap Capacitor

Adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. We selected the bootstrap capacitor breakdown voltage to be at least 10V. Although the theoretical maximum voltage of the capacitor is PVCC-V_{DIODE} (voltage drop across the boot diode), large excursions below ground by the phase node requires we select a capacitor with at least a breakdown rating of 10V. The bootstrap capacitor can be chosen from Equation 33:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 33)}$$

Where:

- Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET
- ΔV_{BOOT} is the maximum decay across the BOOT capacitor

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE}, of 25nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is

0.15µF. A good quality ceramic capacitor such as X7R or X5R is recommended.

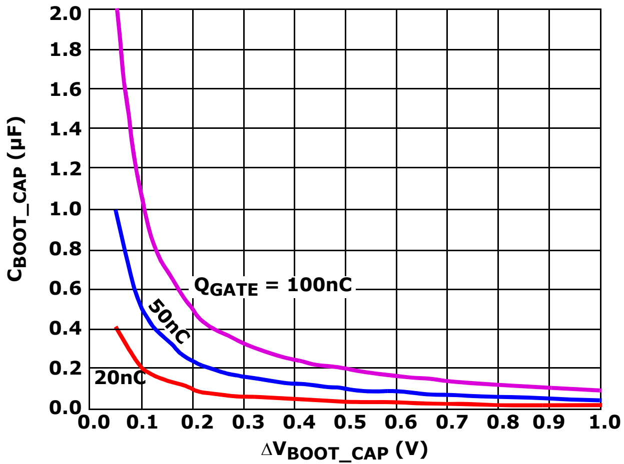


FIGURE 11. BOOT CAPACITANCE vs BOOT RIPPLE VOLTAGE

Driver Power Dissipation

Switching power dissipation in the driver is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. When designing the application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the drivers is approximated as Equation 34:

$$P = F_{sw}(1.5V_UQ_U + V_LQ_L) + P_L + P_U \quad \text{(EQ. 34)}$$

Where:

- F_{SW} is the switching frequency of the PWM signal
- V_U is the upper gate driver bias supply voltage
- V_L is the lower gate driver bias supply voltage
- Q_U is the charge to be delivered by the upper driver into the gate of the MOSFET and discrete capacitors
- Q_L is the charge to be delivered by the lower driver into the gate of the MOSFET and discrete capacitors
- P_L is the quiescent power consumption of the lower driver
- P_U is the quiescent power consumption of the upper driver

MOSFET Selection and Considerations

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum V_{DS} rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

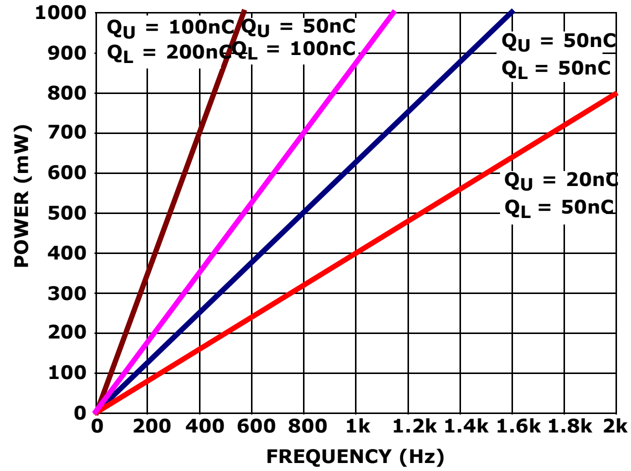


FIGURE 12. POWER DISSIPATION vs FREQUENCY

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low switch charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain-source voltage clamped by its body diode during turn-off, the high-side MOSFET turns off with V_{IN}-V_{OUT}, plus the spike, across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss.

For the low-side MOSFET, (LS), the power loss can be assumed to be conductive only and is written as Equation 35:

$$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)\_LS} \cdot (1 - D) \quad \text{(EQ. 35)}$$

For the high-side MOSFET, (HS), its conduction loss is written as Equation 36:

$$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(ON)\_HS} \cdot D \quad \text{(EQ. 36)}$$

For the high-side MOSFET, its switching loss is written as Equation 37:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot F_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot F_{SW}}{2} \quad \text{(EQ. 37)}$$

Where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation

- t_{OFF} is the time required to drive the device into cut-off

PCB Layout Considerations

Power and Signal Layers Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding. The ground plane layer should have an island located under the IC, the compensation components, and the SREF components. The island should be connected to the rest of the ground plane layer at one point.

Component Placement

There are two sets of critical components in a DC/DC converter; the power components and the small signal components. The power components are the most critical because they switch large amount of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, PHASE and BOOT.

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible (see Figure 13). Input high-frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High-frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target (GPUor CPU), making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

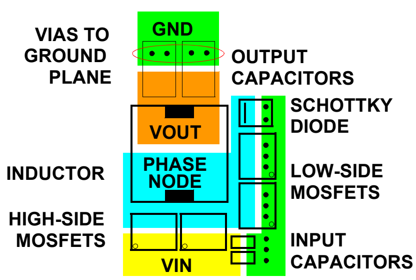


FIGURE 13. TYPICAL POWER COMPONENT PLACEMENT

Signal Ground and Power Ground

The GND pin is the signal-common also known as analog ground of the IC. When laying out the PCB, it is very important that the connection of the GND pin to the bottom setpoint-reference programming-resistor, bottom feedback voltage-divider resistor (if used), and the CSOFT capacitor be made as close as possible to the GND pin on a conductor not shared by any other components.

In addition to the critical single point connection discussed in the previous paragraph, the ground plane layer of the PCB should have a single-point-connected island located under the area encompassing the IC, setpoint reference programming components, feedback voltage divider components, compensation components, CSOFT capacitor, and the interconnecting traces among the components and the IC. The island should be connected using several filled vias to the rest of the ground plane layer at one point that is not in the path of either large static currents or high di/dt currents. The single connection point should also be where the VCC decoupling capacitor and the GND pin of the IC are connected.

Anywhere not within the analog-ground island is Power Ground. Connect the input capacitor(s), the output capacitor(s), and the source of the lower MOSFET(s) to the power ground plane.

Routing and Connection Details

Specific pins (and the trace routing from them), require extra attention during the layout process. The following sub-sections outline concerns by pin name.

VCC PIN

For best performance, place the decoupling capacitor next to the VCC and GND pins. The VCC decoupling capacitor should not share any vias with the PVCC decoupling capacitor.

PVCC PIN

For best performance, place the PVCC decoupling capacitor next to the PVCC and PGND pins, preferably on the same side of the PCB as the ISL62875. The PVCC decoupling capacitor should have a very short and wide trace connection to the PGND pin.

EN, PGOOD, VID0, AND VID1 PINS

These are logic signals that are referenced to the GND pin. Treat as a typical logic signal.

OCSET AND VO PINS

The current-sensing network consisting of R_{OCSET}, R_O, and C_{SEN} must be connected to the inductor pads for accurate measurement of the DCR voltage drop. These components however, should be located physically close to the OCSET and VO pins with traces leading back to the inductor. It is critical that the traces are shielded by the ground plane layer all the way to the inductor pads. The procedure is the same for resistive current sense.

FB, SREF, SET0, SET1, AND SET2 PINS

The input impedance of these pins is high, making it critical to place the loop compensation components, setpoint reference programming resistors, feedback voltage divider resistors, and CSOFT close to the IC, keeping the length of the traces short.

LGATE, PGND, UGATE, BOOT, AND PHASE PINS

The signals going through these traces are boht high dv/dt and di/dt, with high peak charging and discharging current. The PGND pin can only flow current from the gate-source charge of the low-side MOSFETs when LGATE goes low. Ideally, route the trace from the LGATE pin in parallel with the trace from the PGND pin, route the trace from the UGATE pin in parallel with the trace from the PHASE pin, and route the trace from the BOOT pin in parallel with the trace from the PHASE pin. These pairs of traces should be short, wide, and away from other traces with high input impedance; weak signal traces should not be in proximity with these traces on any layer.

Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the upper MOSFET and the source of the lower MOSFET to suppress the turn-off voltage.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
8/09	FN6905.0	Initial Release
9/09	FN6905.1	Page 10: Removed “OVP Rising Threshold Voltage” and “OVP Falling Threshold Voltage” lines from the “Electrical Specifications” table.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL62875

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

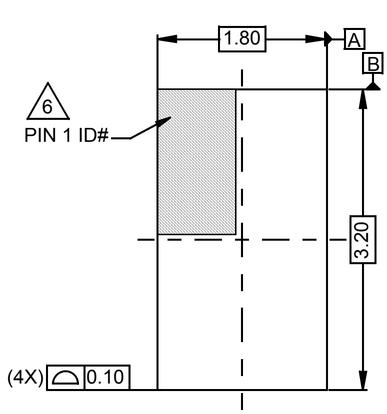
FITs are available from our website at http://rel.intersil.com/reports/search.php

Package Outline Drawing

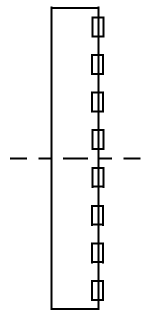
L20.3.2x1.8

20 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (UTQFN)

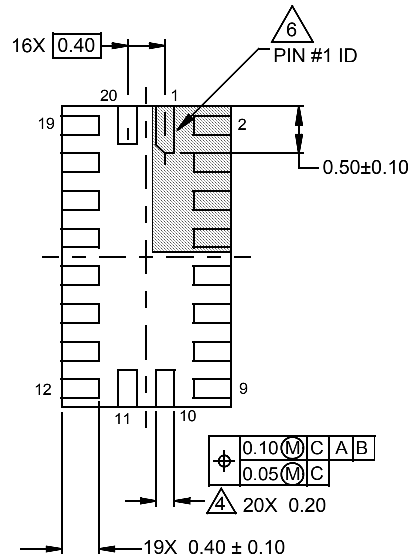
Rev 0, 5/08



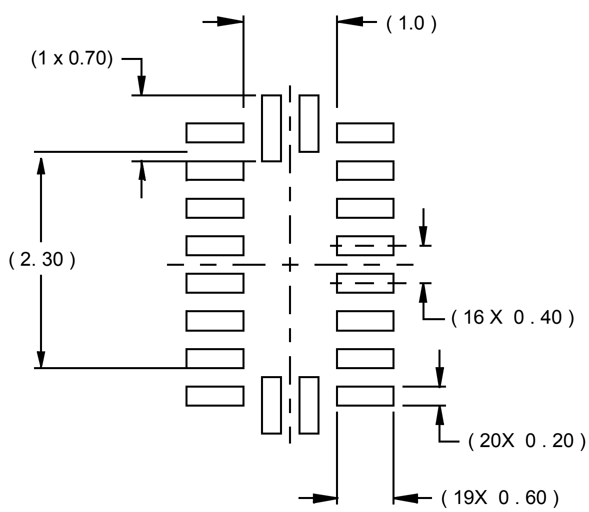
TOP VIEW



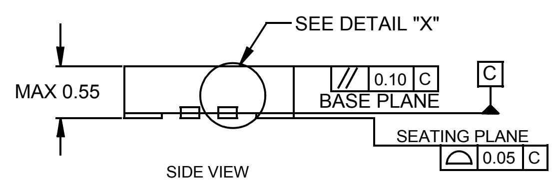
VIEW "A-A"



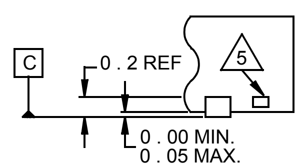
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.