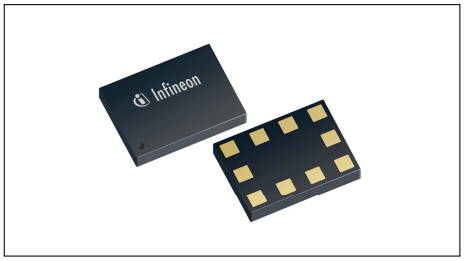
BGSC2341ML10

RF Digitally Tunable Capacitor + SPDT Switch

Features

- Designed for high-linearity applications
- Ultra low R_{ON} resistance of 0.87 Ω at each SPDT throw in ON state
- High operating RF Voltage handling 40 V
- 0.25-2.00 pF Tuning range at 1.8 GHz
- Operating frequencies: 0.4 - 3.8 GHz
- High ESD Robustness
- MIPI 2.1 RFFE compliant control interface
- 2 default USID selectable via USID_SEL pin
- Supply voltage range: 1.65 to 1.95 V
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



1.1 x 1.5 mm^2

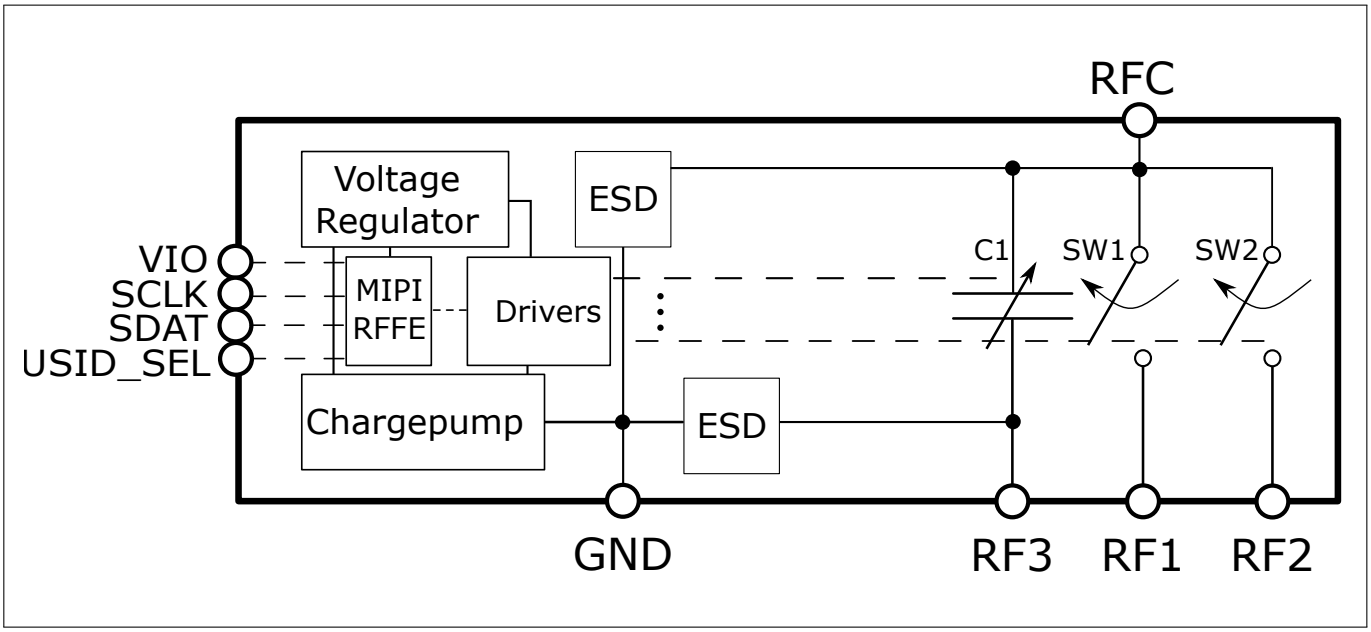
Potential Applications

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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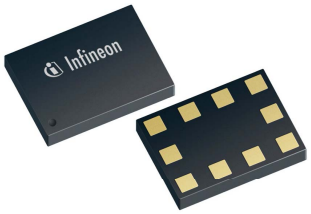
1 Features



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RoHS Halogen-Free Lead-Free Green

Description

The BGSC2341ML10 is a versatile Integrated Circuit (IC) ideal for RF tuning applications such as tunable impedance matching, antenna tuning, tunable filtering. This IC integrates a 8 states tunable capacitor and an extremely low Ron Single Pole Double Throw (SPDT) RF switch function; both controlled by on-chip MIPI2.1 RFFE digital interface. Last but not the least, the BGSC2341ML10 exhibits very good linearity in high RF power conditions and up to RF Voltage of 40 V which is a key attribute in application like antenna tuning. It does not require any additional High Voltage Supply Controller IC and can be powered by a single 1.8 V Power Supply at an extremely low current consumption level. With 1.1 mm x 1.5 mm package dimensions, it is a compact solution fitting well to any small form factor mobile phone-like applications.

Product Name	Marking	Package	Ordering Information
BGSC2341ML10	C2	TSLP-10-2	BGSC 2341ML10 E6327

2 Maximum Ratings

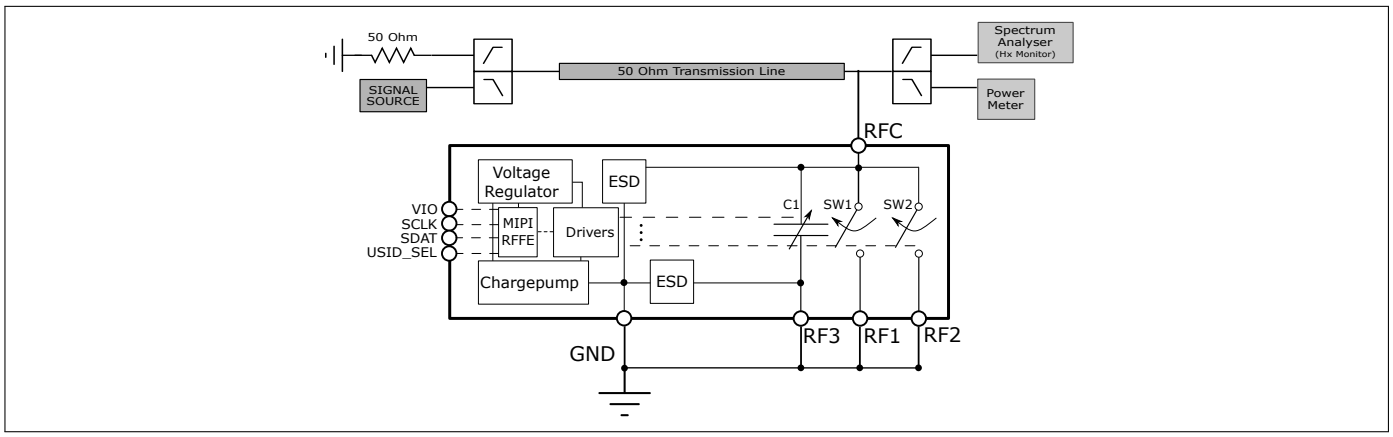

Figure 1: RF operating voltage measurement configuration (Switches 1,2 OFF and C1-Tuner position in Isolation Mode)

Table 1: Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	3.8	GHz	[1]
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	39	dBm	Pulsed RF input duty cycle of 25 % and 4620 µs in ON-state, measured per 3GPP TS 45.005
RF voltage	V_{RF_max}	–	–	45	V	Short term peaks (1 µs in 0.1% duty cycle), exceeding typical linearity, R_{ON} and C_{OFF} parameters, in Isolation mode, test condition schematic in Fig. 1
ESD robustness, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD robustness, HBM [4]	$V_{ESD_{HBM}}$	-750	–	+750	V	
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	40	43	K/W	–
RFFE Supply Voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE Control Voltage Levels	V_{SCLK}, V_{SDAT}, V_{USID_SEL}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{DD}. A high RF ripple at the V_{DD} can exceed the maximum ratings by $V_{DD} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

3 DC Characteristics

Table 2: DC Characteristics at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	1.7	9	µA	VIO shutdown mode
		–	65	110	µA	Power up mode

[1]SCLK and SDATA

4 RF Small Signal Characteristics

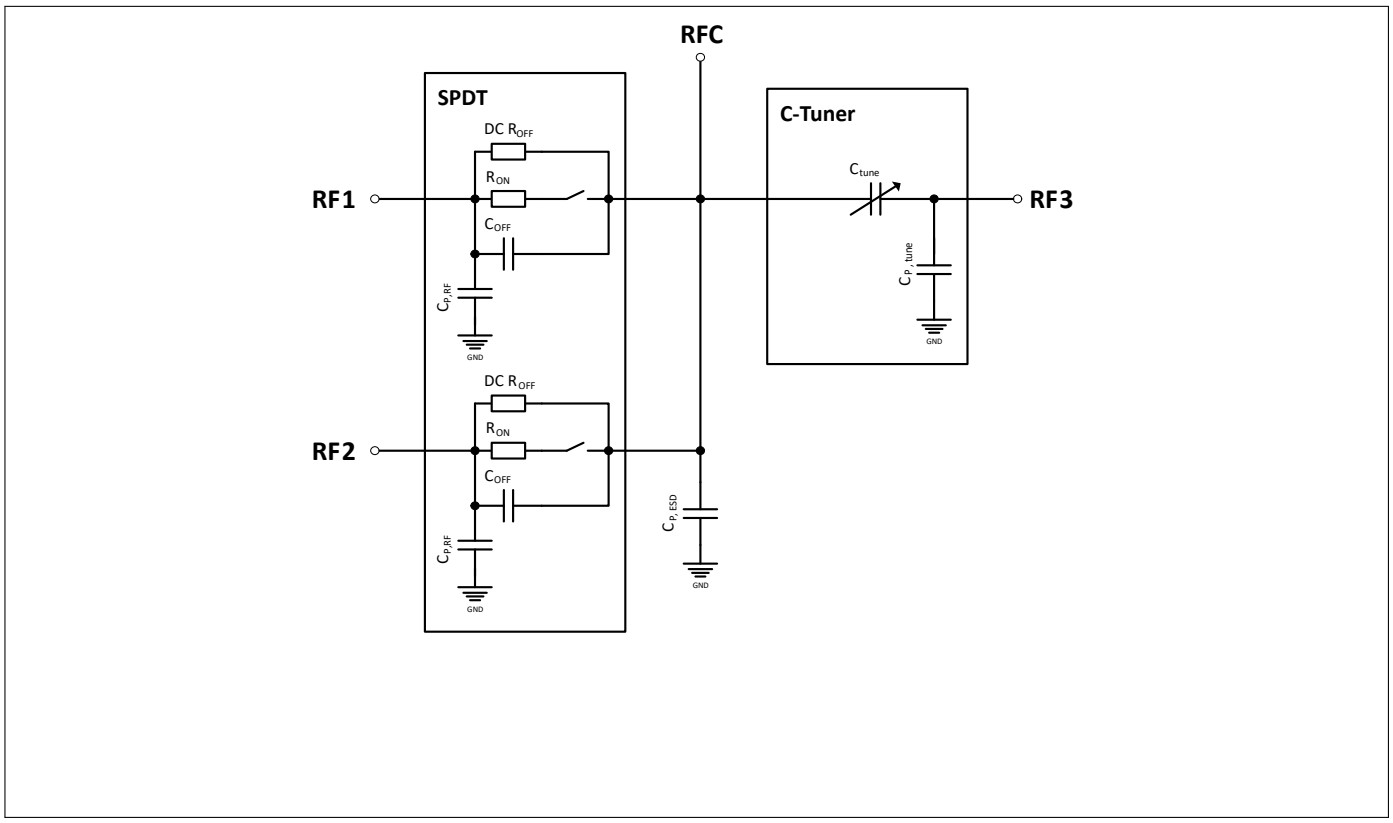

Figure 2: RF measurement equivalent circuit

Table 3: Parametric specifications of DC the equivalent circuit

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
SPDT						
R_{ON} DC ON resistance	R_{ON}	0.66	0.87	1.08	Ω	V_{IO} = 1.65 – 1.95 V,
R_{OFF} DC OFF resistance	R_{OFF}	77	110	133	$K\Omega$	T_A = –40 °C... + 85 °C

Table 4: Parametric specifications of the RF equivalent circuit @ f= 900 MHz [1,2,3]

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
$C_{P,ESD}$ SHUNT capacitance	$C_{P,ESD}$	190	220	285	fF	
C-Tuner						
C_{tune} State 0	C_0	245	260	285	fF	V_{IO} = 1.65 – 1.95 V, T_A = 25°C
C_{tune} State 1	C_1	440	460	520	fF	
C_{tune} State 2	C_2	635	665	750	fF	
C_{tune} State 3	C_3	835	870	970	fF	
C_{tune} State 4	C_4	1030	1075	1210	fF	
C_{tune} State 5	C_5	1220	1280	1430	fF	
C_{tune} State 6	C_6	1435	1500	1675	fF	
C_{tune} State 7	C_7	1685	1775	2000	fF	
$C_{P,tune}$ SHUNT capacitance	$C_{P,tune}$	175	205	245	fF	
SPDT						
C_{OFF} OFF capacitance	C_{OFF}	185	200	225	fF	
$C_{P,RF}$ SHUNT capacitance	$C_{P,RF}$	120	165	225	fF	

1) Network analyser input power: P_{IN} = 0 dBm
2) On application board without any matching components.
3) This C-tuner has a monotonic behaviour: C value will increase if programming a growing C state and decrease if programming a decreasing C state.

Table 5: Parametric specifications of the RF equivalent circuit @ f= 1.8 GHz [1,2,3]

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
$C_{P,ESD}$ SHUNT capacitance	$C_{P,ESD}$	200	215	270	fF	
C-Tuner						
C_{tune} State 0	C_0	250	270	300	fF	V_{IO} = 1.65 – 1.95 V, T_A = 25°C
C_{tune} State 1	C_1	460	500	560	fF	
C_{tune} State 2	C_2	670	725	810	fF	
C_{tune} State 3	C_3	900	1000	1100	fF	
C_{tune} State 4	C_4	1110	1200	1360	fF	
C_{tune} State 5	C_5	1350	1475	1650	fF	
C_{tune} State 6	C_6	1595	1750	1950	fF	
C_{tune} State 7	C_7	1855	2000	2300	fF	
$C_{P,tune}$ SHUNT capacitance	$C_{P,tune}$	160	185	230	fF	
SPDT						
C_{OFF} OFF capacitance	C_{OFF}	185	205	230	fF	
$C_{P,RF}$ SHUNT capacitance	$C_{P,RF}$	110	155	265	fF	

1) Network analyser input power: P_{IN} = 0 dBm
2) On application board without any matching components.
3) This C-tuner has a monotonic behaviour: C value will increase if programming a growing C state and decrease if programming a decreasing C state.

Table 6: Parametric specifications of the RF equivalent circuit @ f= 2.7 GHz [1,2,3]

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
$C_{P,ESD}$ SHUNT capacitance	$C_{P,ESD}$	205	225	260	fF	
C-Tuner						
C_{tune} State 0	C_0	260	290	320	fF	V_{IO} = 1.65 – 1.95 V, T_A = 25°C
C_{tune} State 1	C_1	500	550	610	fF	
C_{tune} State 2	C_2	755	840	935	fF	
C_{tune} State 3	C_3	1050	1180	1300	fF	
C_{tune} State 4	C_4	1275	1400	1610	fF	
C_{tune} State 5	C_5	1590	1800	2000	fF	
C_{tune} State 6	C_6	1940	2200	2460	fF	
C_{tune} State 7	C_7	2345	2660	3240	fF	
$C_{P,tune}$ SHUNT capacitance	$C_{P,tune}$	155	180	210	fF	
SPDT						
C_{OFF} OFF capacitance	C_{OFF}	190	215	250	fF	
$C_{P,RF}$ SHUNT capacitance	$C_{P,RF}$	120	155	185	fF	

1) Network analyser input power: P_{IN} = 0 dBm
2) On application board without any matching components.
3) This C-tuner has a monotonic behaviour: C value will increase if programming a growing C state and decrease if programming a decreasing C state.

5 RF Large Signal Parameters

Table 7: RF large signal specifications at $T_A = -40$ .. $+85$ °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF operating voltage	V_{RF_peak}	–	–	40	V	In Isolation mode, test condition schematic in Fig. 1 for H2/H3 < -35dBm @ 50Ω, T_A = 25 °C
Harmonic Generation up to 12.75 GHz[1,2]						
All RF Ports - Second Order Harmonics	P_{H2}	-	-71	-65	dBm	25 dBm,f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	-	-84	-79	dBm	25 dBm,f_0 = 824 MHz
All RF Ports - Second Order Harmonics	P_{H2}	-	-44	-39	dBm	35 dBm,f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	-	-56	-50	dBm	35 dBm, f_0 = 824 MHz
All RF Ports - Second Order Harmonics	P_{H2}	-	-48	-46	dBm	33 dBm,f_0 = 1800 MHz, T_A = 25 °C
All RF Ports - Third Order Harmonics	P_{H3}	-	-52	-51	dBm	33 dBm,f_0 = 1800 MHz, T_A = 25 °C
All RF Ports	P_{Hx}	–	-87	-65	dBm	26 dBm ,f_0 = 663 MHz, T_A = 25 °C
Intermodulation Distortion IMD2 [1,2]						
IIP2, low	IIP2,l	100	111	–	dBm	IIP2 conditions Table 8
IIP2, high	IIP2,h	100	116	–	dBm	
Intermodulation Distortion IMD3 [1,2]						
IIP3	IIP3	70	73	–	dBm	IIP3 conditions Table 9

[1] Terminating Port Impedance: $Z_0 = 50\,\Omega$
[2] On application board without any matching components

Table 8: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 9: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

6 MIPI RFFE Specification

Warning: Register_0 and Register_1 RF switch control bits are identical. Writing both Registers Register_0 and Register_1 simultaneously will lead to undefined behavior. The unused register (Register_0 or Register_1) must remain 0x00.

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017', the 'MIPI Alliance Errata 01 for MIPI RFFE Specification version 2.1 - 24 February 2019', and the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. W.'

Table 10: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	Up to 26 MHz
Full speed read	Yes	Up to 26 MHz
Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_SEL pin	Yes	See Table 14

Table 11: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up Default power mode is HIGH
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 12: Switching Time Behavior

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Power Up Settling Time	t_{PUP}	–	6.5	13	µs	Time from Power Up plus Switch command 50% last SCLK falling edge to 90% RF-Signal, see Fig. 3
SW1, SW2 SPST Switching Time	$t_{ST_{SW1,SW2}}$	–	10.5	16	µs	Time switching between RF states 50% last SCLK falling edge to 90% RF-Signal, see Fig. 3
C1 C-Tuner Switching Time	$t_{ST_{C1}}$	–	9.5	17	µs	

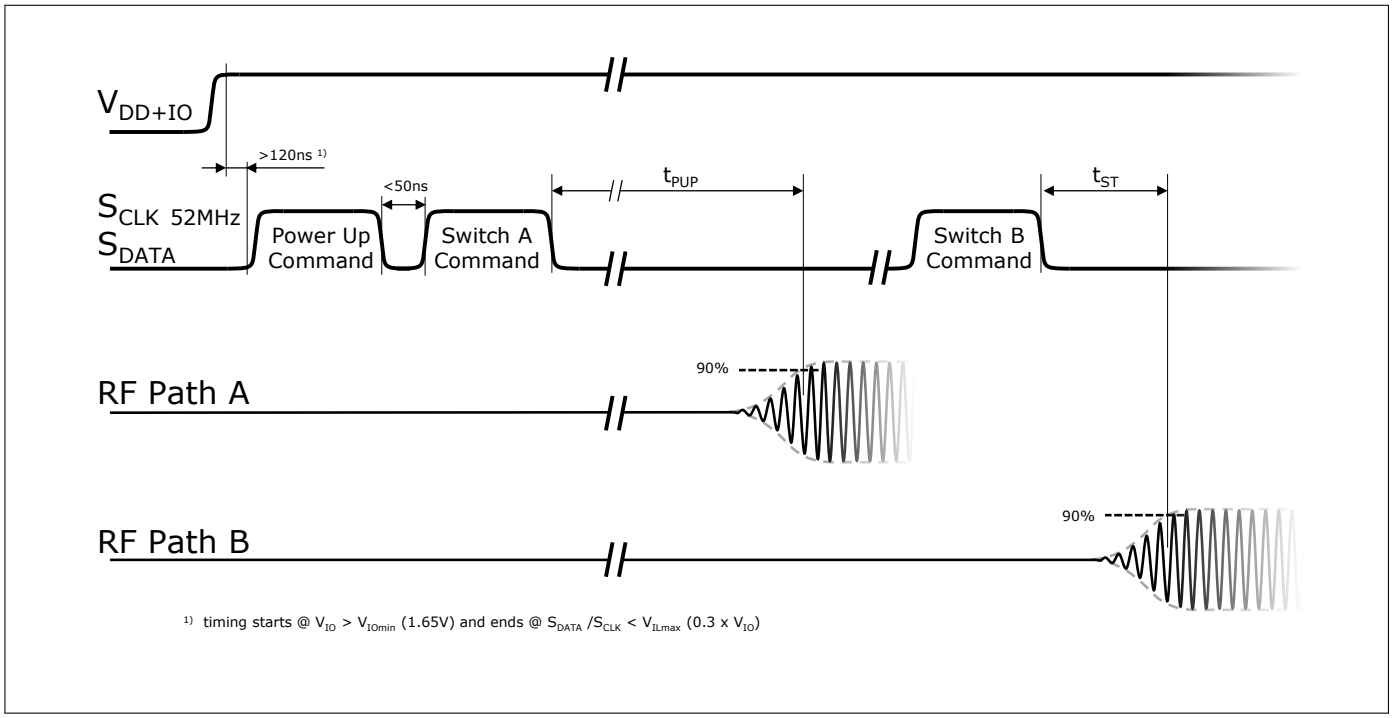

Figure 3: BGSC2341ML10 Switching Time Behavior

Table 13: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	RF Switches and C-Tuner Control	00000000	No	Yes Trigger 0-10	R/W MW
0x01	REGISTER_1	7:0	MODE_CTRL	RF Switches and C-Tuner Control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01001101	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[1:0]	USID_SEL pin	See Tab. 10	No	No	R/W

Table 14: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0001	No	No	R
		3:0	SUB_REVISION	Chip sub revision	0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:4	RESERVED	Reserved for future use	0x0	No	No	R/W
		3:0	BUS_LD[3:0]	Set approximate bus load, default 50 pF 0x8-0xF: Spare	0x4			

Table 15: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_10 are masked. Data is held in shadow registers until the EXT_TRIGGER_10 bit is set to 1.	1	No	No	R/W
				1: Data writes to registers tied to EXT_TRIGGER_10 are not masked. Data writes go directly to the active registers.				MW
		6	TRIGGER_MASK_9	0: Data writes to registers tied to EXT_TRIGGER_9 are masked. Data is held in shadow registers until the EXT_TRIGGER_9 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_9 are not masked. Data writes go directly to the active registers.				
		5	TRIGGER_MASK_8	0: Data writes to registers tied to EXT_TRIGGER_8 are masked. Data is held in shadow registers until the EXT_TRIGGER_8 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_8 are not masked. Data writes go directly to the active registers.				
		4	TRIGGER_MASK_7	0: Data writes to registers tied to EXT_TRIGGER_7 are masked. Data is held in shadow registers until the EXT_TRIGGER_7 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_7 are not masked. Data writes go directly to the active registers.				
		3	TRIGGER_MASK_6	0: Data writes to registers tied to EXT_TRIGGER_6 are masked. Data is held in shadow registers until the EXT_TRIGGER_6 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_6 are not masked. Data writes go directly to the active registers.				
		2	TRIGGER_MASK_5	0: Data writes to registers tied to EXT_TRIGGER_5 are masked. Data is held in shadow registers until the EXT_TRIGGER_5 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_5 are not masked. Data writes go directly to the active registers.				
		1	TRIGGER_MASK_4	0: Data writes to registers tied to EXT_TRIGGER_4 are masked. Data is held in shadow registers until the EXT_TRIGGER_4 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_4 are not masked. Data writes go directly to the active registers.				
		0	TRIGGER_MASK_3	0: Data writes to registers tied to EXT_TRIGGER_3 are masked. Data is held in shadow registers until the EXT_TRIGGER_3 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_3 are not masked. Data writes go directly to the active registers.				

Table 16: Register Mapping, Table IV

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action. Data is held in shadow registers.	0	Yes	No	R/W
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_10				MW
		6	TRIGGER_9	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_9				
		5	TRIGGER_8	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_8				
		4	TRIGGER_7	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_7				
		3	TRIGGER_6	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_6				
		2	TRIGGER_5	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_5				
		1	TRIGGER_4	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_4				
		0	TRIGGER_3	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_3				

Table 17: USID_SEL Selection

Address	Symbol	Configuration	Ext. Condition at USID_SEL Port
USID_SEL6=0110	$Addr_6$	default	ground
USID_SEL9=1001	$Addr_9$	default	to V_{IO}

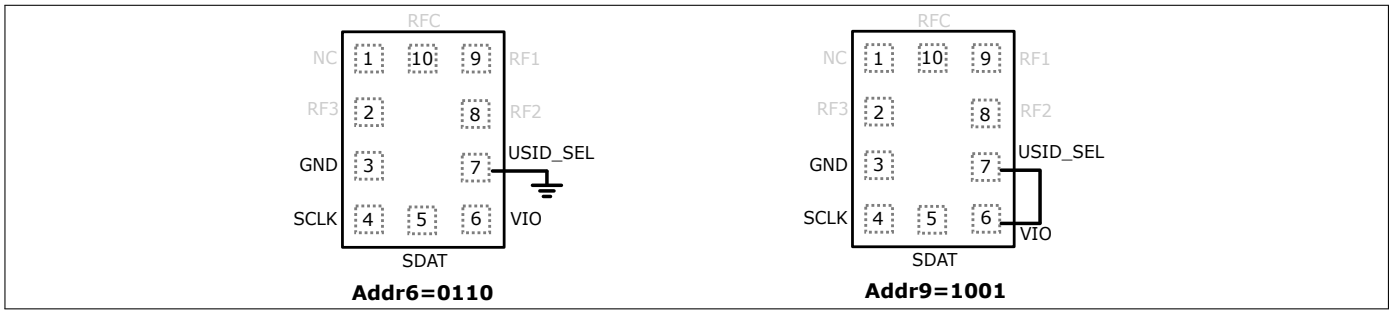

Figure 4: BGSC2341ML10 USID_SEL Pin Configuration

Table 18: Switch MIPI Control Combinations (truth table) [1)]

		REGISTER_0 :C-Tuner control register							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	C_{tune} State 0	X	X	0	X	X	0	0	0
1	C_{tune} State 1	X	X	0	X	X	0	0	1
2	C_{tune} State 2	X	X	0	X	X	0	1	0
3	C_{tune} State 3	X	X	0	X	X	0	1	1
4	C_{tune} State 4	X	X	0	X	X	1	0	0
5	C_{tune} State 5	X	X	0	X	X	1	0	1
6	C_{tune} State 6	X	X	0	X	X	1	1	0
7	C_{tune} State 7	X	X	0	X	X	1	1	1
8	SPDT ALL OFF	X	X	0	0	0	X	X	X
9	SPDT RF SW1 ON	X	X	0	0	1	X	X	X
10	SPDT RF SW2 ON	X	X	0	1	0	X	X	X
11	SPDT RF SW1,SW2 ON	X	X	0	1	1	X	X	X

[1)] measured according to the measurement set-up of Fig. 2

Combination of any state here above mentioned in Table 15 can be programmed in one single MIPI sequence. As an example, programmation of RF1 ON RF2 ON C tuner in state 1 can be done in one MIPI data frame with register 0x1=0bxx011001.

7 Application Information

Pin Configuration and Function

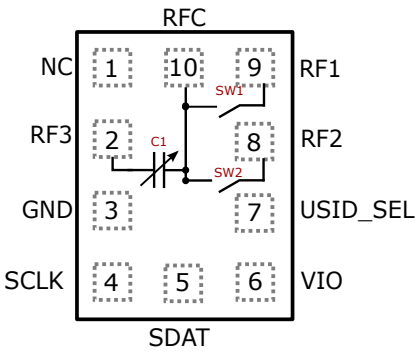

Figure 5: BGSC2341ML10 Pin Configuration (top view)

Table 19: Pin Definition and Function of BGSC2341ML10 in Swap Configuration:USID=0111

Pin No.	Name	Pin Type	Function
1	NC	-	Not Connected
2	RF3	I/O	Input/Output Tunable Capacitor Port
3	GND	I/O	Ground
4	SCLK	I	MIPI Control Signal SCLOCK(Default)
5	SDAT	I/O	MIPI Control Signal SDATA(Default)
6	VIO	I	MIPI/DC Voltage Supply
7	USID_SEL	I	USID_SEL hardware pin for USID selection (see Table.17)
8	RF2	I/O	Input/Output RF Switch 2
9	RF1	I/O	Input/Output RF Switch 1
10	RFC	I/O	Input/Output RF Common Port

Table 20: ESD robustness, System Level Test (SLT)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD SLT [1]	$V_{ESD_{SLT}}$	-8 [2]	–	+8 [2]	kV	RF vs system GND, with 27 nH shunt inductor

[1] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.
[2] For RFC path only.

8 Package Information

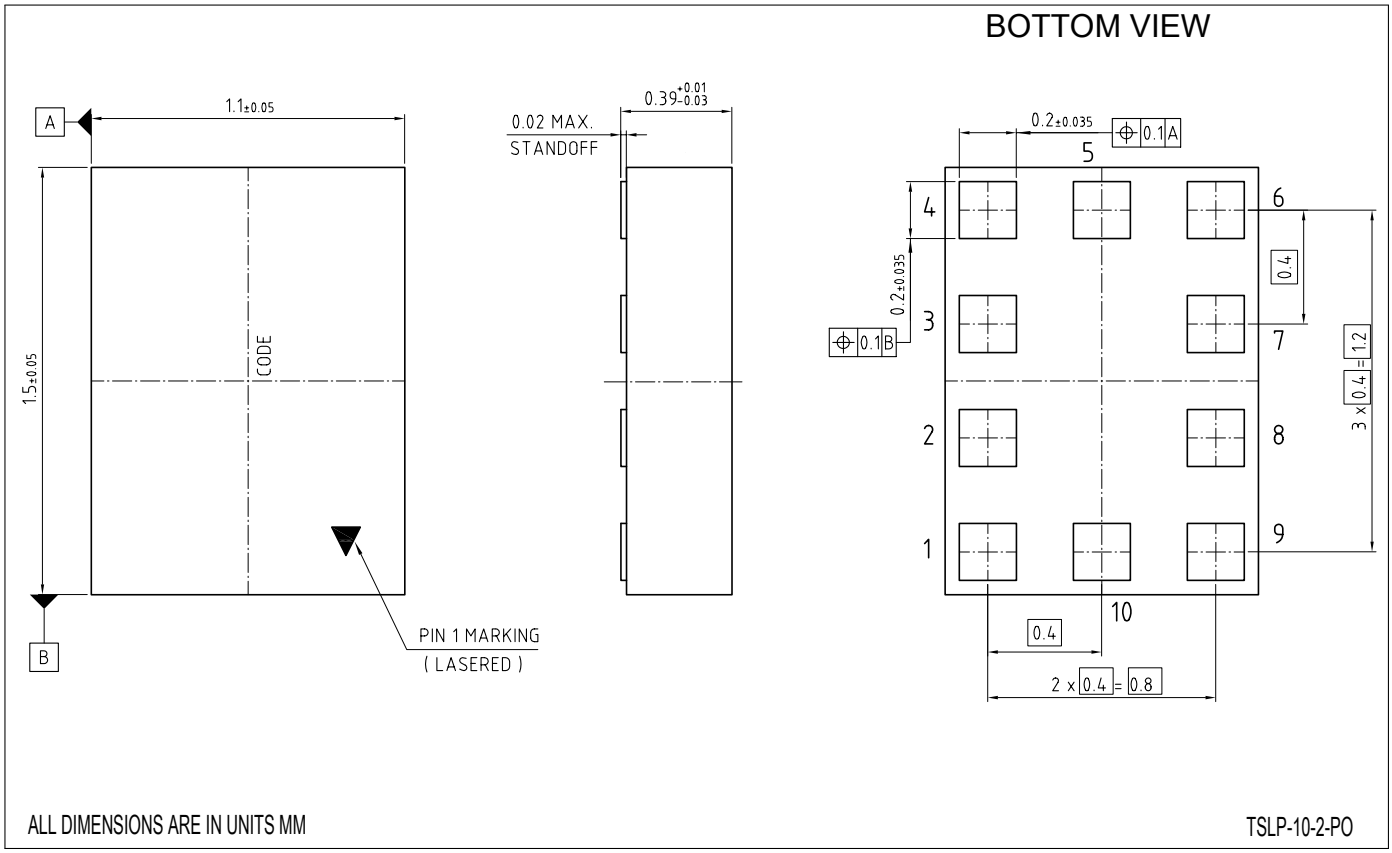

Figure 6: TSLP-10-2 Package Outline (top, side and bottom views)

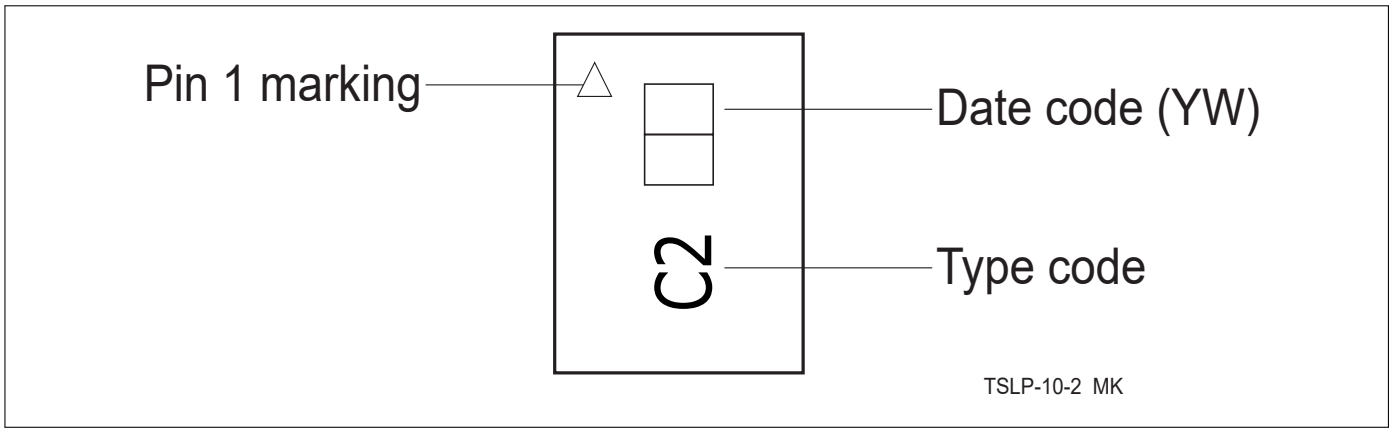

Figure 7: Marking Specification (top view): Date code digits Y and W defined in Table 21/22

Table 21: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

Table 22: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

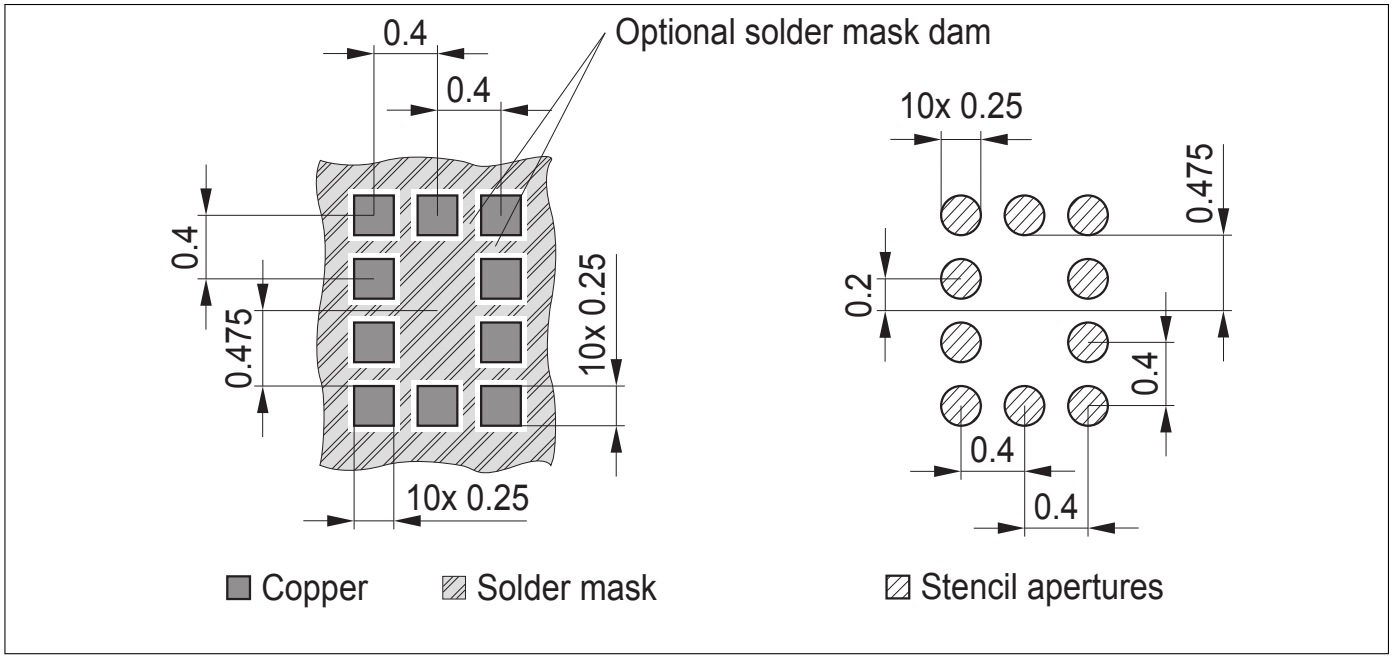

Figure 8: Footprint Recommendation

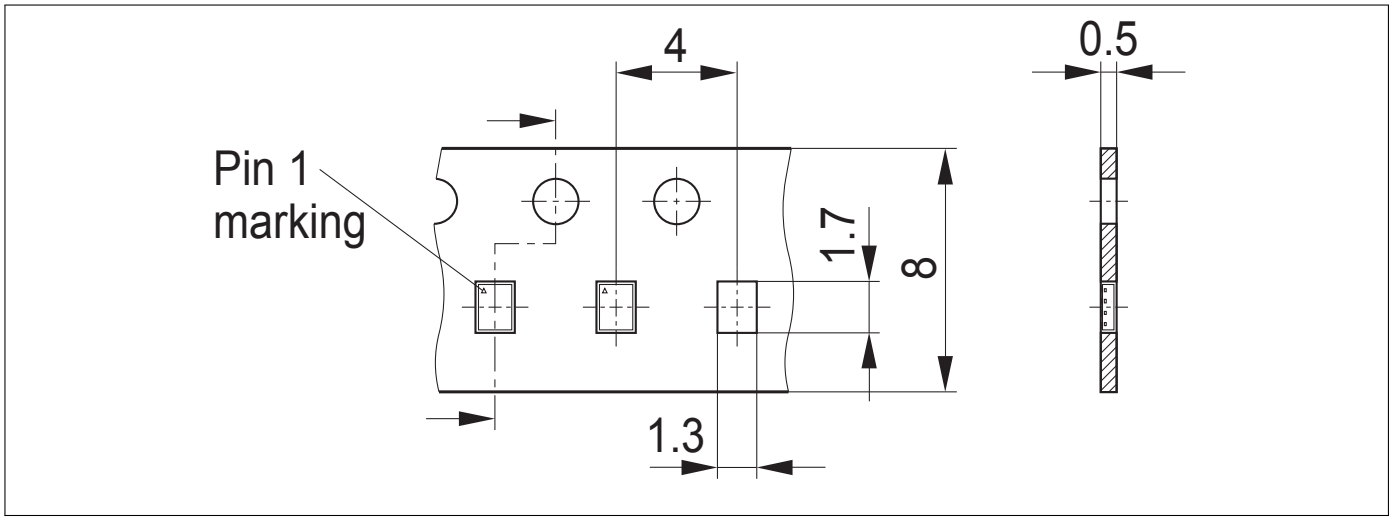

Figure 9: TSLP-10-2 Carrier Tape

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.3, 2021-09-19	
	4th version of the final datasheet with update in Table 4-6 (capacitance performance) and Table 18 (truth table)

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