User's Guide

TPS62102 Buck Converter Evaluation Module User's Guide

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1 Features

The TPS62102 Low-Power High-Efficiency Buck Converter includes:

- 2.5-V to 9-V input range
- 0.8-V to 8-V output range
- Dual auto mode for high efficiency at light loads
- Externally synchornizable
- 0% to 100% duty cycle
- BICMOS for low quiescient, standby, and shutdown currents
- 8-pin SOIC (D) package

2 Description

The TPS62102EVM–01 evaluation module is supplied fully assembled and ready to test. This evaluation module demonstrates an automatic mode switching converter that is capable of 500-mA output current at 3.3 V. The switching frequency of this converter is 1 MHz free running. Other versions of this converter IC are available that have nominal switching frequencies of 300 kHz, 600 kHz, and 2 MHz. Note that the fundamental frequencies have been chosen to minimize interaction with 455-kHz intermediate frequency (IF) circuits. The user needs to supply a power source and suitable load. Figure 2-1 is the schematic of the evaluation module as assembled. In this configuration, the converter should have a closed-loop bandwidth of approximately 40 kHz.

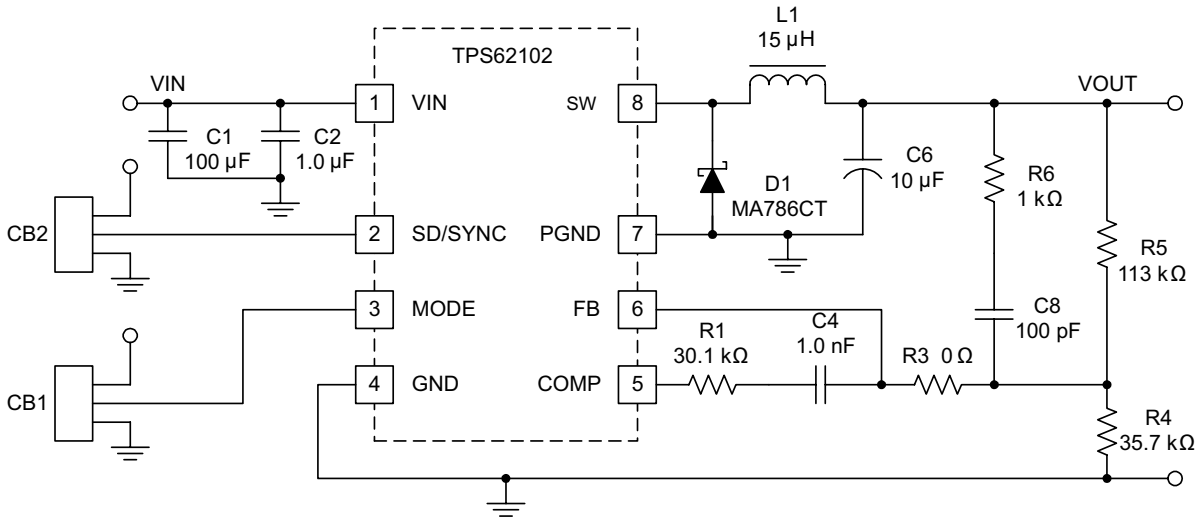

Figure 2-1. Evaulation Module Schematic

This evaluation module allows user control over the SD/SYNC and MODE pins of the TPS62102. As supplied, the MODE (CB1) pin should be left floating. This allows the TPS62102 to automatically determine whether it operates in the continuous frequency mode or in a pulsed frequency modulation (PFM) mode of operation. See the TPS62102 data sheet for details[1].

The SD/SYNC pin is jumpered to ground by default. This allows the TPS62102 to free run. Do not allow this pin to float, as it causes erratic and unpredictable behavior. To synchronize the converter to an external source, connect the source to the middle pin of CB2. The source should pulse its output at a frequency higher than the free running frequency of the converter. Attempting to synchronize to a lower frequency than this results in erratic behavior. The pulse amplitude should be between 2 V and the VIN supplied to the evaluation module. Do not use a pulse amplitude higher than VIN. Minimum pulse width for syncro- nous signals is 50 ns. This pin can also cause the converter to shut down and enter a low-current mode of operation. To do this, pull the SD/SYNC pin to 2 V or more, and hold it there as long as shutdown is desi- red. Shutdown occurs approximately 20 ms after SD/SYNC is brought high.

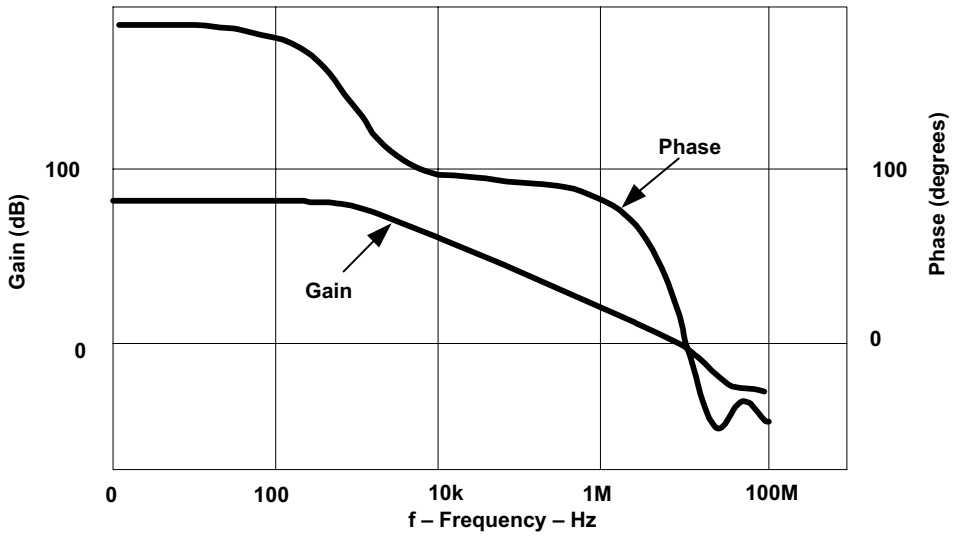

Figure 2-2. Gain/Phase Response for the Internal Error Amplifier

3 Feedback Considerations

Figure 3-1 shows the gain and phase response for the internal error amplifier. In addition to thecompensation configuration used, many other feedback configurations are provided for on the evaluation module by using the optional component footprints. Figure 3-1 shows the schematic of the evaluation module with these additional footprints. As is evident, most any common feedback implementation can be achieved by simply shorting across pads or inserting passive components. The extra footprints are all 1206 size for ease of use.

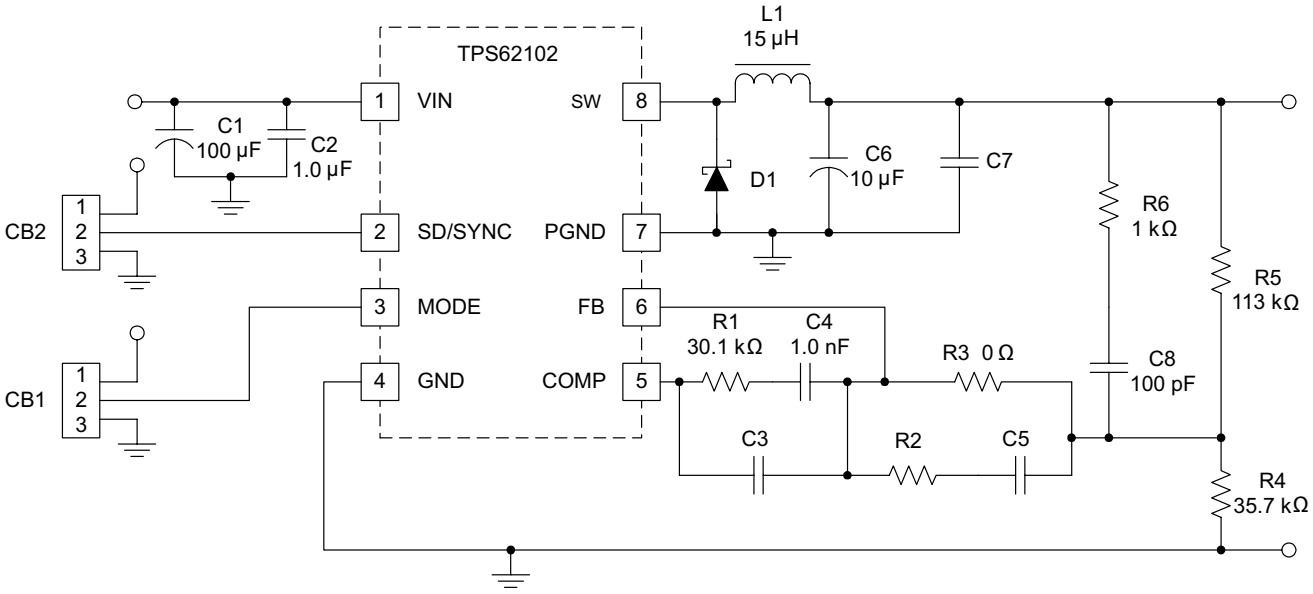

Figure 3-1. Complete Evaulation Module Schematic

3.1 Error Amplifier

The error amplifier in this chip has a significant impact on what can be done with the feedback loop. To get a realistic model, assume that the error amplifier has 80 dB (dc) gain, with a 2-MHz GBWP. This may be a bit conservative, but ensures a stable loop if designed with these constraints.

3.2 Open-Loop Small Signal AC Model

The circuit of Figure 3-2 is used to define the feedback loop for this evaluation module.

3.2.1 Open-Loop Small Signal AC Model

M1 is the lumped gain corresponding to the input voltage and the PWM gain. Since the ramp height in the chip is about 1V the PWM gain is 100%/V or just 1 in the free running case. The 8x factor comes from the input voltage of 8 V. The PWM gain increases with synchronization. For instance, syncronizing a 1-MHz nominal free run oscillator to 1.2 MHz increases the PWM gain to:

$$G_{SYNC} = \frac{F_{SYNC}}{F_{FREE}} \times G_{FREE} \quad (1)$$

where

- G_{FREE} is the free running PWM gain (one here)
- G_{SYNC} is the synchronized PWM gain
- F_{FREE} is the free running oscillator frequency
- F_{SYNC} is the synchronized frequency

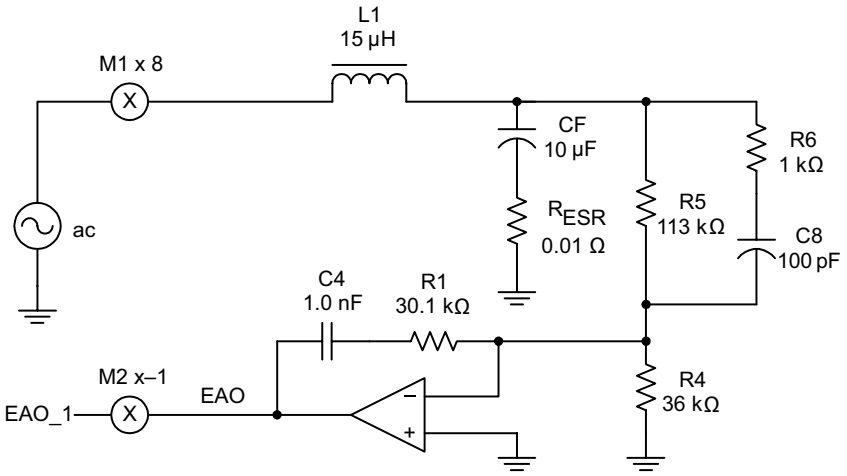

Figure 3-2. Open-Loop Small Signal Alternating Current (AC) Model

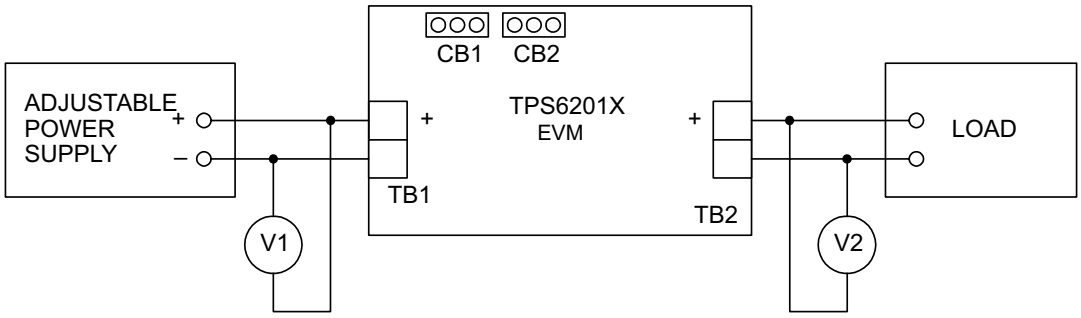

Figure 3-3. Connection Diagram

4 Operating Instructions

4.1 Connect a DC Power Supply to Terminal TB1

The power supply should be capable of supplying up to 10 V at 0.5 A. The power supply should be set to its minimum output voltage level and current limited to 0.5 A.

4.2 Connect the Load to TB2

This load should be capable of handling 0.5 A at 3.5 V.

4.3 Place a Jumper on CB2

- Placing the jumper from pin 1 to pin 2 pulls SD/SYNC high, resulting in converter shutdown.
- Placing a jumper from pin 2 to pin 3 pulls SD/SYNC low, resulting in normal operation.

4.3.1 Placing a Jumper on CB1 is Optional

- A jumper from pin 1 to pin 2 sets MODE high, forcing the converter into the constant-frequency, heavy-load mode.
- A jumper from pin 2 to pin 3 sets MODE low, forcing the converter into the pulsed-variable low power mode.
- Letting MODE float, not using a jumper on CB1, allows the converter to operate in auto-mode, the output load detector circuitry determines if the converter should be running inthe constant-frequency or pulsed-variable frequency mode.

4.4 Turn on the Electronic Load

Adjust the load to operate between 10 mA and 500 mA.

4.5 Turn on the Input Power Supply

Starting with the input dc power supply at its minimum setting, slowly increase the voltage to7 V ±0.5 V.

4.6 Shut Down the Converter

To shut down the converter, decrease the dc input power supply voltage to zero. Turn off the electronic load.

5 Evaluation Module Layouts

Evaluation module layout examples of the TPS62102EVM–01 PCB are shown in Figure 5-1 through Figure 5-3. They are not to scale and appear here only as a reference.

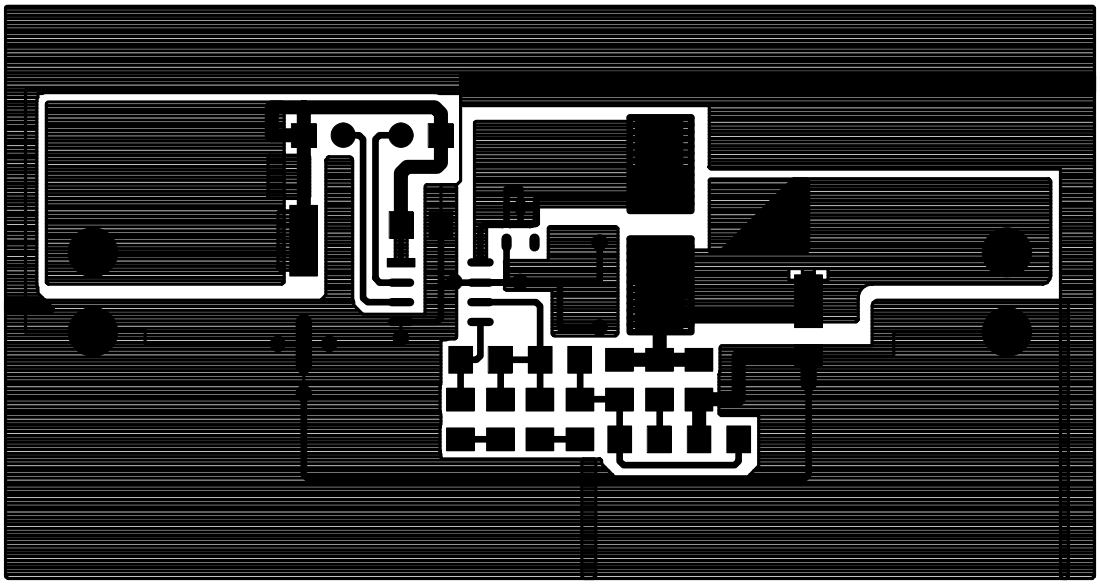

Figure 5-1. Top Layer (Top View)

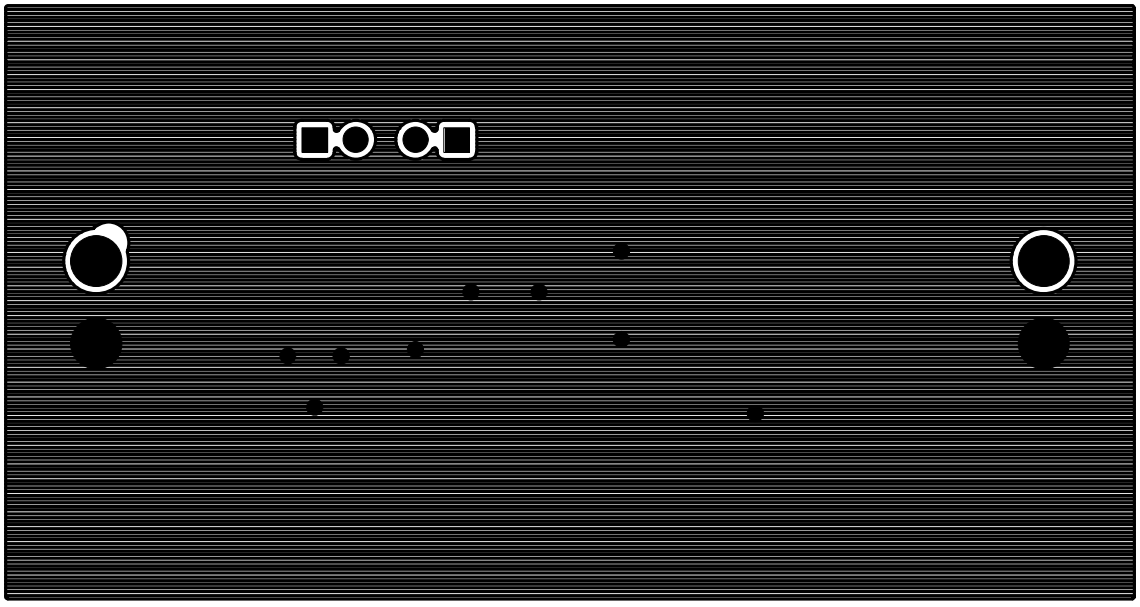

Figure 5-2. Bottom Layer (Top View)

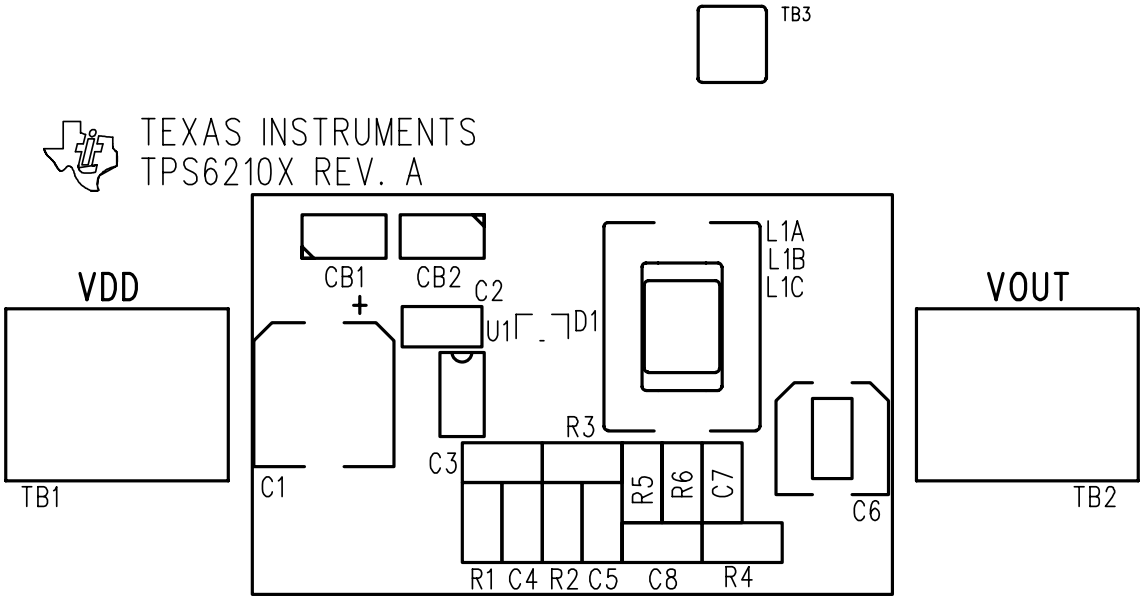

Figure 5-3. Assenmbly Drawing (Top Assembly)

6 Evalulation Module Components

Description	Reference	Qty	Value/Type Number	Manufacturer	PartNumber
Capacitors	C1	1	100mF,±20%,25 V, electrolytic	Panasonic–ECG	ECE–V1EA101UP
	C2	1	1.0mF,+80%/–20%, 25 V, ceramic, Y5V	Panasonic–ECG	ECJ–3YF1E105Z
	C3,C5, C7	0	Forevaluation use only		
	C4	1	1.0nF, ±10%,X7R, 50 V, ceramic	PhycompUSA, Inc.	12062R102K9B20D
	C6	1	10mF,±10%,X7R, 10 V, ceramic	Taiyo Yuden	LMK325BJ106MN
	C8	1	100 pF, ±5%, 50 V, NPO ceramic	PhycompUSA, Inc.	1206CG101J9B200
Diodes	D1	1	100mA, Shottky diode	Panasonic– SSG	MA3X786
Jumpers	CB1,CB2	2	100mil, 3-terminal, strip–line SIP socket	AriesElectronics	12–0511–10
Inductors	L1	1	15mH,inductor	CoilCraft	DT1608–153
Resistors	R1	1	30.1kW,±1%,metal film resistor, 1/8W	Panasonic–ECG	ERJ–8ENF3012V
	R2	0	Forevaluation use only		
	R3	1	0kW,±1%,metal film resistor, 1/8W	PhycompUSA, Inc.	9C12063A0R00FKHF T
	R4	1	35.7kW,±1%,metal film resistor, 1/8W	Panasonic–ECG	ERJ–8ENF3572V
	R5	1	113kW,±1%,metal film resistor, 1/8W	Panasonic–ECG	ERJ–8ENF1133V
	R6	1	1.0kW,±5%,metal film resistor, 1/8W		ERJ–8GEYJ102V
Terminal Blocks	TB1,TB2	2	2–positionterminal block connector	Weidmuller	171602
ICs	U1	1	Low-powersynchronous buck controller	TI	TPS62102DR
PCBs	n/a	1	Printedcircuit board, FR4, 2 oz., 2.800” x 1.500” x 0.063”	n/a	SLUP055

7 References

Texas Instruments, TPS62102 Low-Power High-Efficiency Buck Converter Data Sheet

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2001) to Revision A (June 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

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