Product Change Notification

(Notification - P1808046c-DIGI)

(CST-R2-AD141 / FKZ001)

August 16, 2018

To: *Our Valued Digi-Key Electronics Customer*

Overview: The purpose of this notification is to communicate a product change of select Renesas Electronics America, Inc. (REA) devices.

This notification announces the generation change of 32Mb and 64Mb Low Power SRAM products, with a die shrink from 0.15um to 0.11um process. There is a part number change.

Along with the die shrink, the following items may also change (please see the Appendix for specific details and replacement part availability).

1. Assembly site from Renesas Semiconductor (Beijing, China) to Greatek Electronics Inc. (Taiwan)
2. Base Metal of Lead Frame from 42Alloy to Cu
3. Lead Plating from SN-Cu to Cu
4. Inner structure of package
5. Package dimensions
6. Packing Tray specification
7. Tape and Reel specification
8. Moisture Sensitivity Level from MSL2 to MSL3
9. Electrical specifications

Affected Products: A review of our records indicates the products listed in Appendix 1 may affect your company.

Part numbers given in this list are for active part numbers in REA database at the time of this notification.

Key Dates:

Final last time buy (LTB) orders placed to REA or to a franchised REA distributor.	**June 15th, 2019**
Planned date for last time shipment (LTS) from REA.	**Dec. 15th, 2019**
Replacement part sample availability and mass production	**See Appendix 1**

Response: Please place last time buy (LTB) orders in a timely manner prior to the key dates listed to avoid product availability issues. If you anticipate volumes beyond your regular rate, please contact your REA sales representative with a forecast of your requirements. Shipments between the LTB and LTS dates are Non-Cancelable and Non-Returnable (NCNR).

Please work with your REA sales representative and/or FAE to transition to the replacement devices.

Please contact your REA sales representative for any questions or comments.

Thank you for your attention.

Sincerely,

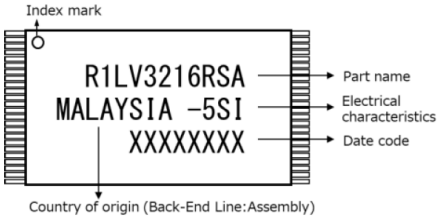
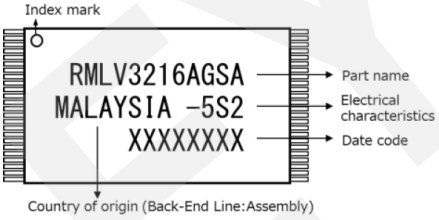
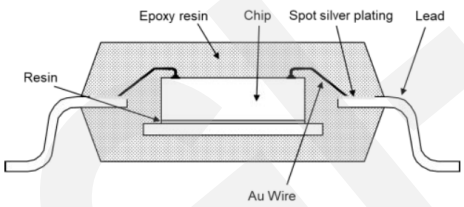
Renesas Electronics America, Inc.

Appendix 1: Affected Part Numbers & Replacement Device Availability for Digi-Key

Density	Package Type	Affected Part Number	Replacement Part Number	Samples	Mass Production
32Mb	48pin-TSOP(I)	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0	Oct. 2018	Jan. 2019
		R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0		
	52pin-µTSOP	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0	Dec. 2018	Mar. 2019
		R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0		
64Mb	48pin-TSOP(I)	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0		
		R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0		
	52pin-µTSOP	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0		
		R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0		
	48ball-FBGA	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0	Oct. 2018	Jan. 2019
		R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0		

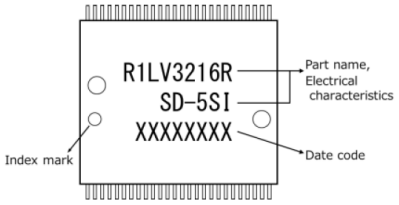
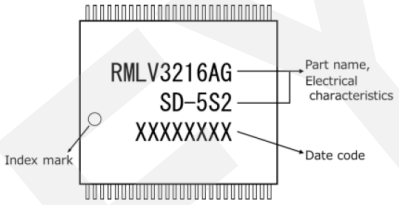
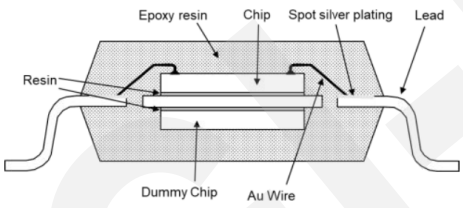
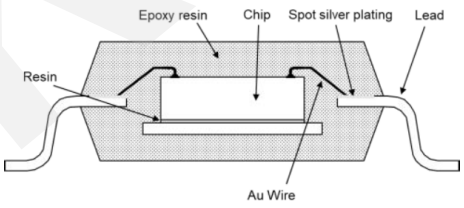
Appendix 2: Change Details

(1) 32Mb 48pin-TSOP(I) Part name： R1LV3216RSA-5SI

Item		EOL product	Successor product
Orderable part name		R1LV3216RSA-5SI#B1 (Tray packing)	RMLV3216AGSA-5S2#AA0 (Tray packing)
		R1LV3216RSA-5SI#S1 (Tape & Reel packing)	RMLV3216AGSA-5S2#KA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Amkor Technology Malaysia (Malaysia)	←
Country of origin display		MALAYSIA	←
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	←
Package marking specification			
Assembly Material	Lead frame material	Cu	←
	Lead plating	Sn (pure tin)	←
	Die bonding	Epoxy paste	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-free)	←
	Inner structure of package		←
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)	←
	Storage number	96pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	362mm x 340mm x 60mm	←
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in orderable part name)

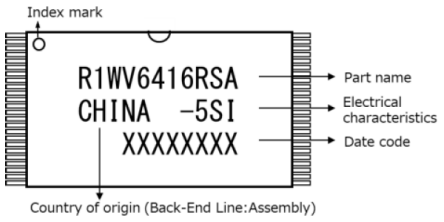
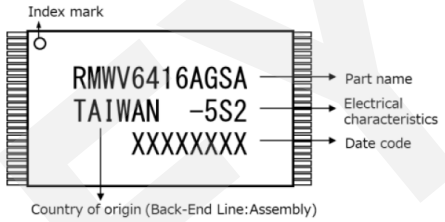
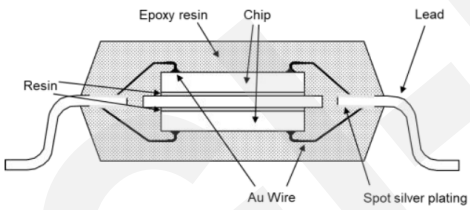
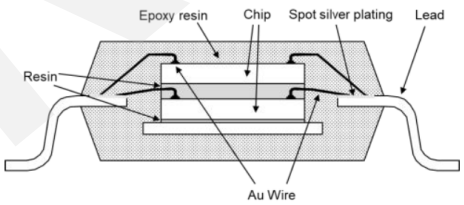
Appendix 3: Change Details

(2) 32Mb 52pin-μTSOP Part name： R1LV3216RSD-5SI

Item		EOL product	Successor product
Orderable part name		R1LV3216RSD-5SI#B0 (Tray packing)	RMLV3216AGSD-5S2#AA0 (Tray packing)
		R1LV3216RSD-5SI#S0 (Tape & Reel packing)	RMLV3216AGSD-5S2#HA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	Changed
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

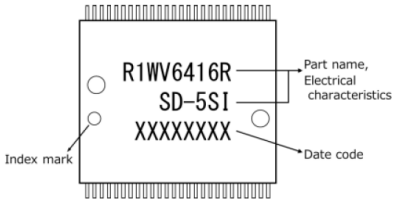
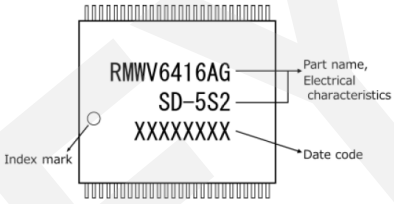
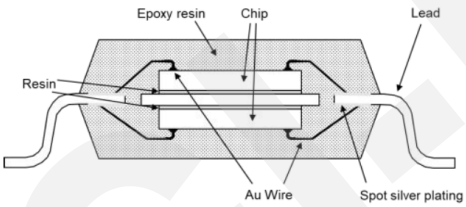
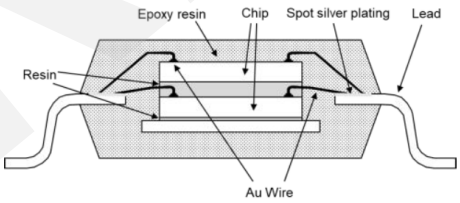
Appendix 4: Change Details

(3) 64Mb 48pin-TSOP(I) Part name： R1WV6416RSA-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RSA-5SI#B0 (Tray packing)	RMWV6416AGSA-5S2#AA0 (Tray packing)
		R1WV6416RSA-5SI#S0 (Tape & Reel packing)	RMWV6416AGSA-5S2#KA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
Country of origin display		CHINA	TAIWAN
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy film
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)	←
	Storage number	96pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	←
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	362mm x 340mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

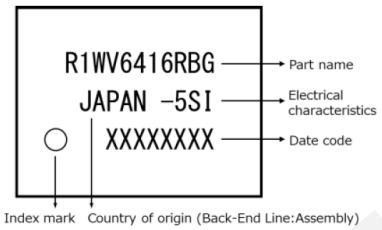
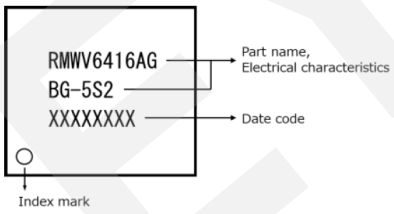
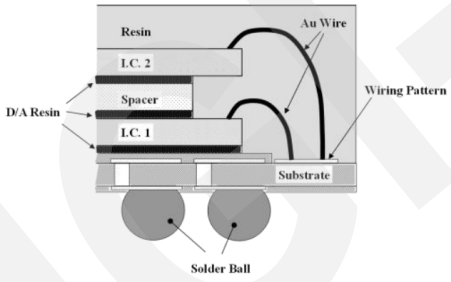
Appendix 5: Change Details

(4) 64Mb 52pin-μTSOP Part name： R1WV6416RSD-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RSD-5SI#B0 (Tray packing)	RMWV6416AGSD-5S2#AA0 (Tray packing)
		R1WV6416RSD-5SI#S0 (Tape & Reel packing)	RMWV6416AGSD-5S2#HA0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		Renesas Semiconductor Beijing (China)	Greatek Electronics Inc. (Taiwan)
JEITA Package Code		P-TSOP(2)52-8.89x10.79-0.40	←
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy film
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-24)	←
	Storage number	230pcs/tray	←
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	New specification
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

Appendix 6: Change Details

(5) 64Mb 48ball-FBGA Part name： R1WV6416RBG-5SI

Item		EOL product	Successor product
Orderable part name		R1WV6416RBG-5SI#B0 (Tray packing)	RMWV6416AGBG-5S2#AC0 (Tray packing)
		R1WV6416RBG-5SI#S0 (Tape & Reel packing)	RMWV6416AGBG-5S2#KC0 (Tape & Reel packing)
Wafer process line		Renesas Semiconductor Manufacturing Co.,Ltd. Saijo Factry (Japan)	←
Memory cell		TFT Load type Capacitor cell	←
Design rule		0.15um	0.11um
Assembly line		J-Devices Kumamoto District (Japan)	←
Country of origin display		JAPAN	No display
JEITA Package Code		P-TFBGA48-8.5x11-0.75	P-TFBGA48-7.5x8.5-0.75
Package Dimensions		8.5 x 11.0mm	7.5 x 8.5mm
Ball Pitch		0.75mm	←
Package marking specification			
Assembly Material	Substrate material	Glass epoxy	←
	Solder ball	Sn-Ag-Cu	←
	Die bonding	Epoxy film	←
	Wire bonding	Au	←
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
	Inner structure of package		←
Die thickness		Current thickness	←
Final test line		Powertech Technology Inc. (Taiwan)	←
Tray packing	Tray	JEDEC Tray with Renesas Logo (Tray type name : L196-121)	JEDEC Tray with Renesas Logo (Tray type name : L196-45) (Same as other 7.5x8.5mm 48ball FBGA Type)
	Storage number	242pcs/tray	253pcs/tray
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	←
	Number of trays (Max.)	10 trays + 1 tray (cover)	←
	Inner box size (LxWxH)	351mm x 175mm x 104mm	←
Tape & Reel packing	Embossed tape	Current specification	New specification (Same as other 7.5x8.5mm 48ball FBGA Type)
	Storage number	1,000pcs/reel	←
	Inner box size (LxWxH)	289mm x 264mm x 60mm	←
Moisture-proof performance		MSL 3	←
Shipping label		Current specification	No change in format (Changes in orderable part name)

Appendix 7: 32Mb Electrical Characteristics (AC/DC)

(1)–a. Electrical characteristics (DC) : 32Mb

Products

Item	EOL product	Successor product
Orderable part name	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0
	R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0
	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0
	R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0

DC conditions

Item	Symbol	EOL product	Symbol	Successor product
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40℃～85℃	Ta	←
Input high voltage	VIH	2.4V(min.) / Vcc+0.2V(max.)	VIH	2.2V(min.) / Vcc+0.3V(max.)
Input low voltage	VIL	-0.2V(min.) / 0.4V(max.)	VIL	-0.3V(min.) / 0.6V(max.)

DC characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Operating Current	Icc1(TTL, Min.Cycle)	55mA(max.) / 40mA(typ.)		Icc1(TTL, Min.Cycle)	35mA(max.) / 27mA(typ.)	
	Icc2(MOS, Cycle=1us)	8mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	4mA(max.) / 2mA(typ.)	
Standby current	ISB(TTL)	0.3mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	12uA(max.) / 4uA(typ.)	ISB1(MOS)	～25℃	4uA(max.) / 0.6uA(typ.)
		～40℃	24uA(max.) / 7uA(typ.)		～40℃	6uA(max.) / 1uA(typ.)
		～70℃	50uA(max.)		～70℃	17uA(max.) / 4uA(typ.)
		～85℃	80uA(max.)		～85℃	24uA(max.) / 8uA(typ.)
Output high voltage	VOH	IOH=-1mA	–	VOH	IOH=-1mA	2.4V(min.)
		IOH=-0.5mA	2.4V(min.)		IOH=-0.5mA	–
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	EOL product	Symbol	Successor product
Input capacitance	C in	10pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Vcc for data retention	VDR	2.0V(min.)		VDR	1.5V(min.)	
Data retention current	IccDR	～25℃	12uA(max.) / 4uA(typ.)	IccDR	～25℃	4uA(max.) / 0.6uA(typ.)
		～40℃	24uA(max.) / 7uA(typ.)		～40℃	6uA(max.) / 1uA(typ.)
		～70℃	50uA(max.)		～70℃	17uA(max.) / 4uA(typ.)
		～85℃	80uA(max.)		～85℃	24uA(max.) / 8uA(typ.)
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

Appendix 7 (cont.): 32Mb Electrical Characteristics (AC/DC)

(1)–b. Electrical characteristics (AC) : 32Mb

Products

Item	EOL product	Successor product
Orderable part name	R1LV3216RSA-5SI#B1	RMLV3216AGSA-5S2#AA0
	R1LV3216RSA-5SI#S1	RMLV3216AGSA-5S2#KA0
	R1LV3216RSD-5SI#B0	RMLV3216AGSD-5S2#AA0
	R1LV3216RSD-5SI#S0	RMLV3216AGSD-5S2#HA0

AC characteristics
Read Cycle

Item	Symbol	EOL product	Symbol	Successor product
Read cycle time	tRC	55ns(min.)	tRC	←
Address access time	tAA	55ns(max.)	tAA	←
Chip select access time	tACS1 / tACS2	55ns(max.)	tACS1 / tACS2	45ns(max.)
Output enable to output valid	tOE	25ns(max.)	tOE	22ns(max.)
Output hold from address change	tOH	10ns(min.)	tOH	←
LB#,UB# access time	tBA	55ns(max.)	tBA	45ns(max.)
Chip select to output in low-Z	tCLZ1 / tCLZ2	10ns(min.)	tCLZ1 / tCLZ2	←
LB#,UB# enable to low-Z	tBLZ	5ns(min.)	tBLZ	←
Output enable to output in low-Z	tOLZ	5ns(min.)	tOLZ	←
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 18ns(max.)
LB#,UB# disable to high-Z	tBHZ	0ns(min.) / 20ns(max.)	tBHZ	0ns(min.) / 18ns(max.)
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 18ns(max.)

Write Cycle

Item	Symbol	EOL product	Symbol	Successor product
Write cycle time	tWC	55ns(min.)	tWC	←
Address valid to end of write	tAW	50ns(min.)	tAW	35ns(min.)
Chip select to end of write	tCW	50ns(min.)	tCW	35ns(min.)
Write pulse width	tWP	40ns(min.)	tWP	35ns(min.)
LB#,UB# valid to end of write	tBW	50ns(min.)	tBW	35ns(min.)
Address setup time	tAS	0ns(min.)	tAS	←
Write recovery time	tWR	0ns(min.)	tWR	←
Data to write time overlap	tDW	25ns(min.)	tDW	←
Data hold from write time	tDH	0ns(min.)	tDH	←
Output enable from end of write	tOW	5ns(min.)	tOW	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 18ns(max.)
Write to output in high-Z	tWHZ	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 18ns(max.)

Appendix 7: 64Mb Electrical Characteristics (AC/DC)

(2)–a. Electrical characteristics (DC) : 64Mb

Products

Item	EOL product	Successor product
Orderable part name	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0
	R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0
	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0
	R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0
	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0
	R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0

DC conditions

Item	Symbol	EOL product	Symbol	Successor product
Supply voltage	Vcc	2.7V～3.6V	Vcc	←
Operating temperature range	Ta	-40℃～85℃	Ta	←
Input high voltage	VIH	2.4V(min.) / Vcc+0.2V(max.)	VIH	2.2V(min.) / Vcc+0.3V(max.)
Input low voltage	VIL	-0.2V(min.) / 0.4V(max.)	VIL	-0.3V(min.) / 0.6V(max.)

DC characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Operating Current	Icc1(TTL, Min.Cycle)	60mA(max.) / 45mA(typ.)		Icc1(TTL, Min.Cycle)	38mA(max.) / 29mA(typ.)	
	Icc2(MOS, Cycle=1us)	10mA(max.) / 5mA(typ.)		Icc2(MOS, Cycle=1us)	5mA(max.) / 2.5mA(typ.)	
Standby current	ISB(TTL)	0.3mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	～25℃	24uA(max.) / 8uA(typ.)	ISB1(MOS)	～25℃	8uA(max.) / 1.2uA(typ.)
		～40℃	48uA(max.) / 14uA(typ.)		～40℃	12uA(max.) / 2uA(typ.)
		～70℃	100uA(max.)		～70℃	34uA(max.)
		～85℃	160uA(max.)		～85℃	46uA(max.)
Output high voltage	VOH	IOH=-1mA	–	VOH	IOH=-1mA	2.4V(min.)
		IOH=-0.5mA	2.4V(min.)		IOH=-0.5mA	–
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	EOL product	Symbol	Successor product
Input capacitance	C in	20pF(max.)	C in	←
Input/Output capacitance	C I/O	20pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	EOL product		Symbol	Successor product	
Vcc for data retention	VDR	2.0V(min.)		VDR	1.5V(min.)	
Data retention current	IccDR	～25℃	24uA(max.) / 8uA(typ.)	IccDR	～25℃	8uA(max.) / 1.2uA(typ.)
		～40℃	48uA(max.) / 14uA(typ.)		～40℃	12uA(max.) / 2uA(typ.)
		～70℃	100uA(max.)		～70℃	34uA(max.)
		～85℃	160uA(max.)		～85℃	46uA(max.)
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

Appendix 7 (cont.): 64Mb Electrical Characteristics (AC/DC)

(2)–b. Electrical characteristics (AC) : 64Mb

Products

Item	EOL product	Successor product
Orderable part name	R1WV6416RSA-5SI#B0	RMWV6416AGSA-5S2#AA0
	R1WV6416RSA-5SI#S0	RMWV6416AGSA-5S2#KA0
	R1WV6416RSD-5SI#B0	RMWV6416AGSD-5S2#AA0
	R1WV6416RSD-5SI#S0	RMWV6416AGSD-5S2#HA0
	R1WV6416RBG-5SI#B0	RMWV6416AGBG-5S2#AC0
	R1WV6416RBG-5SI#S0	RMWV6416AGBG-5S2#KC0

AC characteristics

Read Cycle

Item	Symbol	EOL product	Symbol	Successor product
Read cycle time	tRC	55ns(min.)	tRC	←
Address access time	tAA	55ns(max.)	tAA	←
Chip select access time	tACS1 / tACS2	55ns(max.)	tACS1 / tACS2	←
Output enable to output valid	tOE	25ns(max.)	tOE	←
Output hold from address change	tOH	10ns(min.)	tOH	←
LB#,UB# access time	tBA	55ns(max.)	tBA	←
Chip select to output in low-Z	tCLZ1 / tCLZ2	10ns(min.)	tCLZ1 / tCLZ2	←
LB#,UB# enable to low-Z	tBLZ	5ns(min.)	tBLZ	←
Output enable to output in low-Z	tOLZ	5ns(min.)	tOLZ	←
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	←
LB#,UB# disable to high-Z	tBHZ	0ns(min.) / 20ns(max.)	tBHZ	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	←

Appendix 7 (cont.): 64 Electrical Characteristics (AC/DC)

(2)–b. Electrical characteristics (AC) : 64Mb

Write Cycle

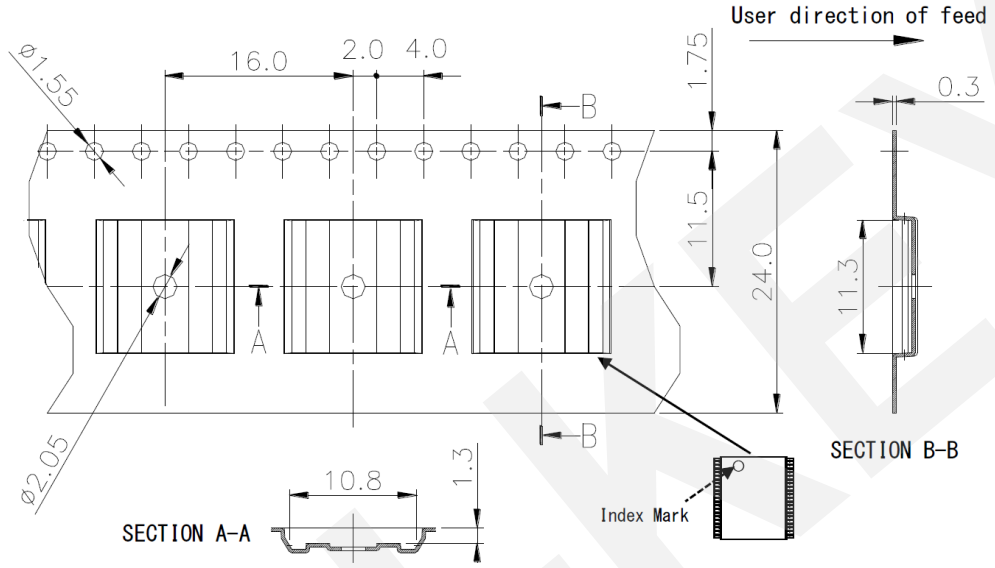
Item	Symbol	**EOL product**	Symbol	**Successor product**
Write cycle time	tWC	55ns(min.)	tWC	←
Address valid to end of write	tAW	50ns(min.)	tAW	45ns(min.)
Chip select to end of write	tCW	50ns(min.)	tCW	45ns(min.)
Write pulse width	tWP	40ns(min.)	tWP	←
LB#,UB# valid to end of write	tBW	50ns(min.)	tBW	45ns(min.)
Address setup time	tAS	0ns(min.)	tAS	←
Write recovery time	tWR	0ns(min.)	tWR	←
Data to write time overlap	tDW	25ns(min.)	tDW	←
Data hold from write time	tDH	0ns(min.)	tDH	←
Output enable from end of write	tOW	5ns(min.)	tOW	←
Output disable to output in high-Z	tOHZ	0ns(min.) / 20ns(max.)	tOHZ	←
Write to output in high-Z	tWHZ	0ns(min.) / 20ns(max.)	tWHZ	←

Appendix 8: Packing Specification

(1) Change the specification of the 52pin-µTSOP Tape & Reel

- The package pocket form, size and seat position are to be changed (see below).
- No change in embossed tape width, pocket pitch and reel diameter.

Pre Change (Embossed tape type name : MTE2416H-52PTG-A)



Post Change (Embossed tape type name : uTSOP-52L)

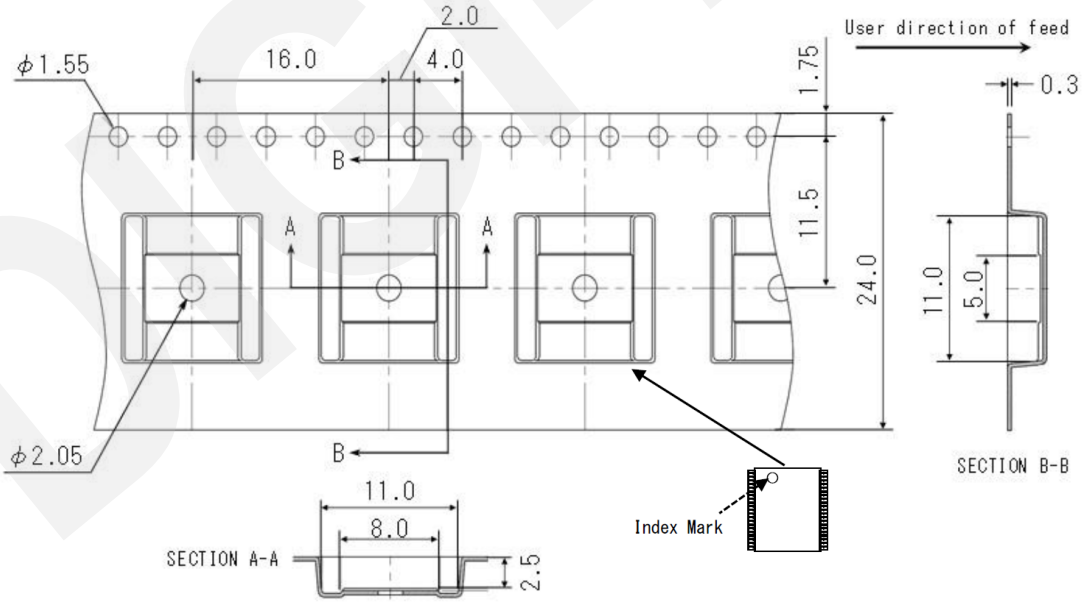


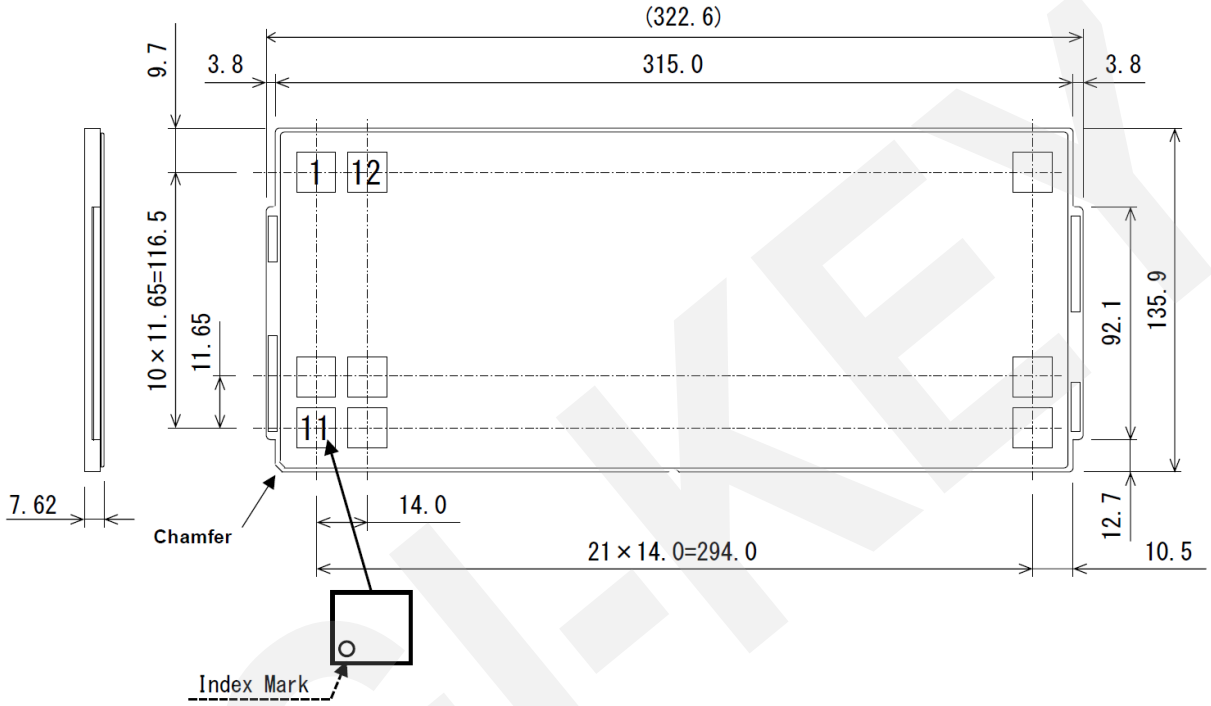
Figure. 52pin-µTSOP Embossed Carrier tape Dimensions (Unit: mm)

Appendix 8 (cont.): Packing Specification

(2) Change the specification of the 48ball-FBGA Tray

- Because of changing package outline size, the tray pocket size is to be changed (see below).
- No change in Laying direction of ICs on a tray.

Pre Change (Tray type name : L196-121, Storage number : 242pcs/tray)



Post Change (Tray type name : L196-45, Storage number : 253pcs/tray)

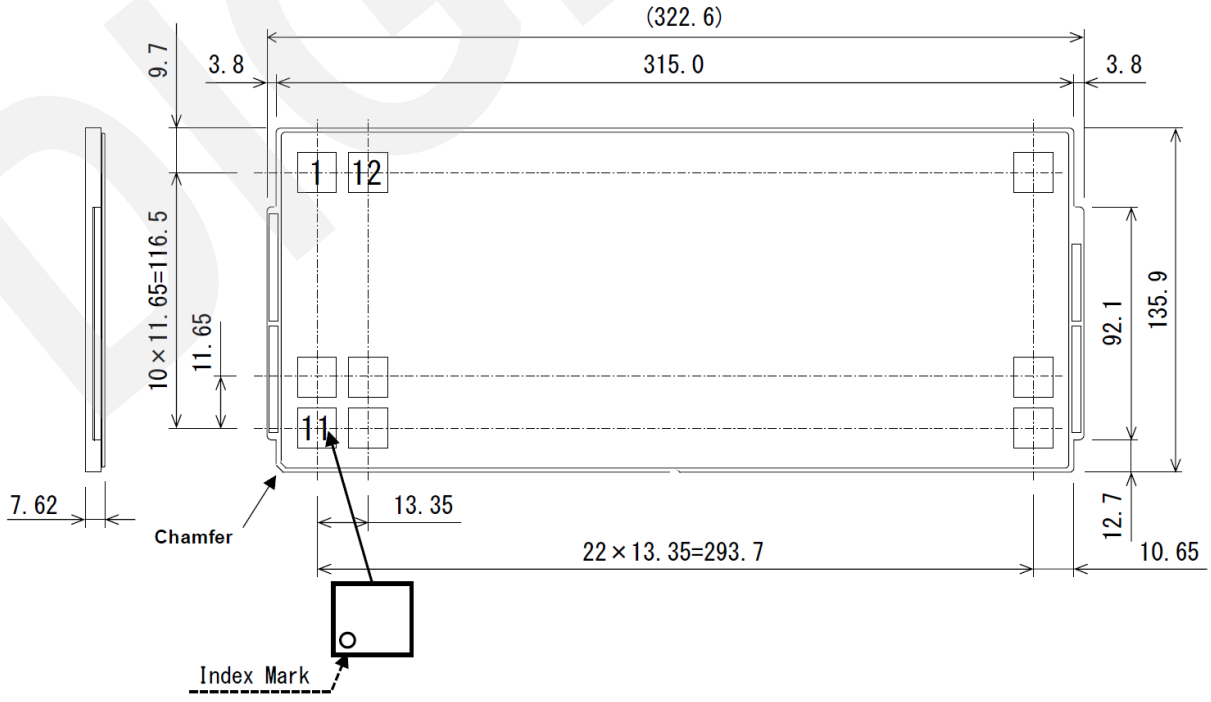


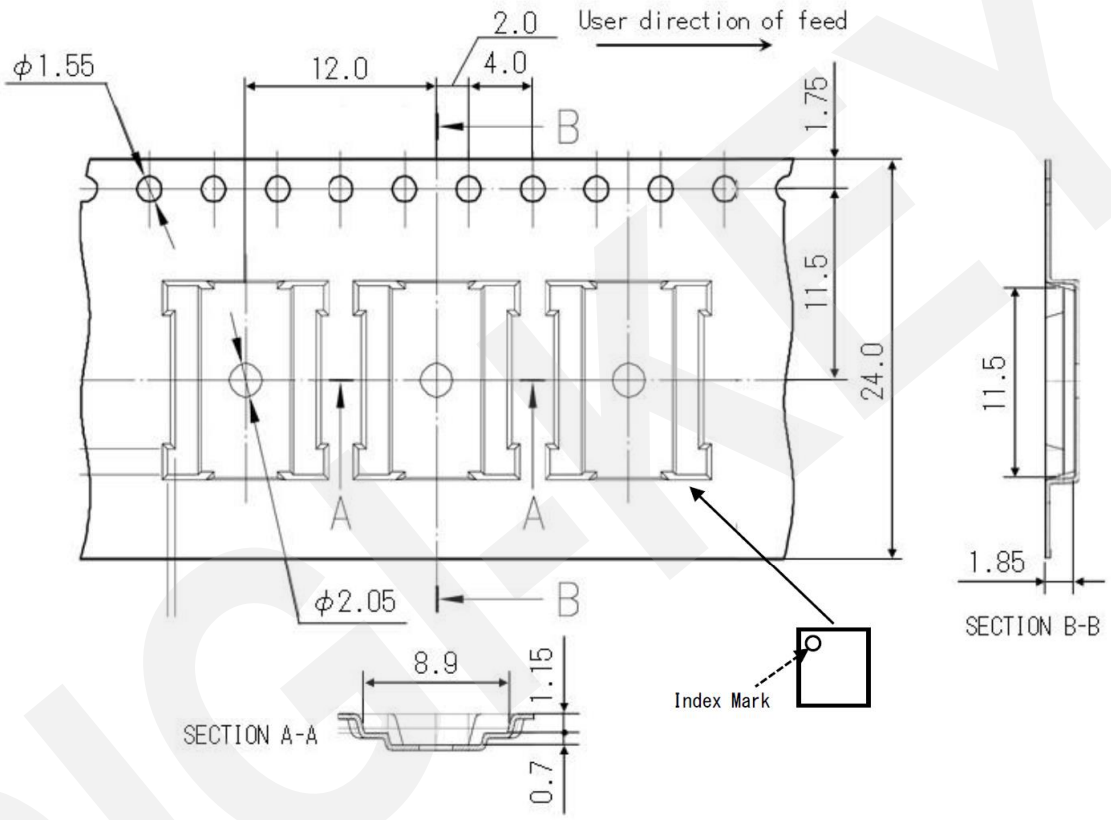
Figure: Dimension of 48ball-FBGA tray and the method to pack ICs (Unit: mm)

Appendix 8 (cont.): Packing Specification

(3) Change the specification of the 48ball-FBGA Tape & Reel

- Because of changing package outline size, the package pocket form, size, seat position and embossed tape width are to be changed (see below).
- No change in pocket pitch and reel diameter.

Pre Change (Embossed tape type name : TE2412-48FHK)



Post Change (Embossed tape type name : MTE1612H-48F7Q)

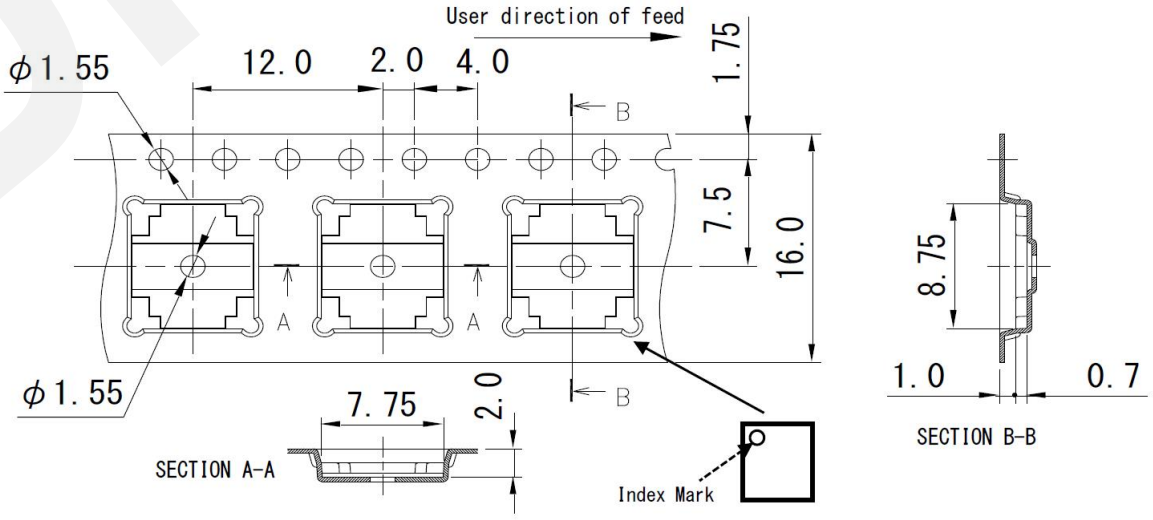


Figure. 48ball-FBGA Embossed Carrier tape Dimensions (Unit: mm)