International
IOR Rectifier

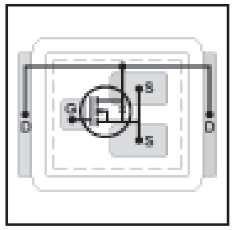
PD - 94364D

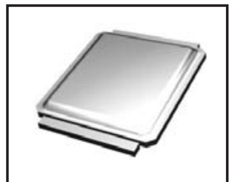
IRF6603

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Qg
30V	3.4mΩ@V_{GS} = 10V	48nC
	5.5mΩ@V_{GS} = 4.5V	

- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques





DirectFET™ ISOMETRIC

Description

The IRF6603 combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, IMPROVING previous best thermal resistance by 80%.

The IRF6603 balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6603 has been optimized for parameters that are critical in synchronous buck converters including Rds(on), gate charge and Cdv/dt-induced turn on immunity. The IRF6603 offers particularly low Rds(on) and high Cdv/dt immunity for synchronous FET applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	+20/-12	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	92	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	27	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	22	
I_{DM}	Pulsed Drain Current ①	200	
P_D @T_A = 25°C	Power Dissipation ⑤	3.6	W
P_D @T_A = 70°C	Power Dissipation ⑤	2.3	
P_D @T_C = 25°C	Power Dissipation	42	
	Linear Derating Factor	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④	—	35	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑥	20	—	
$R_{\theta JC}$	Junction-to-Case ⑦	—	3.0	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	—	

Notes ① through ⑦ are on page 11

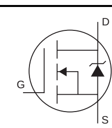
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	28	–––	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	2.4	3.4	mΩ	V_{GS} = 10V, I_D = 25A ③
		–––	3.9	5.5		V_{GS} = 4.5V, I_D = 20A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	–––	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta TJ$	Gate Threshold Voltage Coefficient	–––	-6.3	–––	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	30	µA	V_{DS} = 24V, V_{GS} = 0V
		–––	–––	100		V_{DS} = 24V, V_{GS} = 0V, T_J = 70°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -12V
gfs	Forward Transconductance	56	–––	–––	S	V_{DS} = 15V, I_D = 20A
Q_g	Total Gate Charge	–––	48	72	nC	
Q_{gs1}	Pre-Vth Gate-to-Source Charge	–––	15.6	–––		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	–––	5.2	–––		V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	–––	16.1	–––		I_D = 20A
Q_{godr}	Gate Charge Overdrive	–––	11.1	–––		See Fig. 16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	–––	21.3	–––		
Q_{oss}	Output Charge	–––	28	–––	nC	V_{DS} = 16V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	–––	20	–––	ns	V_{DD} = 15V, V_{GS} = 4.5V ③
t_r	Rise Time	–––	9.9	–––		I_D = 20A
$t_{d(off)}$	Turn-Off Delay Time	–––	24	–––		Clamped Inductive Load
t_f	Fall Time	–––	71	–––		
C_{iss}	Input Capacitance	–––	6590	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	1250	–––		V_{DS} = 15V
C_{rss}	Reverse Transfer Capacitance	–––	520	–––		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	49	mJ
I_{AR}	Avalanche Current ①	–––	20	A
E_{AR}	Repetitive Avalanche Energy ①	–––	4.1	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	25	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	200		
V_{SD}	Diode Forward Voltage	–––	1.0	1.3	V	T_J = 25°C, I_S = 20A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	–––	45	68	ns	T_J = 25°C, I_F = 20A
Q_{rr}	Reverse Recovery Charge	–––	60	90	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

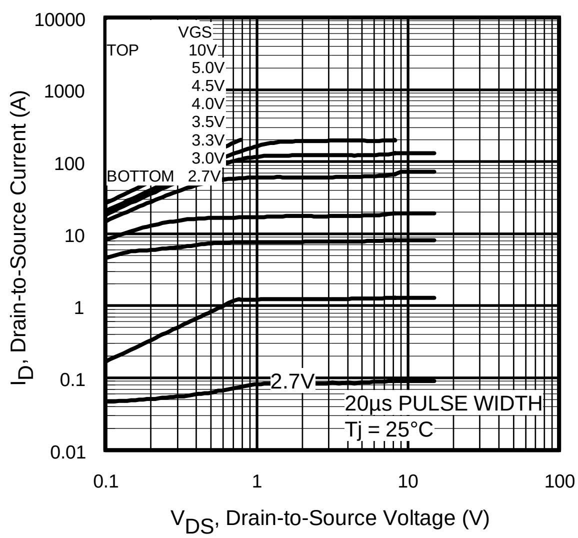


Fig 1. Typical Output Characteristics

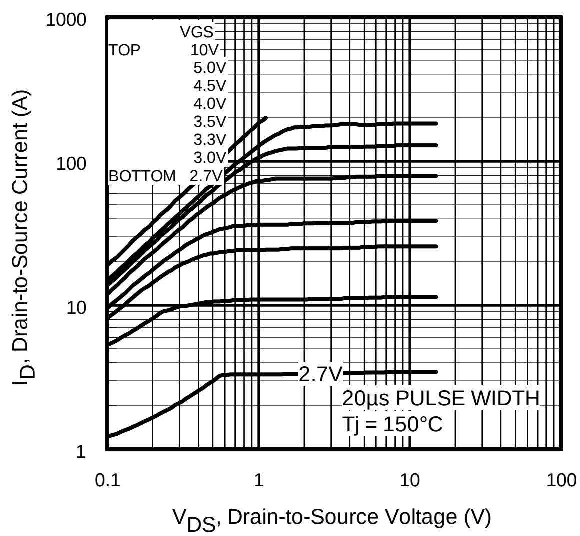


Fig 2. Typical Output Characteristics

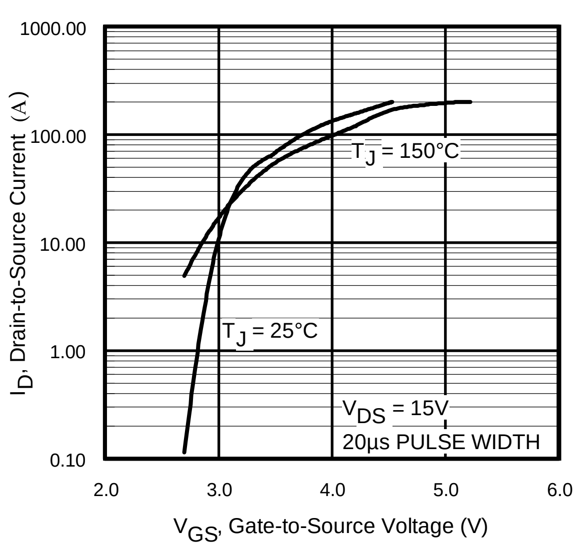


Fig 3. Typical Transfer Characteristics

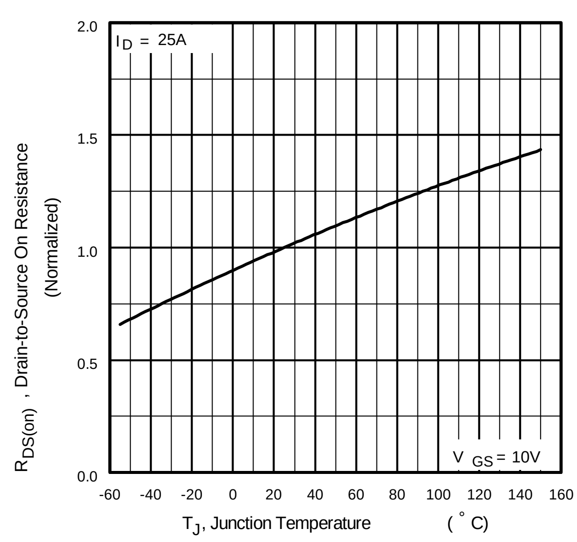


Fig 4. Normalized On-Resistance vs. Temperature

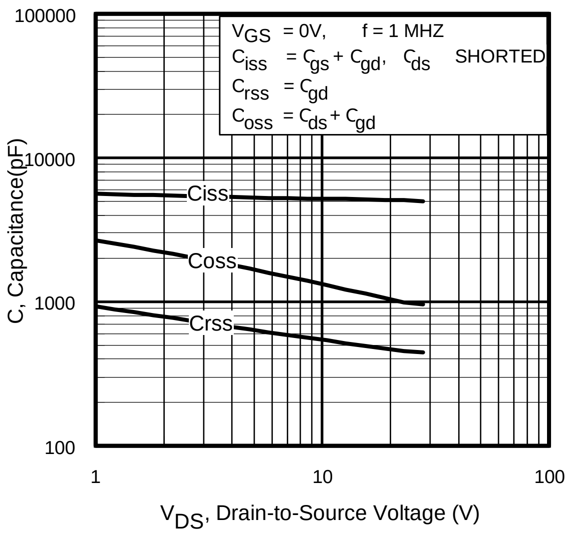


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

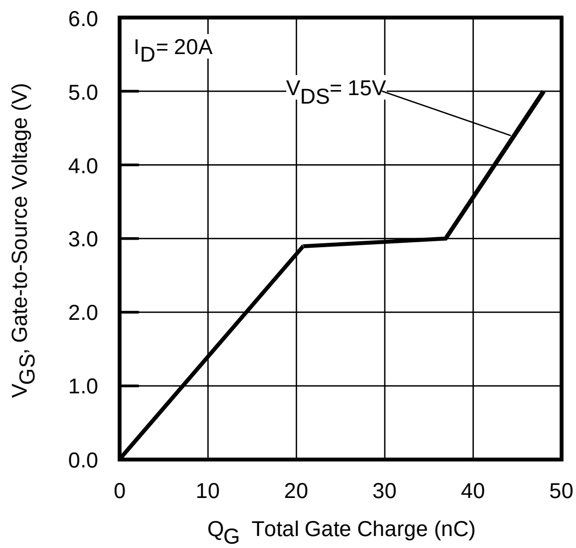


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

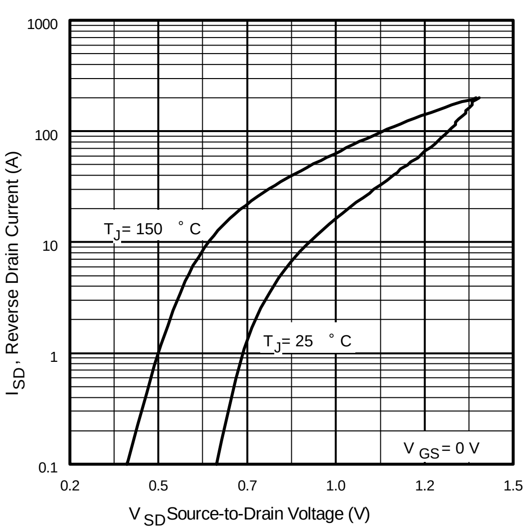


Fig 7. Typical Source-Drain Diode Forward Voltage

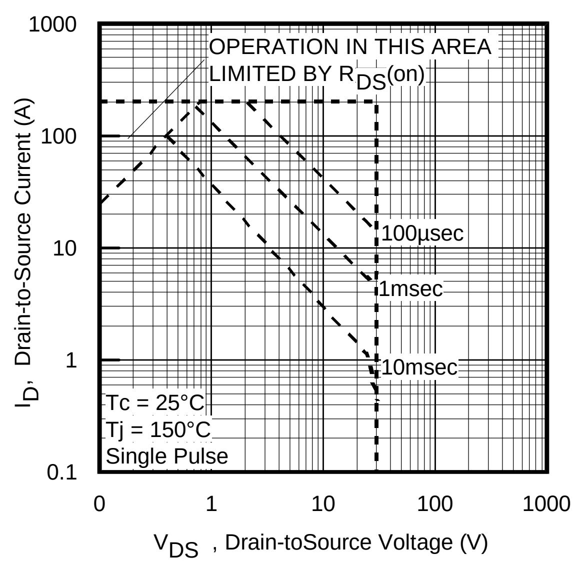


Fig 8. Maximum Safe Operating Area

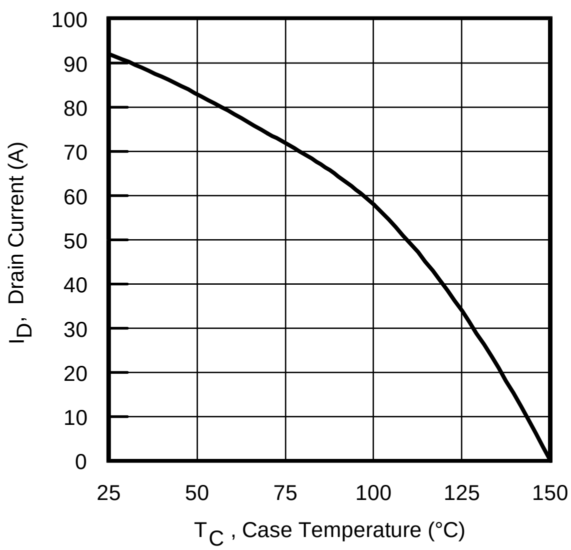


Fig 9. Maximum Drain Current Vs. Case Temperature

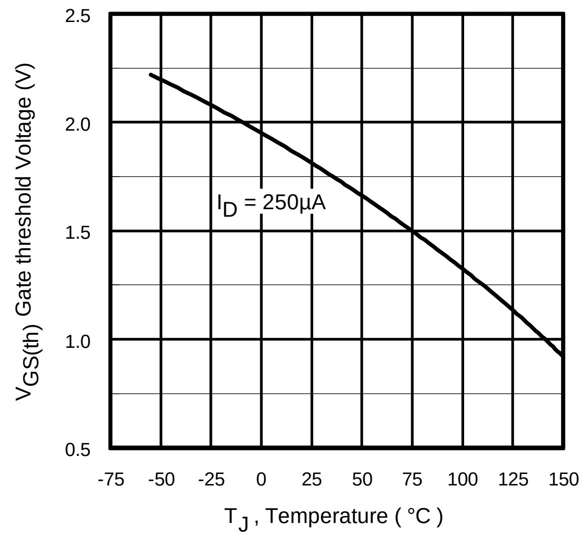


Fig 10. Threshold Voltage Vs. Temperature

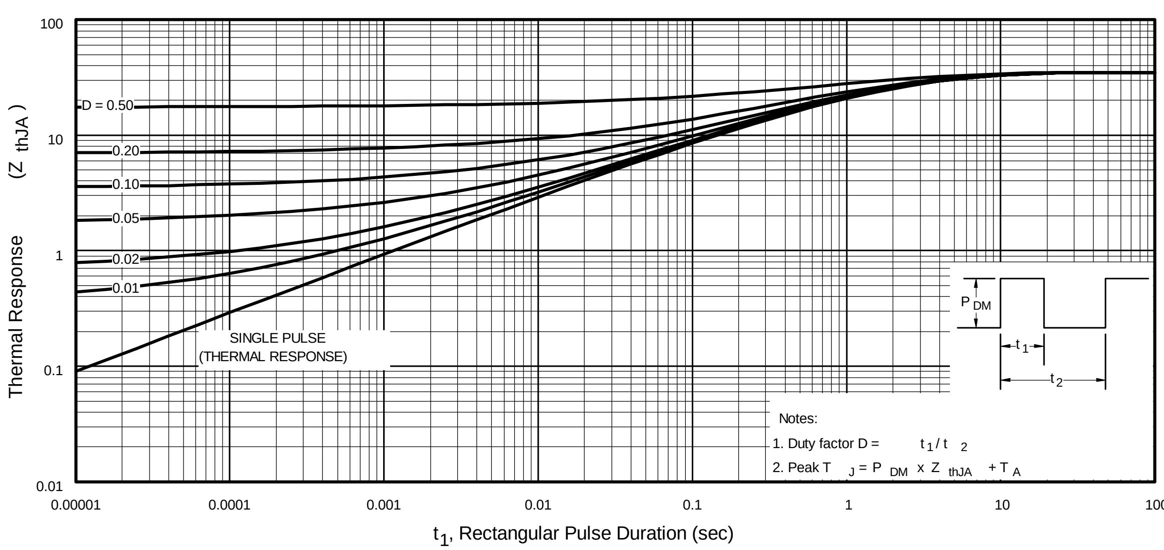


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

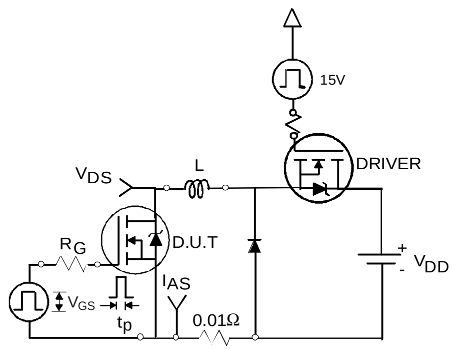


Fig 12a. Unclamped Inductive Test Circuit

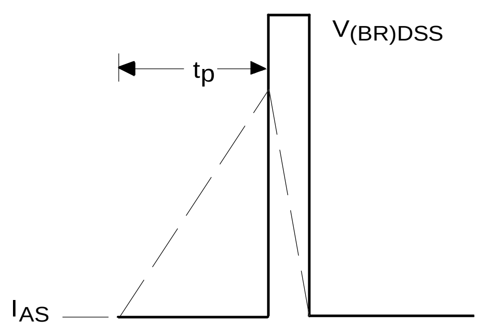


Fig 12b. Unclamped Inductive Waveforms

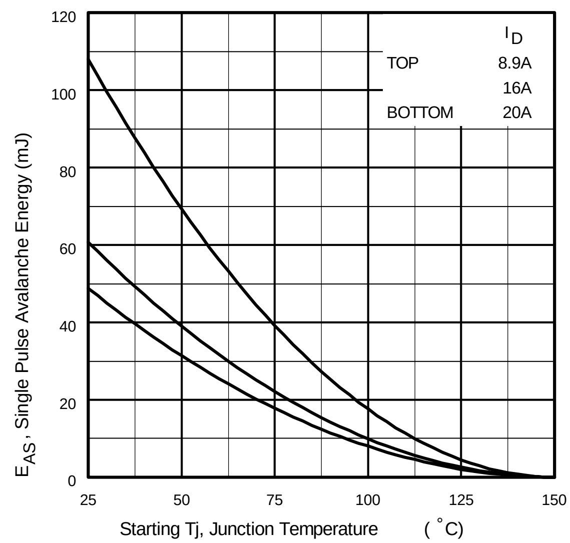


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

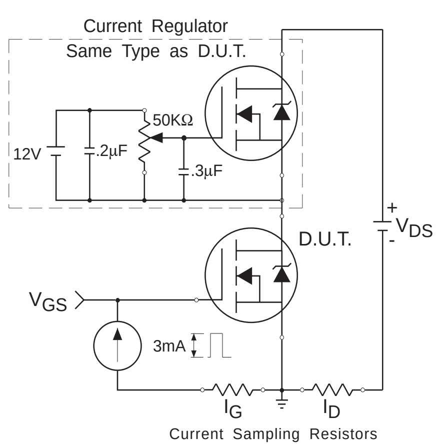


Fig 13. Gate Charge Test Circuit

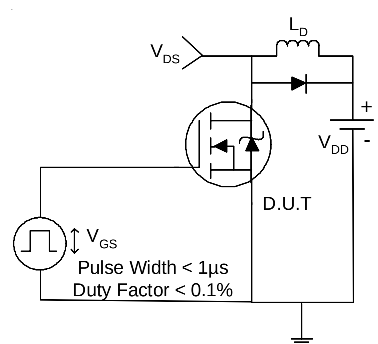


Fig 14a. Switching Time Test Circuit

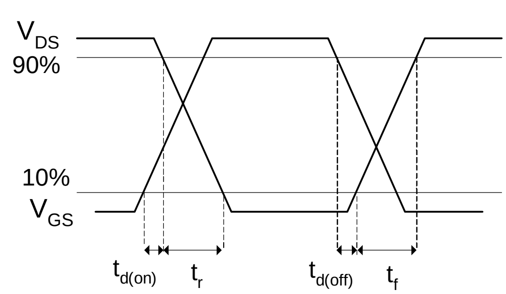
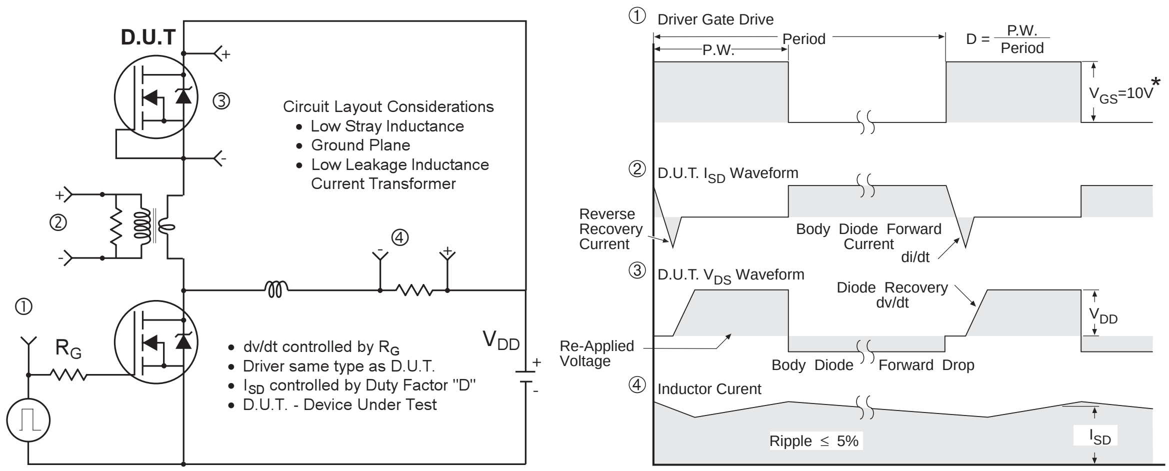


Fig 14b. Switching Time Waveforms



* V_{GS} = 5V for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

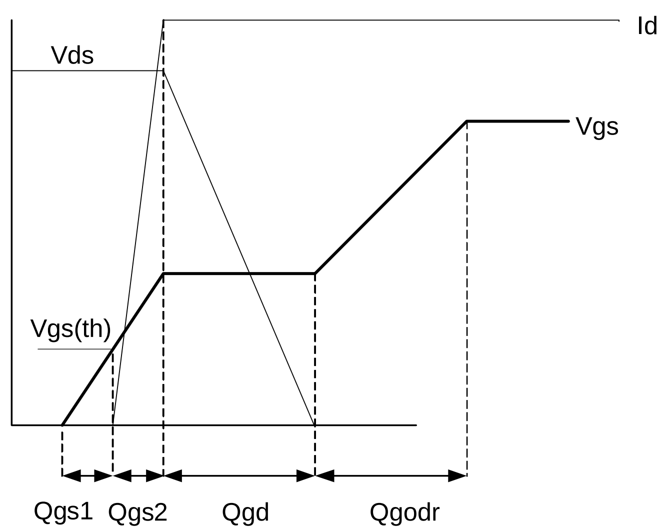


Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^*_{output}$$

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

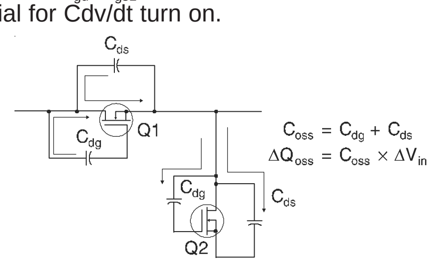
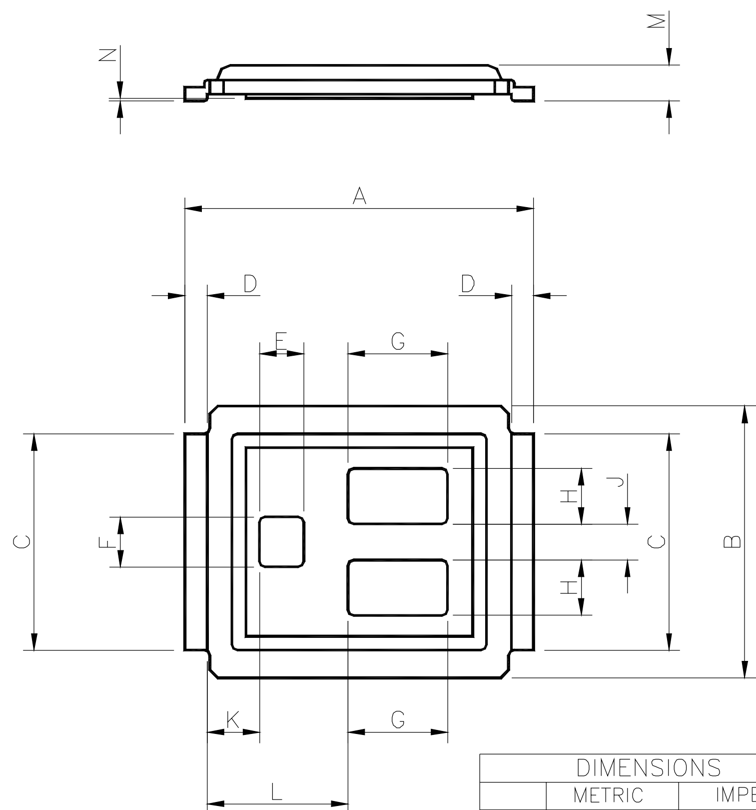


Figure A: Q_{oss} Characteristic

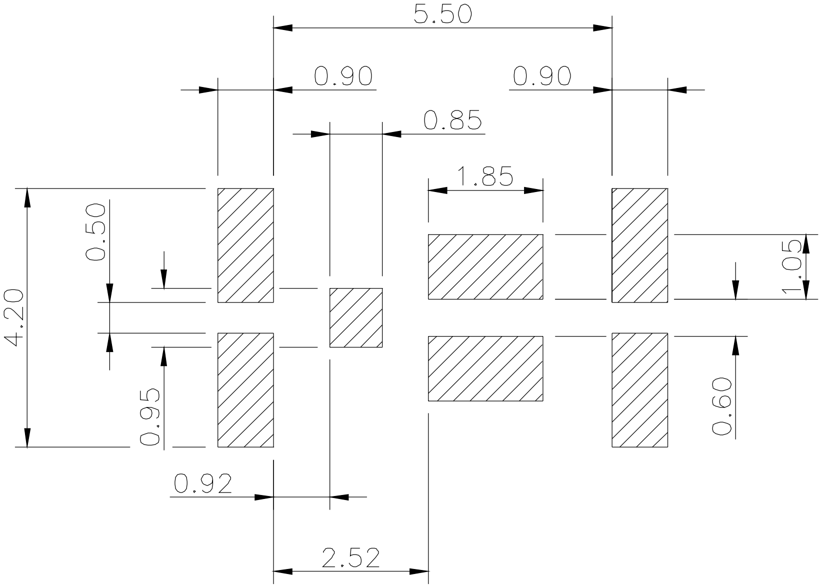
DirectFET™ Outline Dimension, MT Outline
(Medium Size Can, T-Designation).



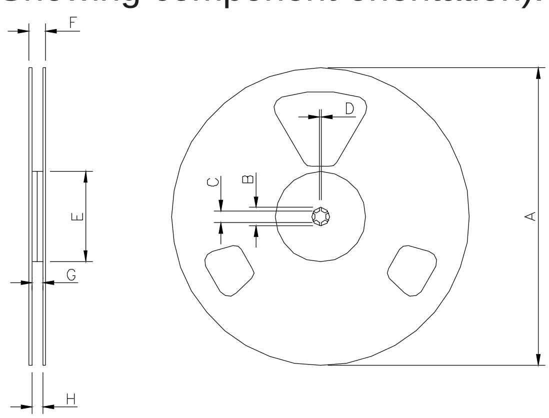
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.78	0.82	0.031	0.032
F	0.88	0.92	0.035	0.036
G	1.78	1.82	0.070	0.072
H	0.98	1.02	0.039	0.040
J	0.63	0.67	0.025	0.026
K	0.88	1.01	0.035	0.039
L	2.46	2.63	0.097	0.104
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003

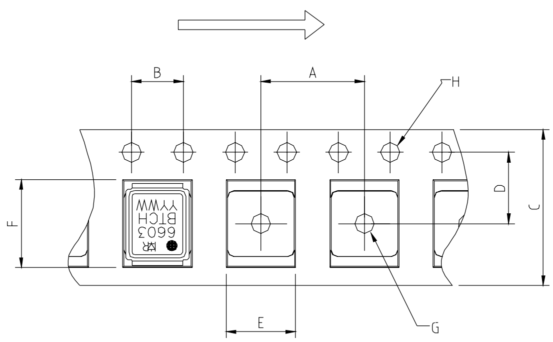
Note: Controlling dimensions are in mm

DirectFET™ Board Footprint, MT Outline (Medium Size Can, T-Designation).



DirectFET™ Tape & Reel Dimension (Showing component orientation).





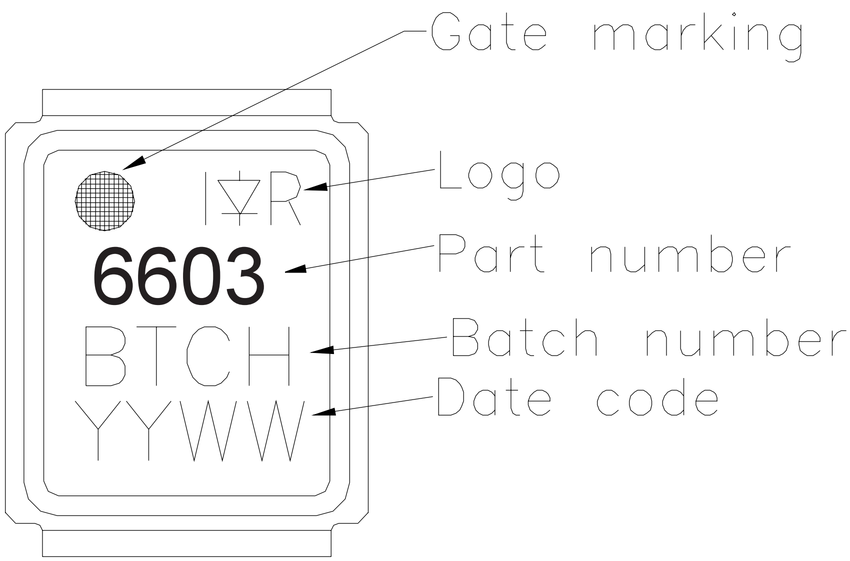
NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts.
(ordered as IRF6603).
For 1000 parts on 7" reel, order IRF6603TR1

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

DirectFET™ Part Marking



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 0.24mH $R_G = 25\Omega$, $I_{AS} = 20A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Surface mounted on 1 in. square Cu board.

⑤ Used double sided cooling , mounting pad.

⑥ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

⑦ T_C measured with thermal couple mounted to top (Drain) of part.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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