User's Guide

TLV3801EVM User's Guide

ABSTRACT

The TLV3801EVM is an evaluation board designed to evaluate the high-speed TLV3801 comparator. The TLV3801EVM has layout options intended to make it simple to evaluate timing performance with different measurement tools. The output of the TLV3801 is designed for low-voltage differential signals (LVDS), that provide high-speed signals to interconnect devices such as FPGAs with minimal power dissipation.

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Trademarks

1 Introduction

The TLV3801EVM is an evaluation board designed to evaluate the high-speed TLV3801 comparator. The TLV3801EVM has layout options intended to make it simple to evaluate timing performance with different measurement tools. The output of the TLV3801 is designed for low-voltage differential signals (LVDS), which provide high-speed signals to interconnect devices such as FPGAs with minimal power dissipation.

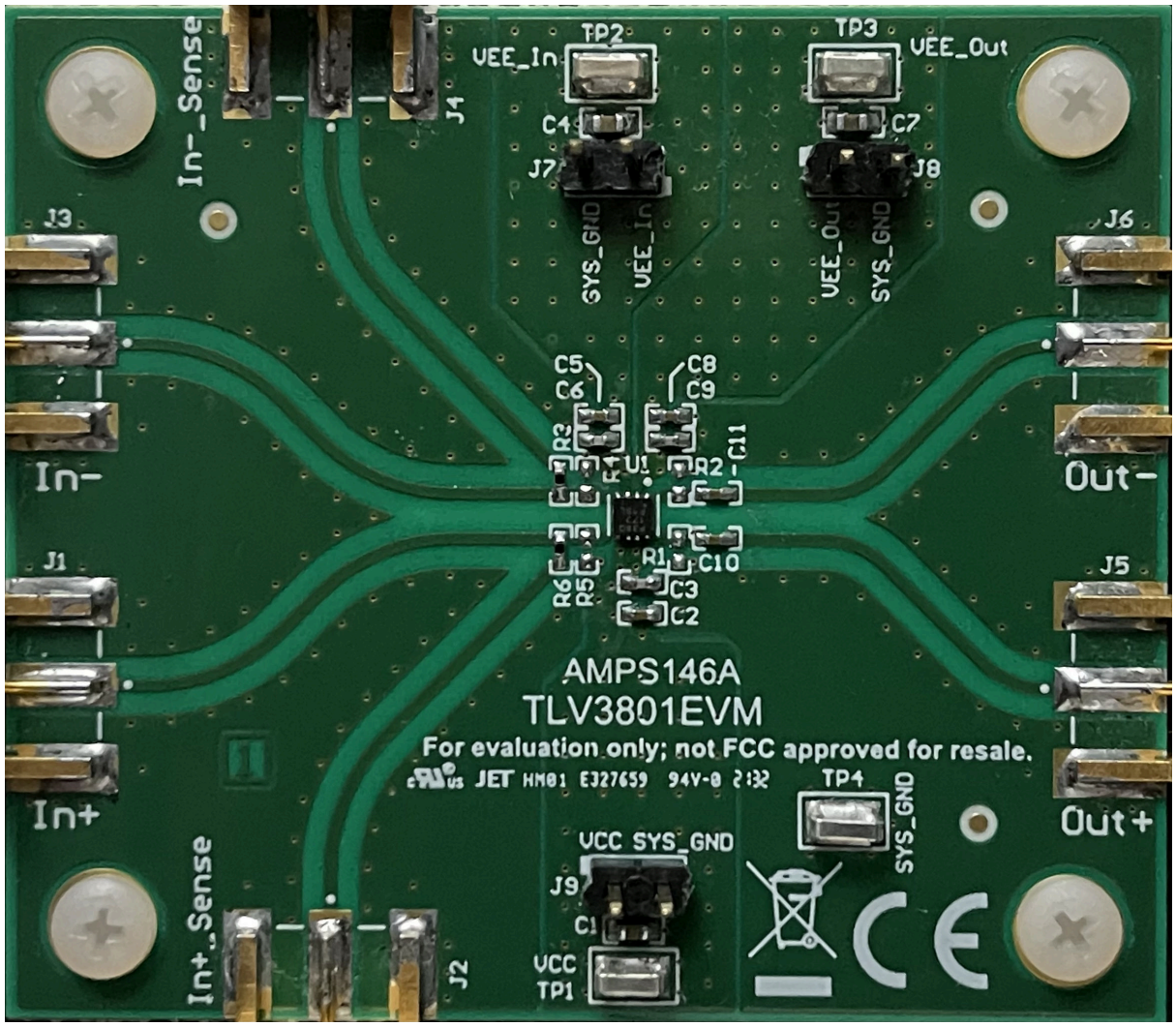

Figure 1-1. TLV3801EVM Board Top View

2 Features

- Low Propagation Delay
- Low Overdrive Dispersion
- High Toggle Frequency
- Narrow Pulse Width Detection Capability
- LVDS Output
- Low Input Offset Voltage
- DSG Package 8-pin WSON

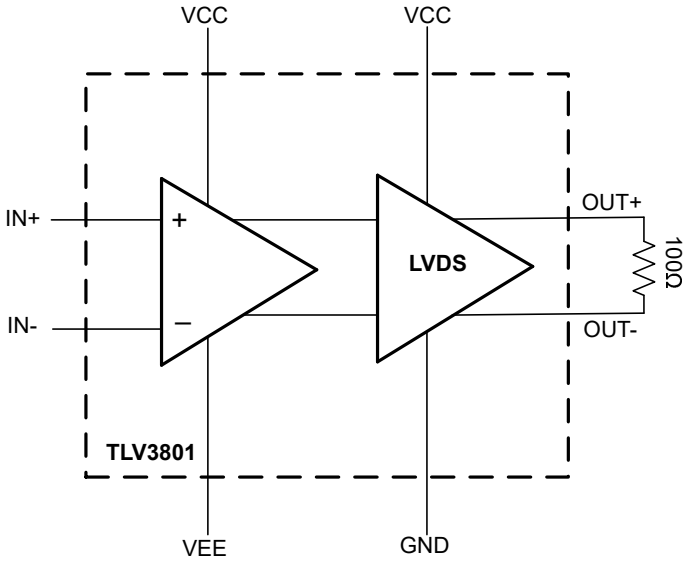

Figure 2-1. TLV3801 Block Diagram

3 EVM Specifications

- Supply Range: +2.7 V to +5.25 V (Single Supply Only)
- Input Common Mode Range: VEE + 1.5 V to VCC + 0.1 V
- Differential Input Voltage Range: (-1.5 V to 1.5 V)

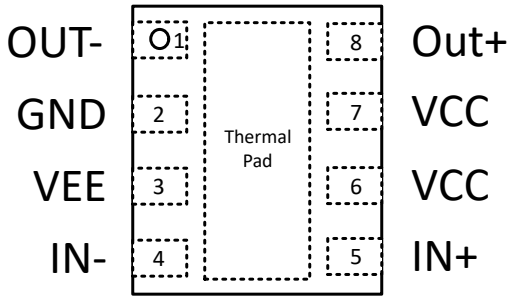

Figure 3-1. TLV3801EVM Pin Assignments

Comparing the device pin assignments to the EVM designations, it is clear that the TLV3801 does not have "VEE_In" and "VEE_Out" pins. The "VEE_In" EVM designation corresponds to the VEE pin on the device. This pin establishes the lower limit for the input common mode range. The minimum input to the device is VEE + 1.5 V.

The "VEE_Out" designator for the EVM corresponds to the GND pin on the TLV3801. The difference between the VCC pin and the GND pin is the output supply voltage. The recommended output supply voltage (VCC - GND) range is 2.4 V to 5.25 V.

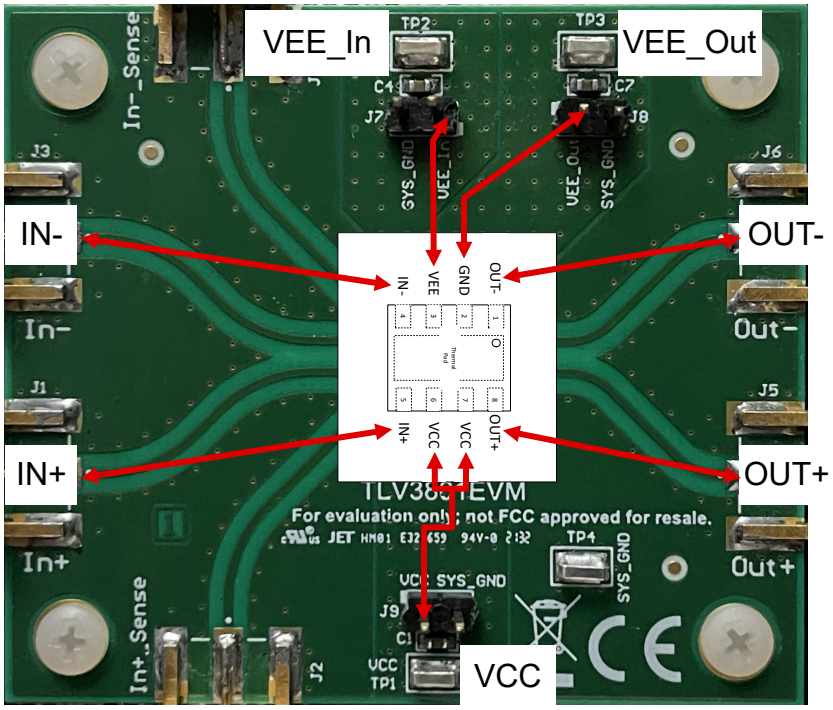

Figure 3-2. How EVM Designations are Mapped to the TLV3801 Pinout

When using a single supply, VEE_In (VEE pin) and VEE_Out (GND) are shorted to SYS_GND on the EVM. When a split supply configuration is used, then VEE_In is not shorted to SYS_GND and VEE_Out is. The split supply requirements are as follows: VCC - VEE (applies to VEE_In) has a range of 2.7 V to 5.5 V and VCC - GND has a range of 2.4 V to 5.25 V.

4 Recommended Equipment

- Dual Channel Power Supply
- High Speed Functional Generator with fast rise/fall time recommended (≤ 500 ps)
- High Speed Oscilloscope with 50-Ω terminations
- SMA Cables/adapters
  - All sensed input voltages and both output signals must have matched cable lengths
    - IN+SENSE, IN-SENSE (only if AC signal), OUT+, and OUT-
  - All other signals can use non-matched cable lengths

5 How to Make a TPHL Propagation Delay Measurement With Split Supplies

Note

Do not turn on power supply until all connections to the device are made to the board.

1. Short VEE_OUT jumper to SYS_GND.
2. Set one channel of the DC power supply to output a -2.5 V voltage and set its current limit to 100 mA. After ensuring that this channel is disabled, connect VEE_IN to this supply.
3. Set one channel of the DC power supply to output a 2.5 V voltage and set its current limit to 100 mA. After ensuring that this channel is disabled, connect VCC to this supply.
4. Ensure that cables connecting to IN+SENSE, OUT+, and OUT- are matched length and impedance. Perform any deskewing if no matched cables are available. For this setup, IN- is a DC voltage reference so the cables used for IN- and IN- SENSE do not need to be matched.
5. On the signal generator output, set the function generator to produce a square wave output with 100 mVpp at 10-MHz, with a 0 V DC offset. This results in a 50 mV overdrive and 50 mV underdrive. Disable the signal generator output. Connect the signal generator output to IN+.
6. Ground the inverting input, IN-, to ground to establish the threshold for the comparator at 0 V.
7. Connect OUTP and OUTN to a 50-Ω terminated channel on the oscilloscope. **Note** that with capacitors C10 and C11 populated, the discharging and charging of these output capacitors will cause the output to be averaged.
8. Connect IN+SENSE, to another 50-Ω terminated scope channel.
9. Enable the VCC/VEE_IN power supply.
10. Verify the total supply current is < 30 mA.
11. Enable the signal generator.
12. Monitor and verify the inputs from IN+SENSE and IN- is 0 V DC.
13. Monitor and verify the outputs for OUT+ and OUT-.

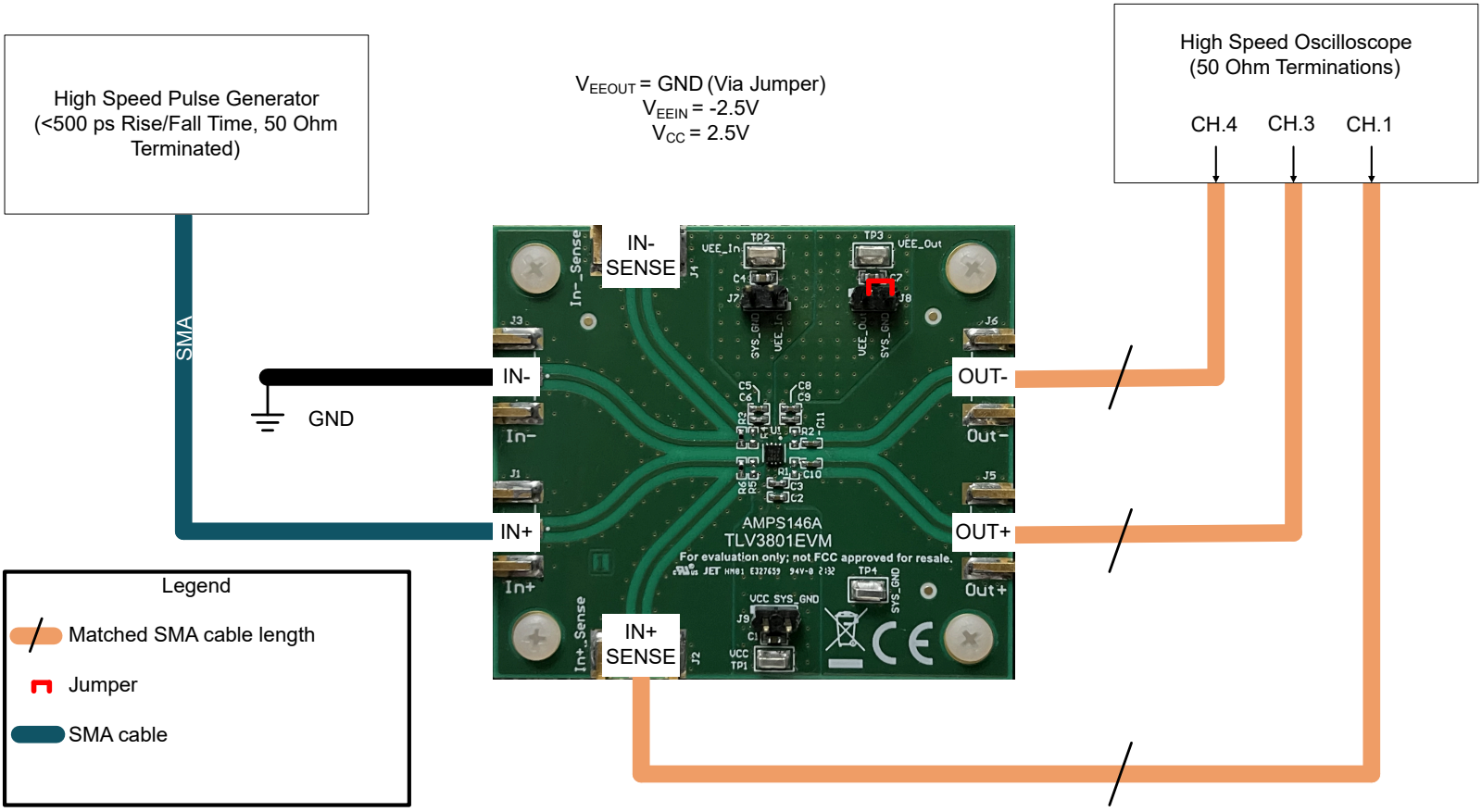

Figure 5-1. TLV3801 EVM Propagation Delay with Latch Setup

Next is a scope shot capture of the inputs and outputs described in the propagation delay procedure. High to Low propagation delay is defined as when the signal generator input (IN+) reaches 0 V to when OUT- reaches 0 V. The propagation delay was measured at approximately 206 ps with the setup described.

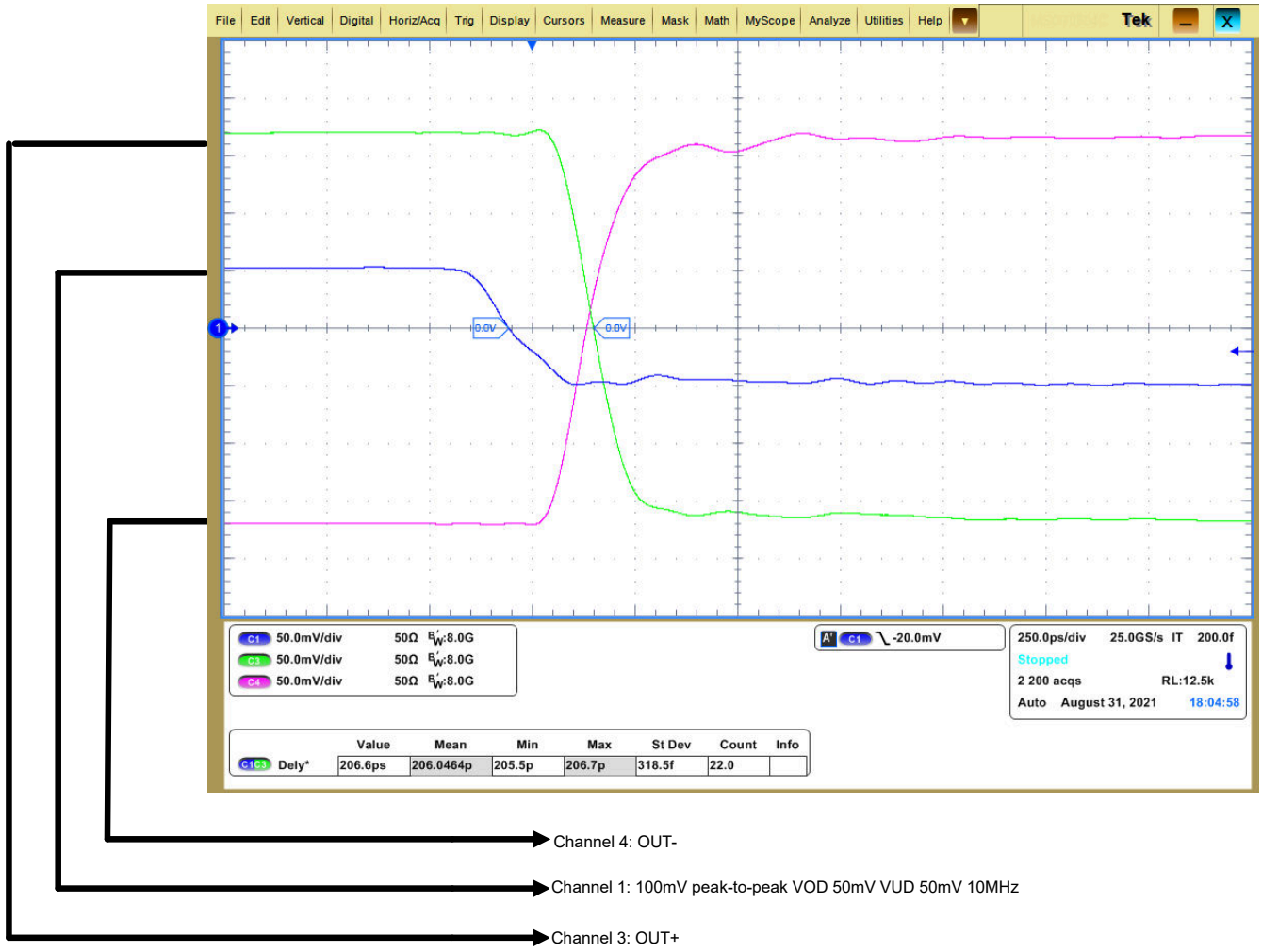

Figure 5-2. Quick Start Example

6 Board Setup

6.1 Supply Voltage

The TLV3801EVM can operate from a single supply or split supply configuration. If using the a single supply (VEE_In and VEE_Out shorted to GND), then the recommended voltage range is from 2.7-V to 5.5-V. When a split supply configuration is used, then VCC - VEE (applies to both VEE_In and VEE_Out) has a range of 2.7-V to 5.5-V and VCC - GND has a range of 2.4-V to 5.25-V. Connect VCC, VEE_In, and VEE_Out using TP1, TP2, and TP3 respectively.

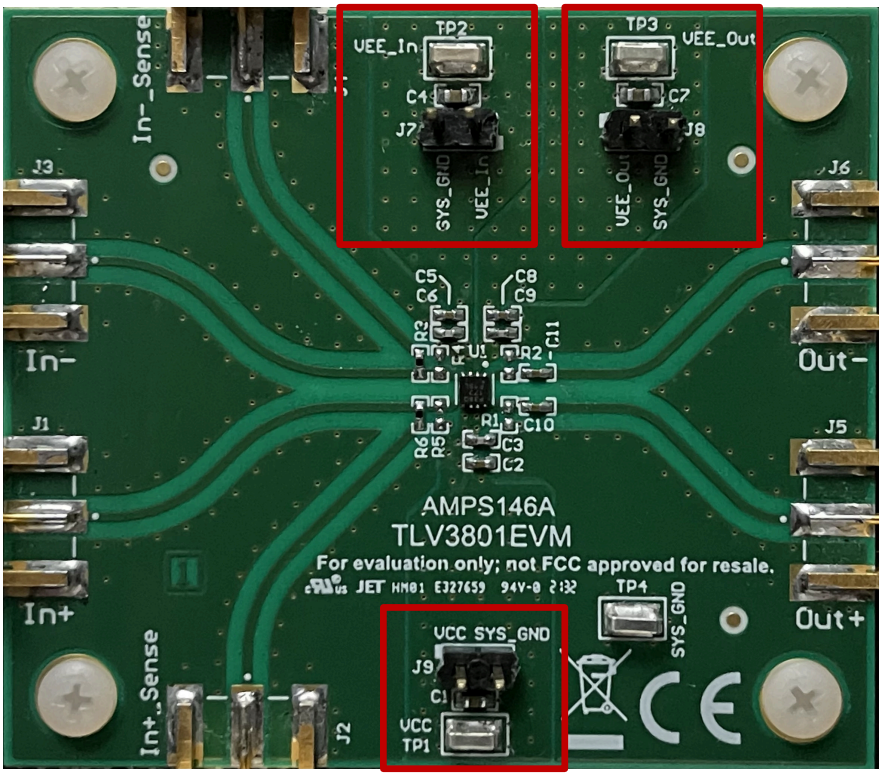

Figure 6-1. TLV3801EVM Supply Voltage Connection

6.2 Inputs

Resistors R6 and R3 are 0-Ω resistors. The input terminals (IN+ and IN-) have corresponding sense lines so that the inputs to the device can be terminated on the lines with 50-Ω to an oscilloscope. This allows the input signals to be observed with minimal loading and distortion. There are also optional input resistors R4 and R5 for direct 50-Ω terminations if required by the input signal generator, otherwise they can be left uninstalled.

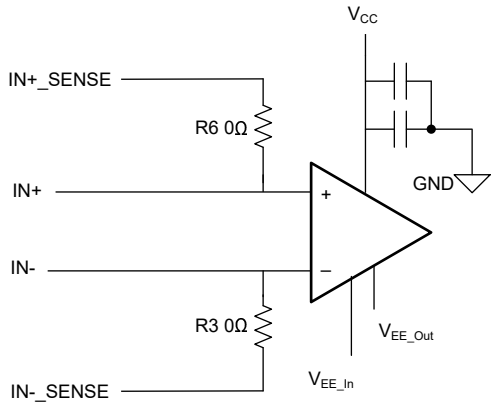

Figure 6-2. Input Side Schematic Without Optional Resistors R4 and R5

Additionally, the pads from R4 and R5 can be used to solder a 100-Ω termination resistor for LVDS input signals.

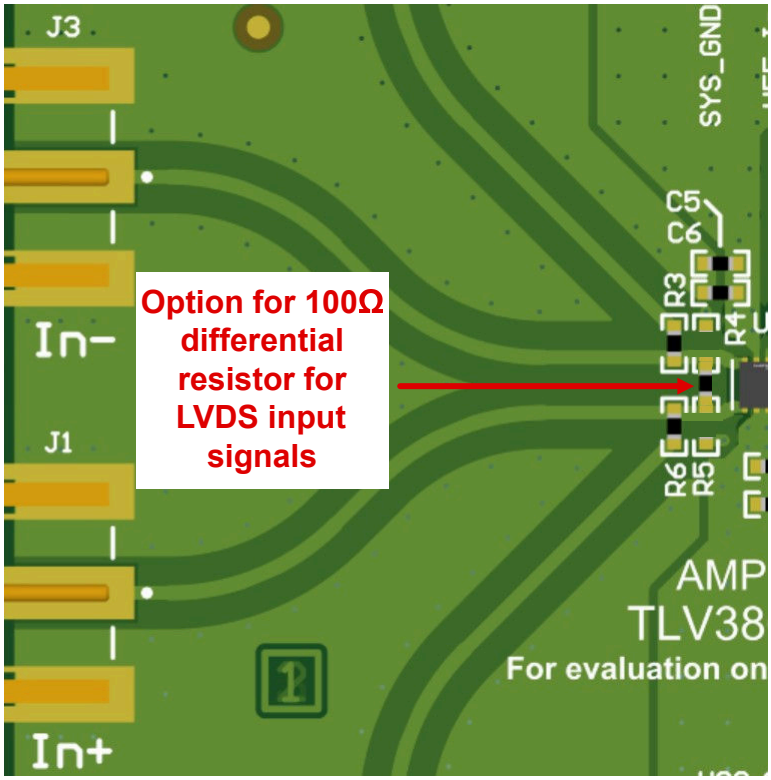

Figure 6-3. Configuration for LVDS Inputs Using the Unused Pads of R4 and R5

6.3 Outputs

C10 and C11 are installed with 0.1-uF capacitors. If a 100-Ω differential probe is unavailable to measure the LVDS output, these capacitors allow for the AC portion of the signal to be seen on a 50-Ω terminated scope. Keep in mind that any duty cycle other than 50% will result in a DC portion of the signal that is not halfway between V_{OH} and V_{OL}. As mentioned earlier, this is because of the charging and discharging of the capacitors. A higher duty cycle will result in a higher DC output voltage because the capacitors are charging more than they are discharging.

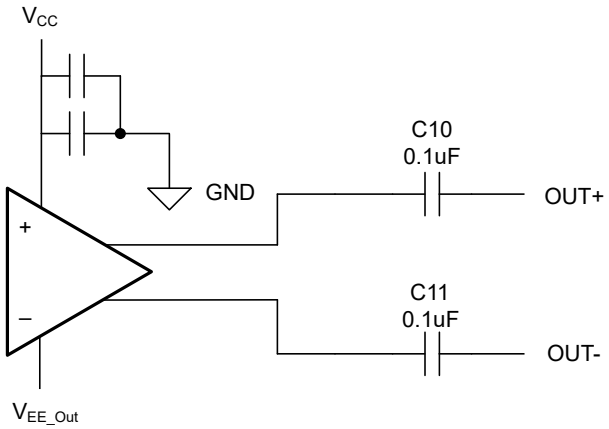

Figure 6-4. Output Side Schematic

If equipment is available to measure the LVDS output with a respect to the 100-Ω resistor or with a differential probe, then C10 and C11 can be replaced with 0-Ω resistors to keep the DC integrity of the output signal.

7 Layout Guidelines

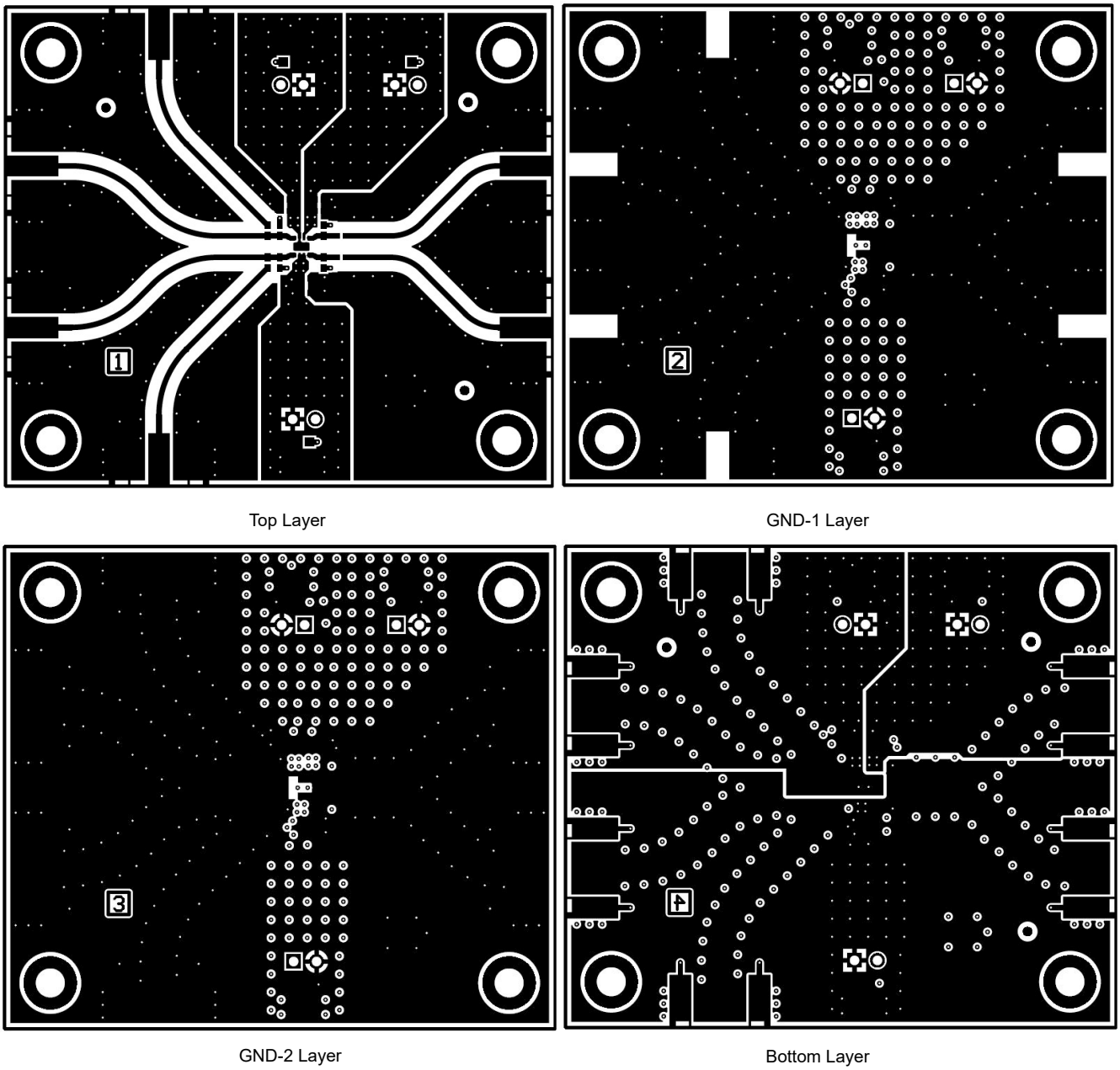

Figure 7-1. Layers

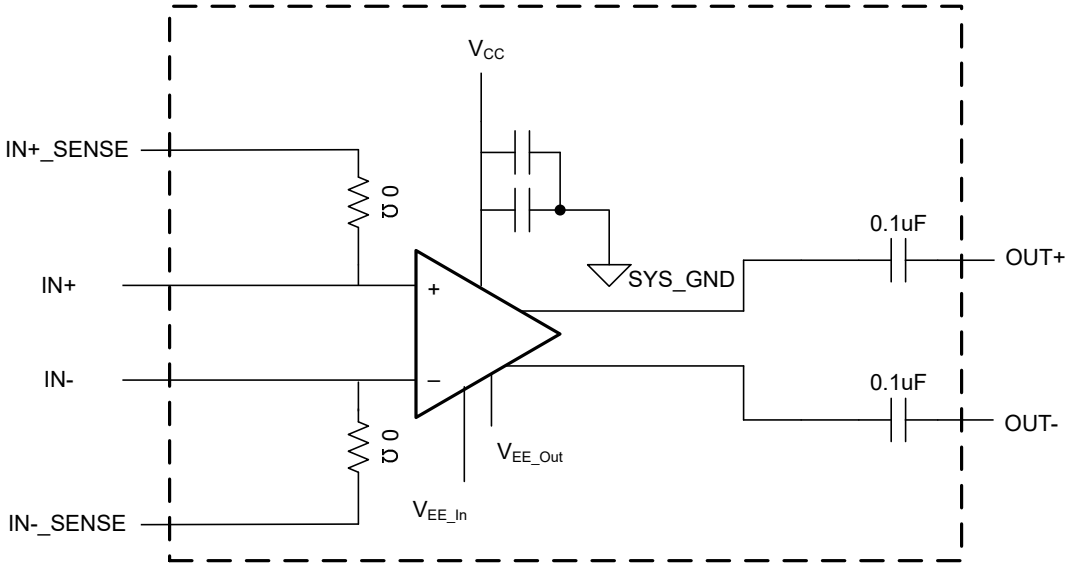

Figure 7-2. TLV3801 EVM Block Diagram

8 Schematic

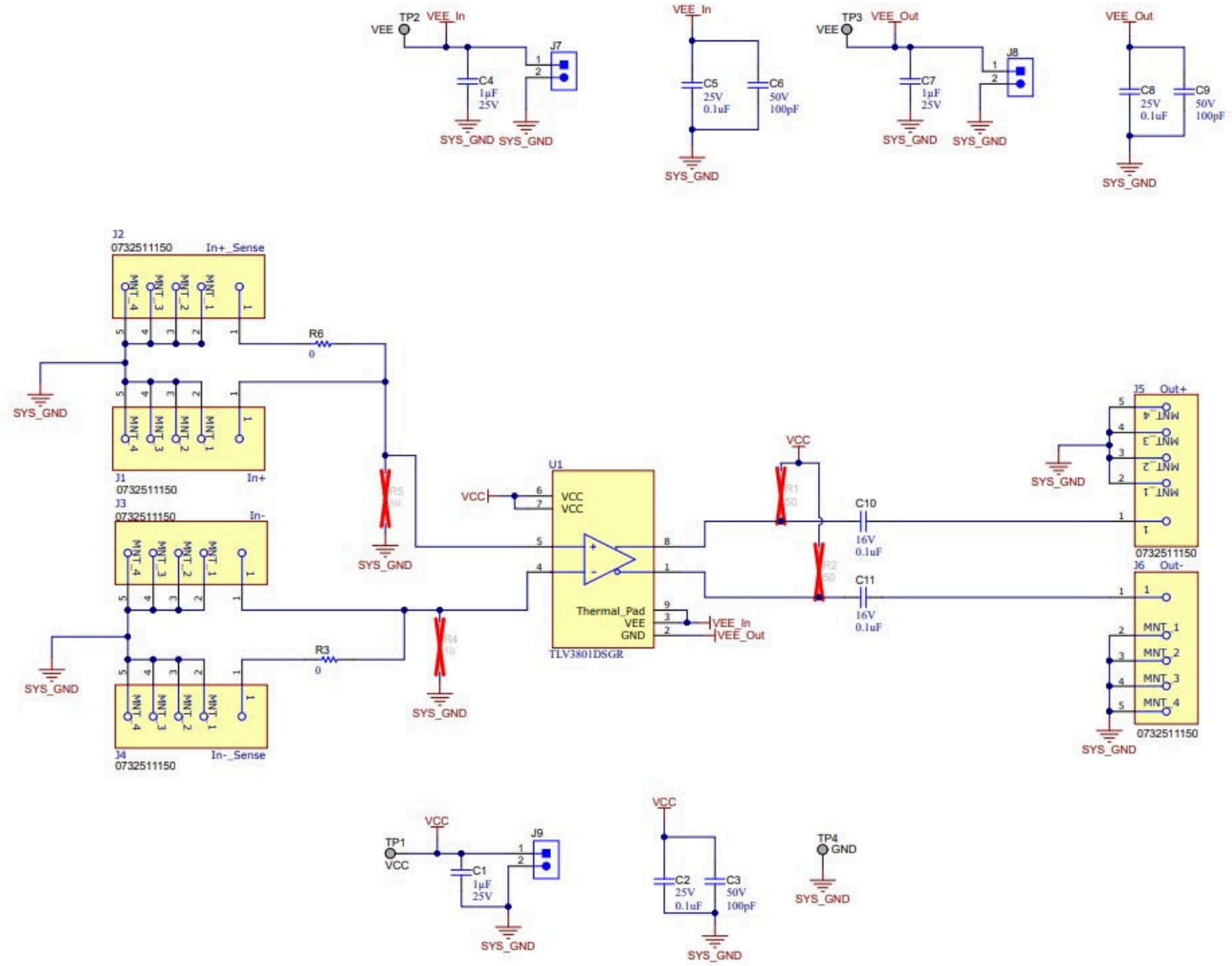

Figure 8-1. TLV3801 EVM Schematic

9 Bill of Materials

Table 9-1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1, C4, C7	3	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71E105KA64D	MuRata
C2, C5, C8	3	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E104KE14D	MuRata
C3, C6, C9	3	100pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	885012205055	Wurth Elektronik
C10, C11	2	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	GCM155R71C104KA55D	MuRata
H1, H2, H3, H4	4		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		HEX STANDOFF 4-40 ALUMINUM 1/2"	4-40 HEX Aluminum standoff 0.500 inches	1893	Keystone
J1, J2, J3, J4, J5, J6	6		SMA Connector Receptacle, Female Socket 50Ohm Board Edge, End Launch Solder		0732511150	Molex Inc
J7, J8, J9	3		Header, 100mil, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	HMTSW-102-07-G-S-240	Samtec
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R3, R6	2	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0EDHP	Vishay-Dale
TP1, TP2, TP3, TP4	4		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		250-ps High-Speed Comparator with LVDS Outputs, WSON8	WSON8	TLV3801DSGR	Texas Instruments
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R1, R2, R4, R5	0	50	RES, 50, 0.1%, 0.5 W, 0402	0402	FC0402E50R0BTBST1	Vishay Thin Film

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