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SUPPLEMENT

FS512S-102 MHz DDR

512 Mb, 1.8 V Serial Peripheral Interface with Multi-I/O Flash

General Description

This supplementary document contains information for the FS512S-102 MHz DDR. Specifications contained in this supplement supersede those in the S25FS512S datasheet. The maximum DDR clock rate was increased from 80 MHz to 102 MHz. Refer to the latest S25FS512S datasheet for full electrical specifications.

Affected Documents/Related Documents

Title	Publication Number
S25FS512S, 512 Mbit, 1.8 V Serial Peripheral Interface with Multi-I/O Flash	002-00488

1. DDR AC Characteristics

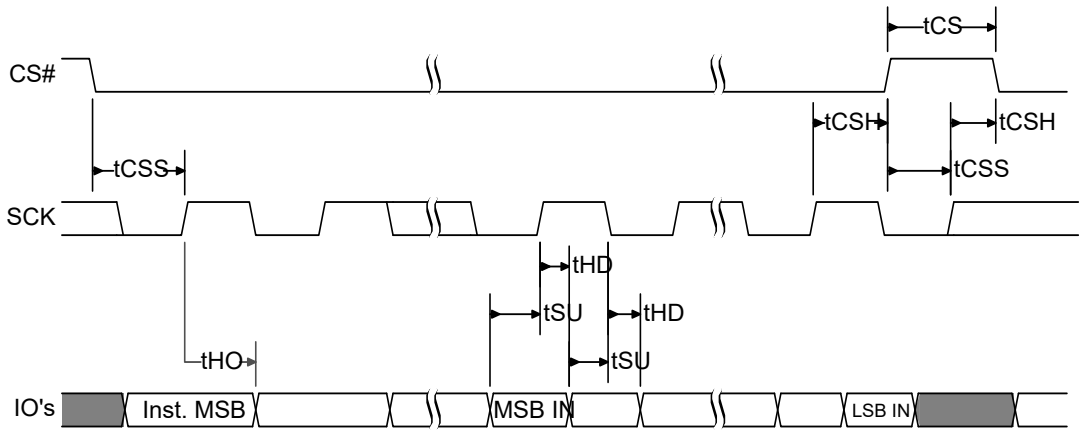
Table 1. DDR AC Characteristics Operation

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	–	102	MHz
$P_{SCK, R}$	SCK clock period for DDR READ instruction	1/ F_{SCK}	–	∞	ns
t_{WH}, t_{CH}	Clock High time	50% P_{SCK} -5%	–	50% P_{SCK} +5%	
t_{WL}, t_{CL}	Clock Low time	50% P_{SCK} -5%	–	50% P_{SCK} +5%	
t_{CS}	CS# High time (Read instructions) CS# High time (Read instructions when Reset feature is enabled)	10 20	–	–	
t_{CSS}	CS# Active Setup time (Relative to SCK)	2	–	–	
t_{CSH}	CS# Active Hold time (Relative to SCK)	3	–	–	
t_{SU}	IO in Setup time	1.5	–	–	
t_{HD}	IO in Hold time	1.5	–	–	
t_V	Clock Low to Output valid	1.5	–	5[1]	
t_{HO}	Output Hold time	1	–	–	
t_{DIS}	Output Disable time Output Disable time (When Reset feature is enabled)	–	–	8 20	
t_{IO_skew}	First IO to last IO data valid time	–	–	400	ps
t_{DPD}	CS# High to Power-down mode	–	–	3	µs
t_{RES}	CS# High to Standby mode without Electronic Signature Read	–	–	30	

Note
1. CL = 15 pF.

1.1 DDR Input Timing

Figure 1. SPI DDR Input Timing



1.2 DDR Output Timing

Figure 2. SPI DDR Output Timing

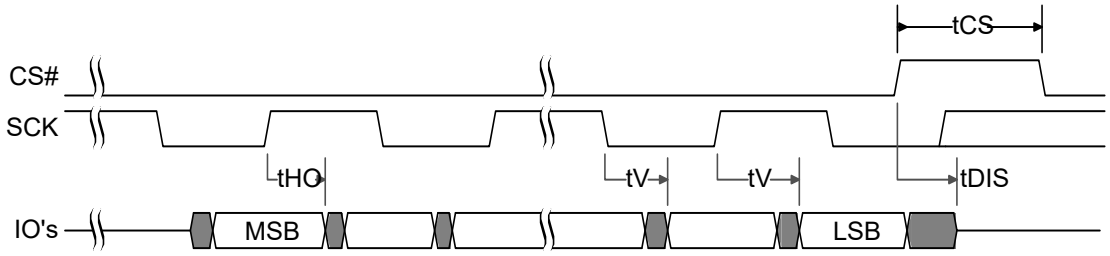
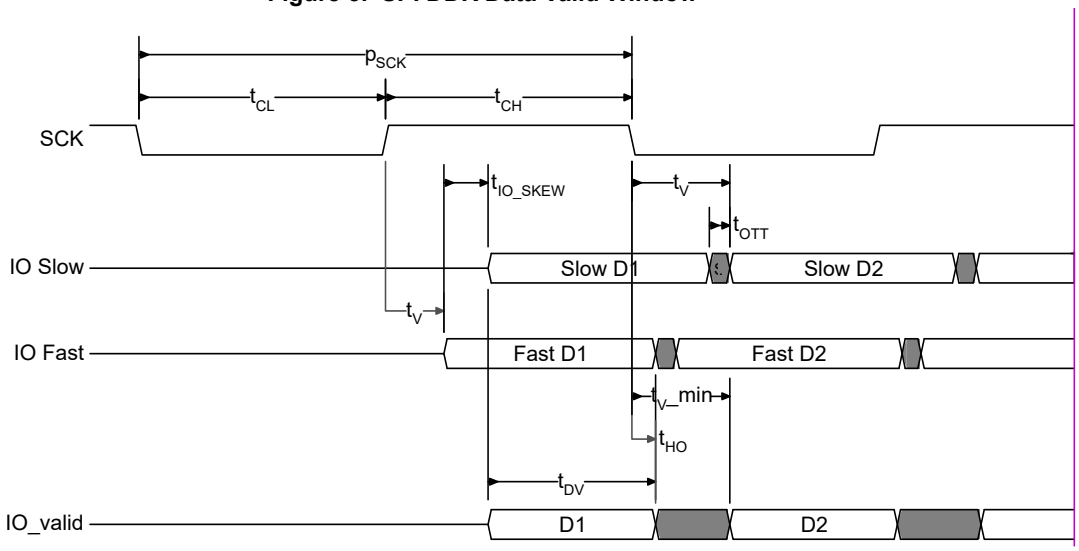


Figure 3. SPI DDR Data Valid Window[2, 3, 4, 5]



The minimum data valid window (t_{DV}) can be calculated as follows:

As an example, assuming: 102 MHz clock frequency = 9.8 ns clock period with DDR operations are specified to have a duty cycle of 45% or higher.

- t_{CLH} = 0.45*PSCK = 0.45 x 9.8 ns = 4.41 ns
- t_{IO_SKEW} = 400 ps
- t_{OTT} = 1.0 ns
- $t_{DV} = t_{CLH} - t_{O\_SKEW} - t_{OTT}$
  t_{DV} = 4.41ns - 400 ps - 1.0 ns = 3.01 ns
- t_V _min = $t_{HO} + t_{O\_SKEW} + t_{OTT}$
  t_V _min = 1.0 ns + 400 ps + 1.0 ns = 2.4 ns

Notes
2. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
3. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
4. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO.
5. t_{OTT} is dependent on system level considerations including:
   a. Memory device output impedance (drive strength).
   b. System level parasitics on the IOs (primarily bus capacitance).
   c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
   d. As an example, assuming that the above considerations result in a memory output slew rate of 2 V/ns and a 3V transition (from 1 to 0 or 0 to 1) is required by the host, the t_{OTT} would be: t_{OTT} = 2V / (2 V/ns) = 1.0 ns.
   e. t_{OTT} is not a specification tested by Cypress, it is system dependent and must be derived by the system designer based on the above considerations.

2. Latency Code

Table 2. Latency Code (Cycles) Versus Frequency[6, 7]

Latency Cycles	Read Command Maximum Frequency (MHz)			
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	Dual I/O (1-2-2)	Quad I/O (1-4-4) QPI (4-4-4)	DDR Quad I/O (1-4-4) DDR QPI (4-4-4)[8]
	Mode Cycles = 0	Mode Cycles = 4	Mode Cycles = 2	Mode Cycles = 1
0	50	80	40	**N/A**
1	66	92	53	**22**
2	80	104	66	**34**
3	92	116	80	**45**
4	104	129	92	**57**
5	116	133	104	**68**
6	129	133	116	**80**
7	133	133	129	**92**
8	133	133	133	**102**
9	133	133	133	**102**
10	133	133	133	**102**
11	133	133	133	**102**
12	133	133	133	**102**
13	133	133	133	**102**
14	133	133	133	**102**
15	133	133	133	**102**

Notes

6. The Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI, command protocols include Continuous Read mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency.
7. Other read commands have fixed latency, e.g., Read always has zero read latency. RSFDP always has eight cycles of latency.
8. DDR QPI is only supported for Latency Cycles 1 through 7 and for clock frequency of up to 92 MHz.

3. DC Characteristics

Table 3. DC Characteristics (-40 °C to +85 °C range)

Symbol	Parameter	Test Conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	200	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	120	

Table 4. DC Characteristics (-40 °C to +105 °C range)

Symbol	Parameter	Test Conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	300	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	150	

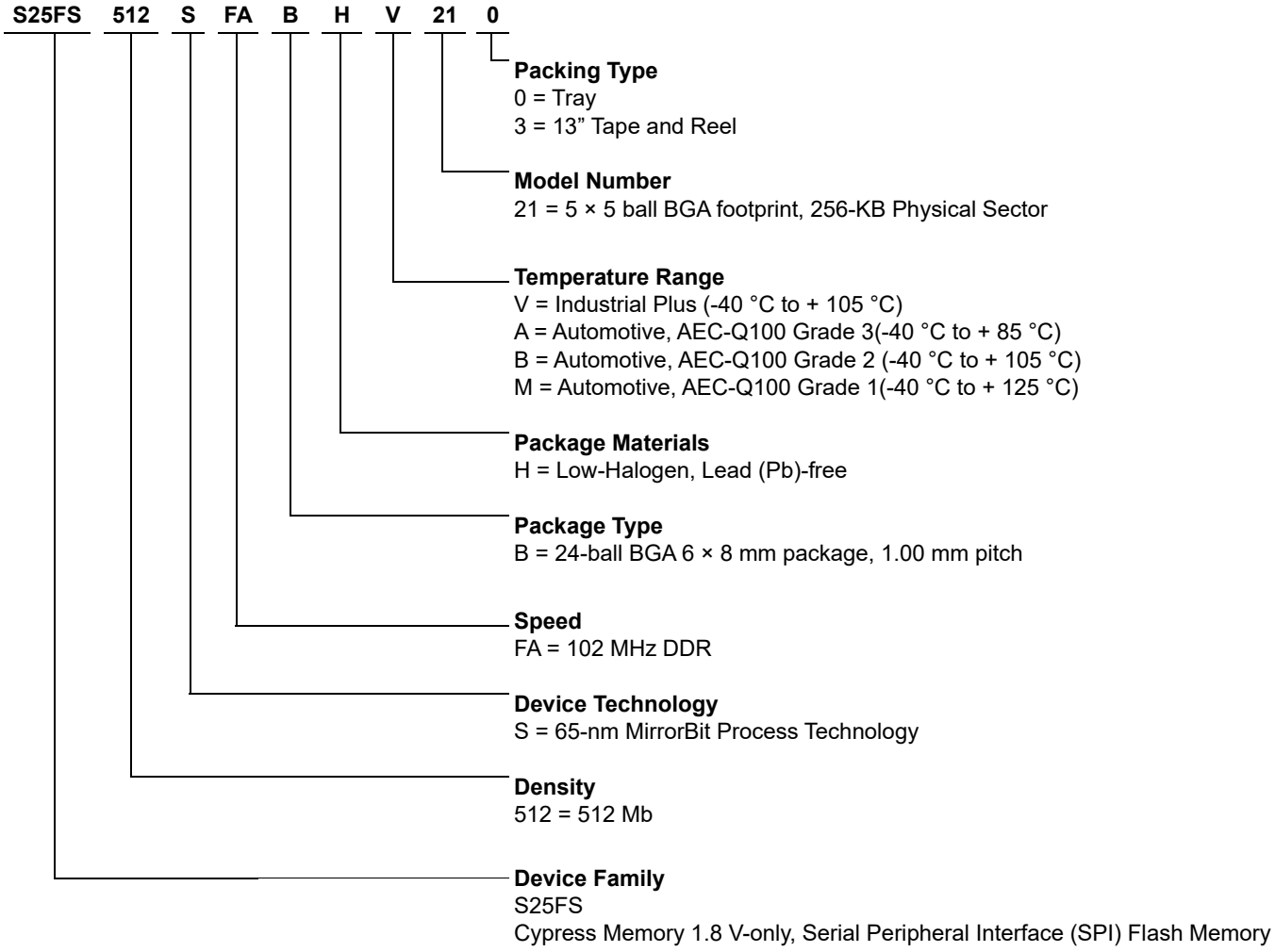
Table 5. DC Characteristics (-40 °C to +125 °C range)

Symbol	Parameter	Test Conditions	Min	Typ[9]	Max	Unit
I_{CC1}	Active power supply current (READ)[10]	Quad DDR at 102 MHz	–	70	100	mA
I_{SB}	Standby current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	25	450	µA
I_{DPD}	Deep power-down (DPD) current	IO3 / RESET#, CS# = VCC; SI, SCK = VCC or VSS	–	8	350	

Notes
9. Typical values are at TAI= 25 °C and VCC = 1.8 V.
10. Outputs unconnected during read data return. Output switching current is not included.

4. Ordering Part Number

The ordering part number is formed by a valid combination of the following:



4.1 Valid Combinations — Standard

Valid combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 6. S25FS512S Valid Combinations: Standard

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
S25FS512S	FA	BHV	21	0, 3	FS512SFVH21

4.2 Valid Combinations — Automotive Grade / AEC-Q100

Table 7 lists the configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 7. S25FS512S Valid Combinations: Automotive Grade / AEC-Q100

Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	Package Marking
S25FS512S	FA	BHB	21	0, 3	FS512SFBH21
S25FS512S	FA	BHA	21	0, 3	FS512SFAH21
S25FS512S	FA	BHM	21	0, 3	FS512SFMH21

Document History Page

Document Title: FS512S-102 MHz DDR, 512 Mb, 1.8 V Serial Peripheral Interface with Multi-I/O Flash Document Number: 002-11269			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	5153521	03/01/2016	Initial release
*A	5608199	02/07/2017	Max DDR clock rate changed from 100 MHz to 102 MHz. Updated Note 3 in Latency Code. Updated Ordering Part Number: Added support for Automotive, AEC-Q100 Grade 2 (–40°C to + 105°C). Added Valid Combinations — Standard. Added Valid Combinations — Automotive Grade / AEC-Q100. Updated Sales and Copyright information.
*B	5944243	12/08/2017	Updated the Cypress logo. Changed datasheet status to Final. Updated t_V max value to 5. Updated Latency Code.
*C	6277137	08/10/2017	Updated Table 2.
*D	7249502	08/25/2021	Added Temperature range and grades (A and M) in Ordering Part Number. Added Table 3 and Table 5 in DC Characteristics. Added OPNs in Table 7.

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